Contents

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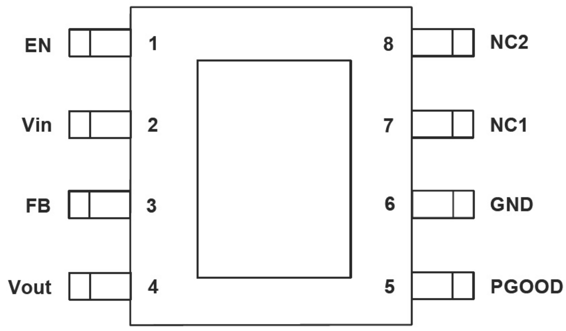
1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 2. Pin description

Name	Pin N°	Description
1	EN	Enables the device when connected to Vin and disables it when forced to GND.
2	VIN	Supply voltage. This pin is connected to the drain of the internal N-mos. Connect this pin to a capacitor larger than 10µF.
3	FB	Connecting this pin to a voltage divider it is possible to program the output voltage between 1.2V and 5V.
4	VOUT	Regulated output voltage. This pin is connected to the source of the internal N-mos. Connect this pin to a capacitor of 10µF.
5	PGOOD	Power good output. The pin is open drain and detects the output voltage. It is forced low if the output voltage is lower than 90% of the programmed voltage.
6	GND	Ground pin
7, 8	NC1-NC2	Internally not connected.

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2 Maximum ratings

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	VIN and PGOOD	14.5	V
	EN, OUT and ADJ	-0.3 to (Vin +0.3)	V

2.2 Thermal data

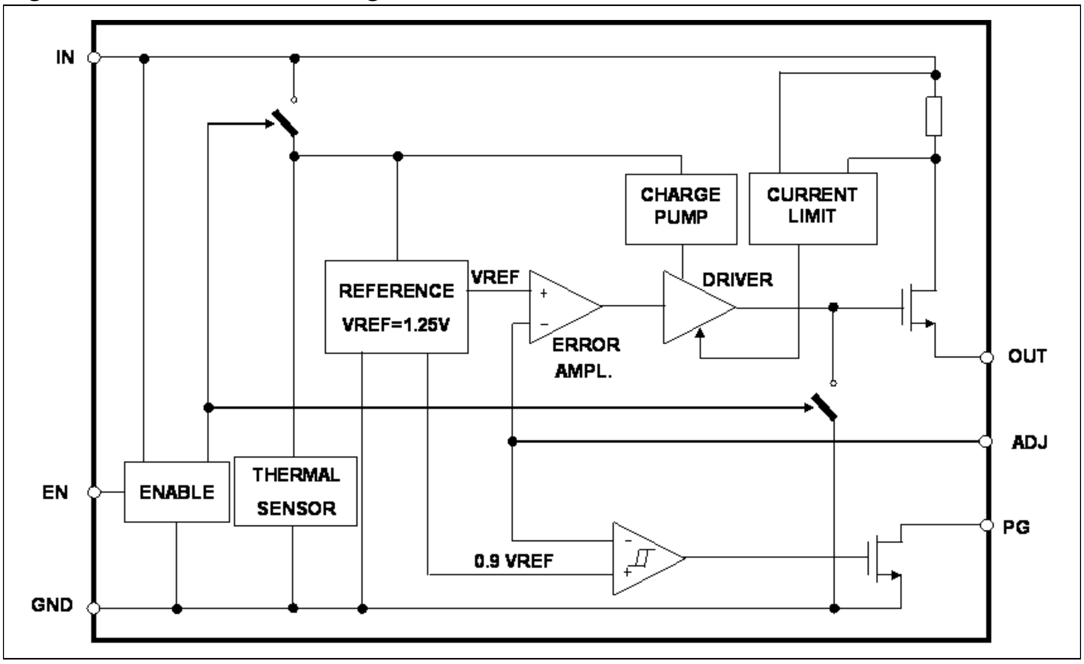
Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient	34 (1)	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to 150	°C

1. Package mounted on board

3 Block diagram

Figure 3. Internal block diagram



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4 Electrical characteristics

Table 5. Electrical characteristcs (T_J = 25°C, V_{IN} = 5V unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2		14	V
V_O	Output voltage	I_O = 0.1A; V_{IN} = 3.3V	1.188	1.2	1.212	V
	Line Regulation	V_{IN} = 2.5V ±10%; I_O = 10mA			5	mV
		V_{IN} = 3.3V ±10%; I_O = 10mA			5	mV
		V_{IN} = 5V ±10%; I_O = 10mA			5	mV
	Load Regulation	V_{IN} = 3.3V; 0.1A < I_O < 2A			15	mV
$r_{DS(on)}$	Drain Source ON resistance				200	mΩ
I_{OCC}	Current limiting		2.3	2.5	2.7	A
Iq	Quiescent current			0.2	0.4	mA
Ish	Shutdown current	2V < V_{IN} < 14V (1)			25	µA
	Ripple Rejection	f = 120Hz, I_O = 1A V_{IN} = 5V, ΔV_{IN} = 2Vpp	60	75		dB
Ven	EN Input Threshold		0.5	0.65	0.8	V
	Pgood threshold	Vo rise		90		%Vo
	Pgood Hysteresis			10		%Vo
	Pgood saturation	Ipgood = 1mA		0.2	0.4	V

1. Specification referred to T from -25°C to 125°C.

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5 Typical electrical performance

Figure 4. Output voltage vs junction temperature

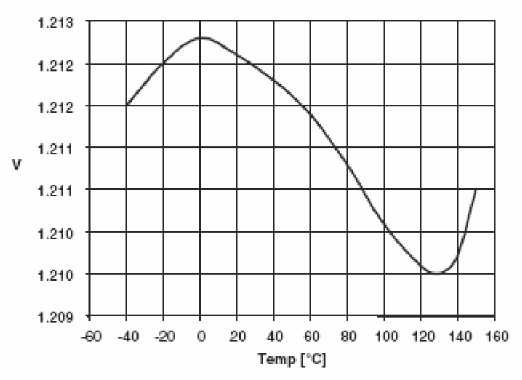


Figure 5. Quiescent current vs junction temperature

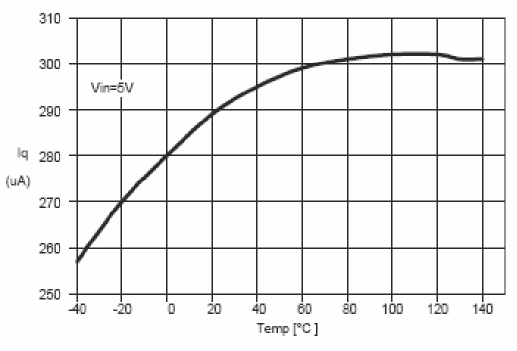
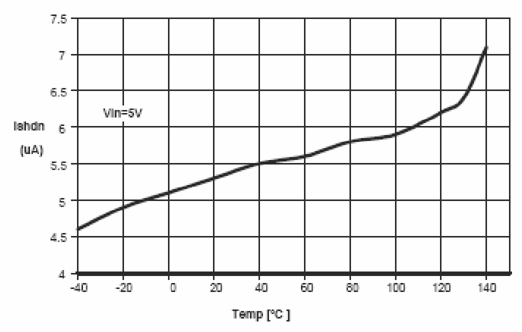


Figure 6. Shutdown current vs junction temperature



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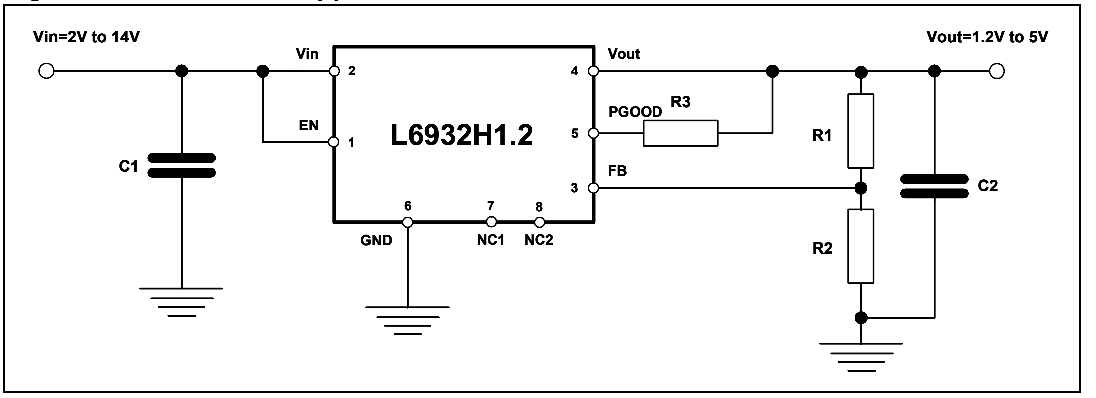
6 Application information

6.1 Application circuit

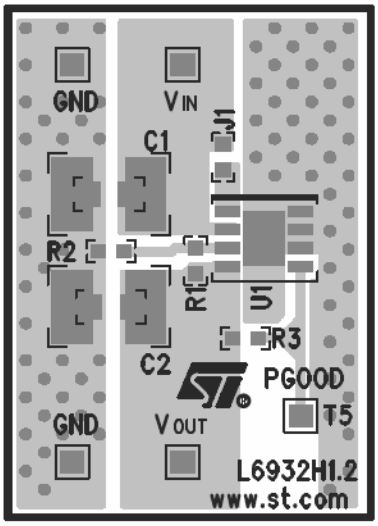
Figure 7. Demoboard application circuit



$$V_{OUT} = \frac{1.2}{R_2} \times (R_1 + R_2)$$

6.2 Demoboard layout

Figure 8. Demoboard layout



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6.3 Component part list

Table 6. Component par list

Reference	Part number	Description	Manufacturer
C1	GRM32ER6C226KE20B	22Uf, 16V	MURATA
C2	GRM32ER6C226KE20B	22Uf, 16V	MURATA
R1		N.M.	
R2		0Ω	
R3		100K	

7 Components selection

7.1 Input capacitor

The input capacitor value depends on a lot of factors such as load transient requirements, input source (battery or DC/DC converter) and its distance from the input cap. Usually a 47µF is enough for any application but a much lower value can be sufficient in many cases.

7.2 Output capacitor

The output capacitor choice depends basically on the load transient requirements. Tantalum, Special Polymer, POSCAP and aluminum capacitors are good and offer very low ESR values. Multilayer ceramic caps have the lowest ESR and can be required for particular applications. Nevertheless in several applications they are ok, the loop stability issue has to be considered (see loop stability section).

Below a list of some suggested capacitor manufacturers

Table 7. Suggested capacitor

Manufacturer	Type	Cap Value (µF)	Rated Voltage (V)
MURATA	CERAMIC	1 to 47	4 to 16
PANASONIC	CERAMIC	1 to 47	4 to 16
TAYO YUDEN	CERAMIC	1 to 47	4 to 16
TDK	CERAMIC	1 to 47	4 to 16
TOKIN	CERAMIC	1 to 47	4 to 16
SANYO	POSCAP	1 to 47	4 to 16
PANASONIC	SP	1 to 47	4 to 16
KEMET	TANTALUM	1 to 47	4 to 16

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7.3 Loop Stability

The stability of the loop is affected by the zero introduced by the output capacitor. The time constant of the zero is given by:

$$T = ESR \times C_{OUT}$$

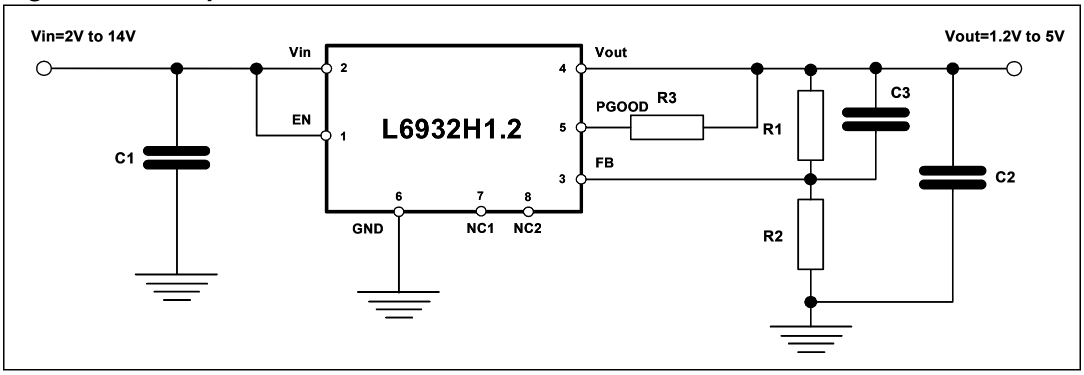
$$F_{ZERP} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

This zero helps to increase the phase margin of the loop until the time constant is higher than some hundreds of nsec, depending also on the output voltage and current.

So, using very low ESR ceramic capacitors could produce oscillations at the output, in particular when regulating high output voltages (adjustable version).

To solve this issue is sufficient to add a small capacitor (e.g. 1nF to 10nF) in parallel to the high side resistor of the external divider, as shown in *Figure 9*.

Figure 9. Compensation network



The thermal resistance junction to ambient of the demoboard is approximately 34°C/W.

This mean that, considering an ambient temperature of 60°C and, a maximum junction temperature of 150°C, the maximum power that the device can handle is 2.7W.

This means that the device is able to deliver a DC output current of 2A only with a very low dropout.

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8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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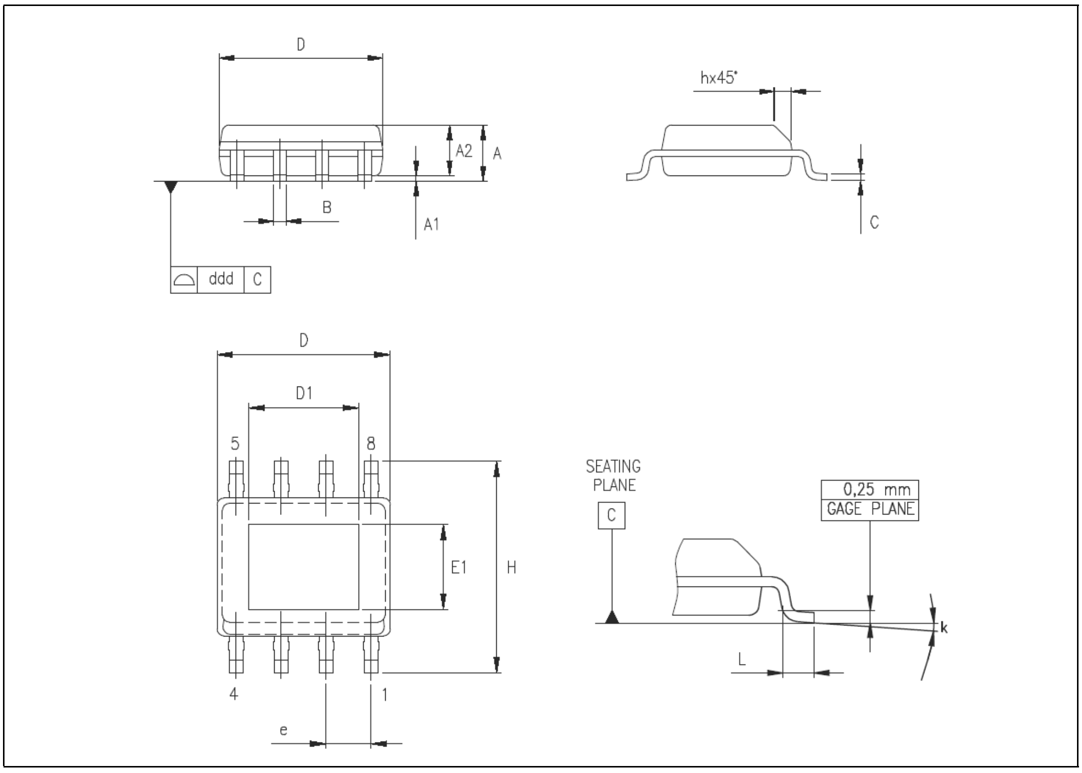
Table 8. HSO-8 Mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
D1		3.1			0.122	
E	3.80		4.00	0.150		0.157
E1		2.4			0.094	
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04

Figure 10. Package dimensions



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9 Revision history

Table 9. Revision history

Date	Revision	Changes
23-Jun-2006	1	First release
07-May-2007	2	Final release, mechanical data pad size updated

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