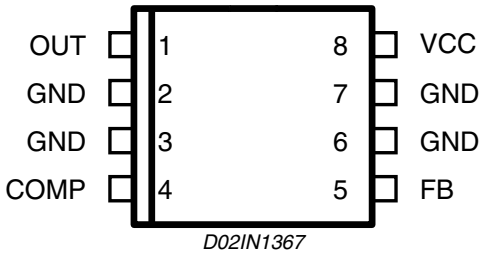
Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N°	Pin	Description
1	OUT	Regulator output.
2,3,6,7	GND	Ground.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23V. An external resistive divider is required for higher output voltages.
8	VCC	Unregulated DC input voltage.

2 Electrical data

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_8	Input voltage	40	V
V_1	Out pin DC voltage Out pin peak voltage at $\Delta t = 0.1\mu s$	-1 to 40 -5 to 40	V V
I_1	Maximum output current	int. limit.	
V_4, V_5	Analog pins	4	V
P_{tot}	Power dissipation at $T_A \leq 70°C$	1.2	W
T_j	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	SO8	Unit
R_{thJA}	Maximum thermal resistance junction-ambient	65 (1)	°C/W

1. Package mounted on board

3 Electrical characteristics

Table 4. Electrical characteristics (T_J = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
V_{CC}	Operating input voltage range	V_o = 1.235V; I_o = 2A	(1)	4.4		36	V
$R_{DS(on)}$	Mosfet on Resistance		(1)		0.250	0.5	Ω
I_l	Maximum limiting current	V_{CC} = 4.4V to 36V		2	2.5	3	A
f_s	Switching frequency		(1)	212	250	280	kHz
				225	250	275	kHz
	Duty cycle			0		100	%
Dynamic characteristics (see test circuit).							
V_5	Voltage feedback	4.4V < V_{CC} < 36V, 20mA < I_O < 2A		1.220	1.235	1.25	V
			(1)	1.198	1.235	1.272	V
h	Efficiency	V_O = 5V, V_{CC} = 12V			90		%
DC characteristics							
I_{qop}	Total operating quiescent current		(1)		3	5	mA
I_q	Quiescent current	Duty cycle = 0; V_{FB} = 1.5V				2.5	mA
Error amplfier							
V_{OH}	High level output voltage	V_{FB} = 1V		3.5			V
V_{OL}	Low level output voltage	V_{FB} = 1.5V				0.4	V
$I_{o\ source}$	Source output current	V_{COMP} = 1.9V; V_{FB} = 1V		200	300		µA
$I_{o\ sink}$	Sink output current	V_{COMP} = 1.9V; V_{FB} = 1.5V		1	1.5		mA
I_b	Source bias current				2.5	4	µA
	DC open loop gain	R_L = ∞		50	65		dB
gm	Transconductance	I_{comp} = -0.1mA to 0.1mA V_{COMP} = 1.9V			2.3		mS

1. Specification Referred to T_J from -40 to 125°C. Specification over the -40 to +125 T_J Temperature range are assured by design, characterization and statistical correlation.

4 Typical characteristics

Figure 3. Output voltage vs. junction temperature

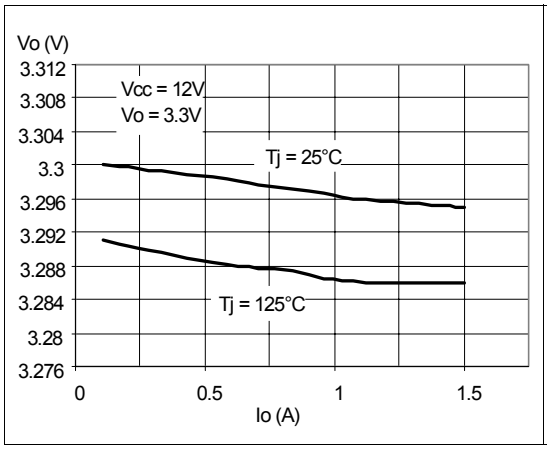


Figure 4. Quiescent current vs. junction temperature

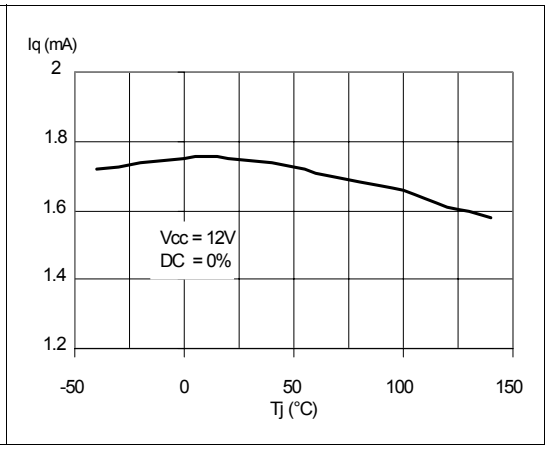


Figure 5. Line regulator

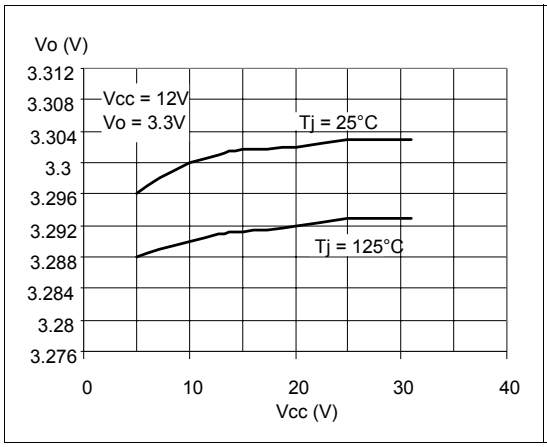


Figure 6. Shutdown current vs. junction temperature

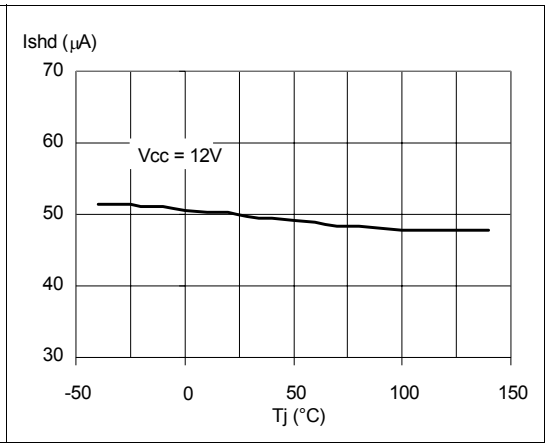


Figure 7. Output voltage vs. junction temperature

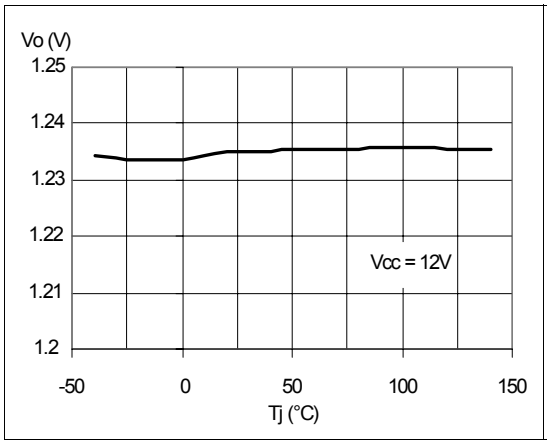
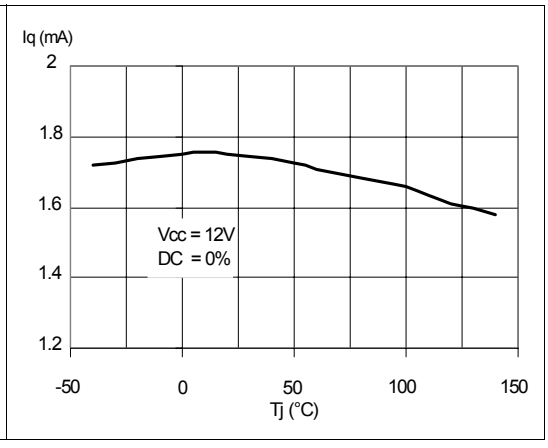


Figure 8. Switching frequency vs. junction temperature



5 Application circuit

In figure 8 is shown the demo board application circuit for the device in SMD version, where the input supply voltage, Vcc, can range from 4.4V to 25V due to the rated voltage of the input capacitor and the output voltage is adjustable from 1.235V to V_{cc}.

Figure 9. Demo board application circuit

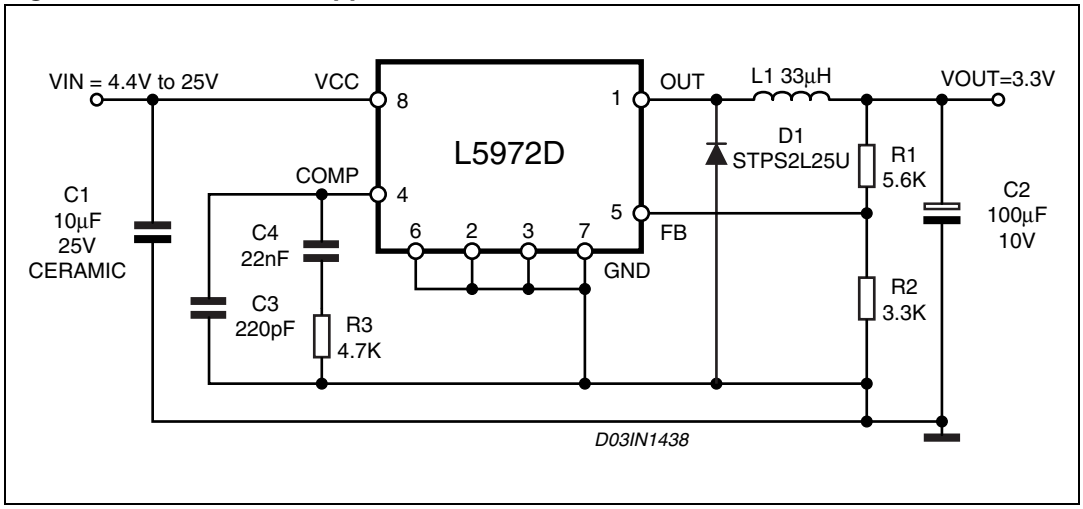


Table 5. Component list

Reference	Part number	Description	Manufacturer
C1	GRM32DR61E106KA12L	10µF, 25V	MURATA
C2	POSCAP 10TPB100M	100µF, 10V	Sanyo
C3	C1206C221J5GAC	220pF, 5%, 50V	KEMET
C4	C1206C223K5RAC	22nF, 10%, 50V	KEMET
R1		5.6K, 1%, 0.1W 0603	Neohm
R2		3.3K, 1%, 0.1W 0603	Neohm
R3		4.7K, 1%, 0.1W 0603	Neohm
D1	STPS2L25U	2A, 25V	ST
L1	DO3316P-333	33µH, 2.1A	COILCRAFT

Figure 10. PCB layout (component side)

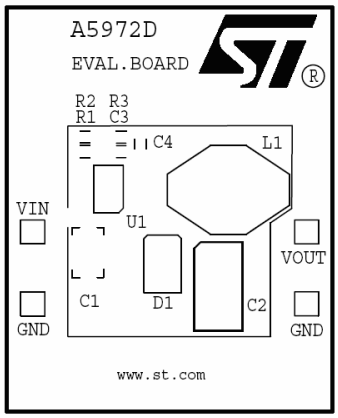


Figure 11. PCB layout (bottom side)

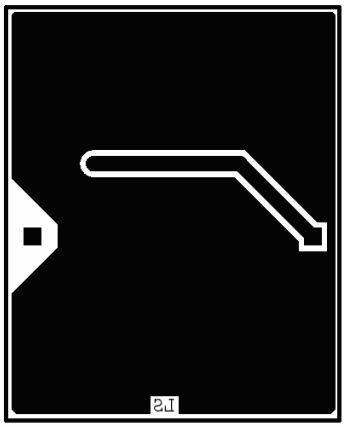
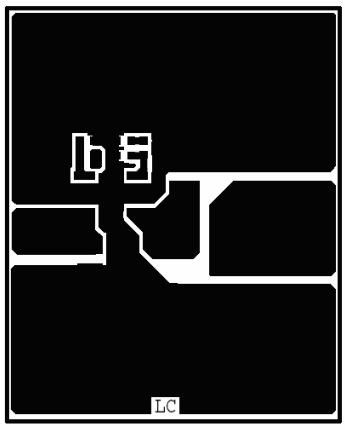


Figure 12. PCB layout (front side)



Sideways two graphs show the T_J versus output current in different conditions of the input and output voltage.

Figure 13. Junction temperature vs output current

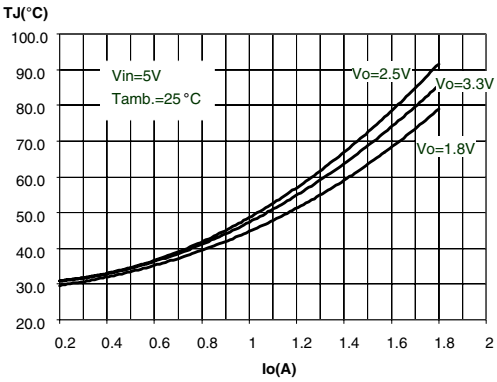


Figure 14. Efficiency vs output current

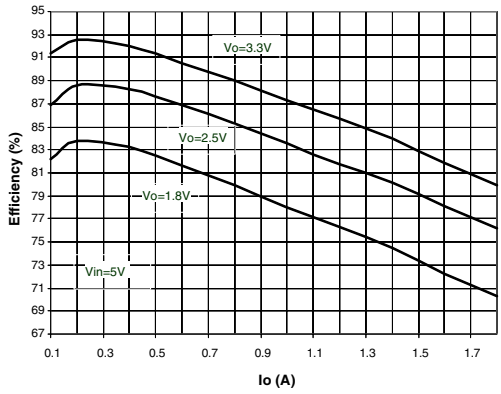


Figure 15. Junction temperature vs output current

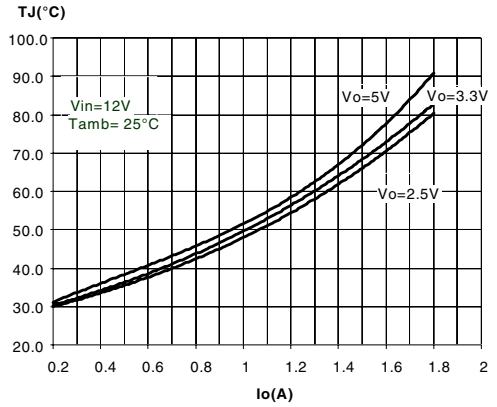
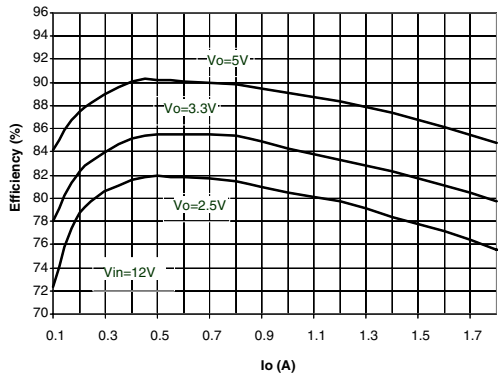


Figure 16. Efficiency vs output current



6 Application ideas

Figure 17. Positive buck-boost regulator

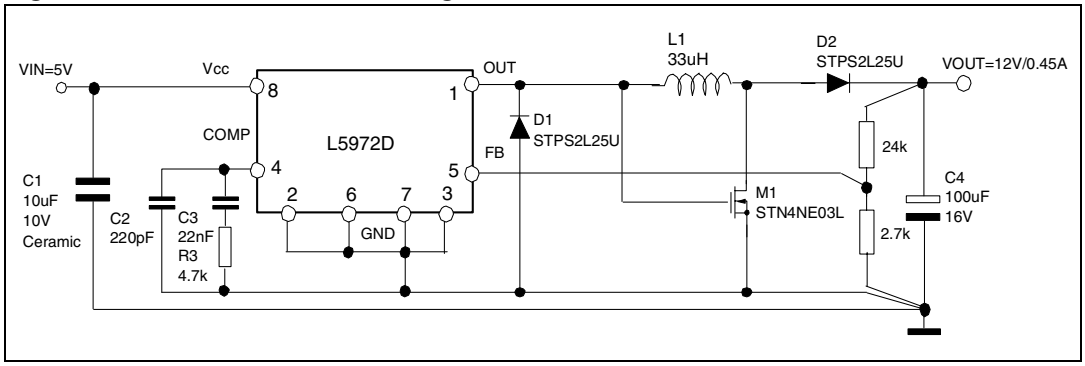


Figure 18. Buck-boost regulator

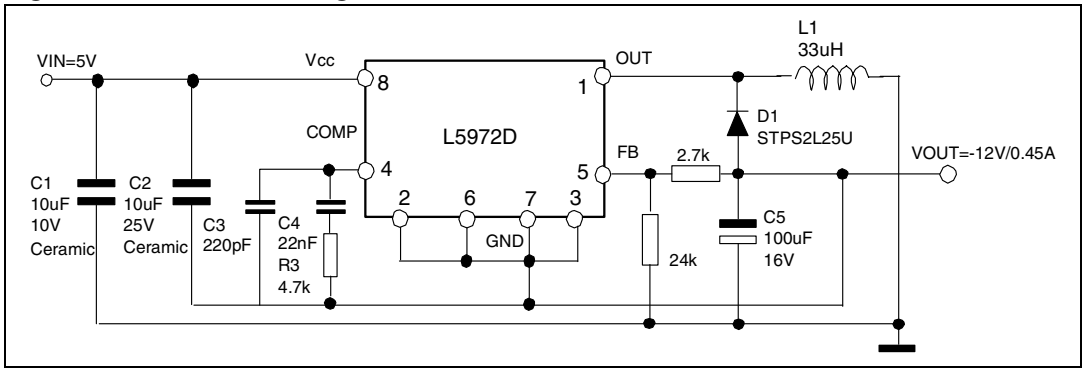
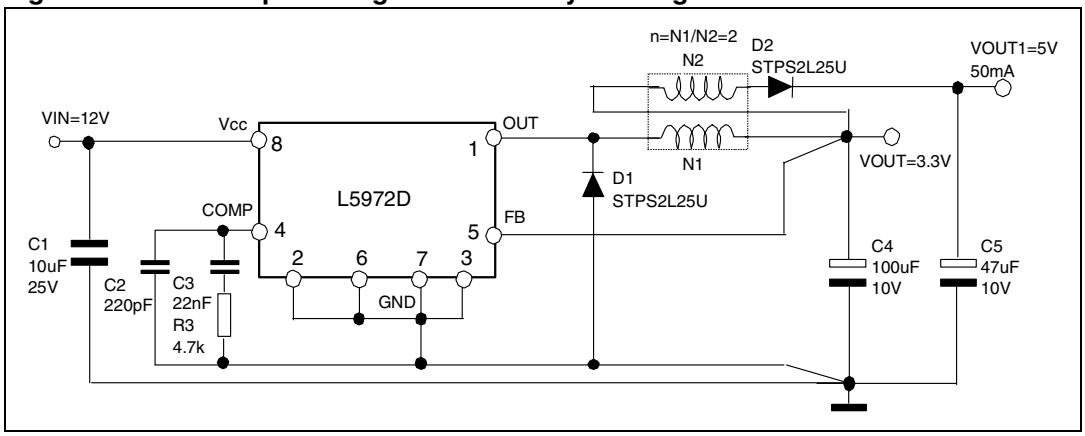


Figure 19. Dual output voltage with auxiliary winding



7 Package mechanical data

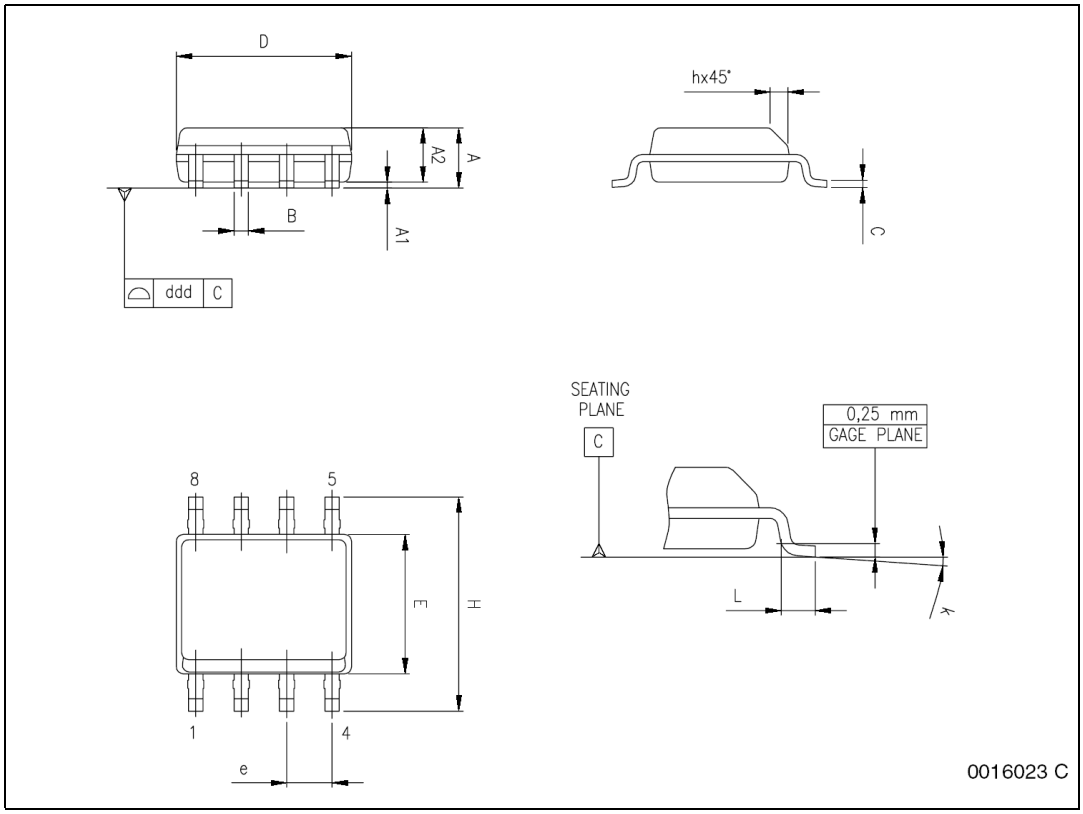
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 6. SO-8 Mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protru-sions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 20. Package dimensions



8 Order codes

Table 7. Order codes

Part number	Package	Packaging
L5972D	SO8	Tube
L5972D013TR	SO8	Tape and reel

9 Revision history

Table 8. Revision history

Date	Revision	Changes
02-Feb-2007	8	Updated *Table 5 on page 7*
10-Apr-2007	9	Mechanical data typo
16-Oct-2007	10	Updated *Section 5: Application circuit on page 7*

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