

Contents

1	Block diagram and pin configuration	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	7
2.3	Electrical characteristics	8
2.4	Electrical characteristics curves	11
2.5	Test circuit and waveforms plot	14
2.5.1	Load regulation	14
3	Application information	16
3.1	Voltage regulator	16
3.2	Reset	17
3.3	Watchdog	18
4	Package and PCB thermal data	19
4.1	SO-8 thermal data	19
4.2	SO-20 thermal data	22
5	Package and packing information	25
5.1	ECOPACK® packages	25
5.2	SO-8 package information	25
5.3	SO-20 package information	27
5.4	SO-8 packing information	28
5.5	SO-20 packing information	30
6	Revision history	31

List of tables

Table 1. Device summary 1

Table 2. Pins description 6

Table 3. Absolute maximum ratings 7

Table 4. Thermal data. 7

Table 5. General 8

Table 6. Reset 9

Table 7. Watchdog 9

Table 8. Watchdog Enable 10

Table 9. SO-8 thermal parameter 21

Table 10. SO-20 thermal parameter 24

Table 11. SO-8 mechanical data 26

Table 12. SO-20 mechanical data 27

Table 13. Document revision history 31

List of figures

Figure 1.	Block diagram	5
Figure 2.	Pins configuration	6
Figure 3.	Output voltage vs. T_j	11
Figure 4.	Output voltage vs. V_s	11
Figure 5.	Drop Voltage vs. Output Current	11
Figure 6.	Current consumption vs. Output Current	11
Figure 7.	Current consumption vs. Input Voltage	11
Figure 8.	Current limitation vs. T_j	11
Figure 9.	Current limitation vs. Input Voltage	12
Figure 10.	Short Circuit Current vs. T_j	12
Figure 11.	Short Circuit Current vs. Input Voltage	12
Figure 12.	V_{WEN_high} vs. T_j	12
Figure 13.	V_{WEN_LOW} vs. T_j	12
Figure 14.	V_{rhth} vs. T_j	12
Figure 15.	V_{rlth} vs. T_j	13
Figure 16.	V_{whth} vs. T_j	13
Figure 17.	V_{wlth} vs. T_j	13
Figure 18.	I_{cr} & I_{cwc} vs. T_j	13
Figure 19.	I_{dr} & I_{cwd} vs. T_j	13
Figure 20.	T_{wop} vs. T_j	13
Figure 21.	PSRR	14
Figure 22.	Load regulation test circuit	14
Figure 23.	Maximum load variation response	15
Figure 24.	L4988 application schematic	16
Figure 25.	Behavior of output current versus regulated voltage V_o	17
Figure 26.	Reset timing diagram	18
Figure 27.	Watchdog timing diagram	18
Figure 28.	SO-8 PC board	19
Figure 29.	SO-8 $R_{thj-amb}$ Vs. PCB copper area in open box free air condition	19
Figure 30.	SO-8 thermal impedance junction ambient single pulse	20
Figure 31.	SO-8 thermal fitting model of a single channel	20
Figure 32.	SO-20 PC board	22
Figure 33.	SO-20 $R_{thj-amb}$ Vs. PCB copper area in open box free air condition	22
Figure 34.	SO-20 thermal impedance junction ambient single pulse	23
Figure 35.	SO-20 thermal fitting model of a single channel	23
Figure 36.	SO-8 package dimensions	25
Figure 37.	SO-20 package dimensions	27
Figure 38.	SO-8 tube shipment (no suffix)	28
Figure 39.	SO-8 tape and reel shipment (suffix "TR")	29
Figure 40.	SO-20 tube shipment (no suffix)	30

1 Block diagram and pin configuration

Figure 1. Block diagram

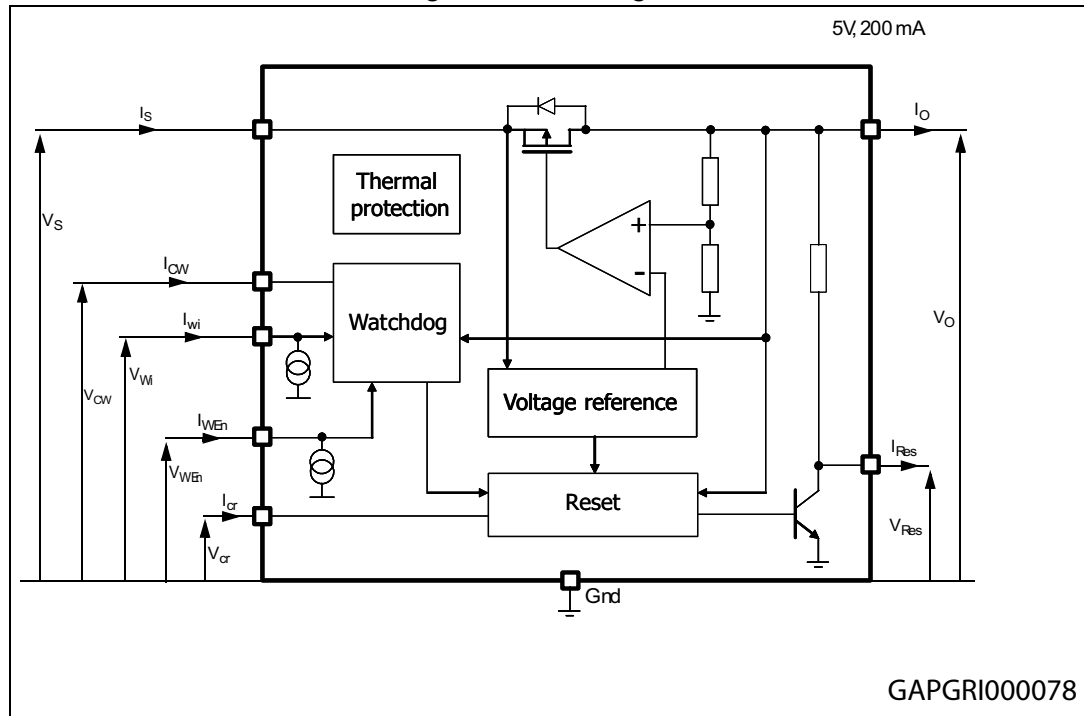
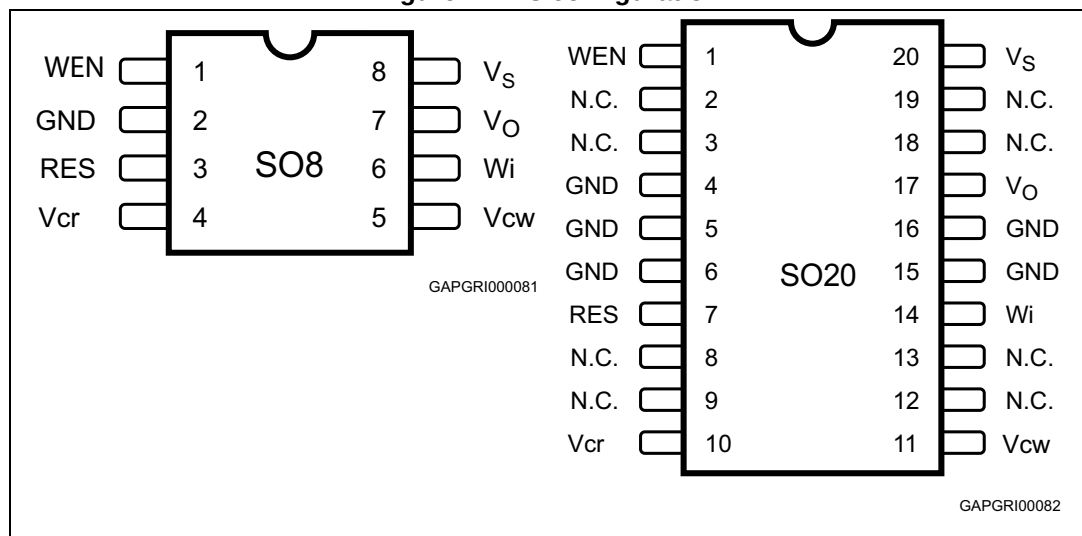


Table 2. Pins description

Pin name	SO8(D)	SO20(MD)	Function
WEn	1	1	Watchdog Enable input If high watchdog functionality is active
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground. Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
Vo	7	17	Voltage regulator output Block to ground with a capacitor >100nF (needed for regulator stability)
Vs	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

Figure 2.Pins configuration



2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{Sdc}	DC supply voltage	-0.3 to 40	V
I_{Sdc}	Input current	Internally limited	
V_{Vo}	DC output voltage	-0.3 to 6 ⁽¹⁾	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{od}	Open Drain output voltage	-0.3 to $V_{Vo} + 0.3$	V
I_{od}	Open Drain output current	Internally limited	
V_{cr}	Reset delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{cw}	Watchdog delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{WEi}	Watchdog Enable input voltage	-0.3 to $V_{Vo} + 0.3$	V
T_j	Junction temperature	-40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

1. Using the typical application schematic with $C_{out} = 10 \mu F$ and $I_{out} = 0 A$, when the regulator is switched-on, an overshoot exceeding 6 V could occur. This behavior does not impact the reliability of the regulator.

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	S08	S016+2+2	Unit
$R_{th-jamb}$	Thermal resistance junction to ambient	130 ⁽¹⁾	51 ⁽²⁾	°C/W

1. With copper area 2 cm²; for details see [Figure 29](#).
 2. With copper area 6 cm²; for details see [Figure 33](#).

2.3 Electrical characteristics

$V_S = 5.6\text{V}$ to 31V , $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$ unless otherwise specified.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vo	V_{O_ref}	Output voltage	$V_S = 6$ to 31V $I_O = 1$ to 200mA	4.9	5.0	5.1	V
Vo	I_{short}	Short circuit current	$V_S = 13.5\text{V}^{(1)}$	200	280	500	mA
Vo	$I_{lim}^{(2)}$	Output current limitation	$V_S = 13.5\text{V}^{(1)}$	200	350	600	mA
V_S, V_O	V_{line}	Line regulation voltage	$V_S = 6$ to 31V $I_O = 1$ to 200mA			25	mV
Vo	V_{load}	Load regulation voltage	$I_O = 1$ to 200mA			25	mV
V_S, V_O	$V_{dp}^{(3)}$	Drop voltage	$I_O = 200\text{mA}$		270	500	mV
V_S, V_O	$V_{dp}^{(3)}$	Drop voltage	$I_O = 150\text{mA}$		200	400	mV
V_S, V_O	SVR	Ripple rejection	$f_r = 100\text{Hz}^{(4)}$		60		dB
V_S, V_O	I_{qn_200}	Quiescent current	$V_S=13.5\text{V}$, $I_O=200\text{mA}$, WEn = high		1.9	2.5	mA
V_S, V_O	I_{qn_50}	Quiescent current	$V_S=13.5\text{V}$, $I_O= 50\text{mA}$, WEn = high		500	700	μA
V_S, V_O	$I_{q_1_we}$	Quiescent current	$V_S=13.5\text{V}$, $I_O < 1\text{mA}$, WEn = high		93	200	μA
V_S, V_O	$I_{q_1_wd}$	Quiescent current	$V_S=13.5\text{V}$, $I_O < 1\text{mA}$, WEn = low		75	150	μA
	T_W	Thermal protection temperature		150		190	$^\circ\text{C}$
	T_{W_hy}	Thermal protection temperature hysteresis			10		$^\circ\text{C}$

1. See [Figure 3](#).
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at $V_S=13.5\text{V}$ and $I_O= 75\text{mA}$.
3. V_S-V_O measured when the output voltage has dropped 100mV from its nominal value obtained at $V_S=13.5\text{V}$ and $I_O= 75\text{mA}$.
4. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Res	Vres_l	Reset output low voltage	$R_{ext} = 5\text{ k}\Omega$ to V_o , $V_o > 1\text{ V}$			0.4	V
Res	I _{Res_h}	Reset output high leakage current	$V_{Res} = 5\text{ V}$			1	μA
Res	R_p_u	Pull up internal resistance	With respect to V_o	12	25	50	$\text{k}\Omega$
Res	V _{o_th}	V_o out of regulation threshold	$V_s = 6\text{ to }31\text{ V}$, $I_o = 1\text{ to }200\text{ mA}$	6%	8%	10%	Below V_{o_ref}
Vcr	Vrlth	Reset timing low threshold	$V_s = 13.5\text{ V}$	10%	13%	16%	V_{o_ref}
Vcr	Vrhth	Reset timing high threshold	$V_s = 13.5\text{ V}$	44%	47%	50%	V_{o_ref}
Vcr	I _{cr}	Charge current	$V_s = 13.5\text{ V}$	8	17.6	30	μA
Vcr	I _{dr}	Discharge current	$V_s = 13.5\text{ V}$	8	17.6	30	μA
Res	Trr_2	Reset reaction time ⁽¹⁾	$V_o = V_{o_th} - 100\text{ mV}$	100	275	1000	μs
Res	Trd	Reset delay time	$V_s = 13.5\text{ V}$, $C_{tr} = 1\text{ nF}$	65		150	ms

1. When V_o becomes lower than 4V, the reset reaction time decreases down to 2 μs assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Wi	V _{ih}	Input high voltage	$V_s = 13.5\text{ V}$	3.5			V
Wi	V _{il}	Input low voltage	$V_s = 13.5\text{ V}$			1.5	V
Wi	V _{ih}	Input hysteresis	$V_s = 13.5\text{ V}$		500		mV
Wi	I _i	Pull down current	$V_s = 13.5\text{ V}$		10	20	μA
Vcw	V _{whth}	High threshold	$V_s = 13.5\text{ V}$	44%	47%	50%	V_{o_ref}
Vcw	V _{wlth}	Low threshold	$V_s = 13.5\text{ V}$	10%	13%	16%	V_{o_ref}
Vcw	I _{cwc}	Charge current	$V_s = 13.5\text{ V}$, $V_{cw} = 0.1\text{ V}$	4	8	14	μA
Vcw	I _{cwd}	Discharge current	$V_s = 13.5\text{ V}$, $V_{cw} = 2.5\text{ V}$	1.0	2.1	4.5	μA
Vcw	Twop	Watchdog period	$V_s = 13.5\text{ V}$, $C_{tw} = 47\text{ nF}$	25	50	90	ms
Res	twol	Watchdog output low time	$V_s = 13.5\text{ V}$, $C_{tw} = 47\text{ nF}$	6	10.5	22	ms

Table 8. Watchdog Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
WEn	V _{En_l}	Enable input low voltage				1	V
WEn	V _{En_h}	Enable input high voltage		3			V
WEn	V _{En_hy}	Enable input hysteresis		500	800	1100	mV
WEn	I _{leak}	Pull down current	WEn = 5V	2	8	20	μA

2.4 Electrical characteristics curves

Figure 3. Output voltage vs. Tj

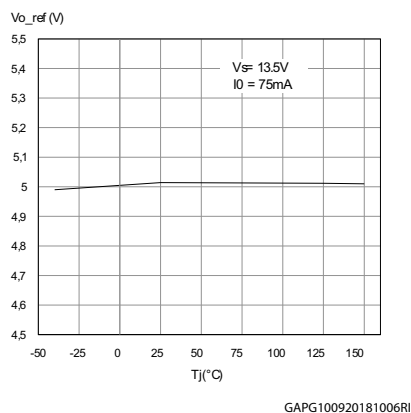


Figure 4. Output voltage vs. Vs

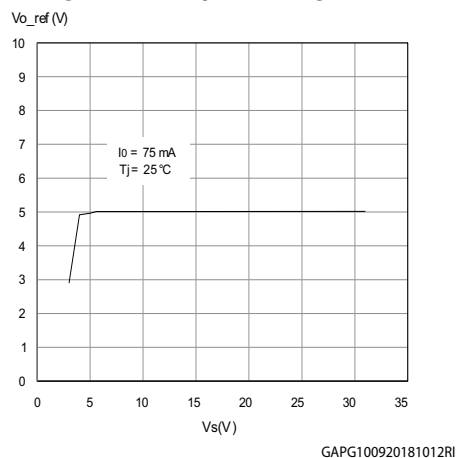


Figure 5. Drop Voltage vs. Output Current

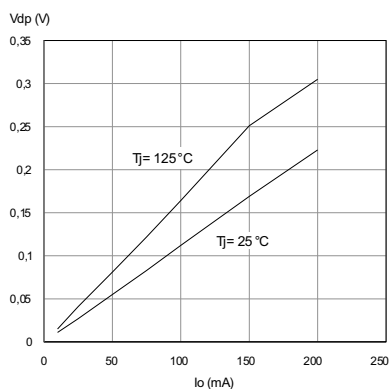


Figure 6. Current consumption vs. Output Current

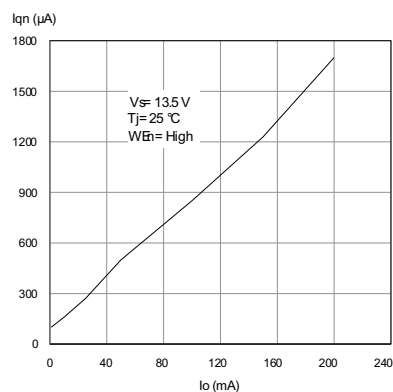


Figure 7. Current consumption vs. Input Voltage

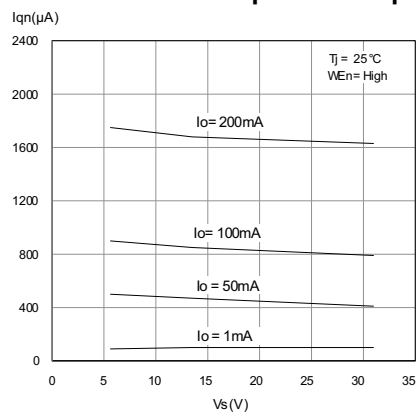


Figure 8. Current limitation vs. Tj

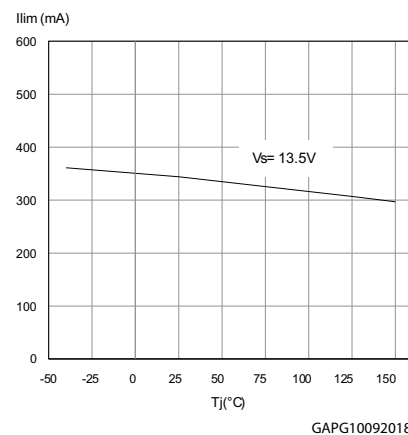


Figure 9. Current limitation vs. Input Voltage

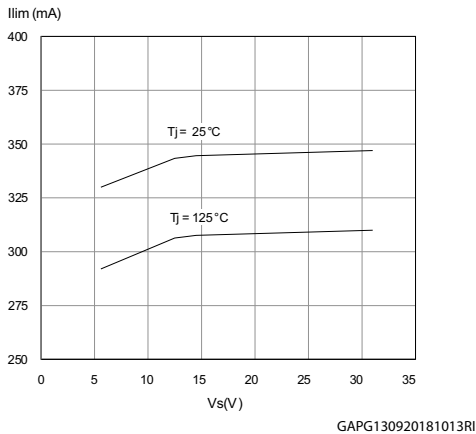


Figure 10. Short Circuit Current vs. Tj

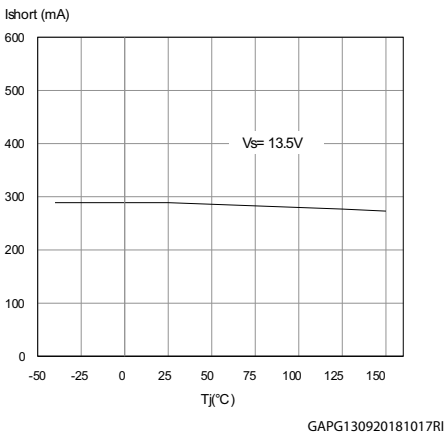


Figure 11. Short Circuit Current vs. Input Voltage

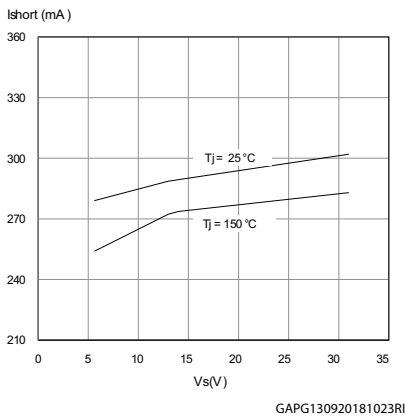


Figure 12. V_{WEn_high} vs. Tj

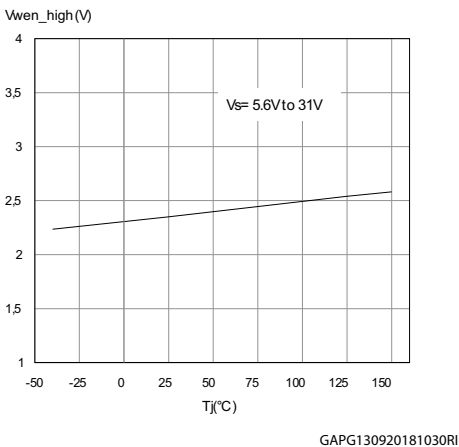


Figure 13. V_{WEn_LOW} vs. Tj

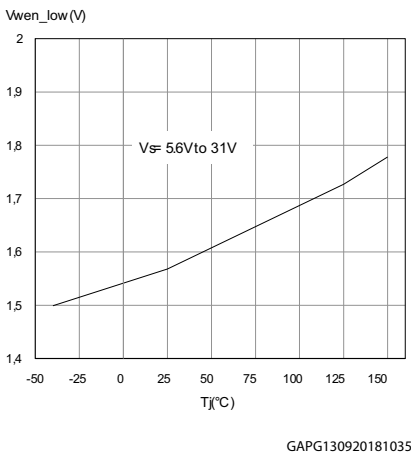


Figure 14. V_{rhth} vs. Tj

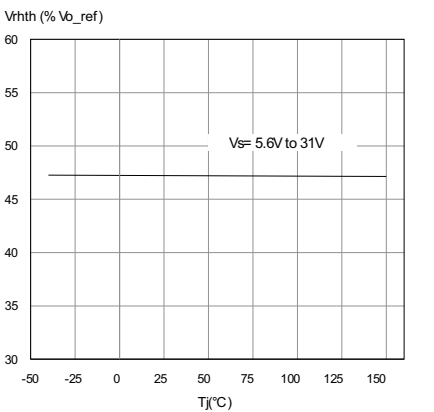
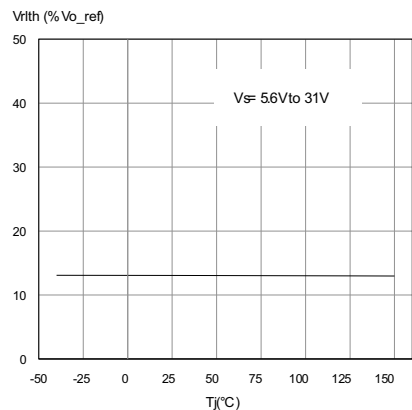
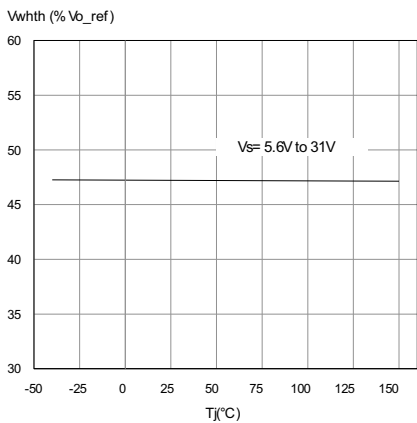


Figure 15. V_{rlth} vs. T_j



GAPG130920181100RI

Figure 16. V_{whth} vs. T_j



GAPG130920181057RI

Figure 17. V_{wlth} vs. T_j

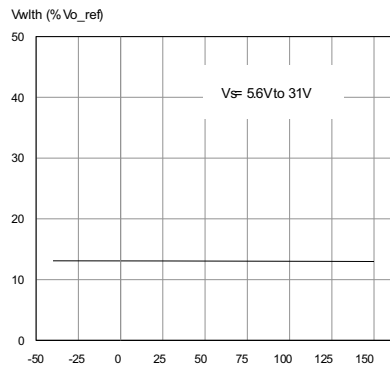


Figure 18. I_{cr} & I_{cwc} vs. T_j

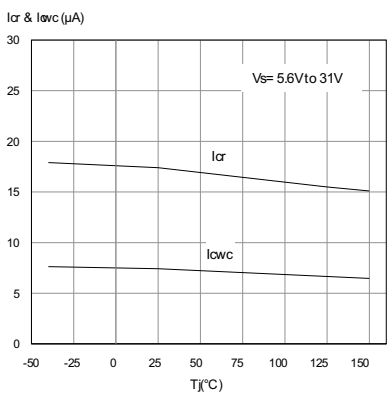


Figure 19. I_{dr} & I_{dwd} vs. T_j

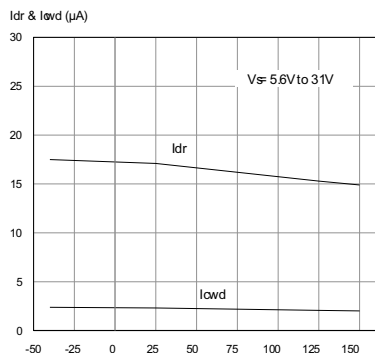
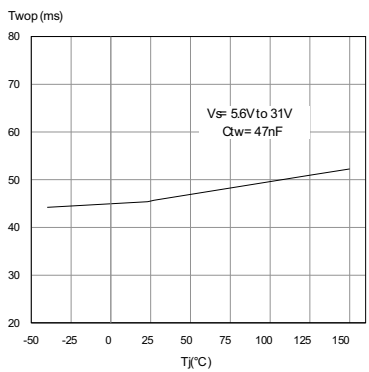
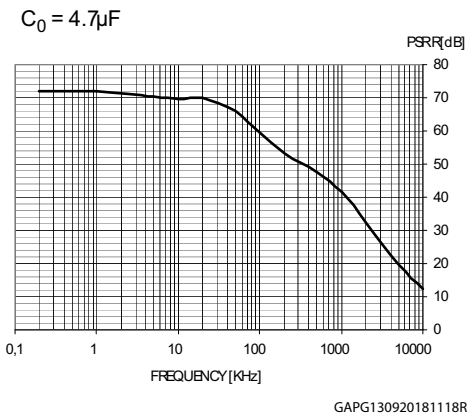


Figure 20. T_{wop} vs. T_j



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Figure 21. PSRR



2.5 Test circuit and waveforms plot

2.5.1 Load regulation

Figure 22. Load regulation test circuit

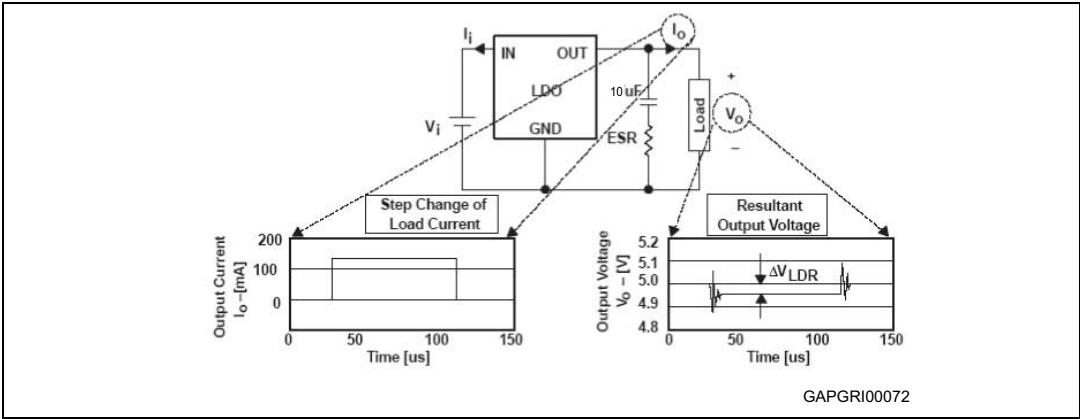
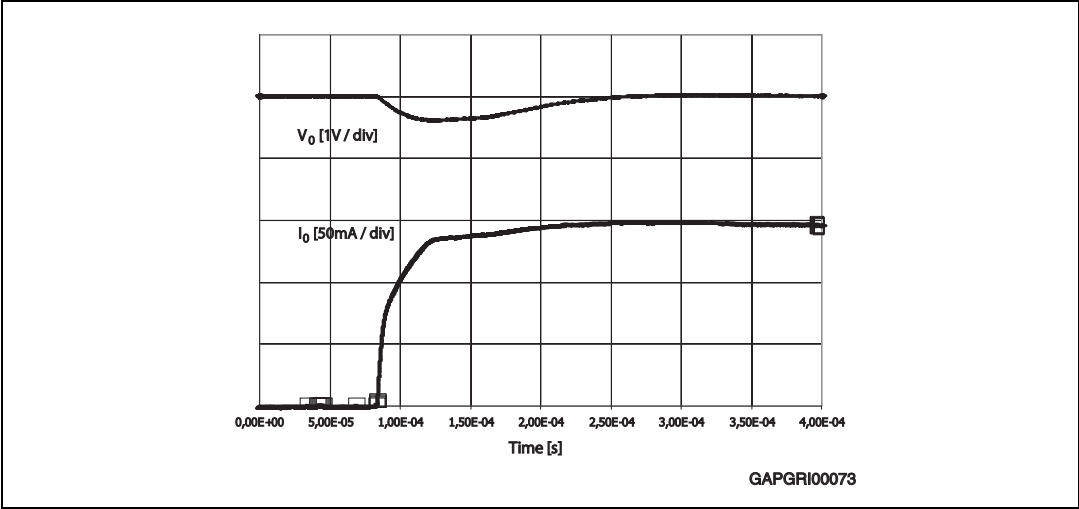
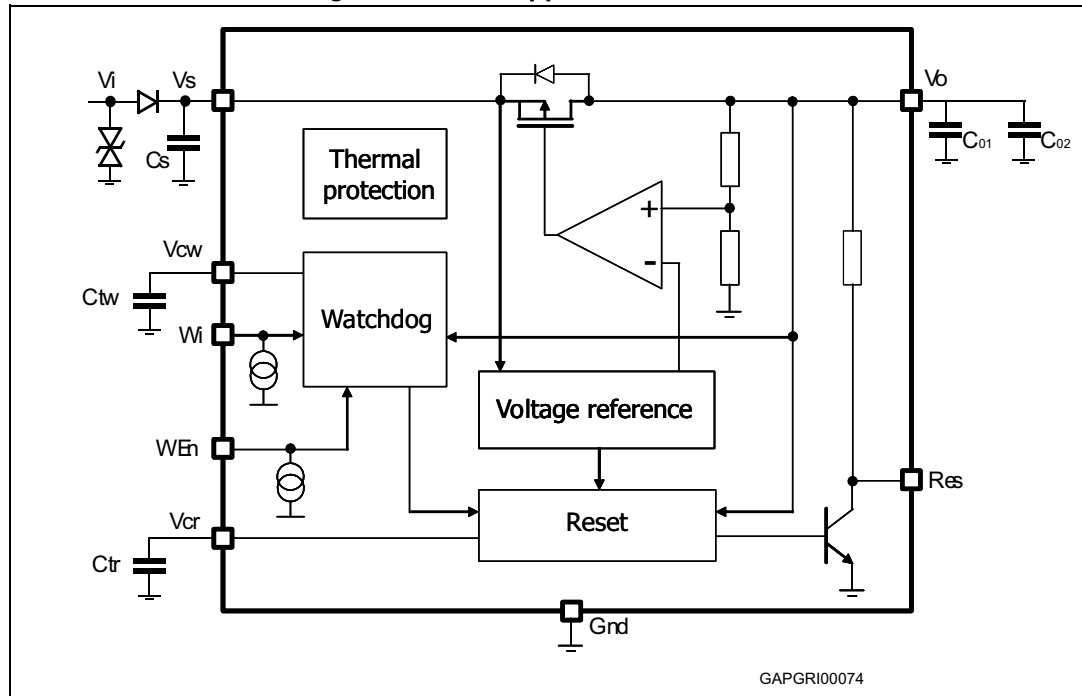


Figure 23.Maximum load variation response



3 Application information

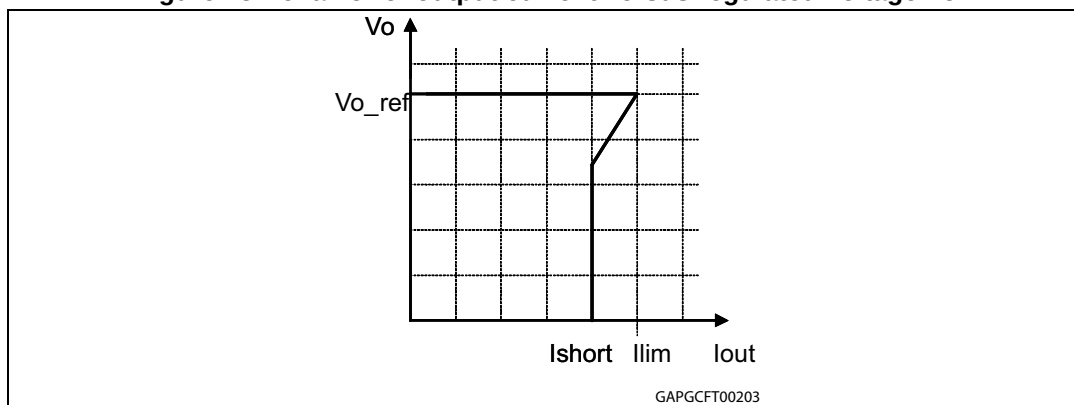
Figure 24.L4988 application schematic



Note: The input capacitor $C_s > 200\text{nF}$ is necessary for the smoothing of line disturbances. The output capacitor $C_{o1} > 100\text{nF}$ is necessary for the stability of the regulation loop. In order to damp output voltage oscillations during high load current surges, it is recommended to put an additional electrolytic capacitor $C_{o2} > 10\mu\text{F}$ at the output pin.

3.1 Voltage regulator

Voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at currents up to 200mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided. The high precision of the output voltage is obtained with a pre-trimmed reference voltage.

Figure 25. Behavior of output current versus regulated voltage V_o 

3.2 Reset

The reset circuit supervises the output voltage V_o . The V_{o_th} reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than V_{o_th} then Res goes low with a reaction time t_{rr} . The reset low signal is guaranteed for an output voltage V_o greater than 1V.

When the output voltage becomes higher than V_{o_th} then Res goes high with a delay t_{rd} . This delay is obtained by an internal oscillator.

The oscillator period is given by:

$$T_{osc} = [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{cr} + [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{dr}$$

where:

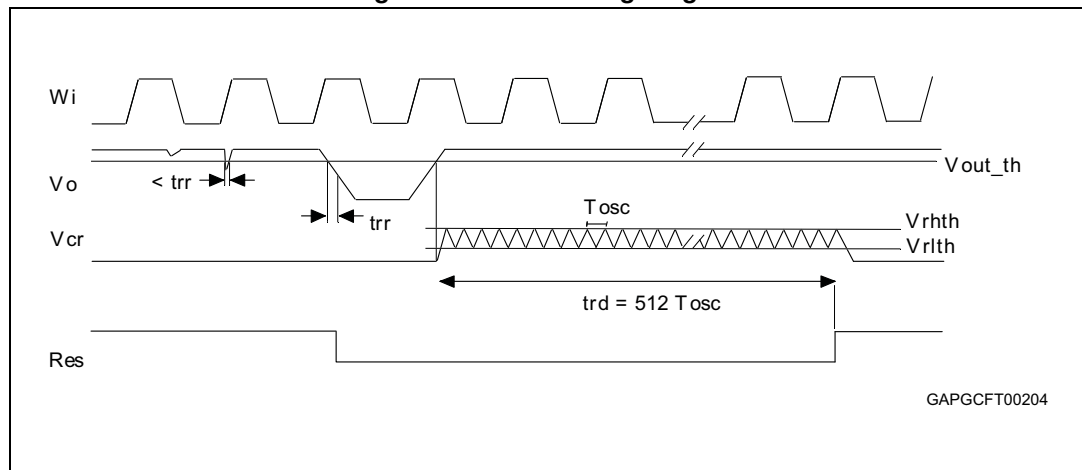
- I_{cr} : is an internally generated charge current
- I_{dr} : is an internally generated discharge current
- V_{rhth} , V_{rlth} : are two voltages defined with the output voltage and a resistor output divider
- C_{tr} : is an external capacitance.

t_{rd} is given by:

$$t_{rd} = 512 \times T_{osc}$$

Reset is active when En is high.

Figure 26.Reset timing diagram



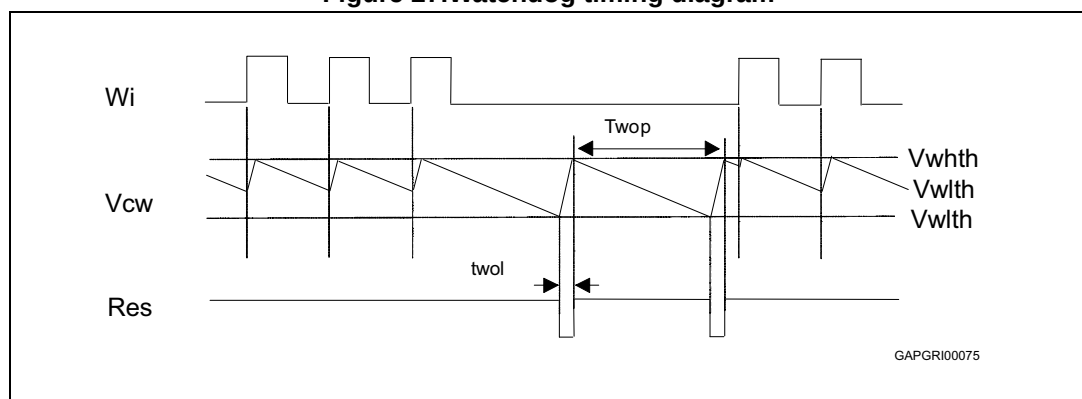
3.3 Watchdog

A connected microcontroller is monitored by the watchdog input **Wi**. If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, C_{tw} . The watchdog circuit discharges the capacitor C_{tw} with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time t , during which the micro-controller must output the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every **Wi** positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth} , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw} .

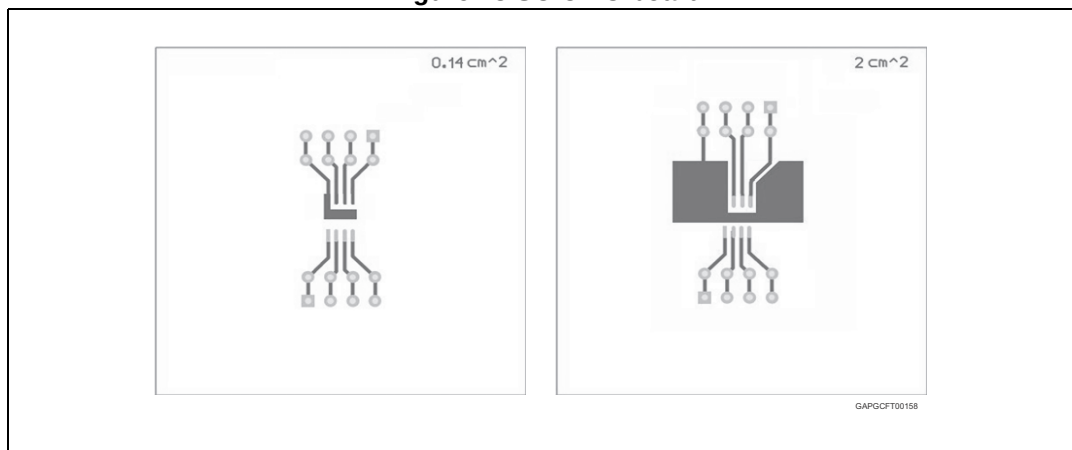
Figure 27.Watchdog timing diagram



4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 28.SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35 μ m, Copper areas: from minimum pad lay-out to 8cm²)

Figure 29.SO-8 $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

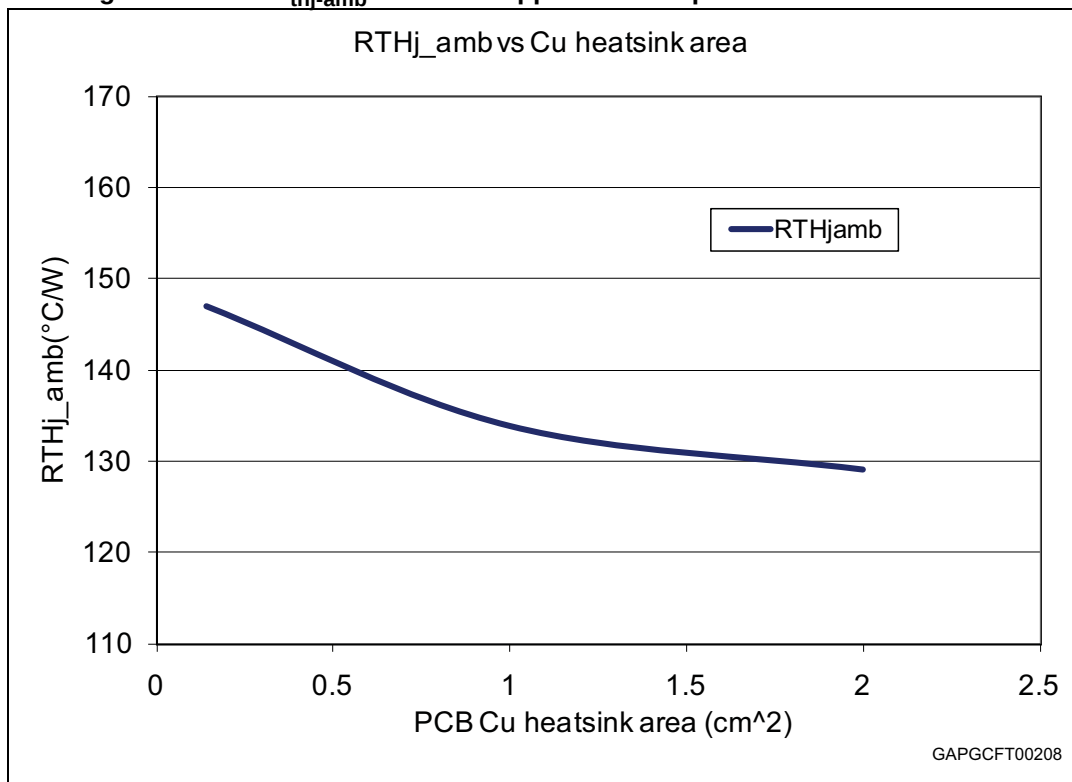
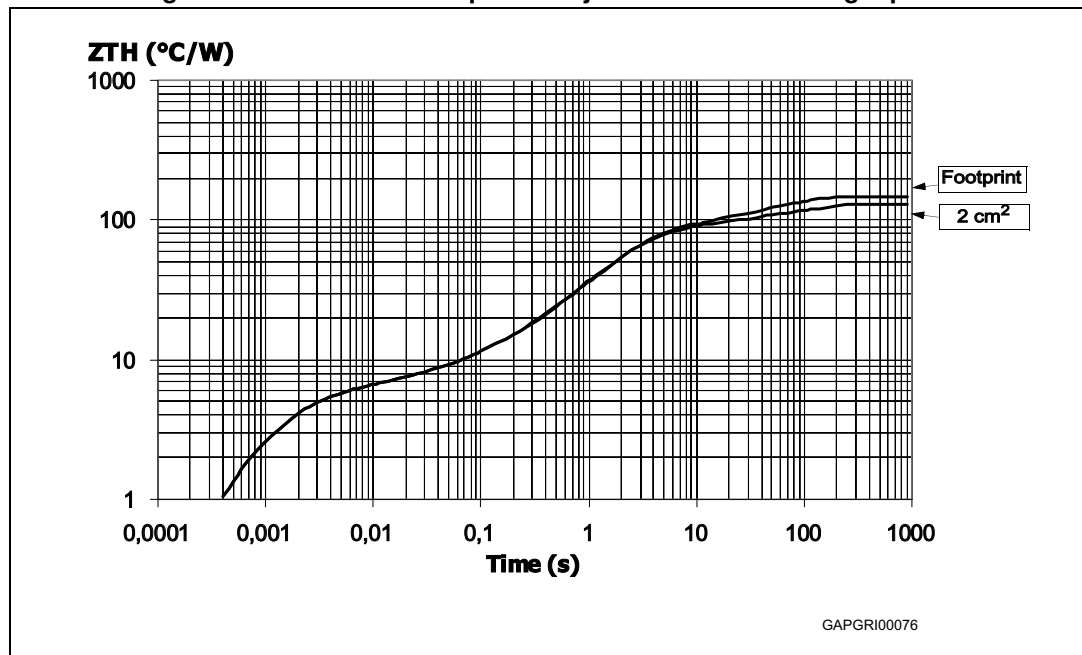


Figure 30.S0-8 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 31.S0-8 thermal fitting model of a single channel

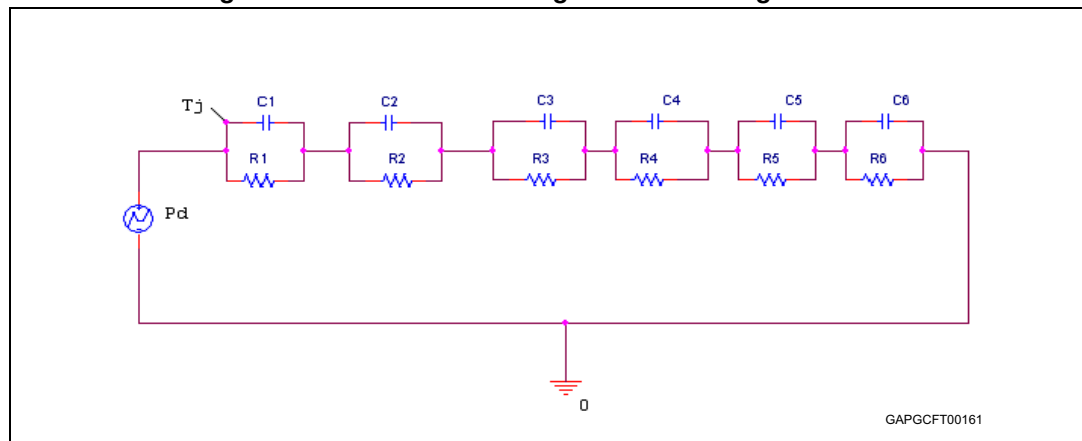
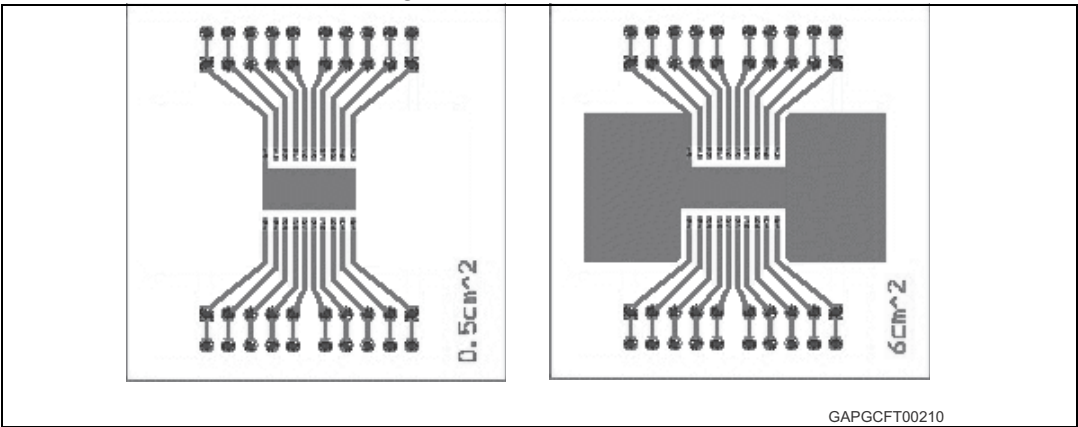


Table 9. SO-8 thermal parameter

Areal island (cm ²)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2	
R4 (°C/W)	41	
R5 (°C/W)	40	
R6 (°C/W)	58	40
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.04	
C5 (W.s/°C)	0.1	
C6 (W.s/°C)	1.05	2

4.2 SO-20 thermal data

Figure 32.SO-20 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm,PCB thickness = 2mm, Cu thickness=35 μ m , Copper areas: from minimum pad lay-out to 8cm²).

Figure 33.SO-20 $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

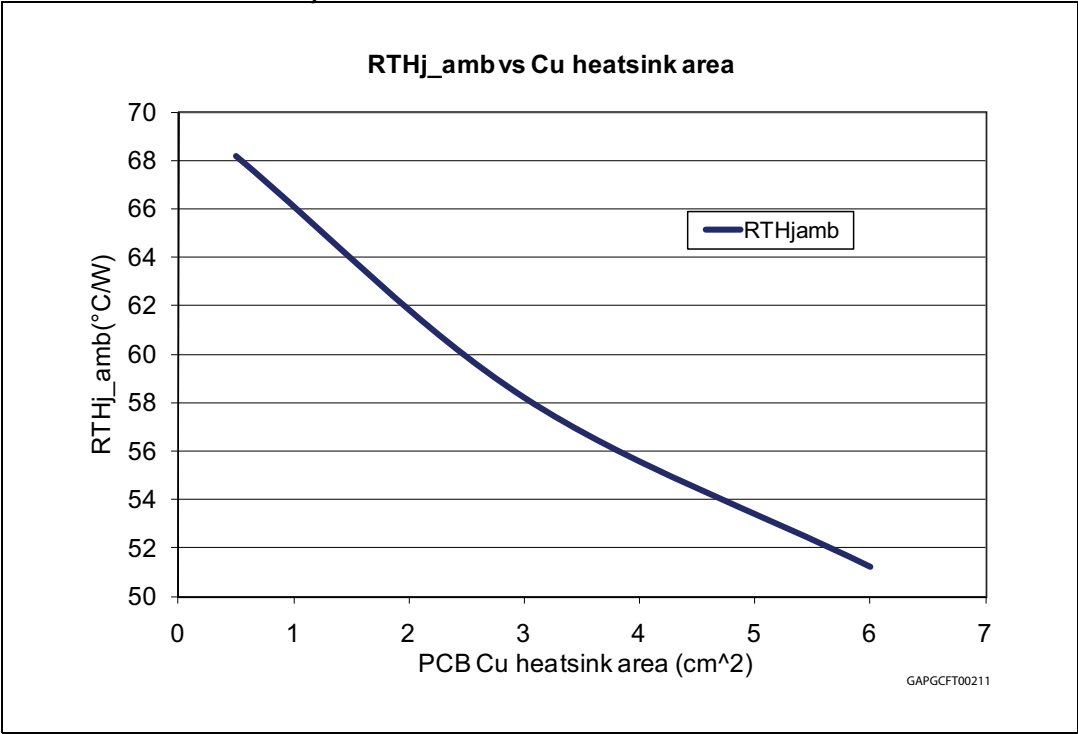
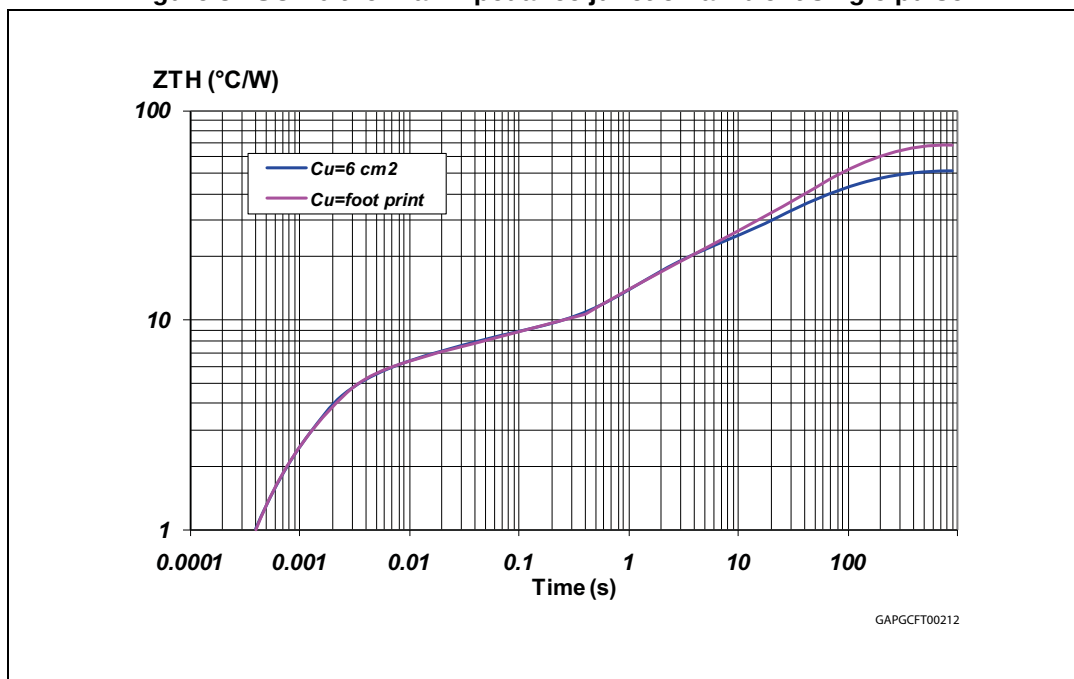


Figure 34. SO-20 thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 35. SO-20 thermal fitting model of a single channel

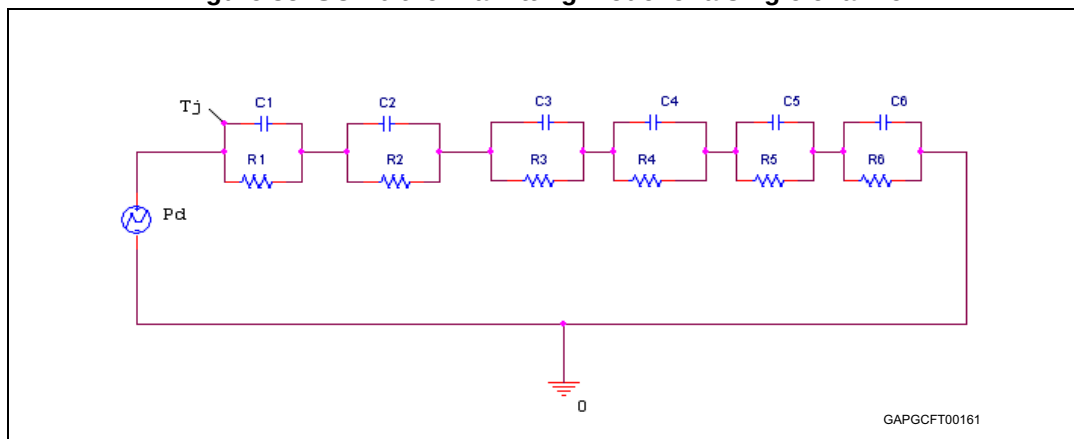


Table 10. SO-20 thermal parameter

Area/island (cm ²)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2.2	
R4 (°C/W)	10	
R5 (°C/W)	15	
R6 (°C/W)	35	18
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	4	7

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.2 SO-8 package information

Figure 36. SO-8 package dimensions

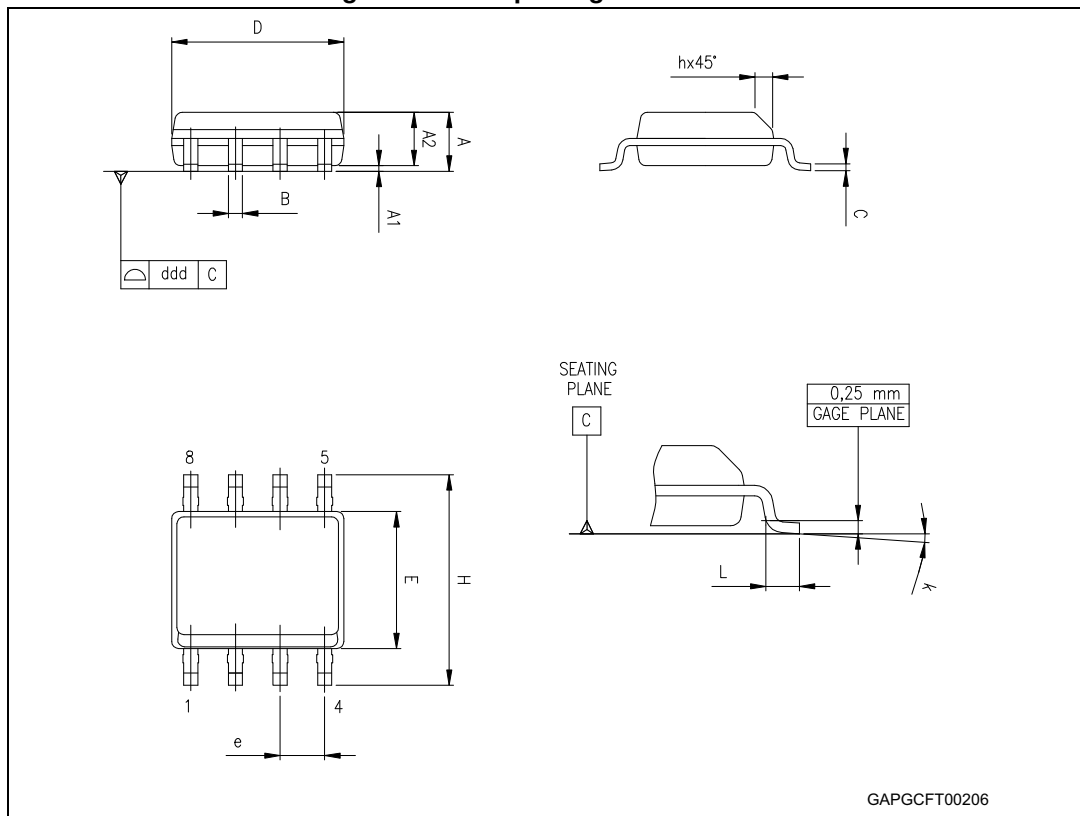


Table 11. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

5.3 SO-20 package information

Figure 37. SO-20 package dimensions

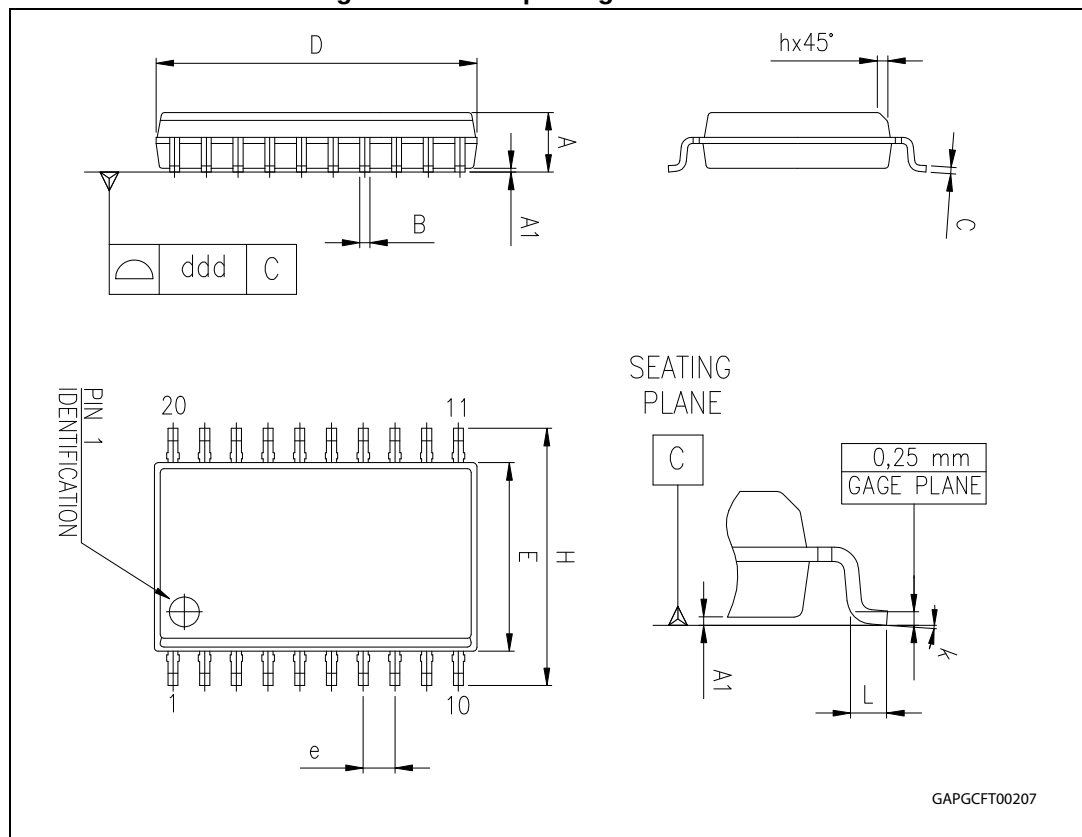


Table 12. SO-20 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D ⁽¹⁾	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27

Table 12. SO-20 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
k	0°		8°
ddd			0.10

1. "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

5.4 SO-8 packing information

Figure 38.SO-8 tube shipment (no suffix)

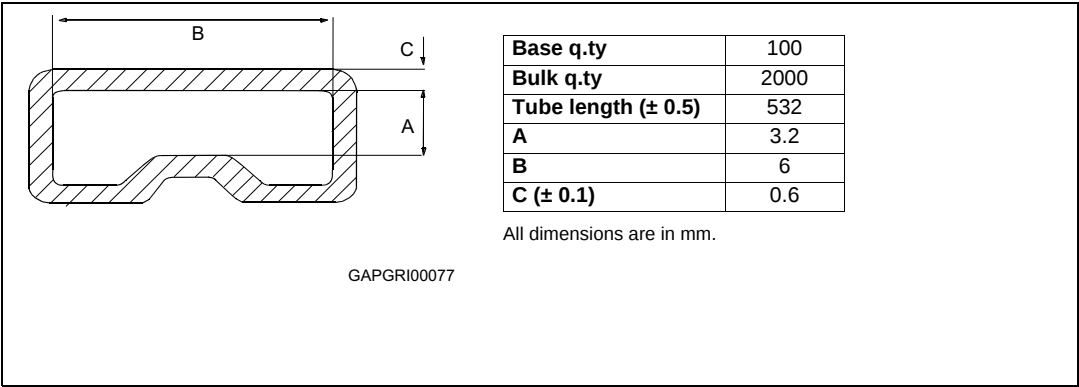
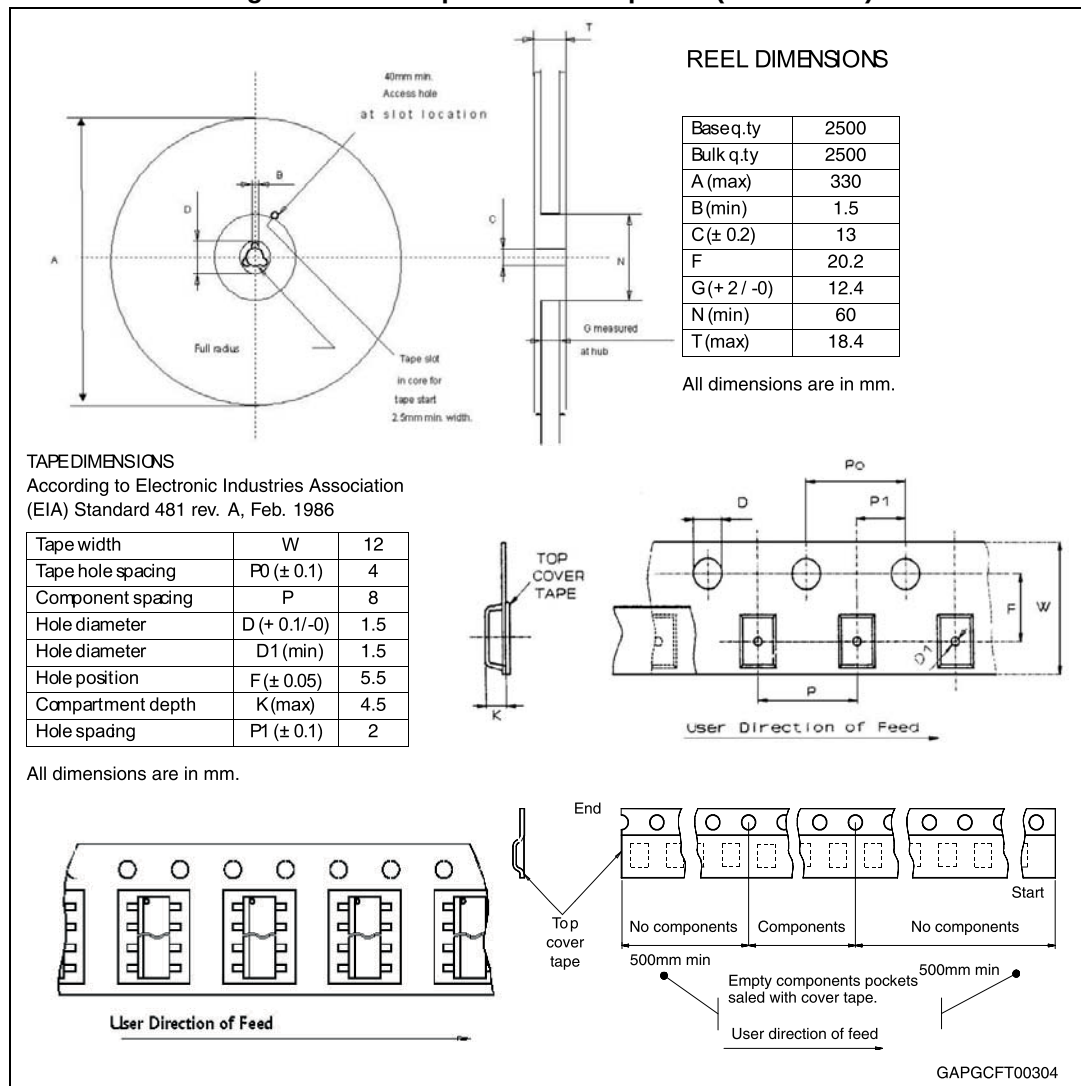
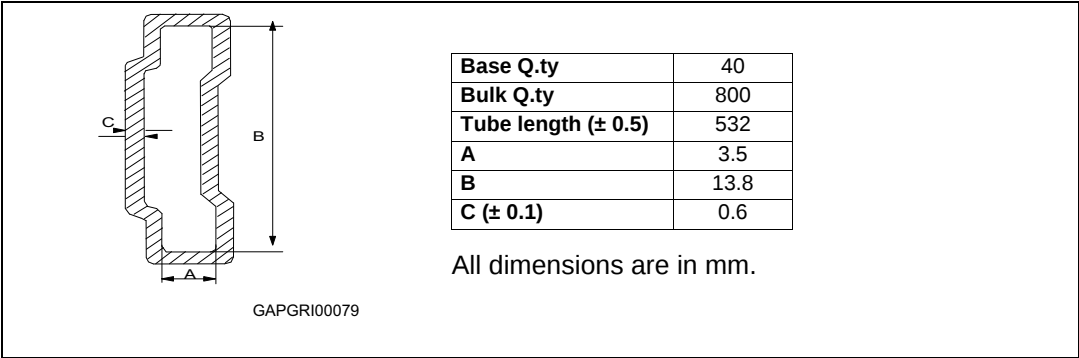


Figure 39.SO-8 tape and reel shipment (suffix "TR")



5.5 SO-20 packing information

Figure 40.SO-20 tube shipment (no suffix)



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
01-Jun-2007	1	Initial release
30-Aug-2007	2	Added features table. Added list of tables and figures. Updated Section 2.3: Electrical characteristics . Added Section 4: Package and PCB thermal data . Added SO-8 packing information and SO-20 packing information .
13-Feb-2008	3	Update Section 2.3: Electrical characteristics .
04-Jun-2008	4	Document restructured. Changed Figure 1: Block diagram . Updated features table on cover page: changed quiescent current value from 80 to 75 μA . Updated Table 5: General : – changed I_{short} typical value from 250 to 280 mA – changed I_{qn_50} typical value from 550 to 500 μA – changed $I_{\text{q}_1_{\text{we}}}$ typical value from 130 to 93 μA – changed $I_{\text{q}_1_{\text{wd}}}$ typical value from 80 to 75 μA . Updated Table 7: Watchdog : – changed V_{wlth} values in $V_{\text{o_ref}}$ percentages – changed V_{whth} values in $V_{\text{o_ref}}$ percentages. Added Figure 24: L4988 application schematic . Added Section 2.4: Electrical characteristics curves . Added Section 2.5: Test circuit and waveforms plot .
05-Apr-2012	5	Update Table 3: Absolute maximum ratings .
20-Sep-2013	6	Updated disclaimer.
13-Sep-2018	7	Updated title and Features . Minor text changes.
18-Sep-2018	8	Typo errors.

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