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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	2.6 1.6	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	4.1	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	18	mJ	$I_D = 0.5\text{A}$; $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.03	mJ	$I_D = 0.5\text{A}$; $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	0.5	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation (non FullPAK) TO-252, TO-251	P_{tot}	-	-	26	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	1.8	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	4.1	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$
Maximum diode commutation speed ³⁾	di/dt	-	-	500	A/ μs	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$, $t_{cond} < 2\mu\text{s}$

2 Thermal characteristics

Table 3 Thermal characteristics DPAK, IPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.85	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	-	- 35	62 -	$^\circ\text{C/W}$	SMD version, device on PCB, minimal footprint SMD version, device on PCB, 6cm ² cooling area ⁴⁾
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}	-	-	260	$^\circ\text{C}$	reflow MSL 1

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.5$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DCLink}=400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

⁴⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70 μm) for drain connection. PCB is vertical without air stream cooling.

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}, I_D=0.03mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=500V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=500V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.70	3.00	Ω	$V_{GS}=13V, I_D=0.4A, T_j=25^\circ C$ $V_{GS}=13V, I_D=0.4A, T_j=150^\circ C$
Gate resistance	R_G	-	6	-	Ω	$f=1\text{ MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	84	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	C_{oss}	-	7	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	6	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	19	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	7.3	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.5A, R_G=5.3\Omega$
Rise time	t_r	-	5.8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.5A, R_G=5.3\Omega$
Turn-off delay time	$t_{d(off)}$	-	23	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.5A, R_G=5.3\Omega$
Fall time	t_f	-	49	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=0.5A, R_G=5.3\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	0.5	-	nC	$V_{DD}=400V, I_D=0.5A, V_{GS}=0\text{ to }10V$
Gate to drain charge	Q_{gd}	-	2.6	-	nC	$V_{DD}=400V, I_D=0.5A, V_{GS}=0\text{ to }10V$
Gate charge total	Q_g	-	4.3	-	nC	$V_{DD}=400V, I_D=0.5A, V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	$V_{DD}=400V, I_D=0.5A, V_{GS}=0\text{ to }10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.83	-	V	$V_{GS}=0V, I_F=0.5A, T_f=25^{\circ}C$
Reverse recovery time	t_{rr}	-	99	-	ns	$V_R=400V, I_F=0.5A, di_F/dt=100A/\mu s$
Reverse recovery charge	Q_{rr}	-	0.3	-	μC	$V_R=400V, I_F=0.5A, di_F/dt=100A/\mu s$
Peak reverse recovery current	I_{rrm}	-	4.2	-	A	$V_R=400V, I_F=0.5A, di_F/dt=100A/\mu s$

4 Electrical characteristics diagrams

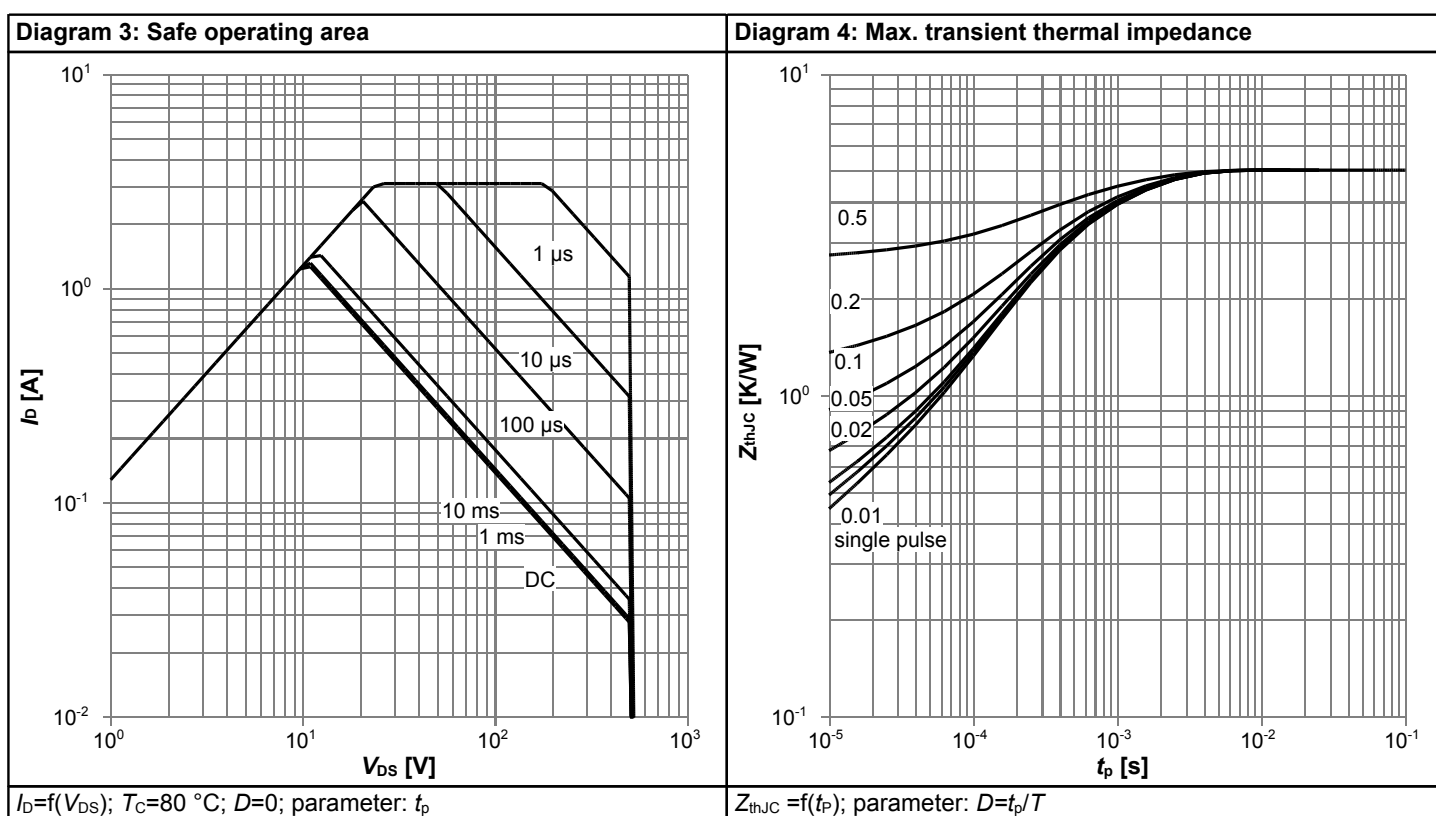
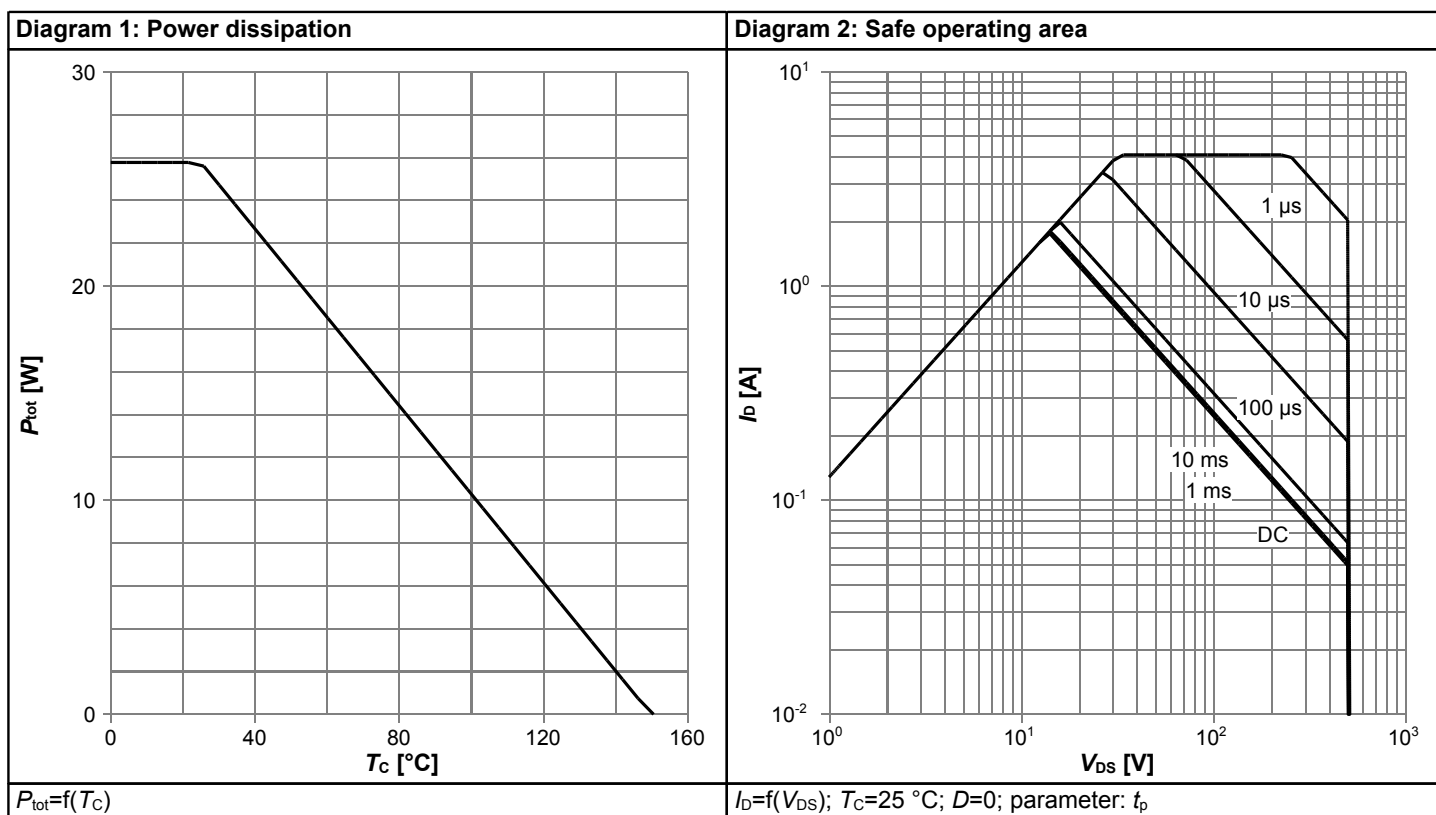
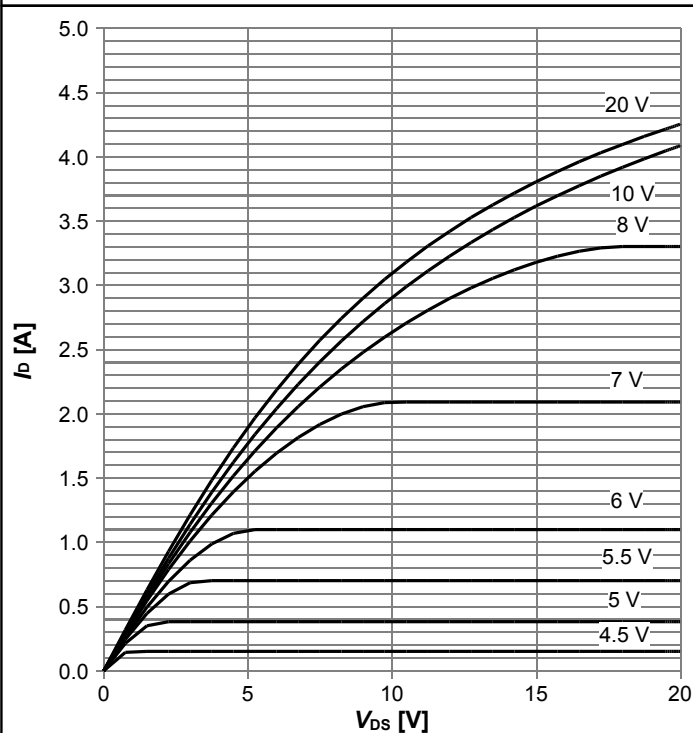
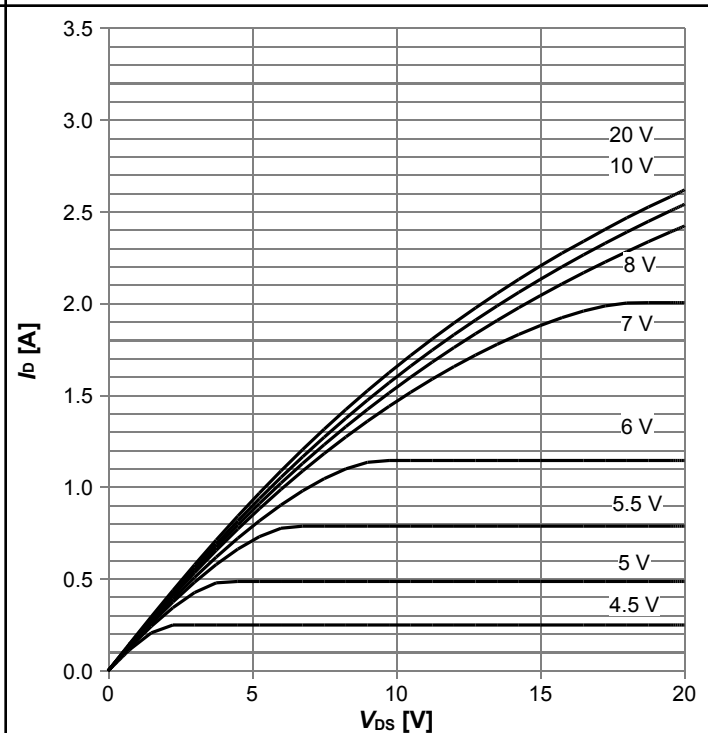


Diagram 5: Typ. output characteristics $T_j=25^\circ\text{C}$



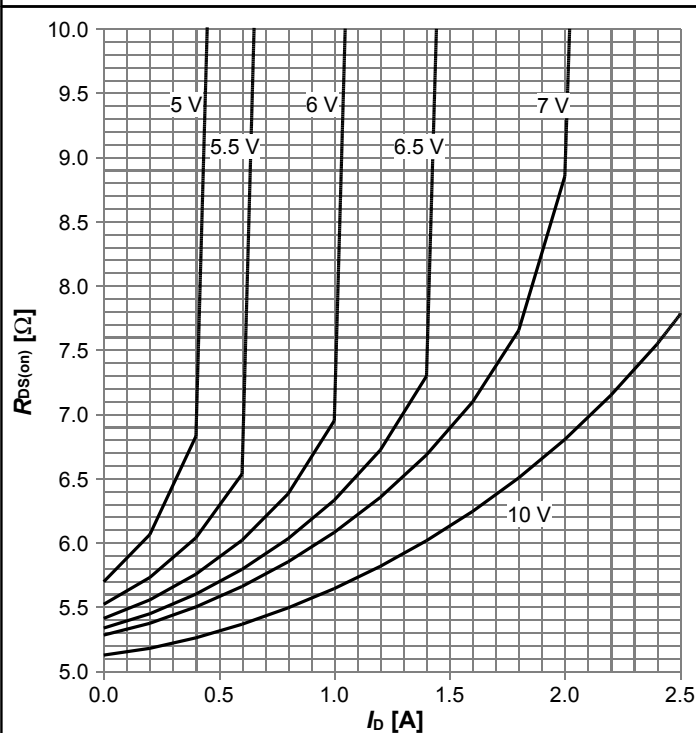
$I_D=f(V_{DS}); T_j=25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics $T_j=125^\circ\text{C}$



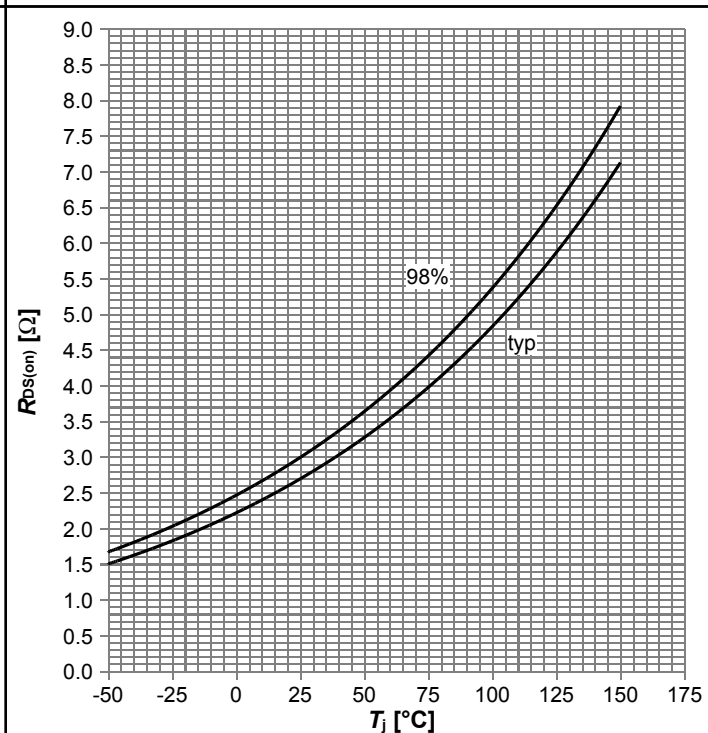
$I_D=f(V_{DS}); T_j=125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



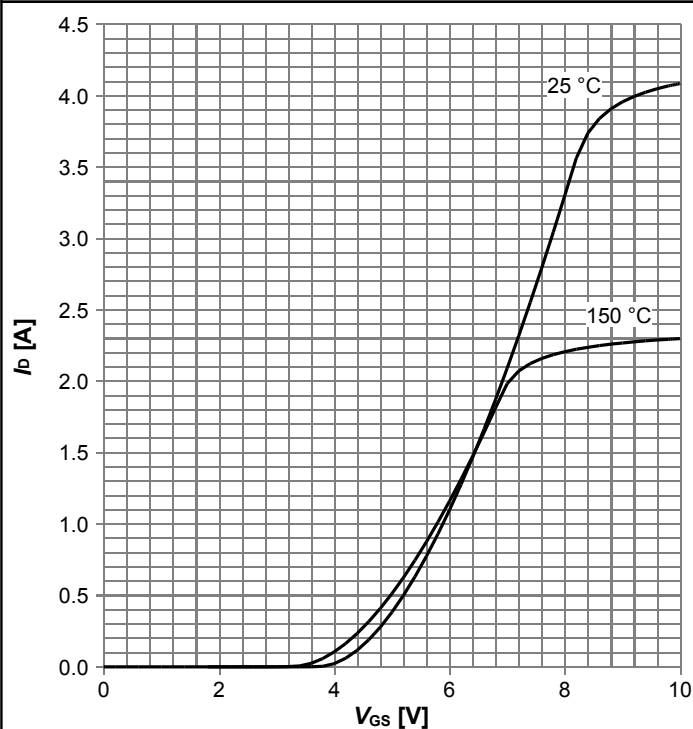
$R_{DS(on)}=f(I_D); T_j=125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance



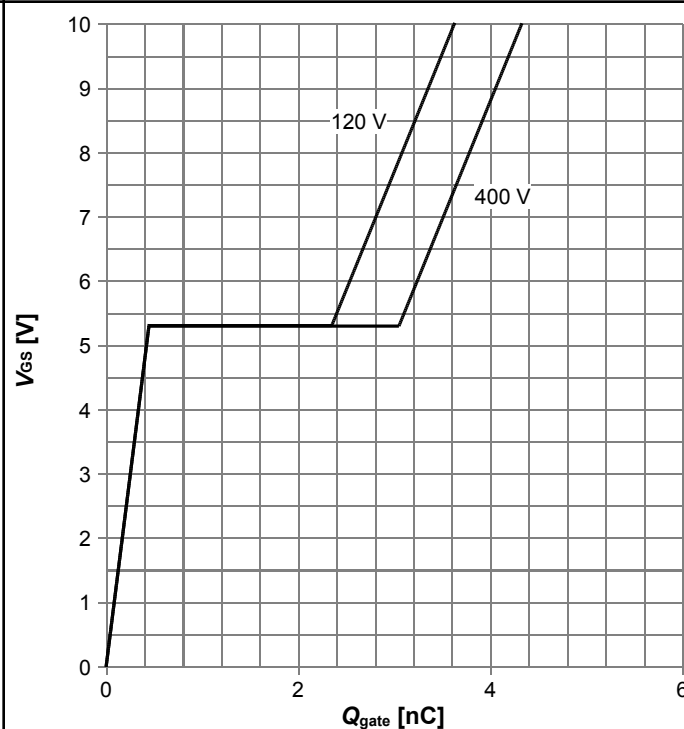
$R_{DS(on)}=f(T_j); I_D=0.4\text{ A}; V_{GS}=13\text{ V}$

Diagram 9: Typ. transfer characteristics



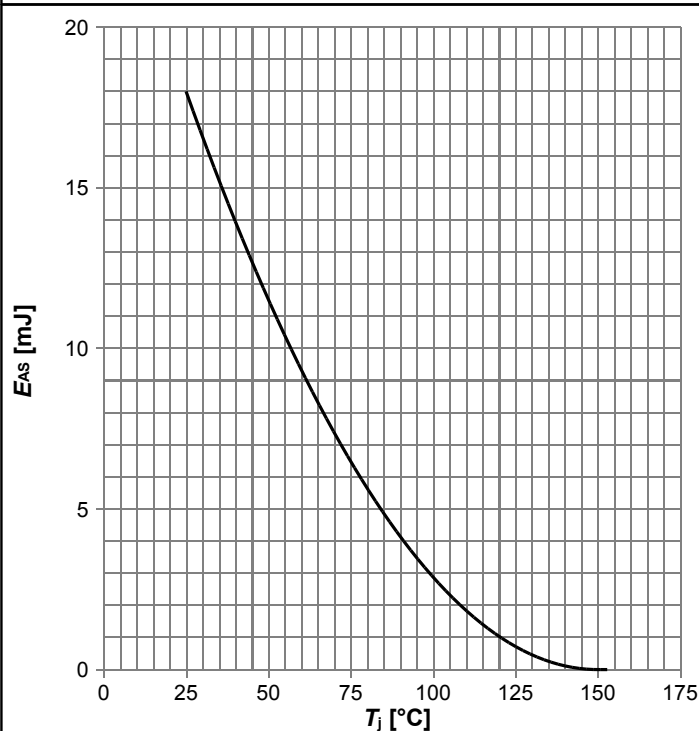
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



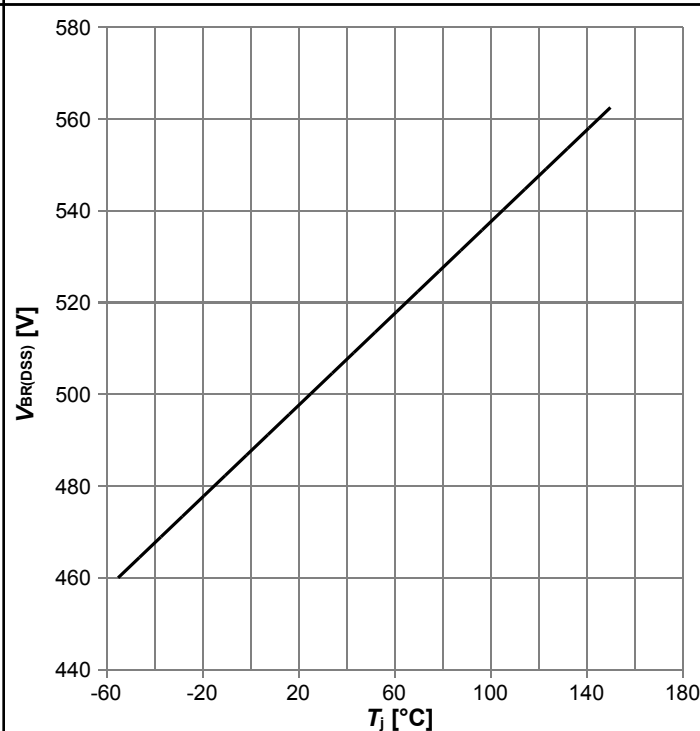
$V_{GS} = f(Q_{gate})$; $I_D = 0.5$ A pulsed; parameter: V_{DD}

Diagram 11: Avalanche energy



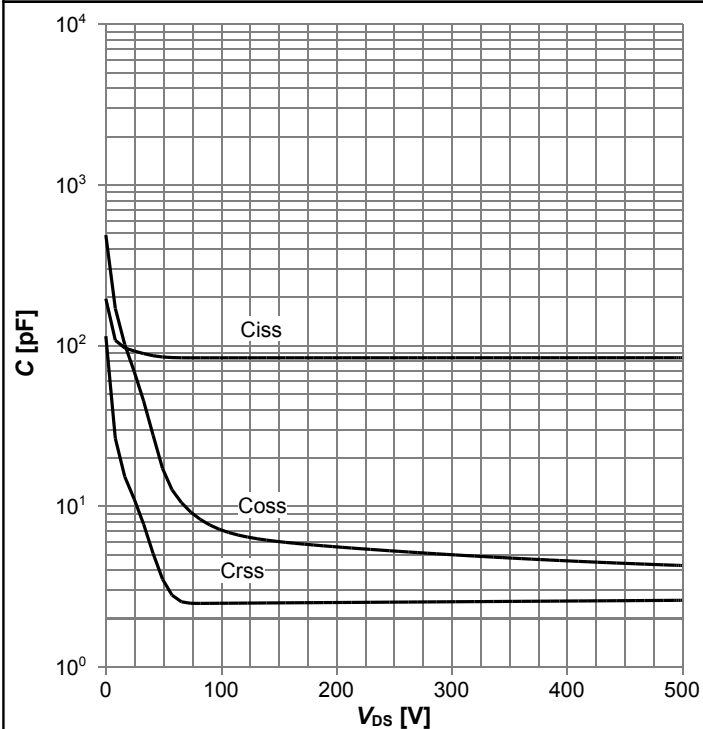
$E_{AS} = f(T_j)$; $I_D = 0.5$ A; $V_{DD} = 50$ V

Diagram 12: Drain-source breakdown voltage



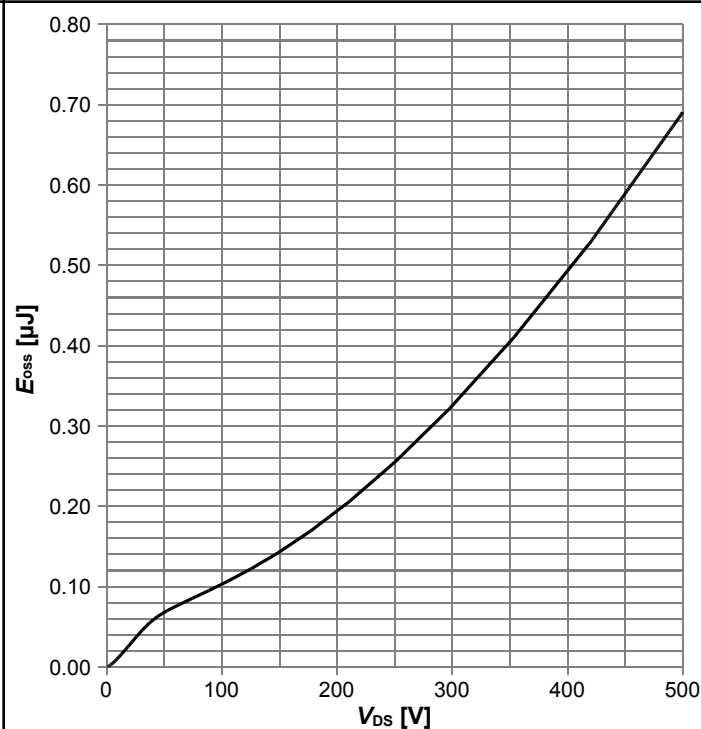
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA

Diagram 13: Typ. capacitances



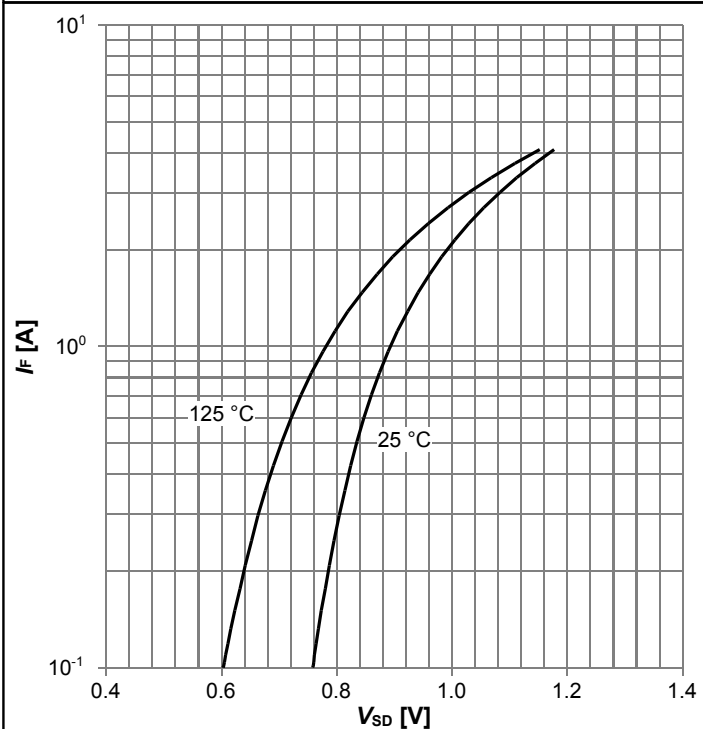
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 14: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

Diagram 15: Forward characteristics of reverse diode



$I_F=f(V_{SD}); \text{parameter: } T_j$

5 Test Circuits

Table 8 Diode characteristics

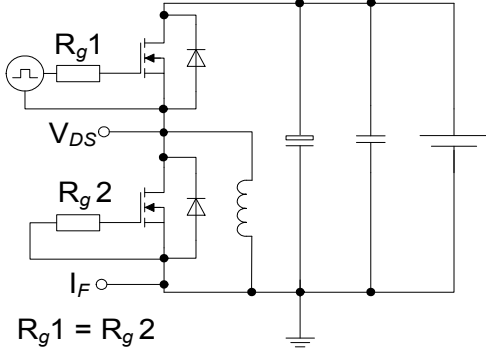
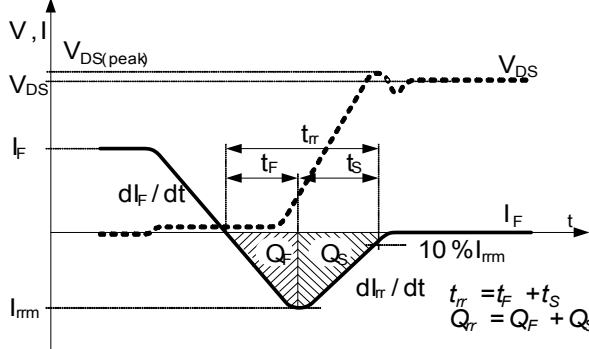
Test circuit for diode characteristics	Diode recovery waveform
 $R_{g1} = R_{g2}$	 $t_{tr} = t_F + t_S$ $Q_{tr} = Q_F + Q_S$

Table 9 Switching times

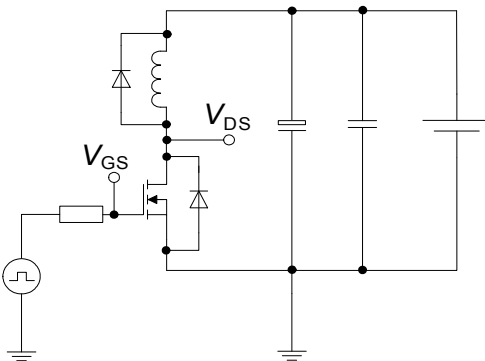
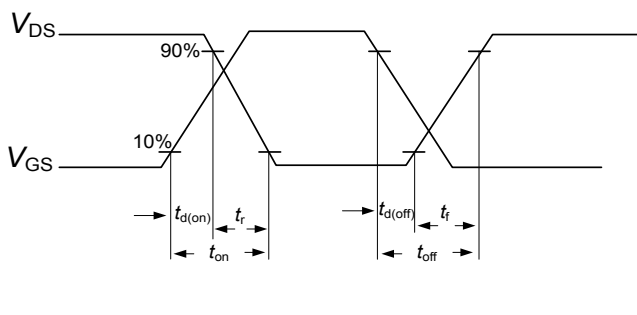
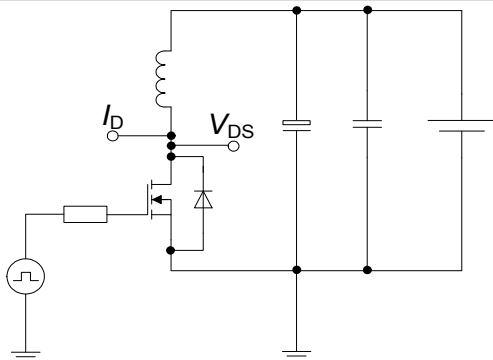
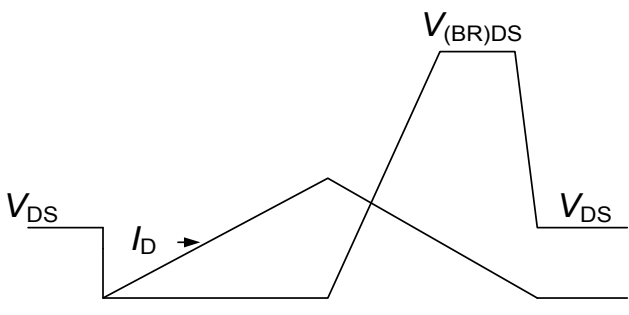
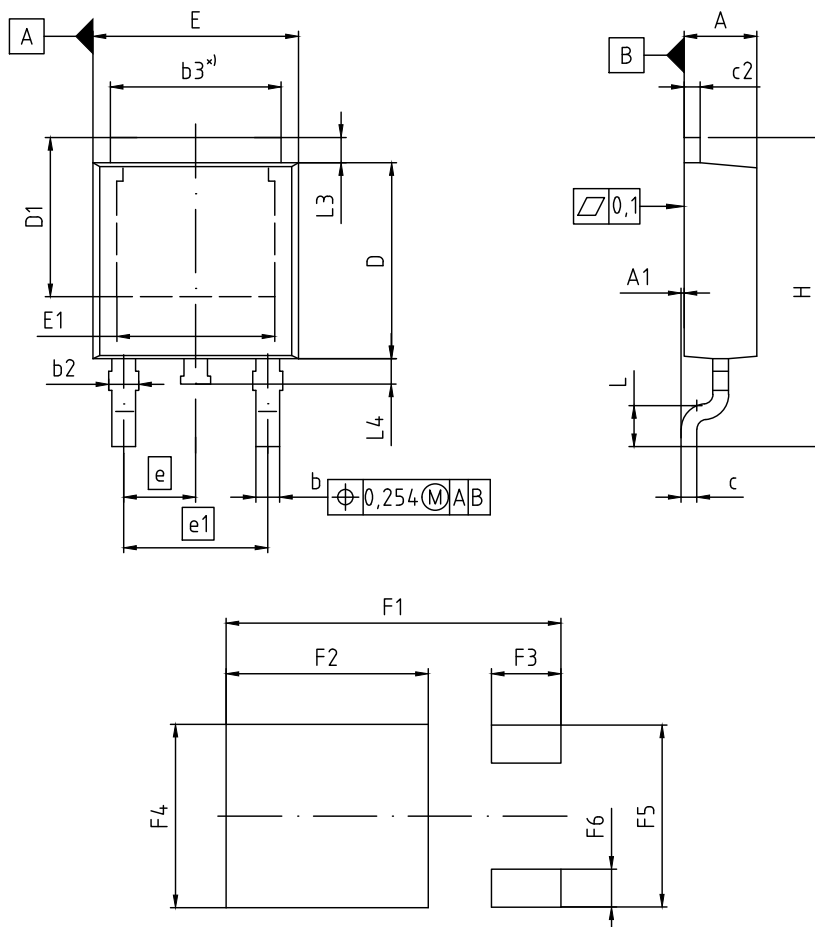
Switching times test circuit for inductive load	Switching times waveform
	 $t_{d(on)}$, t_r, $t_{d(off)}$, t_f, t_{on}, t_{off}

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	 $V_{(BR)DS}$

6 Package Outlines

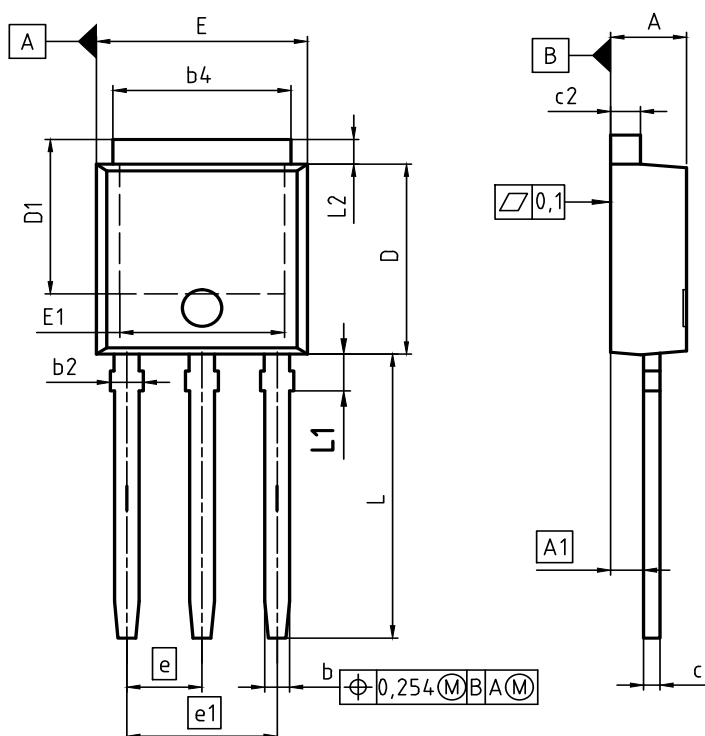


*) mold flash not included

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.60	0.185	0.220
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57 (BSC)		0.180 (BSC)	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

DOCUMENT NO. Z8B00003328
SCALE 0 2.0 4mm
EUROPEAN PROJECTION
ISSUE DATE 01-09-2015
REVISION 05

Figure 1 Outline PG-TO 252, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.90	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.77	0.198	0.227
E	6.35	6.73	0.250	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	8.89	9.65	0.350	0.380
L1	0.85	2.29	0.033	0.090
L2	0.89	1.37	0.035	0.054

DOCUMENT NO. Z8B00003330
SCALE
EUROPEAN PROJECTION
ISSUE DATE 31-08-2015
REVISION 04

Figure 2 Outline PG-TO 251, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPD50R3K0CE, IPU50R3K0CE

Revision: 2016-06-13, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-12-05	Release of final version
2.1	2013-07-16	update to Halogen free mold compound
2.2	2015-11-17	Updated to qualified for standard grade & updated package drawing
2.3	2016-06-13	Updated ID ratings, Zth, SOA and Pd curves

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