

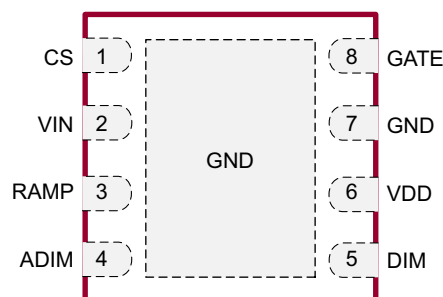
## Ordering Information

Device	Package Options
	8-Lead DFN 3.00x3.00mm body, 0.80mm height (max), 0.65mm pitch
HV9919B	HV9919BK7-G

-G indicates package is RoHS compliant ("Green")

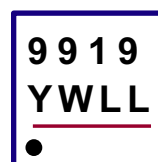


## Pin Description



8-Lead DFN (K7)  
(top view)

## Product Marking



Y = Last Digit of Year Sealed  
W = Code for Week Sealed  
L = Lot Number  
— = "Green" Packaging

8-Lead DFN (K7)

## Absolute Maximum Ratings

Parameter	Value
V <sub>IN</sub> , CS to GND	-0.3 to +45V
V <sub>DD</sub> , GATE, RAMP, DIM, ADIM to GND	-0.3 to +6.0V
CS to VIN	-1.0 to +0.3V
Continuous power dissipation, (T <sub>A</sub> = +25°C)	1.6W
Operating temperature range	-40°C to +125°C
Junction temperature	+150°C
Storage temperature range	-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Resistance

Package	$\theta_{ja}$
8-Lead DFN (K7)	60°C/W

Mounted on FR-4 board, 25mm x 25mm x 1.57mm

## Electrical Characteristics

(V<sub>IN</sub> = 12V, V<sub>DIM</sub> = V<sub>DD</sub>, V<sub>RAMP</sub> = GND, C<sub>VDD</sub> = 1.0μF, R<sub>CS</sub> = 0.5Ω, T<sub>A</sub> = T<sub>J</sub> = -40°C to +125°C\* unless otherwise noted)

Sym	Description	Min	Typ	Max	Units	Conditions
V <sub>IN</sub>	Input DC supply voltage range	4.5	-	40	V	DC input voltage
V <sub>DD</sub>	Internally regulated voltage	4.5	-	5.5	V	V <sub>IN</sub> = 6.0 to 40V
I <sub>IN</sub>	Supply current	-	-	1.5	mA	GATE open
I <sub>IN, SDN</sub>	Shutdown supply current	-	-	900	μA	DIM < 0.7V
I <sub>IN, LIM</sub>	Current limit	-	30	-	mA	V <sub>IN</sub> = 4.5V, V <sub>DD</sub> = 0V
		-	8.0	-		V <sub>IN</sub> = 4.5V, V <sub>DD</sub> = 4.0V
f <sub>OSC</sub>	Oscillator frequency	-	-	2.0	MHz	---
UVLO	V <sub>DD</sub> Undervoltage lockout threshold	-	-	4.5	V	V <sub>DD</sub> rising
ΔUVLO	V <sub>DD</sub> Undervoltage lockout hysteresis	-	500	-	mV	V <sub>DD</sub> falling

\* Guaranteed by design and characterization, 100% tested at T<sub>A</sub> = 25°C. Typical characteristics are given at T<sub>A</sub> = 25°C.

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{DIM} = V_{DD}$ ,  $V_{RAMP} = GND$ ,  $C_{VDD} = 1.0\mu F$ ,  $R_{CS} = 0.5\Omega$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ \* unless otherwise noted)

Sym	Description	Min	Typ	Max	Units	Conditions
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### Sense Comparator

$V_{CS(HI)}$	Sense voltage threshold high	213	230	246	mV	$(V_{IN} - V_{CS})$ rising
$V_{CS(LO)}$	Sense voltage threshold low	158	170	182	mV	$(V_{IN} - V_{CS})$ falling
$t_{DPDH}$	Propagation delay to output high	-	70	-	ns	Falling edge of $(V_{IN} - V_{CS}) = V_{RS(LO)} - 70mV$
$t_{DPDL}$	Propagation delay to output low	-	70	-	ns	Rising edge of $(V_{IN} - V_{CS}) = V_{RS(HI)} + 70mV$
$I_{CS}$	Current-sense input current	-	-	1.0	$\mu A$	$(V_{IN} - V_{CS}) = 200mV$
$I_{CS(HYS)}$	Current-sense threshold hysteresis	-	56	70	mV	---

### DIM Input

$V_{IH}$	Pin DIM input high voltage	2.2	-	-	V	---
$V_{IL}$	Pin DIM input low voltage	-	-	0.7	V	---
$t_{ON}$	Turn-on time	-	100	-	ns	DIM rising edge to $V_{GATE} = 0.5 \times V_{DD}$ , $C_{GATE} = 2.0nF$
$t_{OFF}$	Turn-off time	-	100	-	ns	DIM falling edge to $V_{GATE} = 0.5 \times V_{DD}$ , $C_{GATE} = 2.0nF$

### Gate Driver

$I_{GATE}$	GATE current, source†	0.3	0.5	-	A	$V_{GATE} = GND$
	GATE current, sink†	0.7	1.0	-	A	$V_{GATE} = V_{DD}$
$T_{RISE}$	GATE output rise time	-	40	55	ns	$C_{GATE} = 2.0nF$
$T_{FALL}$	GATE output fall time	-	17	25	ns	$C_{GATE} = 2.0nF$
$V_{GATE(HI)}$	GATE high output voltage	$V_{DD} - 0.5$	-	-	V	$I_{GATE} = 10mA$
$V_{GATE(LO)}$	GATE low output voltage	-	-	0.5	V	$I_{GATE} = -10mA$

### Over-Temperature Protection

$T_{OT}$	Over temperature trip limit†	128	140	-	$^\circ C$	---
$\Delta T_{HYST}$	Temperature hysteresis†	-	60	-	$^\circ C$	---

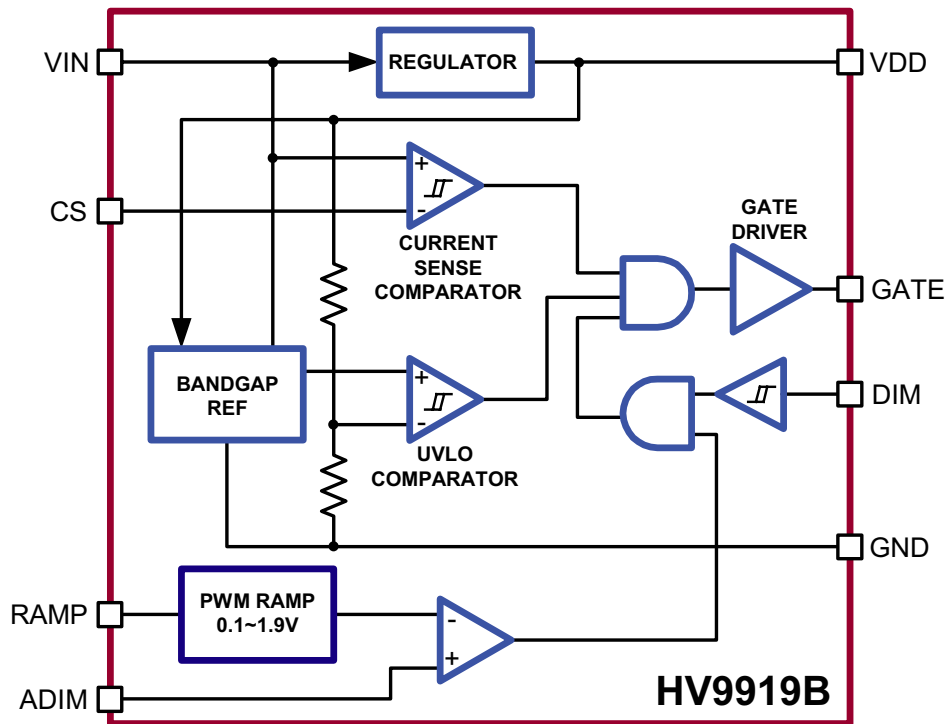
### Analog Control of PWM Dimming

$f_{RAMP}$	Dimming frequency	130	-	300	Hz	$C_{RAMP} = 47nF$
		550	-	1250		$C_{RAMP} = 10nF$
$V_{LOW}$	RAMP threshold, Low	-	0.1	-	V	---
$V_{HIGH}$	RAMP threshold, High	1.8	-	2.1	V	---
$V_{OS}$	ADIM offset voltage	-35	-	+35	mV	---

\* Guaranteed by design and characterization, 100% tested at  $T_A = 25^\circ C$ . Typical characteristics are given at  $T_A = 25^\circ C$ .

† Guaranteed by design and characterization.

## Block Diagram



## Application Information

### General Description

The HV9919B is a step-down, constant current, high-brightness LED (HB LED) driver. The device operates from a 4.5 to 40V input voltage range and provides the gate drive output to an external N-channel MOSFET. A high-side current sense resistor sets the output current and a dedicated PWM dimming input (DIM) allows for a wide range of dimming duty ratios. The PWM dimming could also be achieved by applying a DC voltage between 0 and 2.0V to the analog dimming input (ADIM). In this case, the dimming frequency can be programmed using a single capacitor at the RAMP pin. The high-side current setting and sensing scheme minimizes the number of external components while delivering LED current with a  $\pm 8\%$  accuracy, using a 1% sense resistor.

### Undervoltage Lockout (UVLO)

The HV9919B includes a 3.7V under-voltage lockout (UVLO) with 500mV hysteresis. When  $V_{IN}$  falls below 3.7V, GATE goes low, turning off the external n-channel MOSFET. GATE goes high once  $V_{IN}$  is 4.5V or higher.

### 5.0V Regulator

VDD is the output of a 5.0V regulator capable of sourcing 8.0mA. Bypass VDD to GND with a 1.0 $\mu$ F capacitor.

### DIM Input

The HV9919B allows dimming with a PWM signal at the DIM input. A logic level below 0.7V at DIM forces the  $GATE_{OUTPUT}$  low, turning off the LED current. To turn the LED current on, the logic level at DIM must be at least 2.2V.

### ADIM and RAMP Inputs

The PWM dimming scheme can be also implemented by applying an analog control signal to ADIM pin. If an analog control signal of 0~2.0V is applied to ADIM, the device compares this analog input to a voltage ramp to pulse-width-modulate the LED current. Connecting an external capacitor to RAMP programs the PWM dimming ramp frequency.

$$f_{PWM} = \frac{1}{C_{RAMP} \cdot 120k\Omega}$$

DIM and ADIM inputs can be used simultaneously. In such case,  $f_{PWM(MAX)}$  must be selected lower than the frequency of the dimming signal at DIM. The smaller dimming duty cycle of ADIM and DIM will determine the GATE signal.

When the analog control of PWM dimming feature is not used, RAMP must be wired to GND, and ADIM should be connected to VDD.

One possible application of the ADIM feature of the HV9919B may include protection of the LED load from over-temperature by connecting an NTC thermistor at ADIM, as shown in Figure 1.

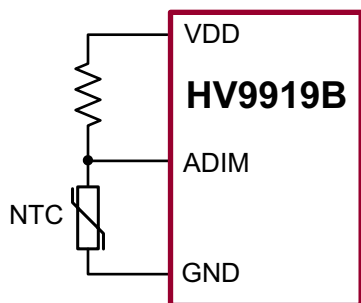


Figure 1

### Setting LED Current with External Resistor $R_{SENSE}$

The output current in the LED is determined by the external current sense resistor ( $R_{SENSE}$ ) connected between VIN and CS. Disregarding the effect of the propagation delays, the sense resistor can be calculated as:

$$R_{SENSE} \approx \frac{1}{2} \cdot \frac{(V_{RS(HI)} + V_{RS(LO)})}{I_{LED}} = \frac{200mV}{I_{LED}}$$

### Selecting Buck Inductor L

The HV9919B regulates the LED output current using an

input comparator with hysteresis (Figure 2). As the current through the inductor ramps up and the voltage across the sense resistor reaches the upper threshold, the voltage at GATE goes low, turning off the external MOSFET. The MOSFET turns on again when the inductor current ramps down through the freewheeling diode until the voltage across the sense resistor equals the lower threshold. Use the following equation to determine the inductor value for a desired value of operating frequency  $f_s$ :

$$L = \frac{(V_{IN} - V_{OUT})V_{OUT}}{f_s V_{IN} \Delta I_O} - \frac{(V_{IN} - V_{OUT})t_{DPDL}}{\Delta I_O} - \frac{V_{OUT}t_{DPDH}}{\Delta I_O}$$

where:

$$\Delta I_O = \frac{V_{RS(HI)} - V_{RS(LO)}}{R_{SENSE}}$$

and  $t_{DPDL}$ ,  $t_{DPDH}$  are the propagation delays. Note, that the current ripple  $\Delta I$  in the inductor L is greater than  $\Delta I_O$ . This ripple can be calculated from the following equation:

$$\Delta I = \Delta I_O + \frac{(V_{IN} - V_{OUT})t_{DPDL}}{L} + \frac{V_{OUT}t_{DPDH}}{L}$$

For the purpose of the proper inductor selection, note that the maximum switching frequency occurs at the highest  $V_{IN}$  and  $V_{OUT} = V_{IN}/2$ .

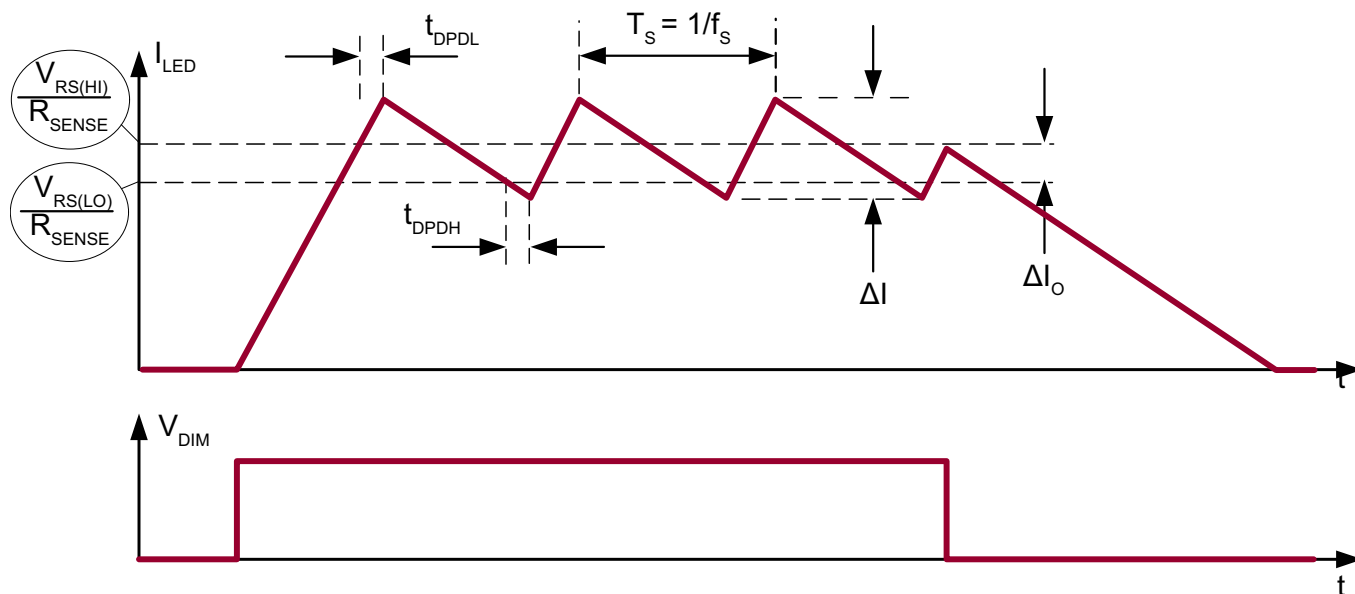


Figure 2

### MOSFET Selection

MOSFET selection is based on the maximum input operating voltage  $V_{IN}$ , output current  $I_{LED}$ , and operating switching frequency. Choose a MOSFET that has a higher breakdown voltage than the maximum operation voltage, low  $R_{DS(ON)}$ , and low total charge for better efficiency. MOSFET threshold voltage must be adequate if operated at the low end of the input-voltage operating range.

### Freewheeling Diode Selection

The forward voltage of the freewheeling diode should be as low as possible for better efficiency. A Schottky diode is a good choice as long as the breakdown voltage is high enough to withstand the maximum operating voltage. The forward current rating of the diode must be at least equal to the maximum LED current.

### LED Current Ripple

The LED current ripple is equal to the inductor current ripple. In cases when a lower LED current ripple is needed, a capacitor can be placed across the LED terminals.

### PCB Layout Guidelines

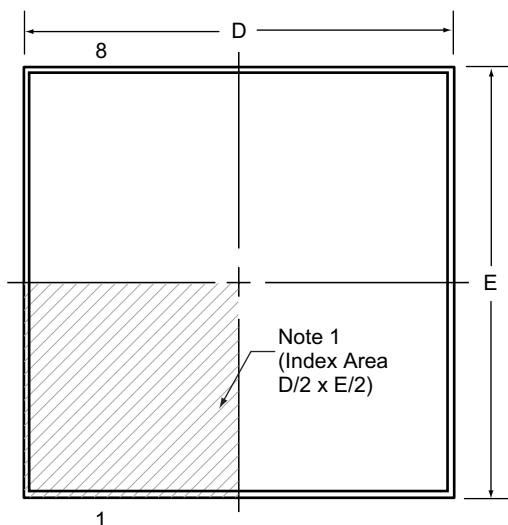
Careful PCB layout is critical to achieve low switching losses and stable operation. Use a multilayer board whenever possible for better noise immunity. Minimize ground noise by connecting high-current ground returns, the input bypass capacitor ground lead, and the output filter ground lead to a single point (star ground configuration). The fast  $di/dt$  loop is formed by the input capacitor  $C_{IN}$ , the free-wheeling diode and the MOSFET. To minimize noise interaction, this loop area should be as small as possible. Place  $R_{SENSE}$  as close as possible to the input filter and  $V_{IN}$ . For better noise immunity, a Kelvin connection is strongly recommended between CS and  $R_{SENSE}$ . Connect the exposed tab of the IC to a large-area ground plane for improved power dissipation.

## Pin Description

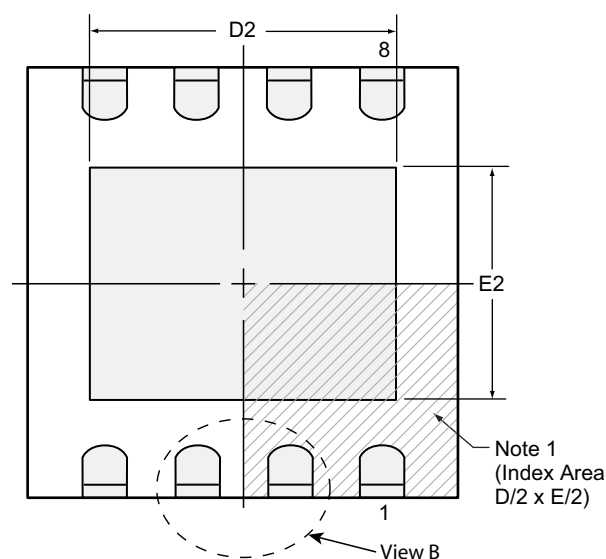
Pin #	Pin	Description
1	CS	Current sense input. Senses LED string current.
2	VIN	Input voltage 4.5 to 40V DC.
3	RAMP	Analog PWM dimming ramp output.
4	ADIM	Analog 0~2.0V signal input for analog control of PWM dimming.
5	DIM	PWM signal input.
6	VDD	Internally regulated supply voltage. Connect a capacitor from VDD to ground.
7	GND	Device ground.
8	GATE	Drives gate of external MOSFET.
TAB	GND	Must be wired to pin 7 on PCB.

## 8-Lead DFN Package Outline (K7)

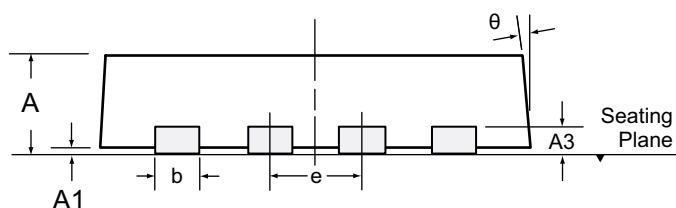
3.00x3.00mm body, 0.80mm height (max), 0.65mm pitch



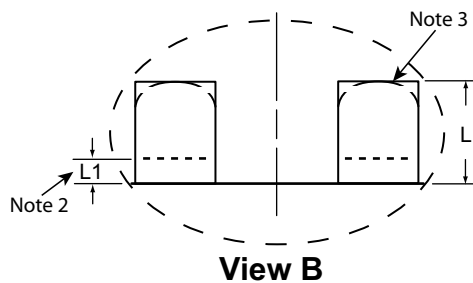
**Top View**



**Bottom View**



**Side View**



**View B**

### Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.25	2.85*	1.60	2.85*	1.35	0.65 BSC	0.30	0.00*	0°
	NOM	0.75	0.02		0.30	3.00	-	3.00	-		0.40	-	-
	MAX	0.80	0.05		0.35	3.15*	2.50	3.15*	1.75		0.50	0.15	14°

JEDEC Registration MO-229, Variation WEEC-2, Issue C, Aug. 2003.

\* This dimension is not specified in the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc. #:** DSPD-8DFNK73X3P065, Version C041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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