

November 2013

FQP20N06

N-Channel QFET[®] MOSFET 60 V, 20 A, 60 m Ω

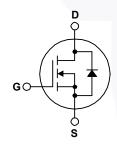
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 20 A, 60 V, $R_{DS(on)}$ = 60 m Ω (Max.) @ V_{GS} = 10 V, I_D = 10 A
- Low Gate Charge (Typ. 11.5 nC)
- · Low Crss (Typ. 25 pF)
- 100% Avalanche Tested
- · 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQP20N06	Unit
V_{DSS}	Drain-Source Voltage		60	V
I_D	Drain Current - Continuous (T _C = 25°	C)	20	Α
	- Continuous (T _C = 100)°C)	14.1	А
I _{DM}	Drain Current - Pulsed	(Note 1)	80	Α
V _{GSS}	Gate-Source Voltage		± 25	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	155	mJ
I _{AR}	Avalanche Current	(Note 1)	20	Α
E _{AR}	Repetitive Avalanche Energy	(Note 1)	5.3	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
P _D	Power Dissipation (T _C = 25°C)		53	W
	- Derate above 25°C		0.35	W/°C
T _J , T _{STG}	Operating and Storage Temperature Ran	ige	-55 to +175	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQP20N06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.85	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP20N06	FQP20N06	TO-220	Tube	N/A	N/A	50 units

FIC	ectrical	Chara	ctor	etice
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T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	60			V
ΔBV_{DSS} / ΔT_{J}	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.07		V/°C
I _{DSS}	Zara Oata Valta va Busin Ouwant	V _{DS} = 60 V, V _{GS} = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V _{DS} = 48 V, T _C = 150°C			10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 25 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -25 V, V _{DS} = 0 V			-100	nA
On Cha	racteristics		,			
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 10 A		0.048	0.06	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 25 V, I _D = 10 A		12		S
Dynam	ic Characteristics					
C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		450	590	pF
C _{oss}	Output Capacitance	f = 1.0 MHz		170	220	pF
C _{rss}	Reverse Transfer Capacitance			25	35	pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V = 20 V L = 10 A		5	20	ns
t _r	Turn-On Rise Time	$V_{DD} = 30 \text{ V, I}_{D} = 10 \text{ A,}$ $R_{G} = 25 \Omega$		45	100	ns
t _{d(off)}	Turn-Off Delay Time	11.6 - 20 22		20	50	ns
t _f	Turn-Off Fall Time	(Note 4)	/	25	60	ns
Qg	Total Gate Charge	V _{DS} = 48 V, I _D = 20 A,		11.5	15	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		3		nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current				20	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-		80	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 20 A	-		1.5	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V, } I_{S} = 20 \text{ A,}$	-	43		ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	-	50	//	nC

(Note 4)

4.5

- **Notes:** 1. Repetitive Rating : Pulse width limited by maximum junction temperature. 2. L = 450 μ H, I $_{AS}$ = 20 A, V $_{DD}$ = 25 V, R $_{G}$ = 25 Ω , starting T $_{J}$ = 25°C. 3. I $_{SD}$ ≤ 20 A, di/dt ≤ 300 A/µs, V $_{DD}$ ≤ BV $_{DSS}$, starting T $_{J}$ = 25°C. 4. Essentially Independent of Operating Temperature.

Gate-Drain Charge

nC

Typical Characteristics

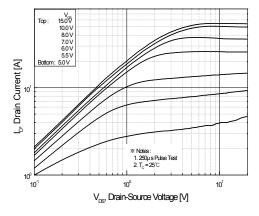


Figure 1. On-Region Characteristics

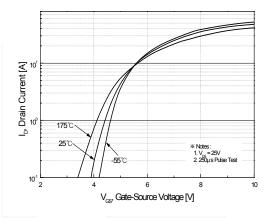


Figure 2. Transfer Characteristics

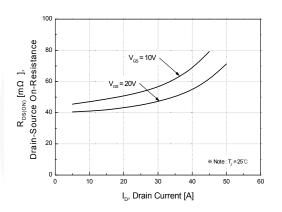


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

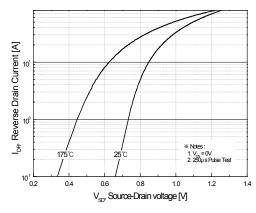


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

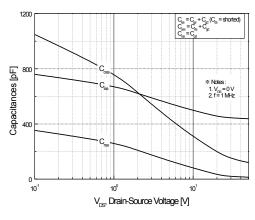


Figure 5. Capacitance Characteristics

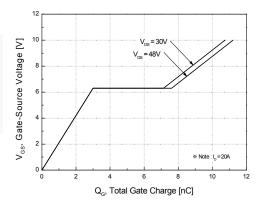
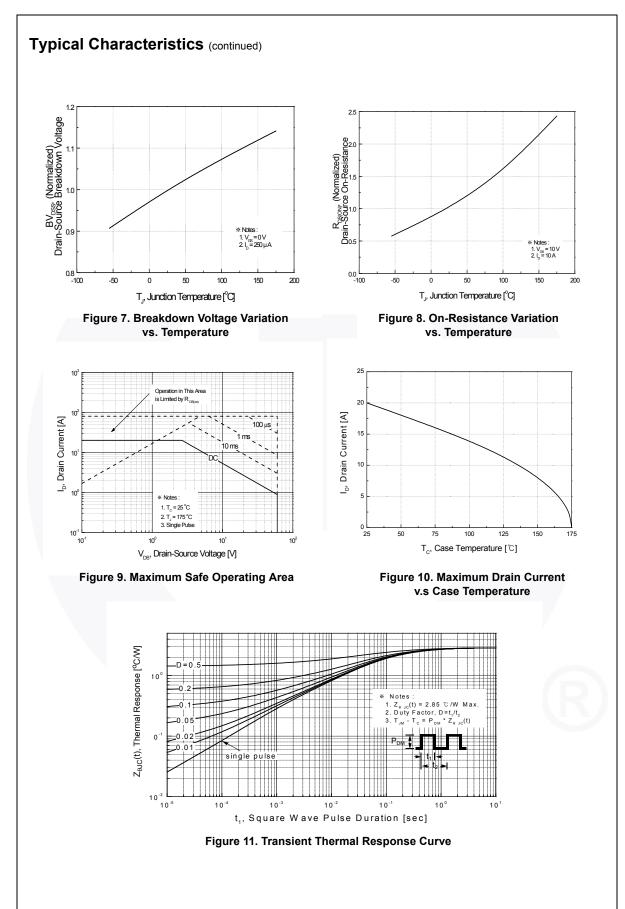


Figure 6. Gate Charge Characteristics



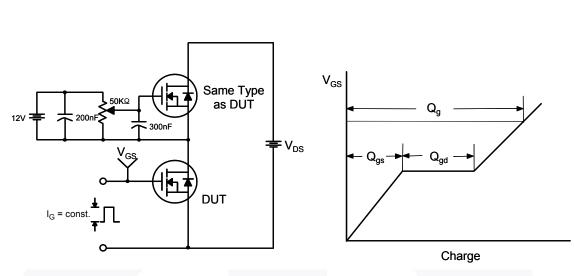
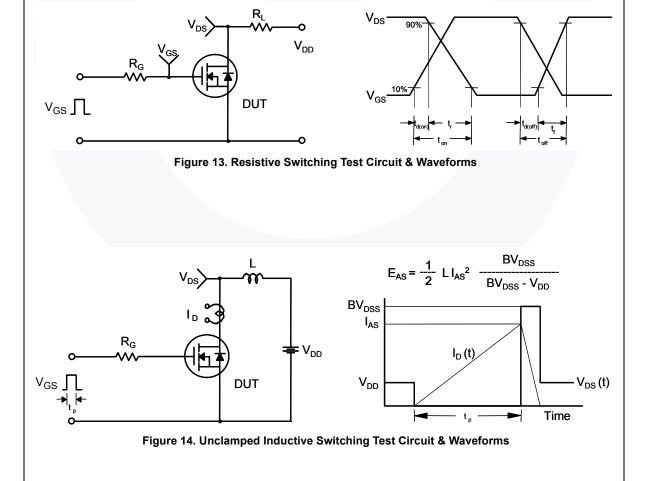
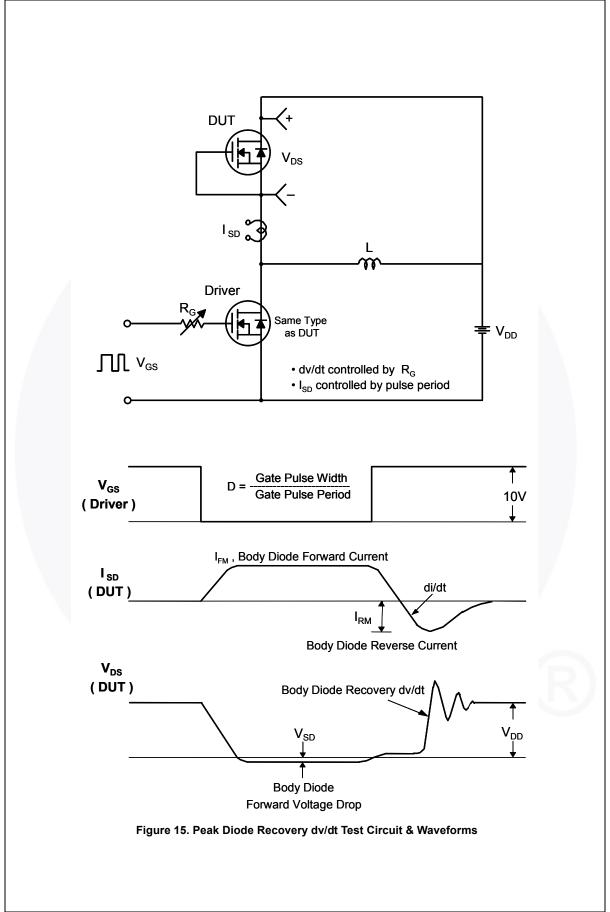
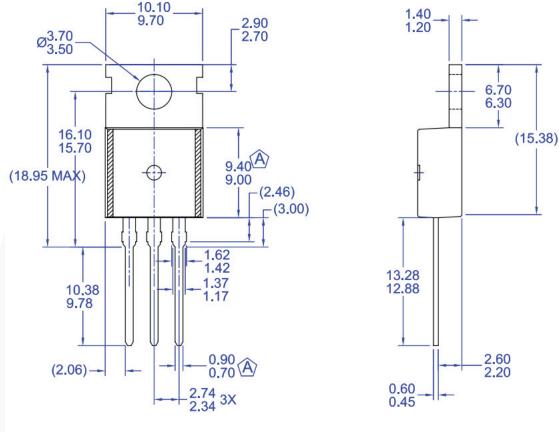


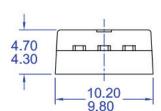
Figure 12. Gate Charge Test Circuit & Waveform





Mechanical Dimensions





NOTES:

- (A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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