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# 1 Block and pin connection diagrams

**Figure 1. Block diagram**

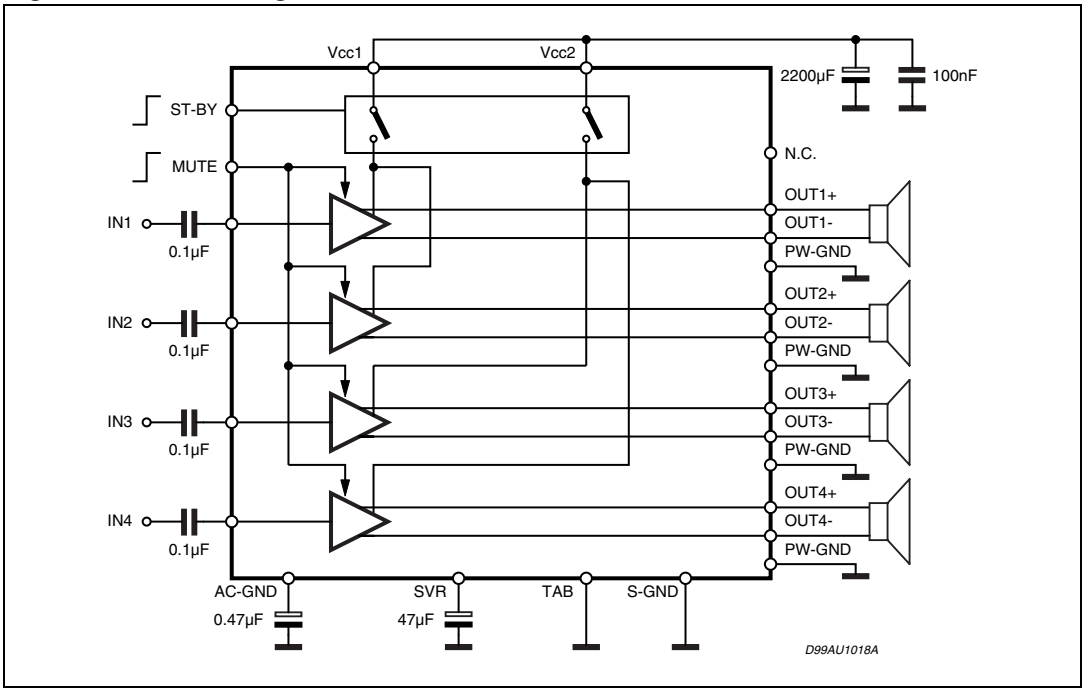
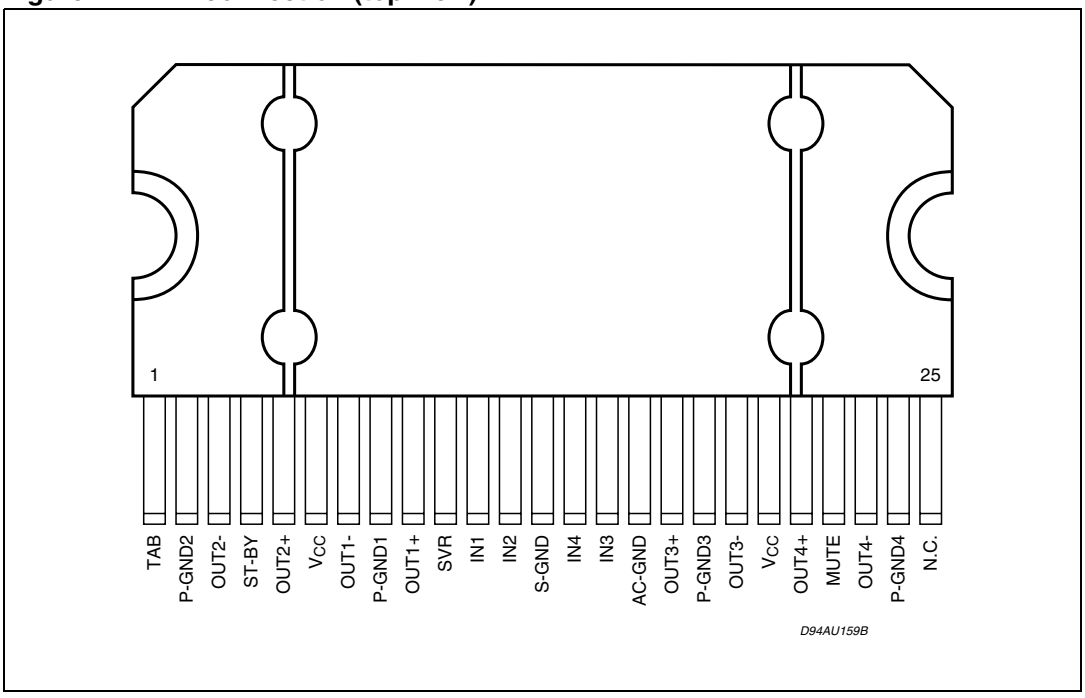



**Figure 2. Pin connection (top view)**



# 2 Electrical specifications

## 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Operating supply voltage | 18 | V |
| $V_{CC\ (DC)}$ | DC supply voltage | 28 | V |
| $V_{CC\ (pk)}$ | Peak supply voltage (t = 50ms) | 50 | V |
| $I_O$ | Output peak current:<br>Repetitive (Duty Cycle 10% at f = 10Hz)<br>Non Repetitive (t = 100µs) | <br>4.5<br>5.5 | <br>A<br>A |
| $P_{tot}$ | Power dissipation, ($T_{case}$ = 70°C) | 80 | W |
| $T_{amb}$ | Operating temperature range | – 40 to 105 | °C |
| $T_j$ | Junction temperature | 150 | °C |
| $T_{stg}$ | Storage temperature | – 55 to 150 | °C |

## 2.2 Thermal data

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction to case max. | 1 | °C/W |

## 2.3 Electrical characteristics

**Table 4. Electrical characteristics**

$V_S$ = 14.4 V; f = 1 kHz; $R_g$ = 600 Ω; $R_L$ = 4 Ω; $T_{amb}$ = 25 °C; Refer to the test and application diagram, unless otherwise specified.

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{q1}$ | Quiescent current | $R_L = \infty$ | | 190 | 350 | mA |
| $V_{OS}$ | Output offset voltage | Play Mode | | | ±80 | mV |
| $\Delta V_{OS}$ | During mute on/off output offset voltage | | | | ±80 | mV |
| $G_v$ | Voltage gain | | 25 | 26 | 27 | dB |
| $\Delta G_v$ | Channel gain unbalance | | | | ±1 | dB |
| $P_o$ | Output power | THD = 10%; $V_S$ = 13.2V | 22 | 24 | | W |
| | | THD = 0.8%; $V_S$ = 13.2V | 16.5 | 18 | | W |
| | | THD = 10%; $V_S$ = 14.4V | 26 | 28 | | W |
| $P_{o\ max}$ | Max.output power (1) | $V_S$ = 14.4V | 43 | 45 | | W |

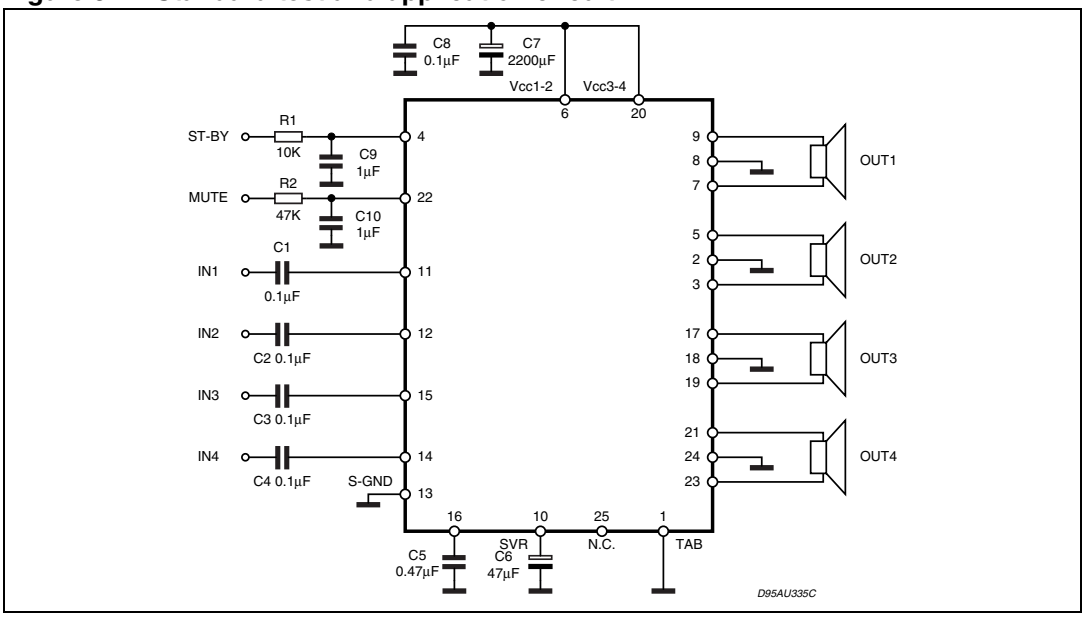
**Table 4. Electrical characteristics (continued)**

$V_S$ = 14.4 V; f = 1 kHz; $R_g$ = 600 Ω; $R_L$ = 4 Ω; $T_{amb}$ = 25 °C; Refer to the test and application diagram, unless otherwise specified.

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| THD | Distortion | $P_o$ = 4W | | 0.04 | 0.15 | % |
| $e_{No}$ | Output noise | "A" Weighted | | 50 | 70 | µV |
| | | Bw = 20 Hz to 20 kHz | | 70 | 100 | µV |
| SVR | Supply voltage rejection | f = 100 Hz; $V_r$ = 1$V_{rms}$ | 50 | 75 | | dB |
| $f_{ch}$ | High cut-off frequency | $P_o$ = 0.5 W | 80 | 200 | | KHz |
| $R_i$ | Input impedance | | 70 | 100 | | KΩ |
| $C_T$ | Cross talk | f = 1 kHz; Po = 4 W | 60 | 70 | | dB |
| | | f = 10 kHz; Po = 4W | | 60 | | dB |
| $I_{SB}$ | Standby current consumption | $V_{St\text{-}by}$ = 1.5 | | | 50 | µA |
| | | $V_{St\text{-}by}$ = 0 V | | | 20 | µA |
| $I_{pin4}$ | Standby pin current | $V_{St\text{-}by}$ = 1.5 to 3.5 V | | | ±1 | µA |
| $V_{SB\ out}$ | Standby out threshold voltage | (Amp: on) | 3.5 | | | V |
| $V_{SB\ IN}$ | Standby in threshold voltage | (Amp: off) | | | 1.5 | V |
| $A_M$ | Mute attenuation | $P_{Oref}$ = 4W | 80 | 90 | | dB |
| $V_{M\ out}$ | Mute out threshold voltage | (Amp: play) | 3.5 | | | V |
| $V_{M\ in}$ | Mute in threshold voltage | (Amp: mute) | | | 1.5 | V |
| $V_{AM\ in}$ | $V_S$ automute threshold | (Amp: mute); Att ≥ 80dB; $P_{Oref}$ = 4Ω | | | 6.5 | V |
| | | (Amp: play); Att < 0.1dB; $P_O$ = 0.5Ω | | 7.6 | 8.5 | V |
| $I_{pin22}$ | Muting pin current | $V_{MUTE}$ = 1.5V (Source current) | 5 | 11 | 20 | µA |
| | | $V_{MUTE}$ = 3.5V | -5 | - | 20 | µA |

1. Saturated square wave output.

**Figure 3. Standard test and application circuit**



## 2.4 PCB and component layout

Referred to the circuit of *Figure 3*.

**Figure 4. Components and top copper layer**

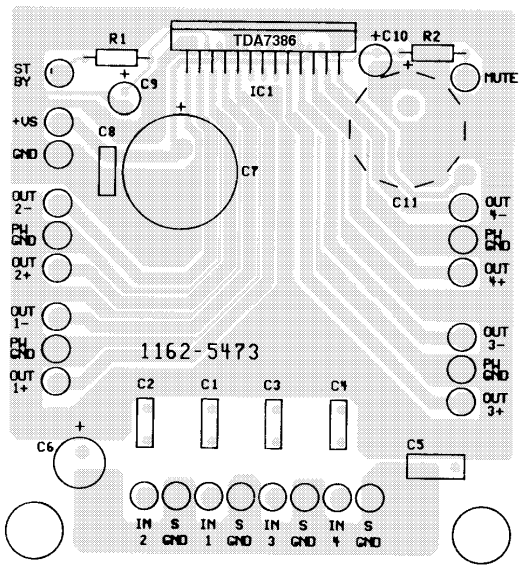
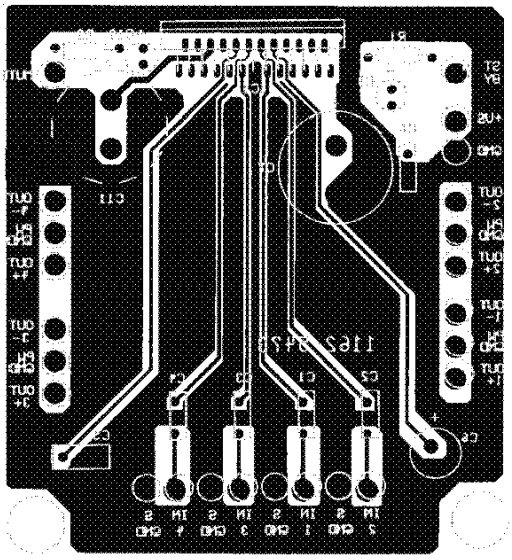



**Figure 5. Bottom copper layer**



## 2.5 Electrical characteristics curves

Figure 6. Quiescent current vs. supply voltage

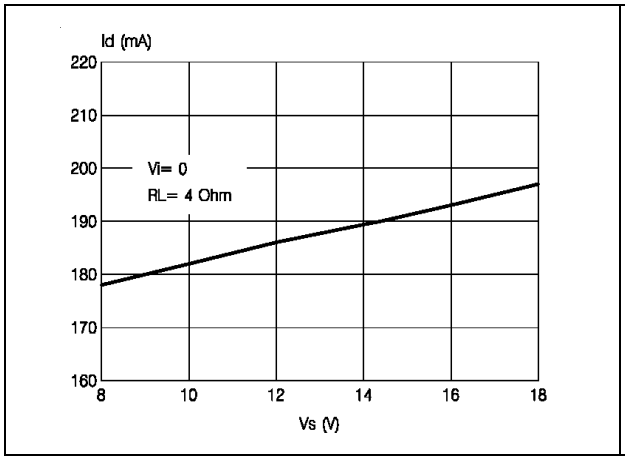



Figure 7. Quiescent output voltage vs. supply voltage

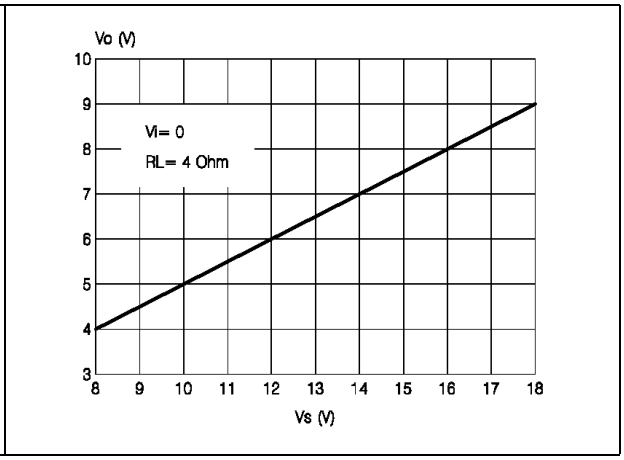



Figure 8. Output power vs. supply voltage

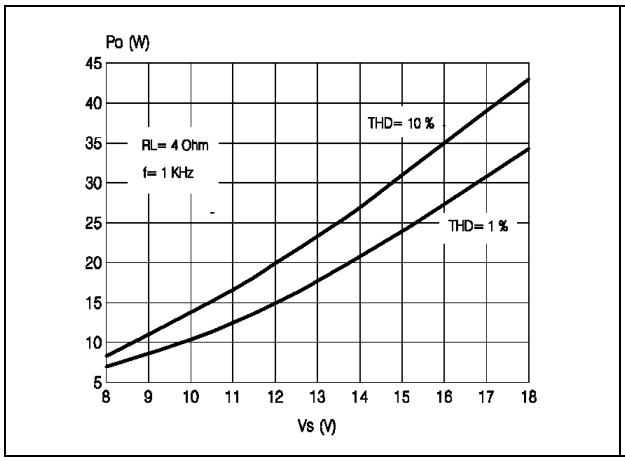



Figure 9. Max. output power vs. supply voltage

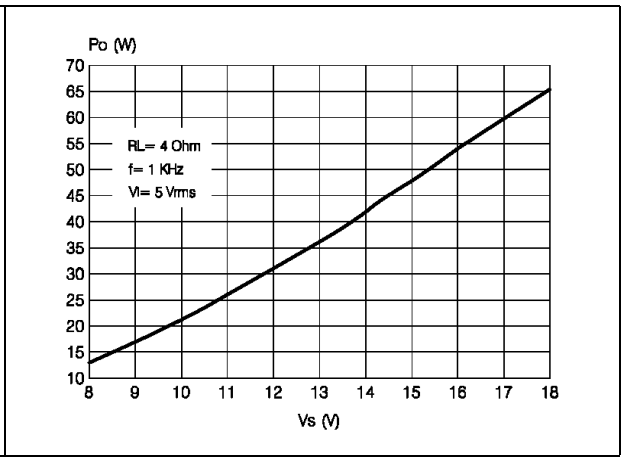



Figure 10. Distortion vs. output power

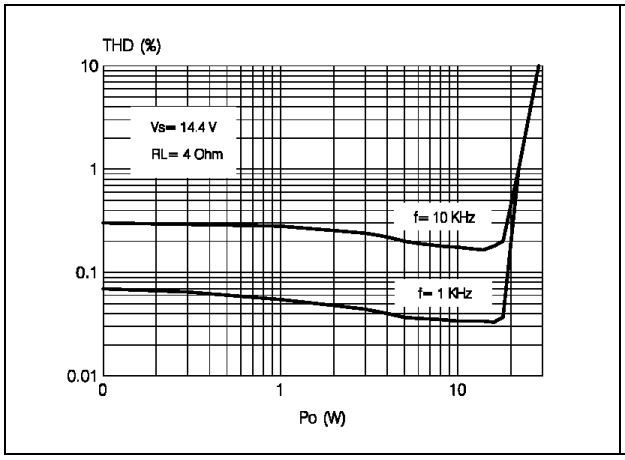



Figure 11. Distortion vs. frequency

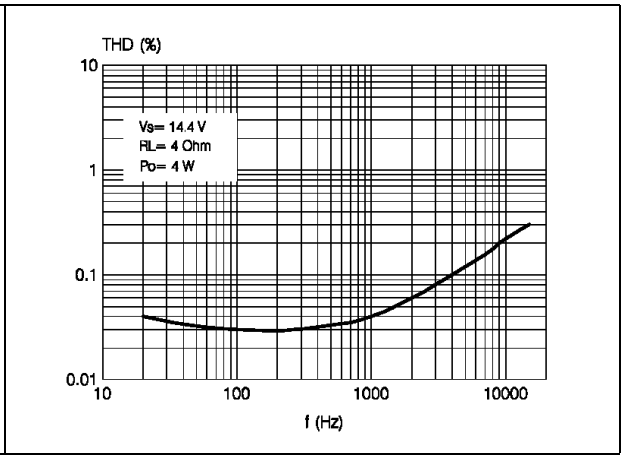


**Figure 12. Supply voltage rejection vs. frequency**

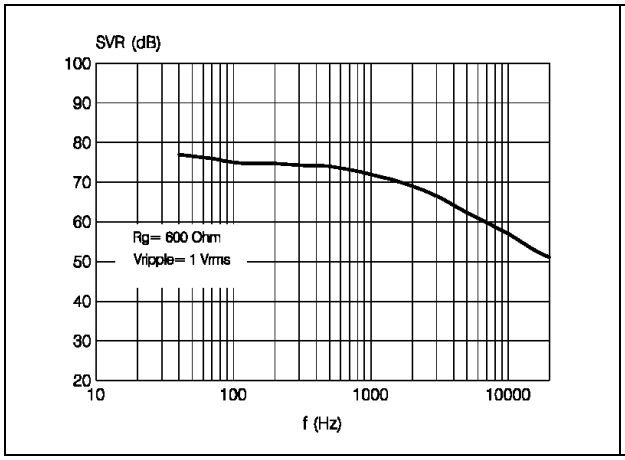



**Figure 13. Crosstalk vs. frequency**

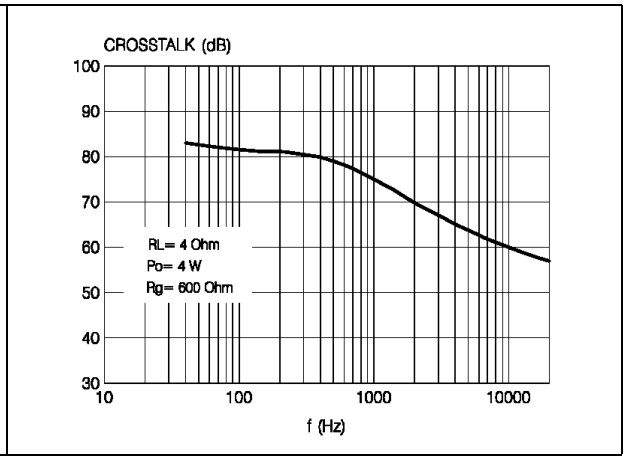



**Figure 14. Output noise vs. source resistance**

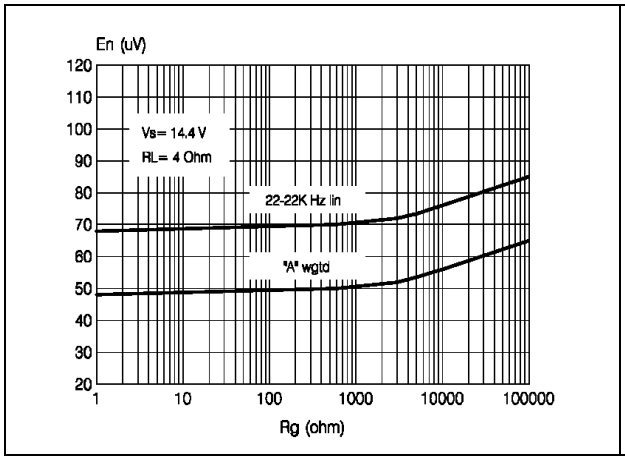
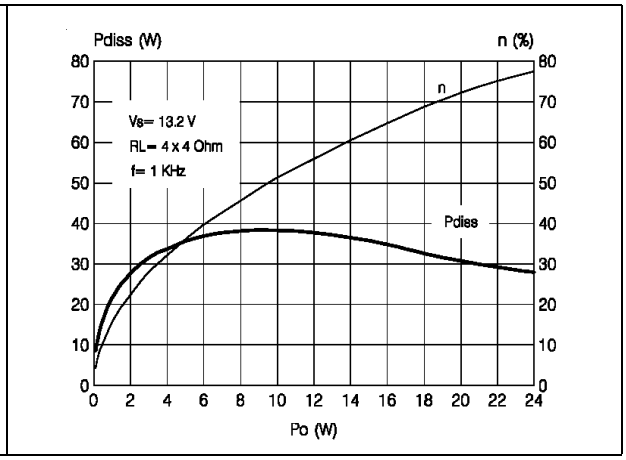



**Figure 15. Power dissipation and efficiency vs. output power**



# 3 Application hints

Referred to the circuit of *Figure 3*.

## 3.1 SVR

Besides its contribution to the ripple rejection, the SVR capacitor governs the turn ON/OFF time sequence and, consequently, plays an essential role in the pop optimization during ON/OFF transients.

To conveniently serve both needs, **ITS MINIMUM RECOMMENDED VALUE IS 10µF**.

## 3.2 Input stage

The TDA7386's inputs are ground-compatible and can stand very high input signals (±8Vpk) without any performances degradation.

If the standard value for the input capacitors (0.1µF) is adopted, the low frequency cut-off will amount to 16 Hz.

## 3.3 Standby and muting

Standby and muting facilities are both CMOS-compatible. If unused, a straight connection to Vs of their respective pins would be admissible.

Conventional/low-power transistors can be employed to drive muting and stand-by pins in absence of true CMOS ports or microprocessors. R-C cells have always to be used in order to smooth down the transitions for preventing any audible transient noises.

Since a DC current of about 10 µA normally flows out of pin 22, the maximum allowable muting-series resistance ($R_2$) is 70 KΩ, which is sufficiently high to permit a muting capacitor reasonably small (about 1µF).

If $R_2$ is higher than recommended, the involved risk will be that the voltage at pin 22 may rise to above the 1.5 V threshold voltage and the device will consequently fail to turn OFF when the mute line is brought down.

About the stand-by, the time constant to be assigned in order to obtain a virtually pop-free transition has to be slower than 2.5V/ms.

# 4 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

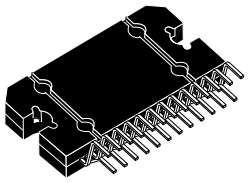
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

**Figure 16. Flexiwatt25 mechanical data and package dimensions**

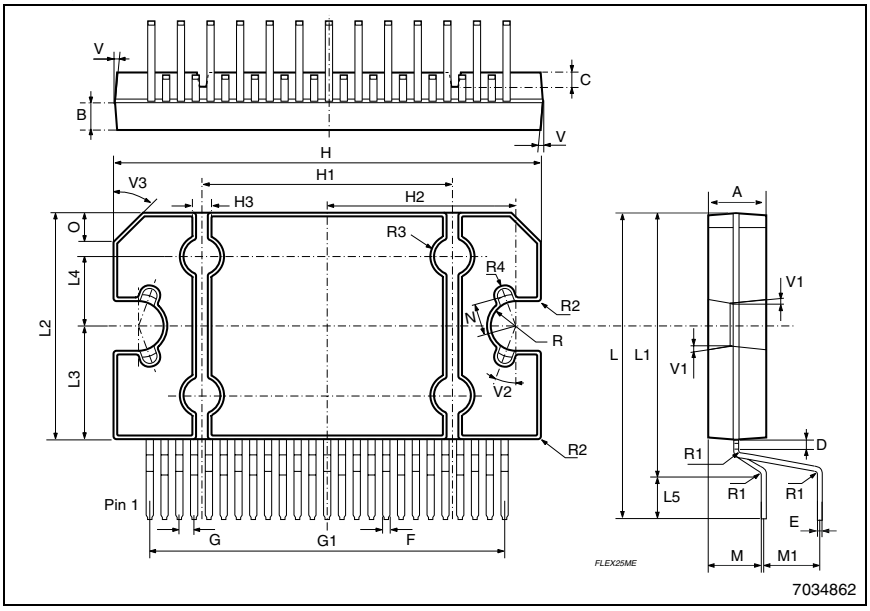
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 4.45 | 4.50 | 4.65 | 0.175 | 0.177 | 0.183 |
| B | 1.80 | 1.90 | 2.00 | 0.070 | 0.074 | 0.079 |
| C | | 1.40 | | | 0.055 | |
| D | 0.75 | 0.90 | 1.05 | 0.029 | 0.035 | 0.041 |
| E | 0.37 | 0.39 | 0.42 | 0.014 | 0.015 | 0.016 |
| F (1) | | | 0.57 | | | 0.022 |
| G | 0.80 | 1.00 | 1.20 | 0.031 | 0.040 | 0.047 |
| G1 | 23.75 | 24.00 | 24.25 | 0.935 | 0.945 | 0.955 |
| H (2) | 28.90 | 29.23 | 29.30 | 1.139 | 1.150 | 1.153 |
| H1 | | 17.00 | | | 0.669 | |
| H2 | | 12.80 | | | 0.503 | |
| H3 | | 0.80 | | | 0.031 | |
| L (2) | 22.07 | 22.47 | 22.87 | 0.869 | 0.884 | 0.904 |
| L1 | 18.57 | 18.97 | 19.37 | 0.731 | 0.747 | 0.762 |
| L2 (2) | 15.50 | 15.70 | 15.90 | 0.610 | 0.618 | 0.626 |
| L3 | 7.70 | 7.85 | 7.95 | 0.303 | 0.309 | 0.313 |
| L4 | | 5 | | | 0.197 | |
| L5 | | 3.5 | | | 0.138 | |
| M | 3.70 | 4.00 | 4.30 | 0.145 | 0.157 | 0.169 |
| M1 | 3.60 | 4.00 | 4.40 | 0.142 | 0.157 | 0.173 |
| N | | 2.20 | | | 0.086 | |
| O | | 2 | | | 0.079 | |
| R | | 1.70 | | | 0.067 | |
| R1 | | 0.5 | | | 0.02 | |
| R2 | | 0.3 | | | 0.12 | |
| R3 | | 1.25 | | | 0.049 | |
| R4 | | 0.50 | | | 0.019 | |
| V | 5° (T p.) | | | | | |
| V1 | 3° (Typ.) | | | | | |
| V2 | 20° (Typ.) | | | | | |
| V3 | 45° (Typ.) | | | | | |

(1): dam-bar protusion not included
(2): molding protusion included

**OUTLINE AND MECHANICAL DATA**



**Flexiwatt25 (vertical)**



# 5 Revision history

**Table 5. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 24-Nov-2001 | 1 | Initial release. |
| 20-Dec-2007 | 2 | Document reformatted.<br>Modified the *Features on page 1*.<br>Modified the *Figure 1* and *2*.<br>Updated the *Table 4: Electrical characteristics*. |
| 29-Oct-2008 | 3 | Updated the *Table 3: Thermal data on page 6*. |
| 19-Nov-2008 | 4 | Update the *Table 2: Absolute maximum ratings on page 6*. |

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