## Ordering Information:

**EMC1402-1-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE**

**EMC1402-2-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE**

**EMC1402-3-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE**

**EMC1402-4-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE**

**Note:** See Table 1.1, "Part Selection" for SMBus addressing options.

**REEL SIZE IS 4,000 PIECES.**

**This product meets the halogen maximum concentration values per IEC61249-2-21**

**For RoHS compliance and environmental information, please visit www.smsc.com/rohs**

*Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.*

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# Chapter 1 Block Diagram

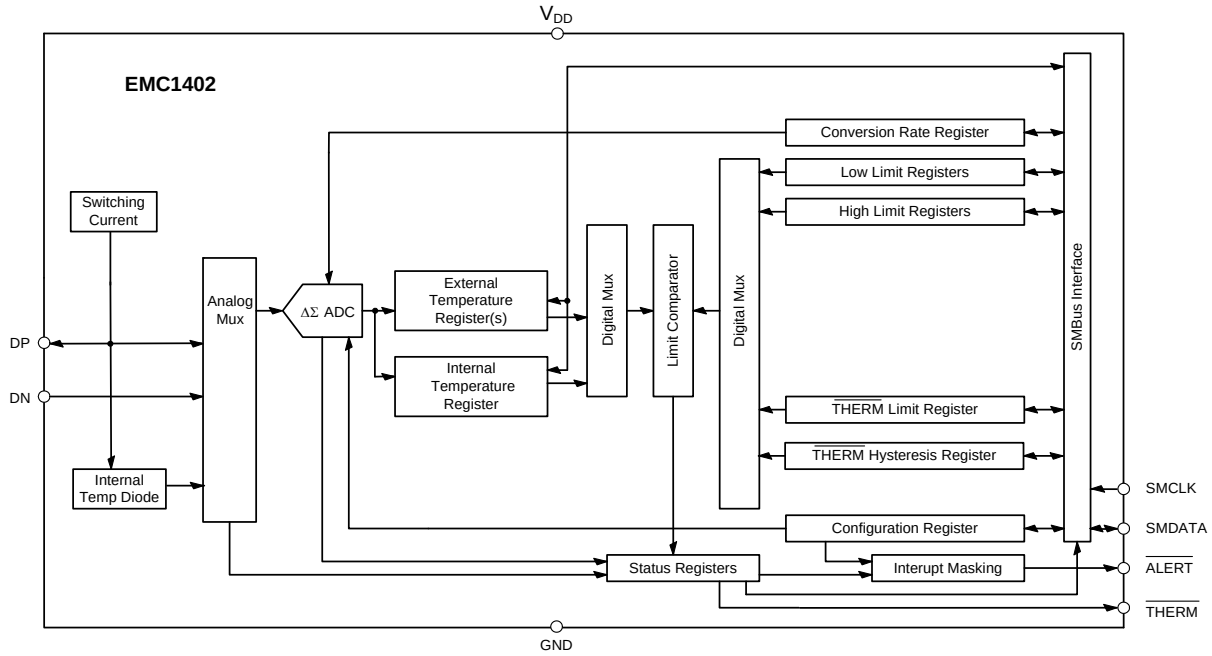



**Figure 1.1 EMC1402 Block Diagram**

## 1.1 Part Selection

The EMC1402 device configuration is highlighted below.

**Table 1.1 Part Selection**

| PART NUMBER | SMBUS ADDRESS | FUNCTIONALITY | | | | PRODUCT ID |
|---|---|---|---|---|---|---|
| | | EXTERNAL DIODES | DIODE 1 DEFAULT CONFIGURATION | DIODE 2 DEFAULT CONFIGURATION | OTHER | |
| EMC1402 - 1 | 1001_100xb | 1 | Detect Diode w/ REC enabled | N/A | Software program-mable and mask-able High Limits<br><br>Software program-mable THERM Limits | 20h |
| EMC1402 - 2 | 1001_101xb | | | | | |
| EMC1402 - 3 | 0011_000xb | | | | | |
| EMC1402 - 4 | 0101_001xb | | | | | |

# Chapter 2 Pin Description

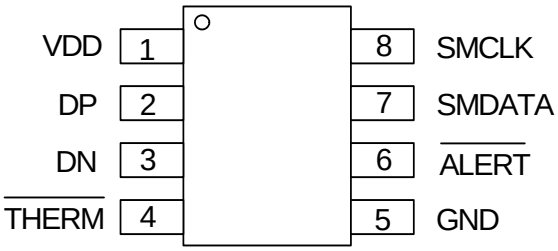



**Figure 2.1 EMC1402 Pin Diagram**

**Table 2.1 EMC1402 Pin Description**

| PIN NUMBER | NAME | FUNCTION | TYPE |
|---|---|---|---|
| 1 | VDD | Power supply | Power |
| 2 | DP | External diode positive (anode) connection | AIO |
| 3 | DN | External diode negative (cathode) connection | AIO |
| 4 | $\overline{\text{THERM}}$ | Active low Critical $\overline{\text{THERM}}$ output signal - requires pull-up resistor | OD (5V) |
| 5 | GND | Ground | Power |
| 6 | $\overline{\text{ALERT}}$ | Active low digital $\overline{\text{ALERT}}$ output signal - requires pull-up resistor | OD (5V) |
| 7 | SMDATA | SMBus Data input/output - requires pull-up resistor | DIOD (5V) |
| 8 | SMCLK | SMBus Clock input - requires pull-up resistor | DI (5V) |

**APPLICATION NOTE:** For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{THERM}}$, and $\overline{\text{ALERT}}$), the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

The pin types are described below:

Power - these pins are used to supply either VDD or GND to the device.

AIO - Analog Input / Output.

DI - Digital Input.

OD - Open Drain Digital Output.

DIOD - Digital Input / Open Drain Output.

# Chapter 3 Electrical Specifications

## 3.1 Absolute Maximum Ratings

**Table 3.1 Absolute Maximum Ratings**

| DESCRIPTION | RATING | UNIT |
|---|---|---|
| Supply Voltage ($V_{DD}$) | -0.3 to 4.0 | V |
| Voltage on 5V tolerant pins ($V_{5VT\_pin}$) | -0.3 to 5.5 | V |
| Voltage on 5V tolerant pins ($\|V_{5VT\_pin} - V_{DD}\|$) (see Note 3.1) | -0.3 to 3.6 | V |
| Voltage on any other pin to Ground | -0.3 to $V_{DD}$ +0.3 | V |
| Operating Temperature Range | -40 to +125 | °C |
| Storage Temperature Range | -55 to +150 | °C |
| Lead Temperature Range | Refer to JEDEC Spec. J-STD-020 | |
| Package Thermal Characteristics for MSOP-8 | | |
| Thermal Resistance ($\theta_{j-a}$) | 140.8 | °C/W |
| ESD Rating, All pins HBM | 2000 | V |

**Note:** Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

**Note 3.1** For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{THERM}}$, and $\overline{\text{ALERT}}$), the pull-up voltage must not exceed 3.6V when the device is unpowered.

## 3.2 Electrical Specifications

**Table 3.2 Electrical Specifications**

| $V_{DD}$ = 3.0V to 3.6V, $T_A$ = -40°C to 125°C, all typical values at $T_A$ = 27°C unless otherwise noted. | | | | | | |
|---|---|---|---|---|---|---|
| **CHARACTERISTIC** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNITS** | **CONDITIONS** |
| DC Power | | | | | | |
| Supply Voltage | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V | |
| Supply Current | $I_{DD}$ | | 430 | 850 | uA | 1 conversion / sec, dynamic averaging disabled |
| | | | 930 | 1200 | uA | 4 conversions / sec, dynamic averaging enabled |
| | | | 1120 | | uA | ≥ 16 conversions / sec, dynamic averaging enabled |
| Standby Supply Current | $I_{DD}$ | | 170 | 230 | uA | Device in Standby mode, no SMBus communications, ALERT and THERM pins not asserted. |
| Internal Temperature Monitor | | | | | | |
| Temperature Accuracy | | | ±0.25 | ±1 | °C | -5°C < $T_A$ < 100°C |
| | | | | ±2 | °C | -40°C < $T_A$ < 125°C |
| Temperature Resolution | | | 0.125 | | °C | |
| External Temperature Monitor | | | | | | |
| Temperature Accuracy | | | ±0.25 | ±1 | °C | +20°C < $T_{DIODE}$ < +110°C<br>0°C < $T_A$ < 100°C |
| | | | ±0.5 | ±2 | °C | -40°C < $T_{DIODE}$ < 127°C |
| Temperature Resolution | | | 0.125 | | °C | |
| Conversion Time all Channels | $t_{CONV}$ | | 190 | | ms | EMC1402, default settings |
| Capacitive Filter | $C_{FILTER}$ | | 2.2 | 2.5 | nF | Connected across external diode |
| $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins | | | | | | |
| Output Low Voltage | $V_{OL}$ | 0.4 | | | V | $I_{SINK}$ = 8mA |
| Leakage Current | $I_{LEAK}$ | | | ±5 | uA | $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins<br>Device powered or unpowered<br>$T_A$ < 85°C<br>pull-up voltage ≤ 3.6V |

## 3.3 SMBus Electrical Characteristics

**Table 3.3 SMBus Electrical Specifications**

| $V_{DD}$ = 3.0V to 3.6V, $T_A$ = -40°C to 125°C, all typical values are at $T_A$ = 27°C unless otherwise noted. | | | | | | |
|---|---|---|---|---|---|---|
| **CHARACTERISTIC** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNITS** | **CONDITIONS** |
| SMBus Interface | | | | | | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{DD}$ | V | 5V Tolerant |
| Input Low Voltage | $V_{IL}$ | -0.3 | | 0.8 | V | 5V Tolerant |
| Input High/Low Current | $I_{IH}$ / $I_{IL}$ | | | ±5 | uA | Powered or unpowered<br>TA < 85°C |
| Hysteresis | | | 420 | | mV | |
| Input Capacitance | $C_{IN}$ | | 5 | | pF | |
| Output Low Sink Current | $I_{OL}$ | 8.2 | | 15 | mA | SMDATA = 0.4V |
| SMBus Timing | | | | | | |
| Clock Frequency | $f_{SMB}$ | 10 | | 400 | kHz | |
| Spike Suppression | $t_{SP}$ | | | 50 | ns | |
| Bus free time Start to Stop | $t_{BUF}$ | 1.3 | | | us | |
| Hold Time: Start | $t_{HD:STA}$ | 0.6 | | | us | |
| Setup Time: Start | $t_{SU:STA}$ | 0.6 | | | us | |
| Setup Time: Stop | $t_{SU:STP}$ | 0.6 | | | us | |
| Data Hold Time | $t_{HD:DAT}$ | 0 | | | us | When transmitting to the master |
| Data Hold Time | $t_{HD:DAT}$ | 0.3 | | | us | When receiving from the master |
| Data Setup Time | $t_{SU:DAT}$ | 100 | | | ns | |
| Clock Low Period | $t_{LOW}$ | 1.3 | | | us | |
| Clock High Period | $t_{HIGH}$ | 0.6 | | | us | |
| Clock/Data Fall time | $t_{FALL}$ | | | 300 | ns | Min = 20+0.1$C_{LOAD}$ ns |
| Clock/Data Rise time | $t_{RISE}$ | | | 300 | ns | Min = 20+0.1$C_{LOAD}$ ns |
| Capacitive Load | $C_{LOAD}$ | | | 400 | pF | per bus line |

# Chapter 4 System Management Bus Interface Protocol

## 4.1 System Management Bus Interface Protocol

TheEMC1402 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1.

For the first 15ms after power-up the device may not respond to SMBus communications.

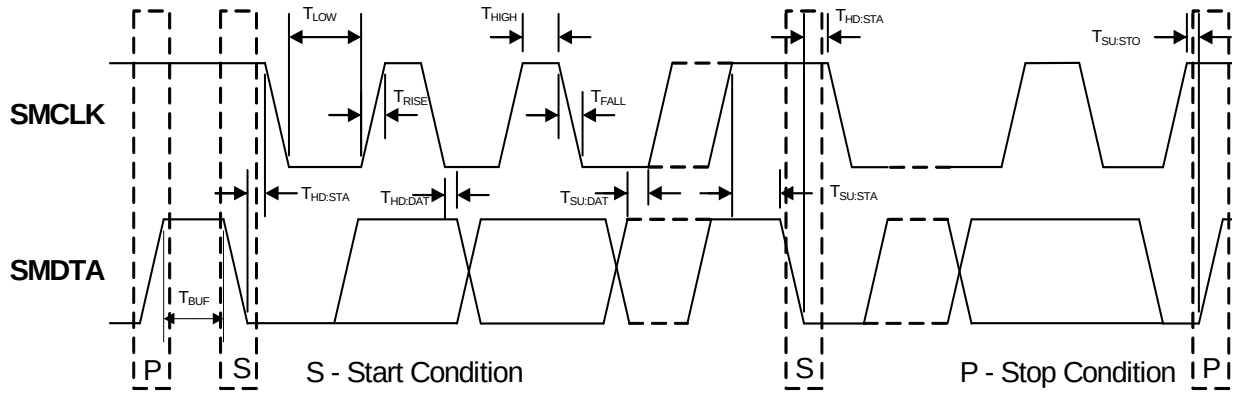



**Figure 4.1 SMBus Timing Diagram**

The EMC1402 is SMBus 2.0 compatible and support Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 4.1.

**Table 4.1 Protocol Format**

| DATA SENT TO DEVICE | DATA SENT TO THE HOST |
|---|---|
| # of bits sent | # of bits sent |

Attempting to communicate with the EMC1402 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

## 4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

**Table 4.2 Write Byte Protocol**

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | REGISTER DATA | ACK | STOP |
|---|---|---|---|---|---|---|---|---|
| 1 -> 0 | 1001_100 | 0 | 0 | XXh | 0 | XXh | 0 | 0 -> 1 |

## 4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

**Table 4.3 Read Byte Protocol**

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | START | SLAVE ADDRESS | RD | ACK | REGISTER DATA | NACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 -> 0 | 1001_100 | 0 | 1 | XXh | 0 | 1 -> 0 | 1001_100 | 1 | 1 | XX | 1 | 0 -> 1 |

## 4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

**Table 4.4 Send Byte Protocol**

| START | SLAVE ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | STOP |
|---|---|---|---|---|---|---|
| 1 -> 0 | 1001_100 | 0 | 0 | XXh | 0 | 0 -> 1 |

## 4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

**Table 4.5 Receive Byte Protocol**

| START | SLAVE ADDRESS | RD | ACK | REGISTER DATA | NACK | STOP |
|---|---|---|---|---|---|---|
| 1 -> 0 | 1001_100 | 1 | 0 | XXh | 1 | 0 -> 1 |

## 4.6 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 4.6.

**Table 4.6 Alert Response Address Protocol**

| START | ALERT RESPONSE ADDRESS | RD | ACK | DEVICE ADDRESS | NACK | STOP |
|---|---|---|---|---|---|---|
| 1 -> 0 | 0001_100 | 1 | 0 | 1001_1000 | 1 | 0 -> 1 |

The EMC1402 will respond to the ARA in the following way:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

**APPLICATION NOTE:** The ARA does not clear the Status Register and if the MASK bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

## 4.7 SMBus Address

The EMC1402 responds to hard-wired SMBus slave address as shown in Table 1.1.

**Note:** Other addresses are available. Contact SMSC for more information.

## 4.8 SMBus Timeout

The EMC1402 supports SMBus Timeout. If the clock line is held low for longer than 30ms, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit in the Consecutive Alert Register (see Section 6.11).

# Chapter 5 Product Description

The EMC1402 is an SMBus temperature sensor. The EMC1402 monitors one internal diode and one externally connected temperature diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1402 and using that data to control the speed of one or more fans.

The EMC1402 has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures exceeds user programmable limits. This allows the EMC1402 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. The second level of monitoring provides a non maskable interrupt on the $\overline{\text{THERM}}$ pin if the measured temperatures meet or exceed a second programmable limit.

Since the EMC1402 automatically corrects for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available with non-resistance error correcting devices. The automatic beta detection feature means that there is no need to program the device according to which type of diode is present. This also includes CPU diodes that require the transistor or BJT model for monitoring their temperature. Therefore, the EMC1402 can power up ready to operate for any system configuration.

Figure 5.1 shows a system level block diagram of the EMC1402.

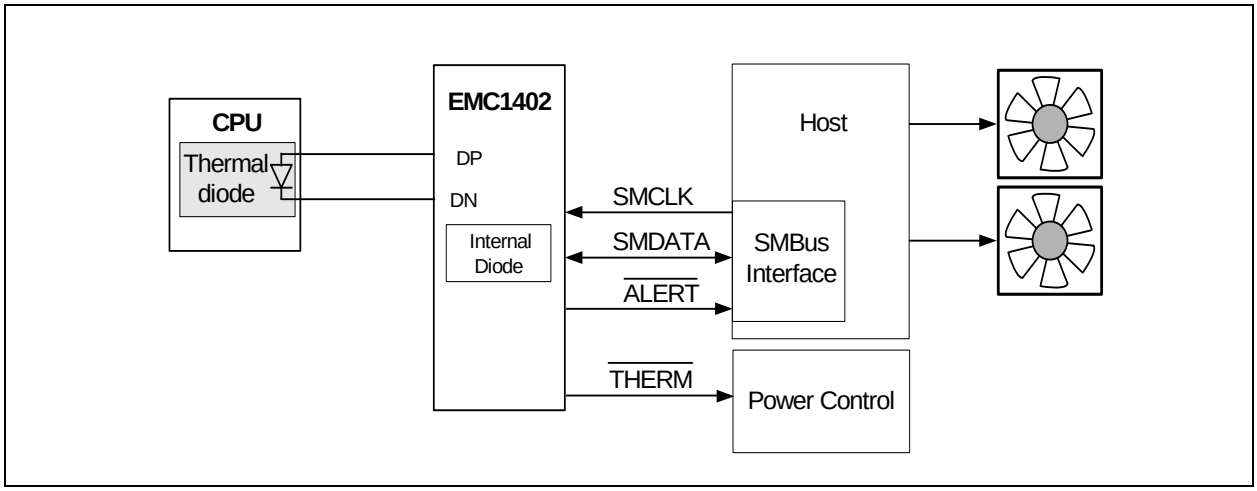



**Figure 5.1 System Diagram for EMC1402**

## 5.1 Modes of Operation

The EMC1402 has two modes of operation.

- Active (Run) - In this mode of operation, the ADC is converting on all temperature channels at the programmed conversion rate. The temperature data is updated at the end of every conversion and the limits are checked. In Active mode, writing to the one-shot register will do nothing.
- Standby (Stop) - In this mode of operation, the majority of circuitry is powered down to reduce supply current. The temperature data is not updated and the limits are not checked. In this mode of operation, the SMBus is fully active and the part will return requested data. Writing to the one-shot register will enable the device to update all temperature channels. Once all the channels are updated, the device will return to the Standby mode.

### 5.1.1 Conversion Rates

The EMC1402 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in Section 6.5. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 6.6.

### 5.1.2 Dynamic Averaging

Dynamic averaging causes the EMC1402 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Section 6.4). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 5.1 for the EMC1402**.**

**Table 5.1 Supply Current vs. Conversion Rate for EMC1402**

| CONVERSION RATE | AVERAGE SUPPLY CURRENT | | AVERAGING FACTOR (BASED ON 11-BIT OPERATION) | |
|---|---|---|---|---|
| | ENABLED (DEFAULT) | DISABLED | ENABLED (DEFAULT) | DISABLED |
| 1 / 16 sec | 660uA | 430uA | 16x | 1x |
| 1 / 8 sec | 660uA | 430uA | 16x | 1x |
| 1 / 4 sec | 660uA | 430uA | 16x | 1x |
| 1 / 2 sec | 660uA | 430uA | 16x | 1x |
| 1 / sec | 660uA | 430uA | 16x | 1x |
| 2 / sec | 930uA | 475uA | 16x | 1x |
| 4 / sec (default) | 950uA | 510uA | 8x | 1x |
| 8 / sec | 1010uA | 630uA | 4x | 1x |
| 16 / sec | 1020uA | 775uA | 2x | 1x |
| 32 / sec | 1050uA | 1050uA | 1x | 1x |
| 64 / sec | 1100uA | 1100uA | 0.5x | 0.5x |

## 5.2 $\overline{\text{THERM}}$ Output

The $\overline{\text{THERM}}$ output is asserted independently of the $\overline{\text{ALERT}}$ output and cannot be masked. Whenever any of the measured temperatures exceed the user programmed THERM Limit values for the programmed number of consecutive measurements, the $\overline{\text{THERM}}$ output is asserted. Once it has been asserted, it will remain asserted until all measured temperatures drop below the THERM Limit minus the THERM Hysteresis (also programmable).

When the THERM pin is asserted, the Therm status bits will likewise be set. Reading these bits will not clear them until the THERM pin is deasserted. Once the THERM pin is deasserted, the THERM status bits will be automatically cleared.

## 5.3 ALERT Output

The ALERT pin is an open drain output and requires a pull-up resistor to $V_{DD}$ and has two modes of operation: interrupt mode and comparator Mode. The mode of the ALERT output is selected via the ALERT / COMP bit in the Configuration Register (see Section 6.4).

### 5.3.1 ALERT Pin Interrupt Mode

When configured to operate in interrupt mode, the ALERT pin asserts low when an out of limit measurement (≥ high limit or < low limit) is detected on any diode or when a diode fault is detected. The ALERT pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the ALERT pin will remain asserted until the appropriate status bits are cleared.

The ALERT pin can be masked by setting the MASK bit. Once the ALERT pin has been masked, it will be de-asserted and remain de-asserted until the MASK bit is cleared by the user. Any interrupt conditions that occur while the ALERT pin is masked will update the Status Register normally.

The ALERT pin is used as an interrupt signal or as an Smbus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more ALERT outputs can be hard-wired together.

### 5.3.2 ALERT Pin Comparator Mode

When the ALERT pin is configured to operate in comparator mode it will be asserted if any of the measured temperatures exceeds the respective high limit. The ALERT pin will remain asserted until all temperatures drop below the corresponding high limit minus the THERM Hysteresis value.

When the ALERT pin is asserted in comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the ALERT pin is deasserted. Once the ALERT pin is deasserted, the status bits will be automatically cleared.

The MASK bit will not block the ALERT pin in this mode, however the individual channel masks (see Section 6.10) will prevent the respective channel from asserting the ALERT pin.

## 5.4 Beta Compensation

The EMC1402 is configured to monitor the temperature of basic diodes (e.g. 2N3904), or CPU thermal diodes. It automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation.Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

## 5.5 Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e. on the processor) metal

resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1402 automatically corrects up to 100 ohms of series resistance.

## 5.6 Programmable External Diode Ideality Factor

The EMC1402 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement which must be corrected for. This correction is typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the EMC1402 provides a 6-bit register for each external diode where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

**APPLICATION NOTE:** When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

## 5.7 Diode Faults

The EMC1402 detects an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT pin asserts (unless masked, see Section 5.8) and the temperature data reads 00h in the MSB and LSB registers (note: the low limit will not be checked). A diode fault is defined as one of the following: an open between DP and DN, a short from $V_{DD}$ to DP, or a short from $V_{DD}$ to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the ALERT pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000degC (-64°C in extended range) resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

## 5.8 Consecutive Alerts

The EMC1402 contains multiple consecutive alert counters. One set of counters applies to the $\overline{\text{ALERT}}$ pin and the second set of counters applies to the $\overline{\text{THERM}}$ pin. Each temperature measurement channel has a separate consecutive alert counter for each of the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

See Section 6.11 for more details on the consecutive alert function.

## 5.9 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled. The typical filter performance is shown in Figure 5.2 and Figure 5.3.

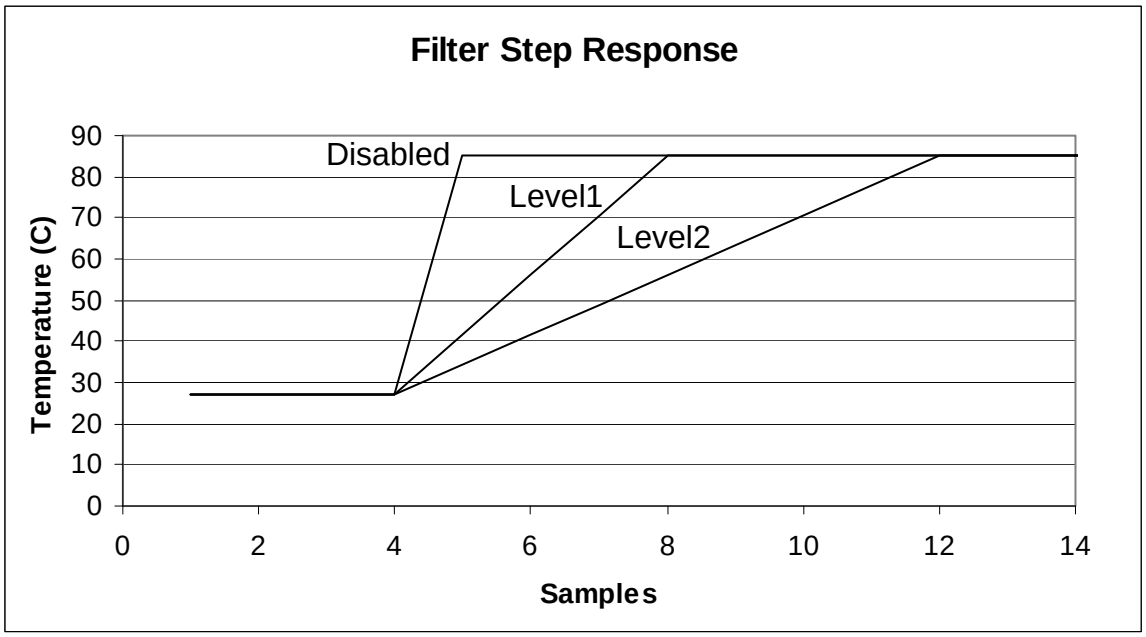



**Figure 5.2 Temperature Filter Step Response**

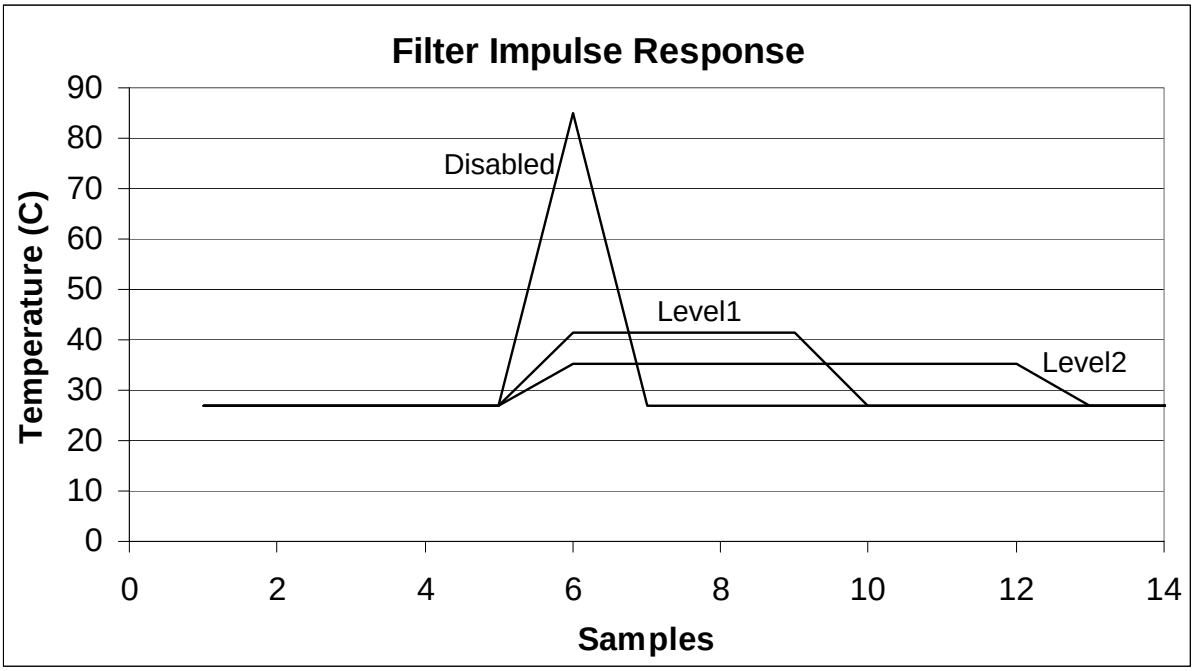



**Figure 5.3 Temperature Filter Impulse Response**

## 5.10 Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. This $\Delta V_{BE}$ is proportional to absolute temperature as shown in the following equation:

$$\Delta V_{BE} = \frac{\eta kT}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right) \quad \textbf{[1]}$$

where:

$k$ = Boltzmann's constant

$T$ = absolute temperature in Kelvin

$q$ = electron charge

$\eta$ = diode ideality factor

Figure 5.4 shows a block diagram of the temperature measurement circuit. The negative terminal for the remote temperature diode, DN, is internally biased with a forward diode voltage referenced to ground.

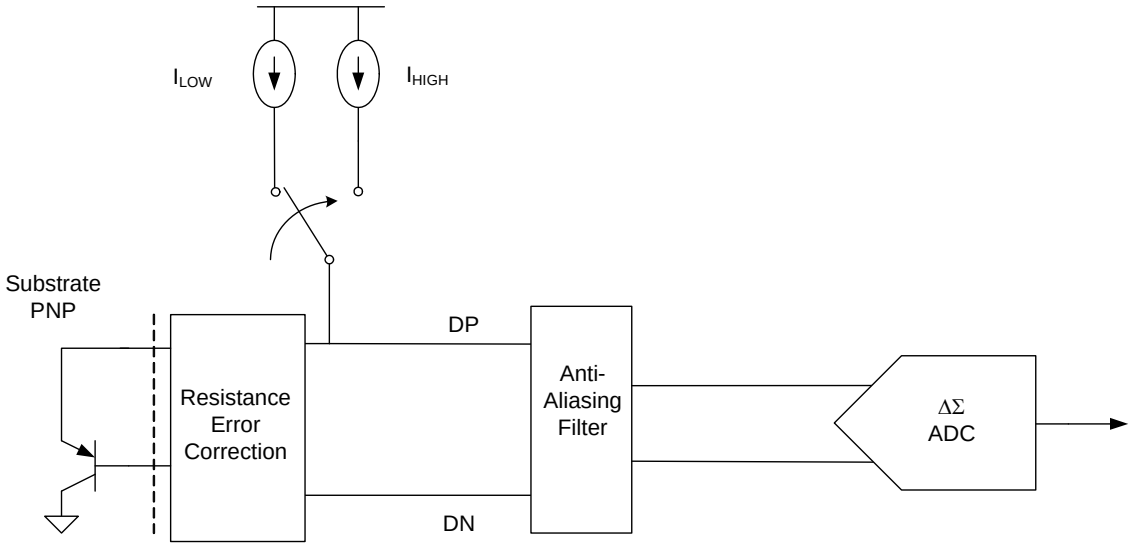



**Figure 5.4 Block Diagram of Temperature Monitoring Circuit**

## 5.11 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1402 has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 5.2 shows the default and extended range formats.

**Table 5.2 Temperature Data Format**

| TEMPERATURE (°C) | DEFAULT RANGE 0°C TO 127°C | EXTENDED RANGE -64°C TO 191°C |
|---|---|---|
| Diode Fault | 000 0000 0000 | 000 0000 0000 |
| -64 | 000 0000 0000 | 000 0000 0000<br>Note 5.2 |
| -1 | 000 0000 0000 | 001 1111 1000 |
| 0 | 000 0000 0000<br>Note 5.1 | 010 0000 0000 |
| 0.125 | 000 0000 0001 | 010 0000 0001 |
| 1 | 000 0000 1000 | 010 0000 1000 |
| 64 | 010 0000 0000 | 100 0000 0000 |
| 65 | 010 0000 1000 | 100 0000 1000 |
| 127 | 011 1111 1000 | 101 1111 1000 |
| 127.875 | 011 1111 1111 | 101 1111 1111 |
| 128 | 011 1111 1111<br>Note 5.3 | 110 0000 0000 |
| 190 | 011 1111 1111 | 111 1111 0000 |
| 191 | 011 1111 1111 | 111 1111 1000 |
| >= 191.875 | 011 1111 1111 | 111 1111 1111<br>Note 5.4 |

**Note 5.1** In default mode, all temperatures < 0°C will be reported as 0°C.

**Note 5.2** In the extended range, all temperatures < -64°C will be reported as -64°C.

**Note 5.3** For the default range, all temperatures > +127.875°C will be reported as +127.875°C.

**Note 5.4** For the extended range, all temperatures > +191.875°C will be reported as +191.875°C.

## 5.12 External Diode Connections

The EMC1402 can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode, or an AMD processor diode. The diode can be connected in a variety of ways as indicated in Figure 5.5.

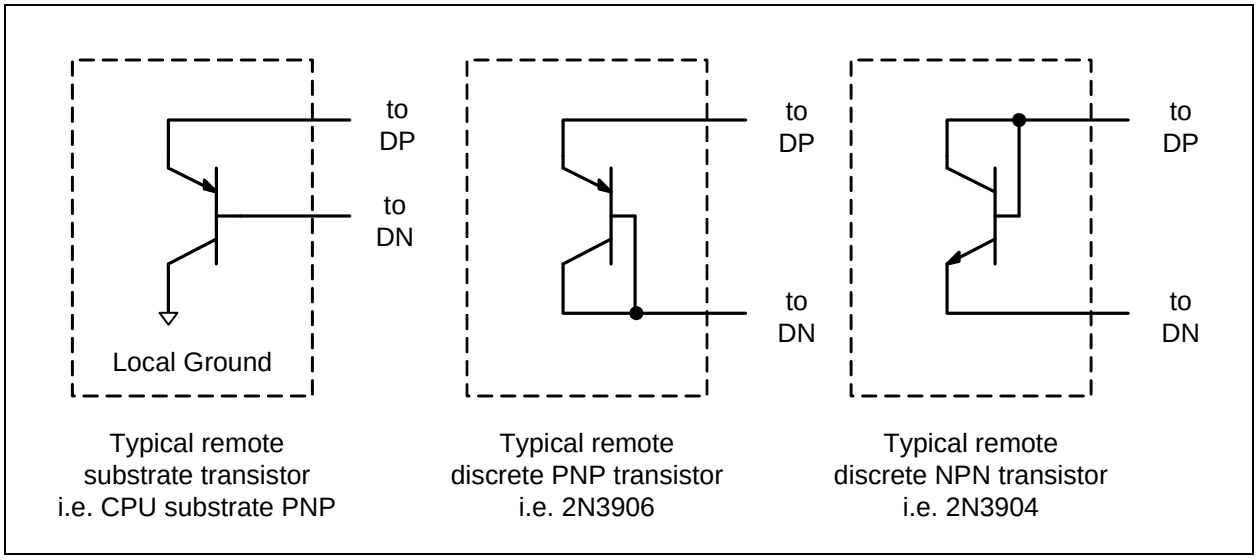



**Figure 5.5 Diode Configurations**

# Chapter 6 Register Description

The registers shown in Table 6.1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

**Table 6.1 Register Set in Hexadecimal Order**

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|---|---|---|---|---|---|
| 00h | R | Internal Diode Data High Byte | Stores the integer data for the Internal Diode | 00h | Page 25 |
| 01h | R | External Diode Data High Byte | Stores the integer data for the External Diode | 00h | |
| 02h | R-C | Status | Stores status bits for the Internal Diode and External Diodes | 00h | Page 25 |
| 03h | R/W | Configuration | Controls the general operation of the device (mirrored at address 09h) | 00h | Page 26 |
| 04h | R/W | Conversion Rate | Controls the conversion rate for updating temperature data (mirrored at address 0Ah) | 06h (4/sec) | Page 27 |
| 05h | R/W | Internal Diode High Limit | Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh) | 55h (85°C) | Page 28 |
| 06h | R/W | Internal Diode Low Limit | Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch) | 00h (0°C) | |
| 07h | R/W | External Diode High Limit High Byte | Stores the integer portion of the high limit for the External Diode (mirrored at register 0Dh) | 55h (85°C) | |
| 08h | R/W | External Diode Low Limit High Byte | Stores the integer portion of the low limit for the External Diode (mirrored at register 0Eh) | 00h (0°C) | |
| 09h | R/W | Configuration | Controls the general operation of the device (mirrored at address 03h) | 00h | Page 26 |
| 0Ah | R/W | Conversion Rate | Controls the conversion rate for updating temperature data (mirrored at address 04h) | 06h (4/sec) | Page 27 |

**Table 6.1 Register Set in Hexadecimal Order (continued)**

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|---|---|---|---|---|---|
| 0Bh | R/W | Internal Diode High Limit | Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h) | 55h (85°C) | Page 28 |
| 0Ch | R/W | Internal Diode Low Limit | Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h) | 00h (0°C) | |
| 0Dh | R/W | External Diode High Limit High Byte | Stores the integer portion of the high limit for the External Diode (mirrored at register 07h) | 55h (85°C) | |
| 0Eh | R/W | External Diode Low Limit High Byte | Stores the integer portion of the low limit for the External Diode (mirrored at register 08h) | 00h (0°C) | |
| 0Fh | W | One shot | A write to this register initiates a one shot update. | 00h | Page 29 |
| 10h | R | External Diode Data Low Byte | Stores the fractional data for the External Diode | 00h | Page 25 |
| 11h | R/W | Scratchpad | Scratchpad register for software compatibility | 00h | Page 28 |
| 12h | R/W | Scratchpad | Scratchpad register for software compatibility | 00h | Page 28 |
| 13h | R/W | External Diode High Limit Low Byte | Stores the fractional portion of the high limit for the External Diode | 00h | Page 28 |
| 14h | R/W | External Diode Low Limit Low Byte | Stores the fractional portion of the low limit for the External Diode | 00h | |
| 19h | R/W | External Diode THERM Limit | Stores the 8-bit critical temperature limit for the External Diode | 55h (85°C) | Page 29 |
| 1Fh | R/W | Channel Mask Register | Controls the masking of individual channels | 00h | Page 29 |
| 20h | R/W | Internal Diode THERM Limit | Stores the 8-bit critical temperature limit for the Internal Diode | 55h (85°C) | Page 29 |
| 21h | R/W | THERM Hysteresis | Stores the 8-bit hysteresis value that applies to all THERM limits | 0Ah (10°C) | |
| 22h | R/W | Consecutive ALERT | Controls the number of out-of-limit conditions that must occur before an interrupt is asserted | 70h | Page 30 |
| 25h | R/W | External Diode 1 Beta Configuration | Stores the Beta Compensation circuitry settings for External Diode 1 | 08h | Page 31 |
| 27h | R/W | External Diode 1 Ideality Factor | Stores the ideality factor for External Diode 1 | 12h (1.008) | Page 32 |
| 29h | R | Internal Diode Data Low Byte | Stores the fractional data for the Internal Diode | 00h | Page 25 |

**Table 6.1 Register Set in Hexadecimal Order (continued)**

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|---|---|---|---|---|---|
| 40h | R/W | Filter Control | Controls the digital filter setting for the External Diode channel | 00h | Page 34 |
| FDh | R | Product ID | Stores a fixed value that identifies each product | Table 6.21 | Page 34 |
| FEh | R | SMSC ID | Stores a fixed value that represents SMSC | 5Dh | Page 35 |
| FFh | R | Revision | Stores a fixed value that represents the revision number | 01h or 04h | Page 35 |

## 6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

## 6.2 Temperature Data Registers

**Table 6.2 Temperature Data Registers**

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | R | Internal Diode High Byte | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 29h | R | Internal Diode Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 01h | R | External Diode High Byte | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 10h | R | External Diode Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |

As shown in Table 6.2, all temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits.

## 6.3 Status Register

**Table 6.3 Status Register**

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 02h | R-C | Status | BUSY | IHIGH | ILOW | EHIGH | ELOW | FAULT | ETHERM | ITHERM | 00h |

The Status Register reports the operating status of the Internal Diode and External Diode 1 channels. When any of the bits are set (excluding the BUSY bit) either the $\overline{\text{ALERT}}$ or $\overline{\text{THERM}}$ pin is being asserted.

The $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins are controlled by the respective consecutive alert counters (see Section 6.11) and will not be asserted until the programmed consecutive alert count has been reached. The status bits (except E1THERM and ITHERM) will remain set until read unless the $\overline{\text{ALERT}}$ pin is configured as a second $\overline{\text{THERM}}$ output (see Section 5.3.2).

Bit 7 - BUSY - This bit indicates that the ADC is currently converting. This bit does not cause either the $\overline{\text{ALERT}}$ or $\overline{\text{THERM}}$ pins to be asserted.

Bit 6 - IHIGH - This bit is set when the Internal Diode channel exceeds its programmed high limit. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 5 - ILOW - This bit is set when the Internal Diode channel drops below its programmed low limit. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 4 - EHIGH - This bit is set when the External Diode channel exceeds its programmed high limit. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 3 - ELOW - This bit is set when the External Diode channel drops below its programmed low limit. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 2 - FAULT - This bit is asserted when a diode fault is detected. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

Bit 1 - ETHERM - This bit is set when the External Diode channel exceeds the programmed THERM limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin. This bit will remain set until the $\overline{\text{THERM}}$ pin is released at which point it will be automatically cleared.

Bit 0 - ITHERM - This bit is set when the Internal Diode channel exceeds the programmed THERM limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin. This bit will remain set until the $\overline{\text{THERM}}$ pin is released at which point it will be automatically cleared.

## 6.4 Configuration Register

**Table 6.4 Configuration Register**

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 03h | R/W | Configuration | MASK_ ALL | RUN/ STOP | ALERT/ COMP | RECD | - | RANGE | DAVG_ DIS | - | 00h |
| 09h | | | | | | | | | | | |

The Configuration Register controls the basic operation of the device. This register is fully accessible at either address.

Bit 7 - MASK_ALL - Masks the $\overline{\text{ALERT}}$ pin from asserting.

- '0' (default) - The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set the $\overline{\text{ALERT}}$ pin will be asserted.
- '1' - The $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition unless it is configured as a secondary $\overline{\text{THERM}}$ pin. The Status Register will be updated normally.

Bit 6 - RUN / STOP - Controls Active/Standby modes.

- '0' (default) - The device is in Active mode and converting on all channels.
- '1' -The device is in Standby mode and not converting.

Bit 5 - ALERT/COMP - Controls the operation of the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin acts as described in Section 5.3.
- '1' - The $\overline{\text{ALERT}}$ pin acts in comparator mode as described in Section 5.3.2. In this mode the MASK_ALL bit is ignored.

Bit 4 - RECD - Disables the Resistance Error Correction (REC) for External Diode.

- '0' (default)- REC is enabled for the External Diode.

- '1' - REC is disabled for the External Diode 1.

Bit 2 - RANGE - Configures the measurement range and data format of the temperature channels.

- '0' (default) - The temperature measurement range is 0°C to +127.875°C and the data format is binary.
- '1' -The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see Table 5.2).

Bit 1 - DAVG_DIS - Disables the dynamic averaging feature on all temperature channels.

- '0' (default) - The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 5.1.
- '1' - The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced as shown in Table 5.1.

## 6.5 Conversion Rate Register

**Table 6.5 Conversion Rate Register**

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 04h | R/W | Conversion Rate | - | - | - | - | CONV[3:0] | | | | 06h (4/sec) |
| 0Ah | | | | | | | | | | | |

The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

Bits 3-0 - CONV[3:0] - Determines the conversion rate as shown in Table 6.6.

**Table 6.6 Conversion Rate**

| CONV[3:0] | | | | | CONVERSIONS / SECOND |
|---|---|---|---|---|---|
| HEX | 3 | 2 | 1 | 0 | |
| 0h | 0 | 0 | 0 | 0 | 1 / 16 |
| 1h | 0 | 0 | 0 | 1 | 1 / 8 |
| 2h | 0 | 0 | 1 | 0 | 1 / 4 |
| 3h | 0 | 0 | 1 | 1 | 1 / 2 |
| 4h | 0 | 1 | 0 | 0 | 1 |
| 5h | 0 | 1 | 0 | 1 | 2 |
| 6h | 0 | 1 | 1 | 0 | 4 (default) |
| 7h | 0 | 1 | 1 | 1 | 8 |
| 8h | 1 | 0 | 0 | 0 | 16 |
| 9h | 1 | 0 | 0 | 1 | 32 |
| Ah | 1 | 0 | 1 | 0 | 64 |
| Bh - Fh | All others | | | | 1 |

## 6.6 Limit Registers

**Table 6.7 Temperature Limit Registers**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 05h<br>0Bh | R/W | Internal Diode High Limit | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 06h<br>0Ch | R/W | Internal Diode Low Limit | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 07h<br>0Dh | R/W | External Diode High Limit High Byte | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 13h | R/W | External Diode High Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |
| 08h<br>0Eh | R/W | External Diode Low Limit High Byte | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h (0°C) |
| 14h | R/W | External Diode Low Limit Low Byte | 0.5 | 0.25 | 0.125 | - | - | - | - | - | 00h |

The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted.

The data format for the limits must match the selected data format for the temperature so that if the extended temperature range is used, the limits must be programmed in the extended data format.

The limit registers with multiple addresses are fully accessible at either address.

When the device is in standby mode, updating the limit registers will have no affect until the next conversion cycle occurs. This can be initiated via a write to the One Shot Register or by clearing the RUN / STOP bit in the Configuration Register (see Section 6.4).

## 6.7 Scratchpad Registers

**Table 6.8 Scratchpad Register**

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 11h | R/W | Scratchpad | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 00h |
| 12h | R/W | Scratchpad | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 00h |

The Scratchpad Registers are Read Write registers that are used for place holders to be software compatible with legacy programs. Reading from the registers will return what is written to them.

## 6.8 One Shot Register

**Table 6.9 One Shot Register**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Fh | W | One Shot | Writing to this register initiates a single conversion cycle. Data is not stored and always reads 00h | | | | | | | | 00h |

The One Shot Register is used to initiate a one shot command. Writing to the one shot register, when the device is in standby mode and BUSY bit (in Status Register) is '0', will immediately cause the ADC to update all temperature measurements. Writing to the One Shot Register while the device is in active mode will have no affect.

## 6.9 Therm Limit Registers

**Table 6.10 Therm Limit Registers**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 19h | R/W | External Diode THERM Limit | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 20h | R/W | Internal Diode THERM Limit | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 55h (85°C) |
| 21h | R/W | THERM Hysteresis | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 0Ah (10°C) |

The THERM Limit Registers are used to determine whether a critical thermal event has occurred. If the measured temperature exceeds the THERM Limit, then the $\overline{\text{THERM}}$ pin is asserted. The limit setting must match the chosen data format of the temperature reading registers.

Unlike the $\overline{\text{ALERT}}$ pin, the $\overline{\text{THERM}}$ pin cannot be masked. Additionally, the $\overline{\text{THERM}}$ pin will be released once the temperature drops below the corresponding threshold minus the THERM Hysteresis.

## 6.10 Channel Mask Register

**Table 6.11 Channel Mask Register**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1Fh | R/W | Channel Mask | - | - | - | - | - | - | E MASK | INT MASK | 00h |

The Channel Mask Register controls individual channel masking. When a channel is masked, the $\overline{\text{ALERT}}$ pin will not be asserted when the masked channel reads a diode fault or out of limit error. The channel mask does not mask the $\overline{\text{THERM}}$ pin.

Bit 1 - EMASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode channel is out of limit or reports a diode fault.

- '0' (default) - The External Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

- '1' - The External Diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

Bit 0 - INTMASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the Internal Diode temperature is out of limit.

- '0' (default) - The Internal Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit.
- '1' - The Internal Diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit.

## 6.11 Consecutive ALERT Register

**Table 6.12 Consecutive ALERT Register**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 22h | R/W | Consecutive ALERT | TIME OUT | CTHRM[2:0] | | | CALRT[2:0] | | | - | 70h |

The Consecutive ALERT Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the $\overline{\text{ALERT}}$ or THERM pin is asserted. Additionally, the Consecutive ALERT Register controls the SMBus Timeout functionality.

An out-of-limit condition (i.e. HIGH, LOW, or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if no out-of-limit condition or diode fault condition occurs in a consecutive reading.

When the ALERT pin is configured as an interrupt, when the consecutive alert counter reaches its programmed value, the following will occur: the STATUS bit(s) for that channel and the last error condition(s) (i.e. EHIGH) will be set to '1', the $\overline{\text{ALERT}}$ pin will be asserted, the consecutive alert counter will be cleared, and measurements will continue.

When the $\overline{\text{ALERT}}$ pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature exceeds the High Limit. Additionally, once the consecutive alert counter reaches the programmed limit, the $\overline{\text{ALERT}}$ pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the THERM Hysteresis value.

For example, if the CALRT[2:0] bits are set for 4 consecutive alerts, the high limits are set at 70°C, and none of the channels are masked, then the $\overline{\text{ALERT}}$ pin will be asserted after the following four measurements:

1. Internal Diode reads 71°C and the external diode reads 69°C. Consecutive alert counter for INT is incremented to 1.
2. Both the Internal Diode and the External Diode read 71°C. Consecutive alert counter for INT is incremented to 2and for EXT is set to 1.
3. The External Diode reads 71°C and the Internal Diode reads 69°C. Consecutive alert counter for INT is cleared and EXT is incremented to 2.
4. The Internal Diode reads 71°C and the external diode reads 71°C. Consecutive alert counter for INT is set to 1 and EXT is incremented to 3.
5. The Internal Diode reads 71°C and the external diode reads 71°C. Consecutive alert counter for INT is incremented to 2 and EXT is incremented to 4. The appropriate status bits are set for EXT and the $\overline{\text{ALERT}}$ pin is asserted. EXT counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

Bit 7 - TIMEOUT - Determines whether the SMBus Timeout function is enabled.

- '0' (default) - The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol.

- '1' - The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30ms, then the device will reset the SMBus protocol.

Bits 6-4 - CTHRM[2:0] - Determines the number of consecutive measurements that must exceed the corresponding THERM Limit before the $\overline{\text{THERM}}$ pin is asserted. All temperature channels use this value to set the respective counters. The consecutive THERM counter is incremented whenever any measurement exceed the corresponding THERM Limit.

If the temperature drops below the THERM limit, then the counter is reset. If a number of consecutive measurements above the THERM limit occurs, then the $\overline{\text{THERM}}$ pin is asserted low.

Once the $\overline{\text{THERM}}$ pin has been asserted, the consecutive therm counter will not reset until the corresponding temperature drops below the THERM Limit minus the THERM Hysteresis value.

The bits are decoded as shown in Table 6.13. The default setting is 4 consecutive out of limit conversions.

Bits 3-1 - CALRT[2:0] - Determine the number of consecutive measurements that must have an out of limit condition or diode fault before the $\overline{\text{ALERT}}$ pin is asserted. All temperature channels use this value to set the respective counters. The bits are decoded as shown in Table 6.13. The default setting is 1 consecutive out of limit conversion.

**Table 6.13 Consecutive Alert / THERM Settings**

| 2 | 1 | 0 | NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS |
|---|---|---|---|
| 0 | 0 | 0 | 1 (default for CALRT[2:0]) |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 1 | 1 | 4 (default for CTHRM[2:0]) |

## 6.12 Beta Configuration Registers

**Table 6.14 Beta Configuration Registers**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 25h | R/W | External Diode 1 Beta Configuration | - | - | - | - | ENABLE | BETA[2:0] | | | 08h |

This register is used to set the Beta Compensation factor that is used for the external diode channel.

Bit 3 - ENABLE - Enables the Beta Compensation factor autodetection function.

- '0' - The Beta Compensation Factor autodetection circuitry is disabled. The External Diode will always use the Beta Compensation factor set by the BETA[2:0] bits.
- '1' (default) - The Beta Compensation factor autodetection circuitry is enabled. At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETA[2:0] bits will be automatically updated to indicate the current setting.

Bit 2-0 - BETA[2:0] - These bits always reflect the current beta configuration settings. If autodetection circuitry is enabled, then these bits will be updated automatically and writing to these bits will have no effect. If the autodetection circuitry is disabled, then these bits will determine the beta configuration setting that is used for their respective channels.

Care should be taken when setting the BETA[2:0] bits when the autodetection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, then the circuit may introduce measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as an AMD processor diode), then the BETA[2:0] bits should be set to '111b'.

**Table 6.15 CPU Beta Values**

| HEX | ENABLE | BETA[2:0] | | | MINIMUM BETA |
|---|---|---|---|---|---|
| | | 2 | 1 | 0 | |
| 0h | 0 | 0 | 0 | 0 | 0.11 |
| 1h | 0 | 0 | 0 | 1 | 0.18 |
| 2h | 0 | 0 | 1 | 0 | 0.25 |
| 3h | 0 | 0 | 1 | 1 | 0.33 |
| 4h | 0 | 1 | 0 | 0 | 0.43 |
| 5h | 0 | 1 | 0 | 1 | 1.00 |
| 6h | 0 | 1 | 1 | 0 | 2.33 |
| 7h | 0 | 1 | 1 | 1 | Disabled |
| 8h - Fh | 1 | X | X | X | Autodetection |

## 6.13 External Diode Ideality Factor Registers

**Table 6.16 Ideality Configuration Registers**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 27h | R/W | External Diode 1 Ideality Factor | - | - | IDEALITY[5:0] | | | | | | 12h |

These registers store the ideality factors that are applied to the external diodes. Table 6.17 defines each setting and the corresponding ideality factor. Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors, therefore it is not recommended that these settings be updated without consulting SMSC.

**Table 6.17 Ideality Factor Look-Up Table (Diode Model)**

| SETTING | FACTOR | SETTING | FACTOR | SETTING | FACTOR |
|---|---|---|---|---|---|
| 08h | 0.9949 | 18h | 1.0159 | 28h | 1.0371 |
| 09h | 0.9962 | 19h | 1.0172 | 29h | 1.0384 |
| 0Ah | 0.9975 | 1Ah | 1.0185 | 2Ah | 1.0397 |
| 0Bh | 0.9988 | 1Bh | 1.0200 | 2Bh | 1.0410 |

**Table 6.17 Ideality Factor Look-Up Table (Diode Model) (continued)**

| SETTING | FACTOR | SETTING | FACTOR | SETTING | FACTOR |
|---|---|---|---|---|---|
| 0Ch | 1.0001 | 1Ch | 1.0212 | 2Ch | 1.0423 |
| 0Dh | 1.0014 | 1Dh | 1.0226 | 2Dh | 1.0436 |
| 0Eh | 1.0027 | 1Eh | 1.0239 | 2Eh | 1.0449 |
| 0Fh | 1.0040 | 1Fh | 1.0253 | 2Fh | 1.0462 |
| 10h | 1.0053 | 20h | 1.0267 | 30h | 1.0475 |
| 11h | 1.0066 | 21h | 1.0280 | 31h | 1.0488 |
| 12h | 1.0080 | 22h | 1.0293 | 32h | 1.0501 |
| 13h | 1.0093 | 23h | 1.0306 | 33h | 1.0514 |
| 14h | 1.0106 | 24h | 1.0319 | 34h | 1.0527 |
| 15h | 1.0119 | 25h | 1.0332 | 35h | 1.0540 |
| 16h | 1.0133 | 26h | 1.0345 | 36h | 1.0553 |
| 17h | 1.0146 | 27h | 1.0358 | 37h | 1.0566 |

For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to Table 6.18 when using a CPU substrate transistor.

**Table 6.18 Substrate Diode Ideality Factor Look-Up Table (BJT Model)**

| SETTING | FACTOR | SETTING | FACTOR | SETTING | FACTOR |
|---|---|---|---|---|---|
| 08h | 0.9869 | 18h | 1.0079 | 28h | 1.0291 |
| 09h | 0.9882 | 19h | 1.0092 | 29h | 1.0304 |
| 0Ah | 0.9895 | 1Ah | 1.0105 | 2Ah | 1.0317 |
| 0Bh | 0.9908 | 1Bh | 1.0120 | 2Bh | 1.0330 |
| 0Ch | 0.9921 | 1Ch | 1.0132 | 2Ch | 1.0343 |
| 0Dh | 0.9934 | 1Dh | 1.0146 | 2Dh | 1.0356 |
| 0Eh | 0.9947 | 1Eh | 1.0159 | 2Eh | 1.0369 |
| 0Fh | 0.9960 | 1Fh | 1.0173 | 2Fh | 1.0382 |
| 10h | 0.9973 | 20h | 1.0187 | 30h | 1.0395 |
| 11h | 0.9986 | 21h | 1.0200 | 31h | 1.0408 |
| 12h | 1.0000 | 22h | 1.0213 | 32h | 1.0421 |
| 13h | 1.0013 | 23h | 1.0226 | 33h | 1.0434 |
| 14h | 1.0026 | 24h | 1.0239 | 34h | 1.0447 |
| 15h | 1.0039 | 25h | 1.0252 | 35h | 1.0460 |
| 16h | 1.0053 | 26h | 1.0265 | 36h | 1.0473 |

**Table 6.18 Substrate Diode Ideality Factor Look-Up Table (BJT Model) (continued)**

| SETTING | FACTOR | SETTING | FACTOR | SETTING | FACTOR |
|---|---|---|---|---|---|
| 17h | 1.0066 | 27h | 1.0278 | 37h | 1.0486 |

**APPLICATION NOTE:** When measuring a 65nm Intel CPUs, the Ideality Setting should be the default 12h. When measuring 45nm Intel CPUs, the Ideality Setting should be 15h.

## 6.14 Filter Control Register

**Table 6.19 Filter Configuration Register**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 40h | R/W | Filter Control | - | - | - | - | - | - | FILTER[1:0] | | 00h |

The Filter Configuration Register controls the digital filter on the External Diode channel.

Bits 1-0 - FILTER[1:0] - Control the level of digital filtering that is applied to the External Diode temperature measurements as shown in Table 6.20. See Figure 5.2and Figure 5.3 for examples on the filter behavior.

**Table 6.20 Filter Settings**

| FILTER[1:0] | | AVERAGING |
|---|---|---|
| 1 | 0 | |
| 0 | 0 | Disabled (default) |
| 0 | 1 | Level 1 |
| 1 | 0 | Level 1 |
| 1 | 1 | Level 2 |

## 6.15 Product ID Register

**Table 6.21 Product ID Register**

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FDh | R | Product ID | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h EMC1402 |

The Product ID Register holds a unique value that identifies the device.

## 6.16 SMSC ID Register (FEh)

**Table 6.22 Manufacturer ID Register**

| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FEh | R | SMSC ID | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5Dh |

The Manufacturer ID register contains an 8 bit word that identifies the SMSC as the manufacturer of the EMC1402.

## 6.17 Revision Register (FFh)

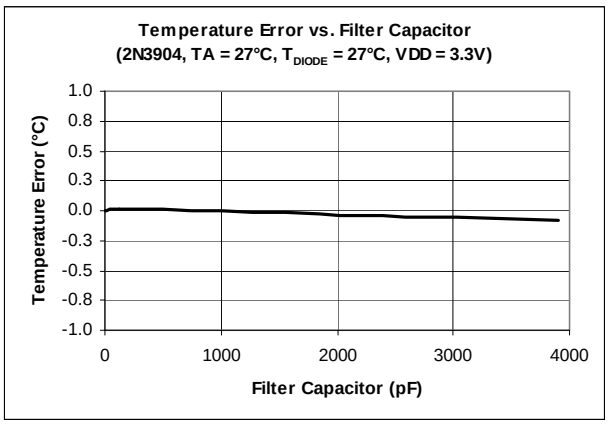
**Table 6.23 Revision Register**

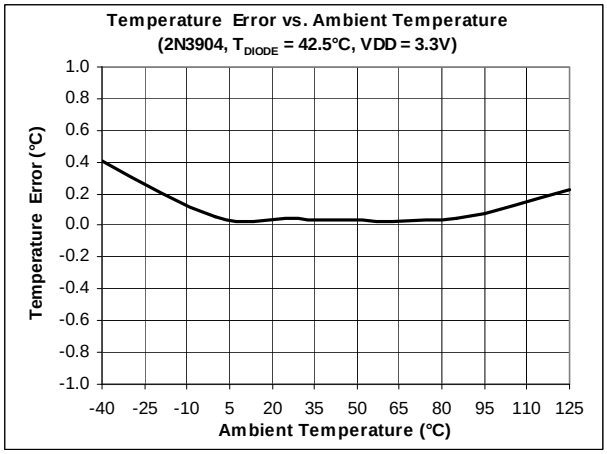
| ADDR. | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FFh | R | Revision | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h |
| FFh | R | Revision | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04h |

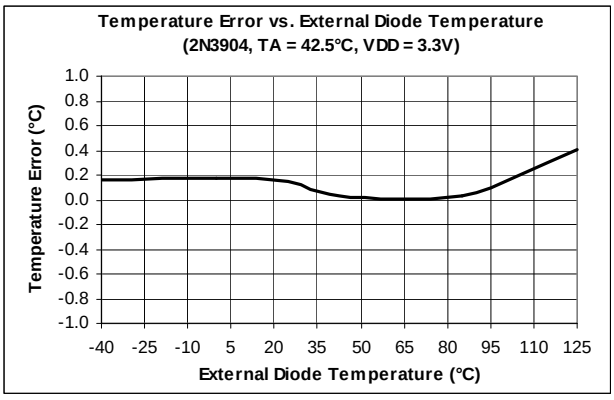
The Revision register contains an 8-bit word that identifies the die revision. It can be 01h or 04h.

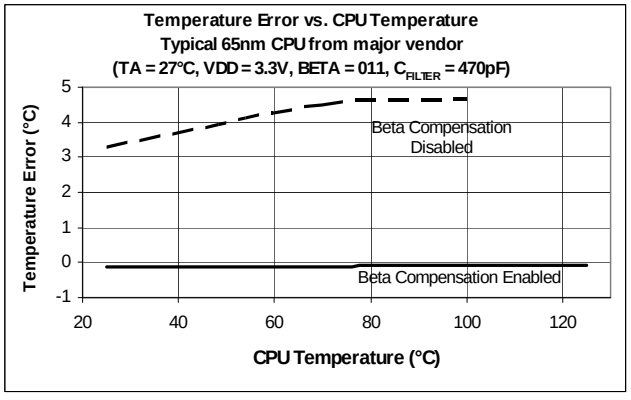
**ENGINEERING NOTE:**

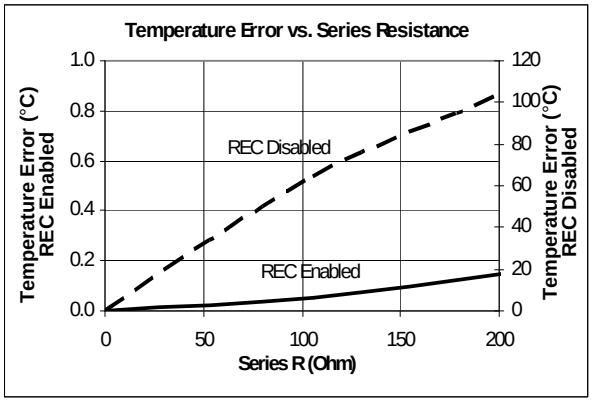
# Chapter 7 Typical Operating Curves

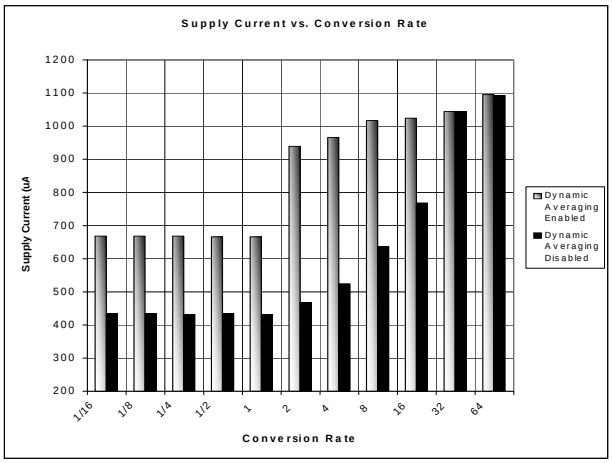




# Chapter 8 Package Information

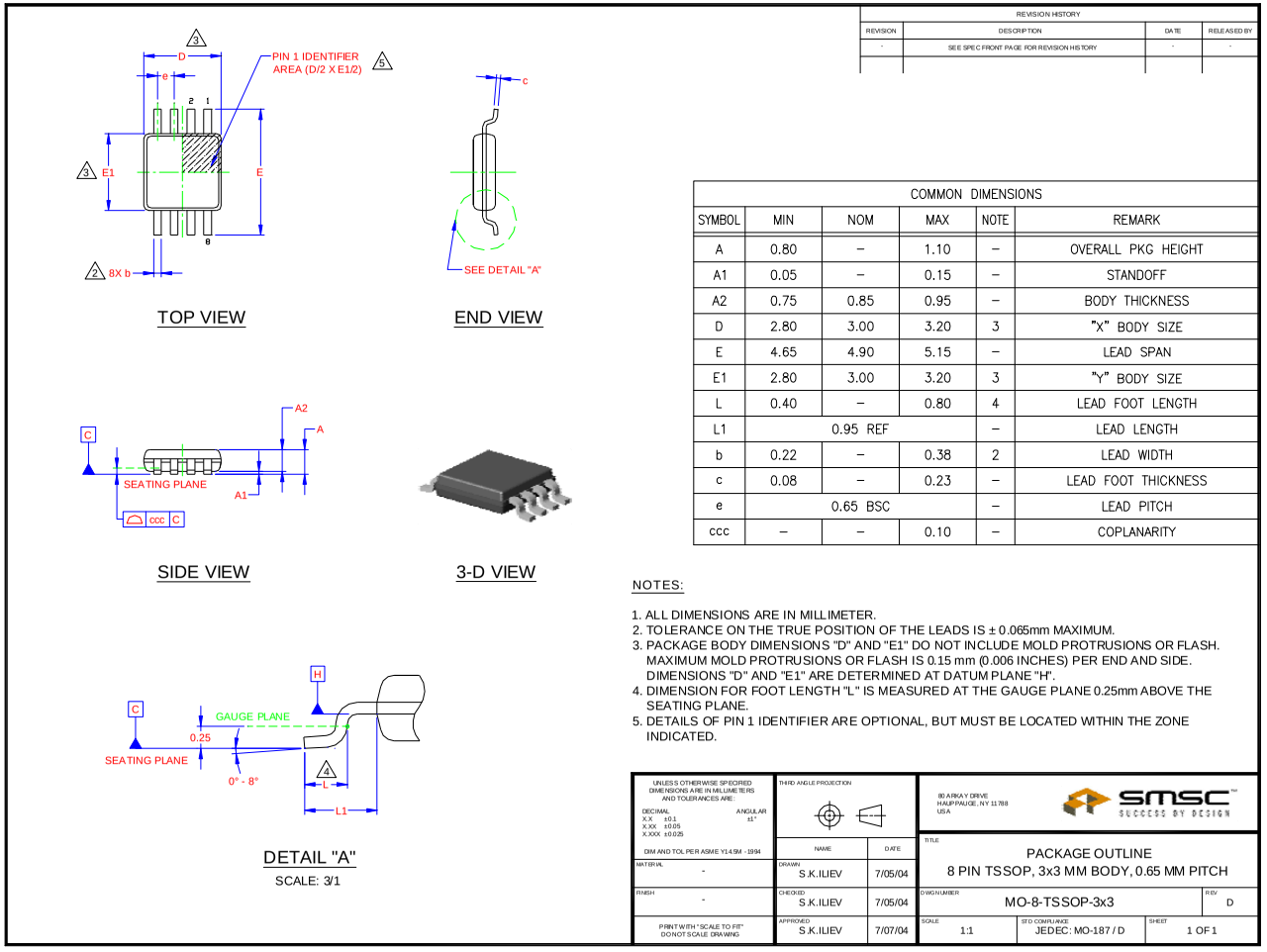



**Figure 8.1 8-Pin MSOP / TSSOP Package**

## 8.1 Package Markings

All devices will be marked on the first line of the top side with “1402”. On the second line, they will be marked with the appropriate -X number (-1, -2, etc), the Functional Revision “B” and Country Code (CC).

# Chapter 9 Datasheet Revision History

**Table 9.1 Customer Revision History**

| REVISION LEVEL & DATE | SECTION/FIGURE/ENTRY | CORRECTION |
|---|---|---|
| Rev. 2.0 (08-10-12) | Table 3.3, "SMBus Electrical Specifications" | Added conditions for $t_{HD:DAT}$. Data hold time minimum of 0.3µs is required when receiving from the master. Data hold time is 0µs min when transmitting to the master. |
| | Section 6.17, "Revision Register (FFh)" | Added row to indicate that revision ID can be 04h. Revision ID may be 04h or 01h. |
| Rev. 1.36 (07-02-09) | Table 2.1, "EMC1402 Pin Description" | In pin description table, added to function column: “requires pull-up resistor” for SMDATA and SMCLK pins |
| | Table 2.1, "EMC1402 Pin Description" | Identified 5V tolerant pins. Added the following application note below table: “For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, THERM, and ALERT), the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.” |
| | Table 3.1, "Absolute Maximum Ratings" | Updated voltage limits for 5V tolerant pins with pull-up resistors.<br><br>Added the following note below table: “For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, THERM, and ALERT), the pull-up voltage must not exceed 3.6V when the device is unpowered.” |
| | Table 3.2, "Electrical Specifications" | Added leakage current. |
| Rev. 1.35 (04-17-09) | Table 2.1, "EMC1402 Pin Description" | “Preliminary” removed from table title |
| Rev. 1.34 (02-27-09) | Table 5.2, "Temperature Data Format" | Extended range for -1 updated from 001 1111 1111 to 001 1111 1000 |