TABLE 1. ELECTRICAL TESTS: DUAL SUPPLIES

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{INH}=2.4V, V_{INL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	3/	1,2,3	All	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V^+=+13.5V, V^-=-13.5V, I_S=-10mA, V_D=±8.5V	1 2,3	All		30 45	Ω
Drain-Source ON Resistance Matching between Channels 4/	Δr_{DS} (ON)	V^+=+15V, V^-=-15V, I_S=-10mA, V_D=±10V	1 2,3	All		3.0 5.0	Ω
On-Resistance Flatness 4/	$r_{FLAT(ON)}$	V^+=+15V, V^-=-15V, I_S=-10mA, V_D=±5V, 0V	1 2,3	All		4.0 6.0	Ω
Source-OFF Leakage Current	$I_{S(OFF)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	All	-0.25 -10	0.25 10	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	All	-0.25 -10	0.25 10	nA
Drain-ON Leakage Current	$I_{D(ON)}$ or $I_{S(ON)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	All	0.4 40	0.4 40	nA
INPUT							
Input Current/Voltage High	I_{INH}	V_{IN}= 2.4V, all others = 0.8V	1,2,3	All	-0.5	0.5	µA
Input Current/Voltage Low	I_{INL}	V_{IN}= 0.8V, all others = 2.4V	1,2,3	All	-0.5	0.5	µA
SUPPLY							
Power-Supply Range					±4.5	±20	V
Positive Supply Current	I+	All channels on or off, V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Negative Supply Current	I-	All channels on or off, V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Logic Supply Current	I_L	All channels on or off, V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Ground Current	I_{GND}	All channels on or off, V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{INH}=2.4V, V_{INL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
DYNAMIC							
Turn-On Time	t_{ON}	VD=±10V, Figure 2	9 10,11	All		175 220	ns
Turn-Off Time	t_{OFF}	VD=±10V, Figure 2	9 10,11	All		145 160	ns
Charge Injection 3/	Q	C_L=1.0nF, V_{GEN}=0V, R_{GEN}=0Ω Figure 4	9	All		10	pC

TABLE 1. ELECTRICAL TESTS: SINGLE SUPPLY

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{INH}=2.4V, V_{INL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	3/	1,2,3	All	0	12	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V^+=+10.8V, I_S=-10mA, V_D=3.8V	1 2,3	All		80 100	Ω
SUPPLY							
Positive Supply Current	I+	All channels on or off, V^+=+13.2, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Negative Supply Current	I-	All channels on or off, V^+=+13.2V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Logic Supply Current	I_L	All channels on or off, V_L=5.25V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Ground Current	I_{GND}	All channels on or off, V_L=5.25V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
DYNAMIC							
Turn-On Time	t_{ON}	V_S=8V, Figure 2	9 10,11	All		250 315	ns
Turn-Off Time	t_{OFF}	V_S=8V, Figure 2	9 10,11	All		125 140	ns
Charge Injection 3/	Q	C_L=1.0nF, V_{GEN}=0V, R_{GEN}=0Ω Figure 8	9	All		10	pC

NOTE 2: This data sheet uses the algebraic convention, where the most negative value is a minimum and the most positive value is a maximum.

NOTE 3: Guaranteed by design.

NOTE 4: $\Delta r_{ON}=\Delta r_{ON}(max)-\Delta r_{ON}(min)$. On-resistance match between channels and flatness are guarantee only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

FIGURE 2: SWITCHING TIME TEST CIRCUIT: See Commercial Data Sheet
FIGURE 3: BREAK-BEFORE-MAKE INTERVAL: See Commercial Data Sheet
FIGURE 4: CHARGE INJECTION: See Commercial Data Sheet

Package		**ORDERING INFORMATION:**	
16 pin CERDIP	DG411AK/883B	DG412AK/883B	DG413AK/883B
16 pin Flatpack	DG411AL/883B	DG412AL/883B	DG413AL/883B
20 pin LCC	DG411AZ/883B	DG412AZ/883B	DG413AZ/883B

TRUTH TABLES:

DG411 LOGIC	DG411 SWITCH	DG412 LOGIC	DG412 SWITCH	DG413 LOGIC	DG413 SWITCHES 1,2	DG413 SWITCHES 3,4
0	ON	0	OFF	0	ON	OFF
1	OFF	1	ON	1	OFF	ON

TERMINAL CONNECTIONS:

	DG411/412/413	DG411/412/413
	J16	LCC20
1	IN1	NC
2	D1	IN1
3	S1	D1
4	V-	S1
5	GND	V-
6	S4	NC
7	D4	GND
8	IN4	S4
9	IN3	D4
10	D3	IN4
11	S3	NC
12	V_L	IN3
13	V+	D3
14	S2	S3
15	D2	V_L
16	IN2	NC
17		V+
18		S2
19		D2
20		IN2

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9,10,11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.