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Pin Configuration

Figure 1. 32-Pin PLCC
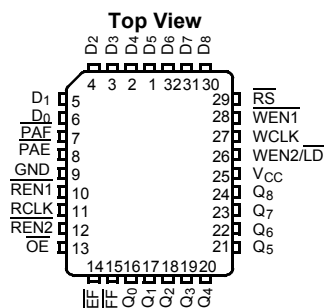
Figure 2. 32-Pin TQFP
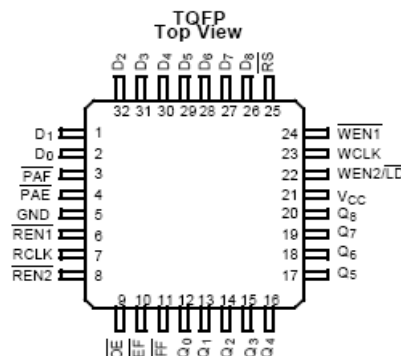
Selection Guide

Description		CY7C42X1V-15	CY7C42X1V-25	CY7C42X1V-35	Unit
Maximum Frequency		66.7	40	28.6	MHz
Maximum Access Time		11	15	20	ns
Minimum Cycle Time		15	25	35	ns
Minimum Data or Enable Set-up		4	6	7	ns
Minimum Data or Enable Hold		1	1	2	ns
Maximum Flag Delay		10	15	20	ns
Active Power Supply Current	Commercial	20	20	20	mA

	CY7C4421V	CY7C4201V	CY7C4211V	CY7C4221V	CY7C4231V	CY7C4241V	CY7C4251V
Density	64 x 9	256 x 9	512 x 9	1K x 9	2K x 9	4K x 9	8K x 9

Pin Definitions

Signal Name	Description	I/O	Description
D_{0-8}	Data Inputs	I	**Data Inputs for 9-bit bus**.
Q_{0-8}	Data Outputs	O	**Data Outputs for 9-bit bus**.
WEN1	Write Enable 1	I	**The only write enable when device is configured to have programmable flags.** Data is written on a LOW-to-HIGH transition of WCLK when WEN1 is asserted and FF is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when WEN1 is LOW and WEN2/LD and FF are HIGH.
WEN2/$\overline{LD}$ Dual Mode Pin	Write Enable 2	I	**If HIGH at reset, this pin operates as a second write enable**. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, WEN2/LD is held LOW to write or read the programmable flag offsets.
	Load	I	
$\overline{REN1}$, $\overline{REN2}$	Read Enable Inputs	I	**Enables the device for Read operation**.
WCLK	Write Clock	I	**The rising edge clocks data into the FIFO when WEN1 is LOW and WEN2/LD is HIGH and the FIFO is not Full**. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.

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Pin Definitions (continued)

Signal Name	Description	I/O	Description
RCLK	Read Clock	I	**The rising edge clocks data out of the FIFO when REN1 and REN2 are LOW and the FIFO is not Empty.** When WEN2/LD is LOW, RCLK reads data out of the programmable flag offset register.
EF	Empty Flag	O	**When EF is LOW, the FIFO is empty. EF is synchronized to RCLK.**
FF	Full Flag	O	**When FF is LOW, the FIFO is full. FF is synchronized to WCLK.**
PAE	Programmable Almost Empty	O	**When PAE is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO.**
PAF	Programmable Almost Full	O	**When PAF is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO.**
RS	Reset	I	**Resets device to empty condition.** A reset is required before an initial read or write operation after power-up.
OE	Output Enable	I	**When OE is LOW, the FIFO's data outputs drive the bus to which they are connected.** If OE is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

Functional Description

The CY7C42X1V provides four status pins: Empty, Full, Almost Empty, Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty-7 and Full-7.

The flags are synchronous, i.e., they change state relative to either the Read Clock (RCLK) or the Write Clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle

All configurations are fabricated using an advanced 0.65μ P-Well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Architecture

The CY7C42X1V consists of an array of 64 to 8K words of nine bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, REN1, REN2, WEN1, WEN2, RS), and flags (EF, PAE, PAF, FF.)

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset (RS) cycle. This causes the FIFO to enter the Empty condition signified by EF being LOW. All data outputs (Q_{0-8}) go LOW t_{RSF} after the rising edge of RS. In order for the FIFO to reset to its default state, a falling edge must occur on RS and the user must not read or write while RS is LOW. All flags are guaranteed to be valid t_{RSF} after RS is taken LOW.

FIFO Operation

When the WEN1 signal is active LOW and WEN2 is active HIGH, data present on the D_{0-8} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the REN1 and REN2 signals are active LOW, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of RCLK while REN1 and REN2 are active. REN1 and REN2 must set up t_{ENS} before RCLK for it to be a valid read function. WEN1 and WEN2 must occur t_{ENS} before WCLK for it to be a valid write function.

An Output Enable (OE) pin is provided to three-state the Q_{0-8} outputs when OE is asserted. When OE is enabled (LOW), data in the output register will be available to the Q_{0-8} outputs after t_{OE}.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Write Enable 1 (WEN1). If the FIFO is configured for programmable flags, Write Enable 1 (WEN1) is the only write enable control pin. In this configuration, when Write Enable 1 (WEN1) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WEN2/LD). This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/LD) is set active HIGH at Reset (RS=LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable (WEN1) is LOW and Write Enable 2/Load (WEN2/LD) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK.) Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

When WEN2/$\overline{\text{LD}}$ is held LOW during Reset, this pin is the load (LD) enable for flag offset programming. In this configuration, WEN2/$\overline{\text{LD}}$ can be used to access the four 8-bit offset registers contained in the CY7C42X1V for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/$\overline{\text{LD}}$ and $\overline{\text{WEN1}}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset Least Significant Bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset Most Significant Bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{\text{LD}}$ and $\overline{\text{WEN1}}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while

WEN2/$\overline{\text{LD}}$ and $\overline{\text{WEN1}}$ are LOW writes data to the empty LSB register again. *Figure 3* shows the register sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/$\overline{\text{LD}}$ input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{\text{LD}}$ is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{\text{LD}}$ is LOW and both $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be performed simultaneously on the offset registers.

Figure 3. Offset Register Location and Default Values
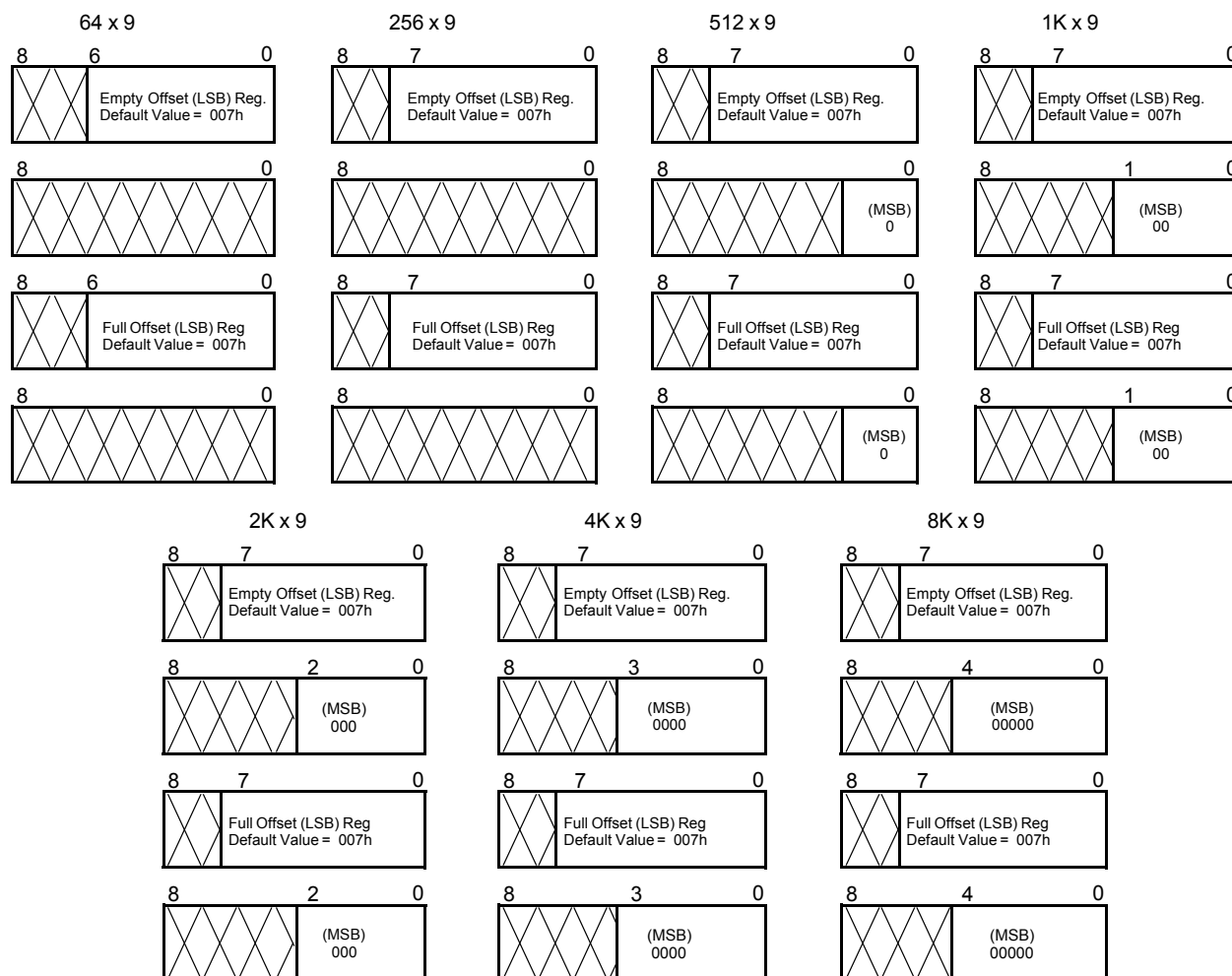
Programmable Flag (PAE, PAF) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable Almost Empty Flag (PAE) and programmable Almost Full Flag (PAF) states are determined by their corresponding offset registers and the difference between the read and write pointers.

Table 1. Writing the Offset Registers

LD	WEN	WCLK[1]	Selection
0	0	⌐	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	⌐	No Operation
1	0	⌐	Write Into FIFO
1	1	⌐	No Operation

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of PAE. PAE is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is

LOW when the FIFO contains n or fewer unread words. PAE is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of PAF. PAE is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4421V (64 – m), CY7C4201V (256 – m), CY7C4211V (512 – m), CY7C4221V (1K – m), CY7C4231V (2K – m), CY7C4241V (4K – m), and CY7C4251V (8K – m). PAF is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Table 2. Status Flags

Number of Words in FIFO			FF	PAF	PAE	EF
CY7C4421V	**CY7C4201V**	**CY7C4211V**				
0	0	0	H	H	L	L
1 to n[2]	1 to n[2]	1 to n[2]	H	H	L	H
(n+1) to 32	(n+1) to 128	(n+1) to 256	H	H	H	H
33 to (64−(m+1))	129 to (256−(m+1))	257 to (512−(m+1))	H	H	H	H
(64−m)[3] to 63	(256−m)[3] to 255	(512−m)[3] to 511	H	L	H	H
64	256	512	L	L	H	H

Number of Words in FIFO				FF	PAF	PAE	EF
CY7C4221V	**CY7C4231V**	**CY7C4241V**	**CY7C4251V**				
0	0	0	0	H	H	L	L
1 to n[2]	1 to n[2]	1 to n[2]	1 to n[2]	H	H	L	H
(n+1) to 512	(n+1) to 1024	(n+1) to 2048	(n+1) to 4096	H	H	H	H
513 to (1024 −(m+1))	1025 to (2048 −(m+1))	2049 to (4096 −(m+1))	4097 to (8192 −(m+1))	H	H	H	H
(1024−m)[3] to 1023	(2048−m)[3] to 2047	(4096−m)[3] to 4095	(8192−m)[3] to 8191	H	L	H	H
1024	2048	4096	8192	L	L	H	H

Notes
1. The same selection sequence applies to reading from the registers. REN1 and REN2 are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
2. n = Empty Offset (n=7 default value).
3. m = Full Offset (m=7 default value).

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. A composite flag should be created for each of the end-point status flags (EF and FF). The partial status flags (PAE and PAF) can be detected from any one device. *Figure* demonstrates a 18-bit word width by using two CY7C42X1Vs. Any word width can be attained by adding additional CY7C42X1Vs.

When the CY7C42X1V is in a Width Expansion Configuration, the Read Enable (REN2) control input can be grounded (see *Figure*). In this configuration, the Write Enable 2/Load (WEN2/LD) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

The CY7C42X1 devices provide four flag pins to indicate the condition of the FIFO contents. Empty, Full, PAE, and PAF are synchronous.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of WEN1 and WEN2/LD. FF is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of REN1 and REN2. EF is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Figure 4. Block Diagram of 64 x 9, 256 x 9, 512 x 9, 1024 x 9, 2048 x 9, 4096 x 9, 8192 x 9 Low-Voltage Synchronous FIFO Memory Used in a Width-Expansion Configuration
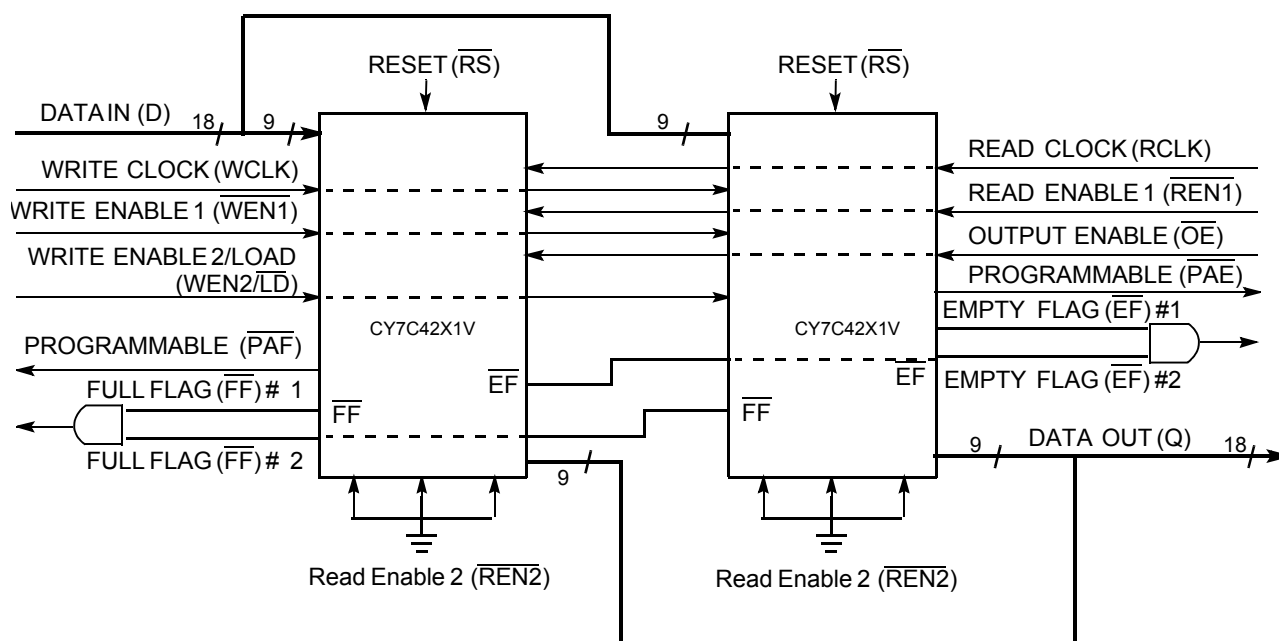
Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied .... –55°C to +125°C

Supply Voltage to Ground Potential................ –0.5V to +5.0V

DC Voltage Applied to Outputs
in High-Z State.. –0.5V to +5.0V

DC Input Voltage .... –0.5V to +5.0V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage... > 2001V
(per MIL-STD-883, Method 3015)

Latch up Current.. > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 300 mV
Industrial	–40° to +85°C	3.3V ± 300 mV

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C42X1V-15 Min	7C42X1V-15 Max	7C42X1V-25 Min	7C42X1V-25 Max	7C42X1V-35 Min	7C42X1V-35 Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	5.0	2.0	5.0	2.0	5.0	V
V_{IL}	Input LOW Voltage		–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.	–10	+10	–10	+10	–10	+10	μA
I_{OZL} I_{OZH}	Output OFF, High Z Current	OE ≥ V_{IH}, V_{SS} < V_O < V_{CC}	–10	+10	–10	+10	–10	+10	μA
I_{CC}[4]	Active Power Supply Current	Com'l		20		20		20	mA
I_{SB}[5]	Average Standby Current	Com'l		6		6		6	mA

Capacitance[6]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Figure 5. AC Test Loads and Waveforms[7, 8]
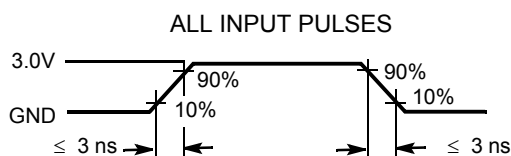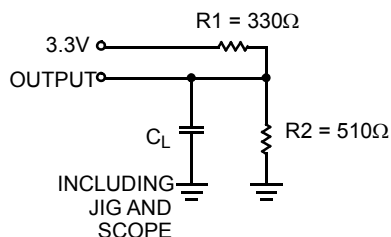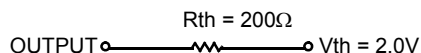
Notes
4. Outputs open. Tested at Frequency = 20 MHz.
5. All inputs = V_{CC} – 0.2V, except WCLK and RCLK, which are switching at 20 MHz.
6. Tested initially and after any design or process changes that may affect these parameters.
7. C_L = 30 pF for all AC parameters except for t_{OHZ}.
8. C_L = 5 pF for t_{OHZ}.

Switching Characteristics Over the Operating Range

Parameter	Description	7C42X1V-15		7C42X1V-25		7C42X1V-35		Unit
		Min	Max	Min	Max	Min	Max	
t_S	Clock Cycle Frequency		66.7		40		28.6	MHz
t_A	Data Access Time	2	11	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	15		25		35		ns
t_{CLKH}	Clock HIGH Time	6		10		14		ns
t_{CLKL}	Clock LOW Time	6		10		14		ns
t_{DS}	Data Set-Up Time	4		6		7		ns
t_{DH}	Data Hold Time	1		2		2		ns
t_{ENS}	Enable Set-Up Time	4		6		7		ns
t_{ENH}	Enable Hold Time	1		2		2		ns
t_{RS}	Reset Pulse Width[9]	15		25		35		ns
t_{RSS}	Reset Set-Up Time	10		15		20		ns
t_{RSR}	Reset Recovery Time	10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		18		25		35	ns
t_{OLZ}	Output Enable to Output in Low Z[10]	0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[10]	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		11		15		20	ns
t_{REF}	Read Clock to Empty Flag		11		15		20	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		16		22		25	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		16		22		25	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	15		18		20		ns

Notes
9. Pulse widths less than minimum values are not allowed.
10. Values guaranteed by design, not currently tested.

[+] Feedback

Switching Waveforms

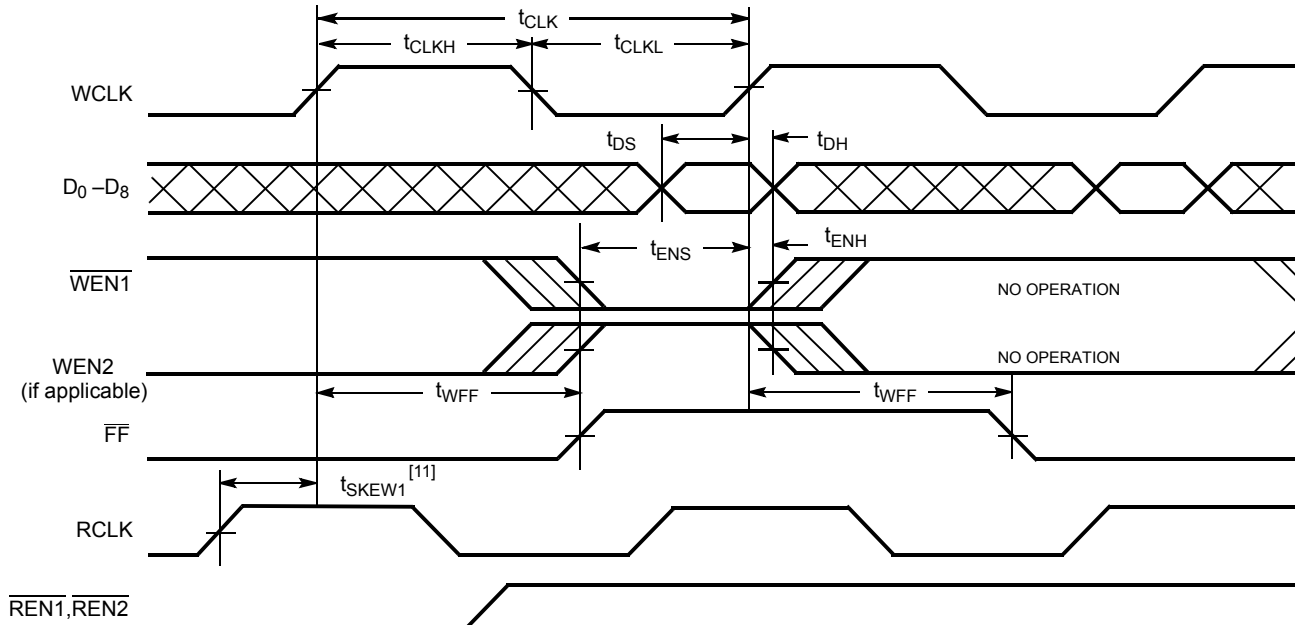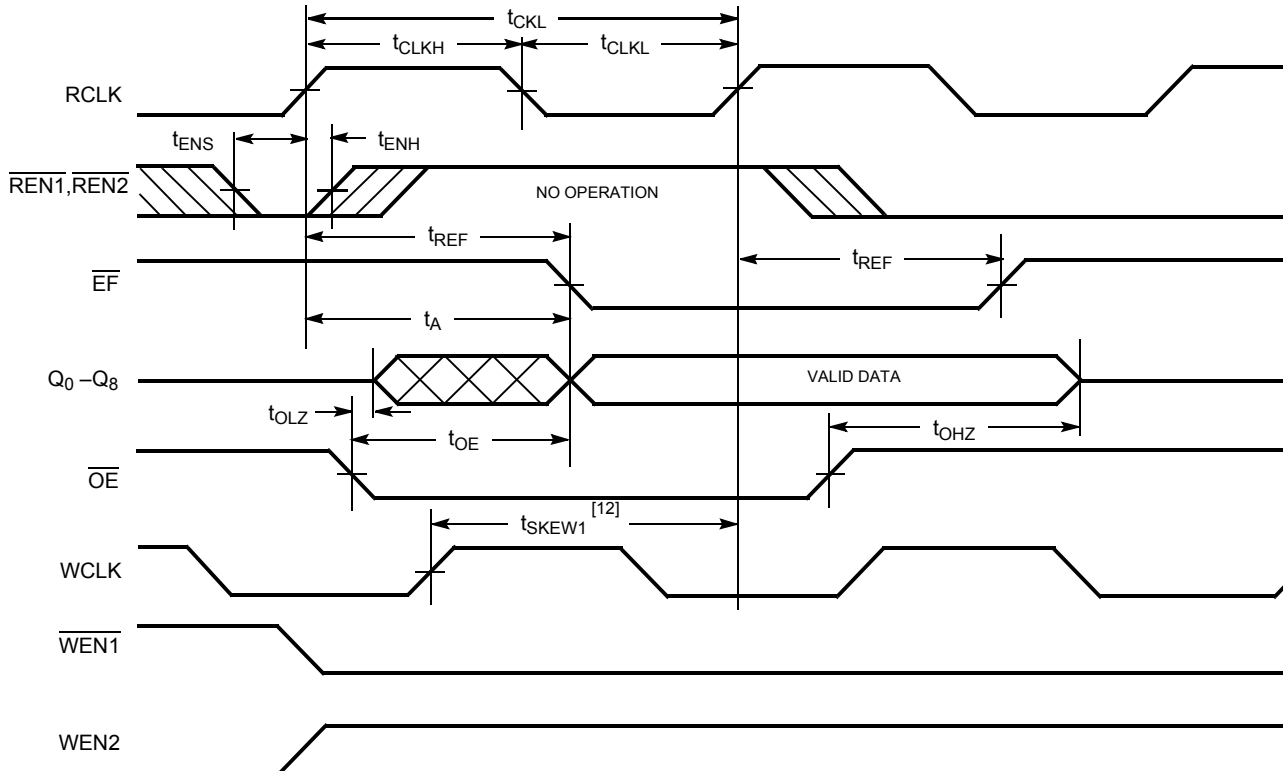**Figure 6. Write Cycle Timing**


Figure 7. Read Cycle Timing

Notes

11. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then FF may not change state until the next WCLK rising edge.

12. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then EF may not change state until the next RCLK rising edge.

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Switching Waveforms (continued)

Figure 8. Reset Timing[13]
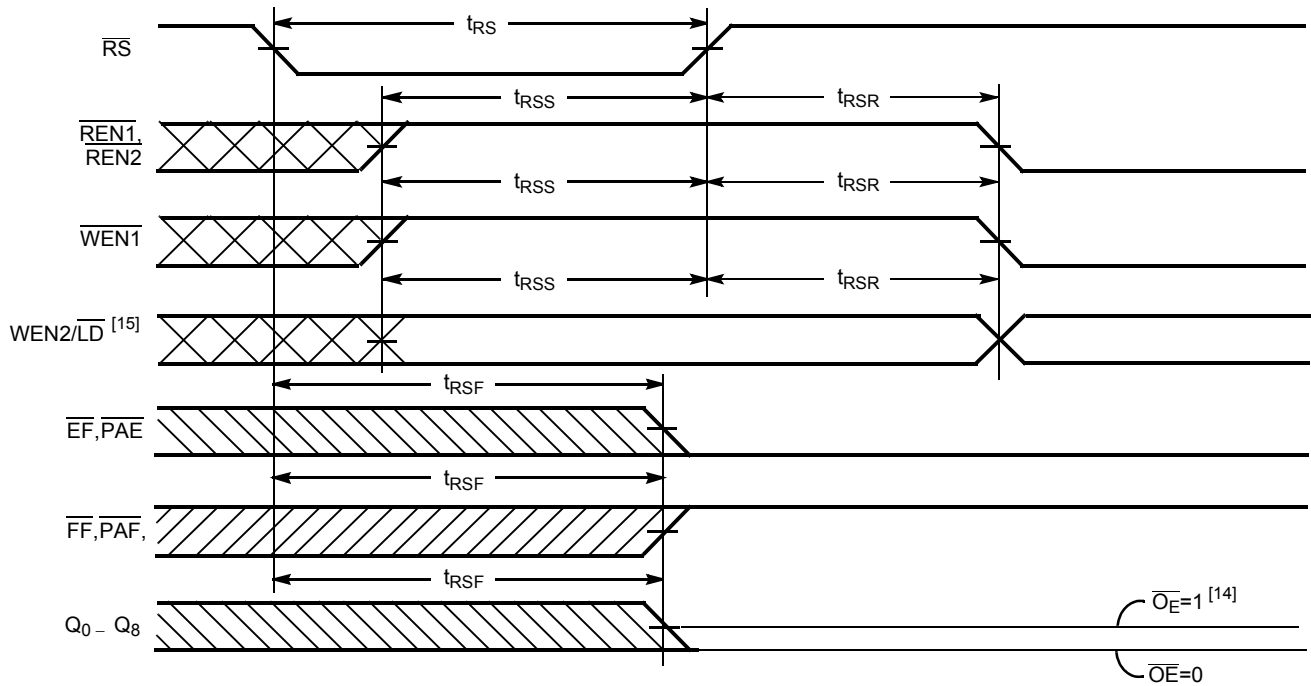
Notes
13. The clocks (RCLK, WCLK) can be free-running during reset.
14. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
15. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

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Switching Waveforms (continued)

Figure 9. First Data Word Latency after Reset with Simultaneous Read and Write
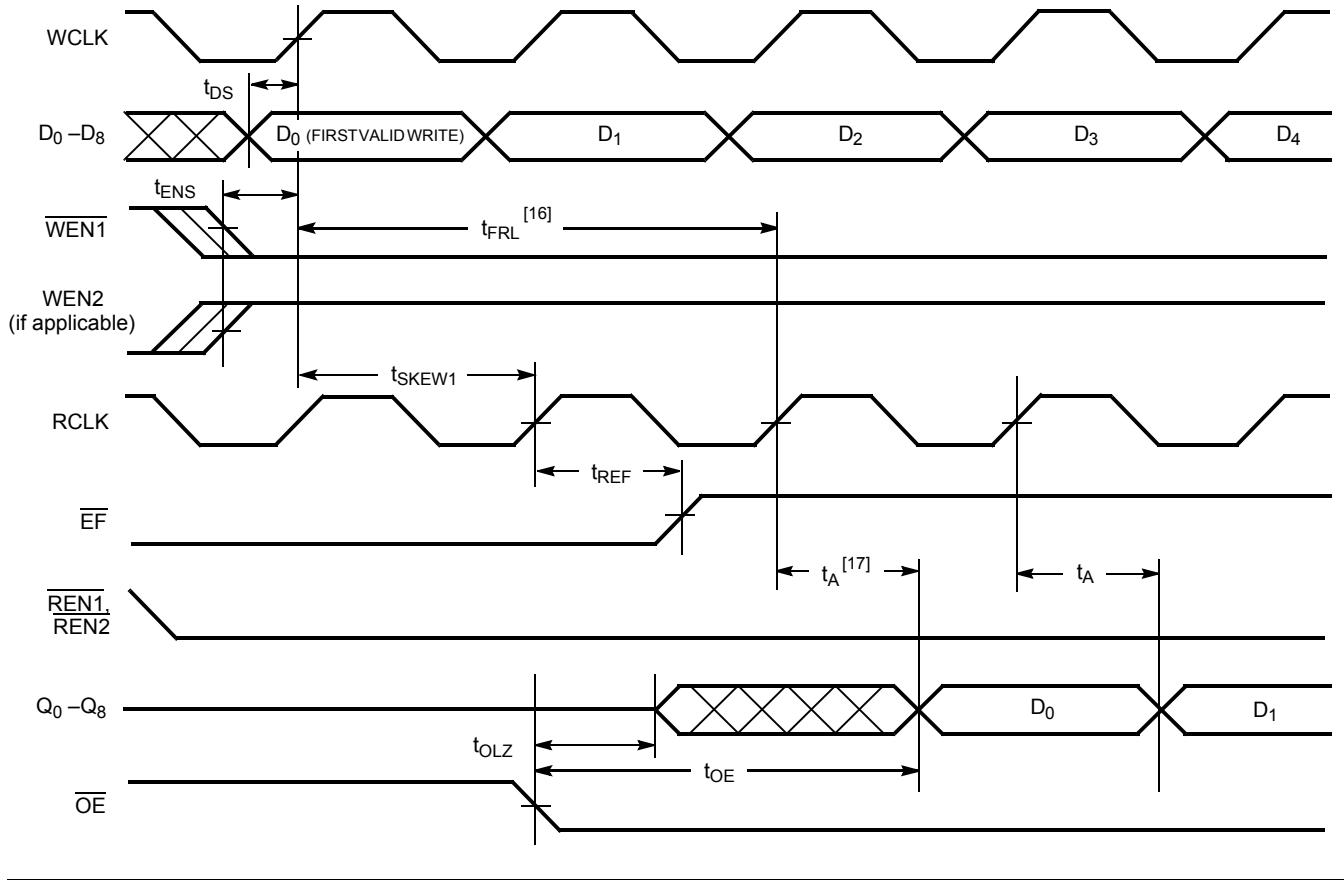
Notes

16. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW1}$. When $t_{SKEW1} <$ minimum specification, t_{FRL} (maximum) = either $2*t_{CLK} + t_{SKEW1}$ or t_{CLK} + t_{SKEW1}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
17. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Switching Waveforms (continued)

Figure 10. Empty Flag Timing
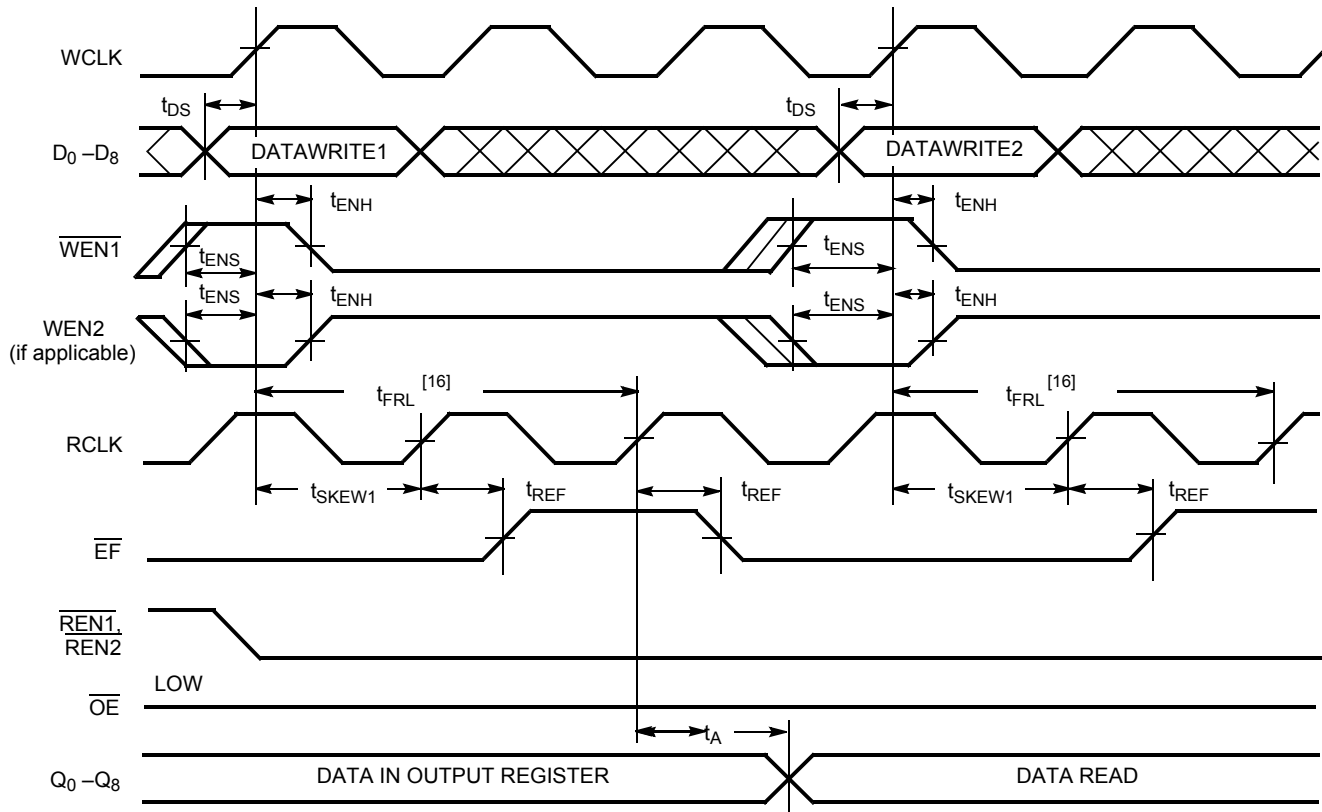
Switching Waveforms (continued)

Figure 11. Full Flag Timing

NO WRITE NO WRITE NO WRITE

WCLK

t_{SKEW1} [11] t_{DS} t_{SKEW1} [11] DATA WRITE

$D_0 - D_8$ DATA WRITE

t_{WFF} t_{WFF} t_{WFF}

$\overline{FF}$

$\overline{WEN1}$

WEN2
(if applicable)

RCLK

$\overline{REN1},$
REN2 t_{ENS} t_{ENH} t_{ENS} t_{ENH}

$\overline{OE}$ LOW

$Q_0 - Q_8$ DATA IN OUTPUT REGISTER t_A DATA READ t_A NEXT DATA READ
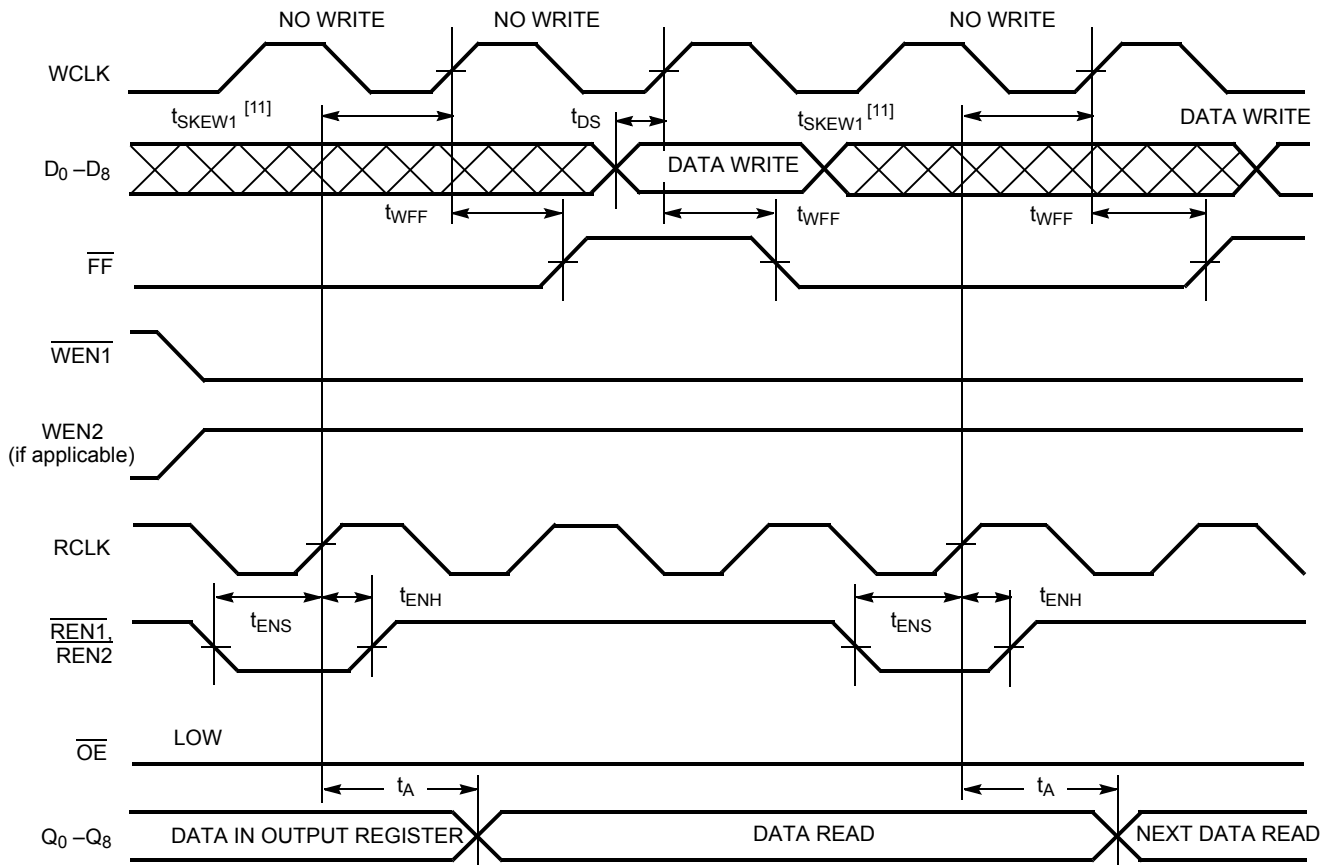
Figure 12. Programmable Almost Empty Flag Timing

t_{CLKH} t_{CLKL}

WCLK

t_{ENS} t_{ENH}

$\overline{WEN1}$

WEN2
(if applicable) t_{ENS} t_{ENH}

$\overline{PAE}$ Note 19 N + 1 WORDS
INFIFO Note 20 t_{PAE}

t_{SKEW2} [18] t_{PAE}

RCLK

t_{ENS} t_{ENS} t_{ENH}

$\overline{REN1},$
REN2
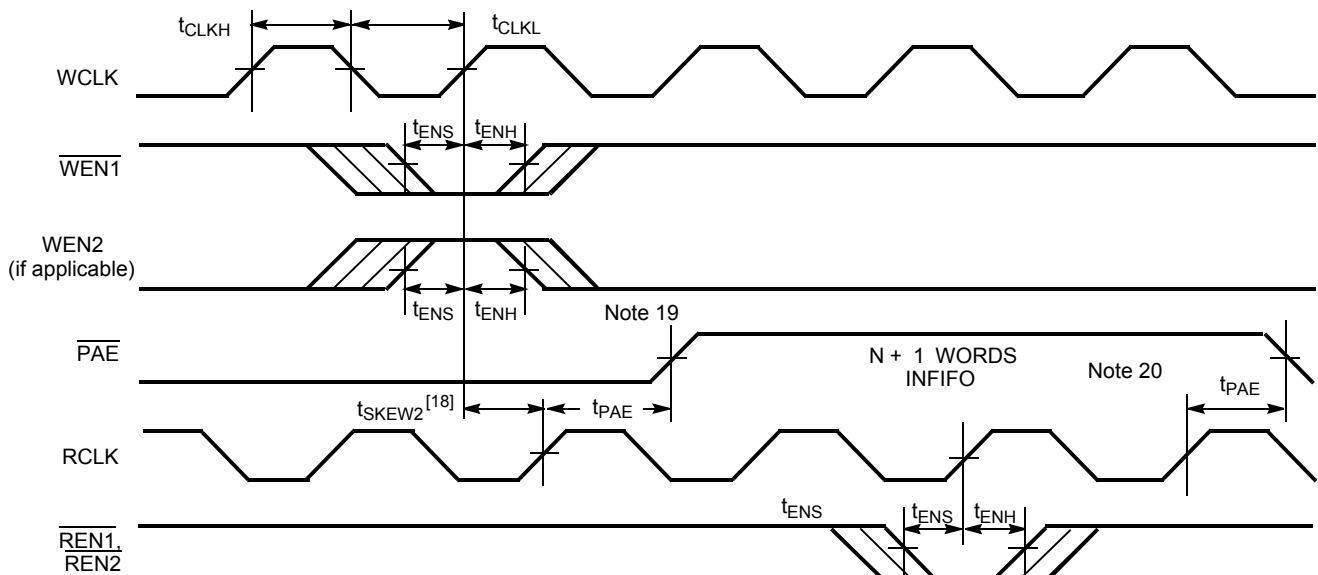
Notes
18. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
19. PAE offset = n.
20. If a read is performed on this rising edge of the read clock, there will be Empty + (n−1) words in the FIFO when $\overline{PAE}$ goes LOW.

Switching Waveforms (continued)

Figure 13. Programmable Almost Full Flag Timing

Note 21
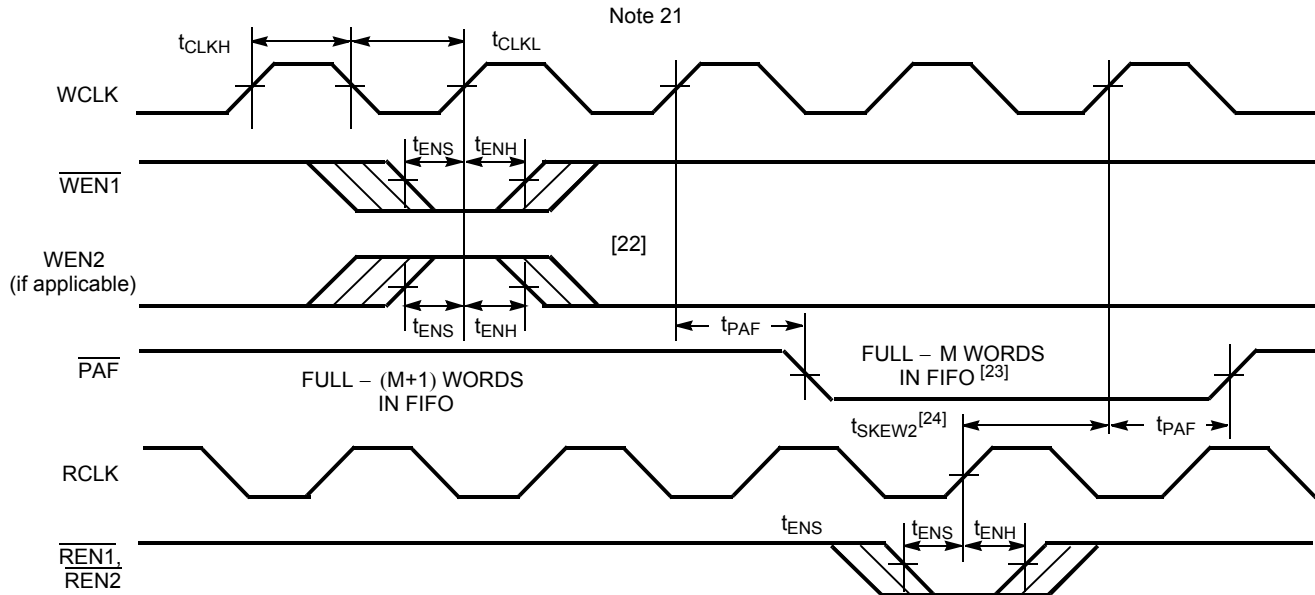
Figure 14. Write Programmable Registers
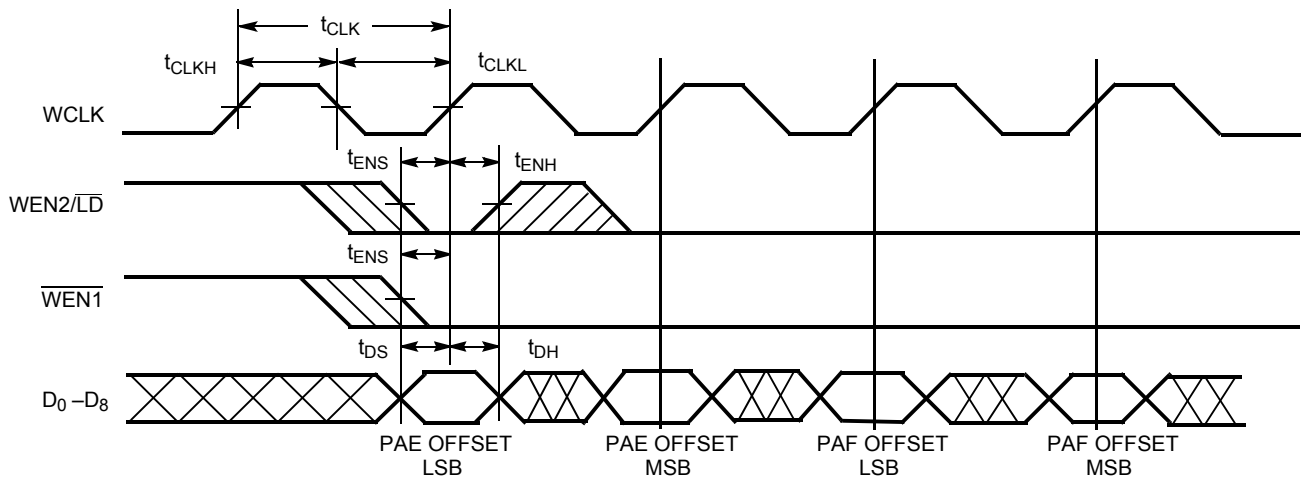
Notes
21. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
22. PAF offset = m.
23. 64–m words for CY7C4421V, 256-m words in FIFO for CY7C4201V, 512–m words for CY7C4211V, 1024–m words for CY7C4221V, 2048–m words for CY7C4231V, 4096–m words for CY7C4241V, 8192–m words for CY7C4251V.
24. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK.

[+] Feedback

Switching Waveforms (continued)

Figure 15. Read Programmable Registers
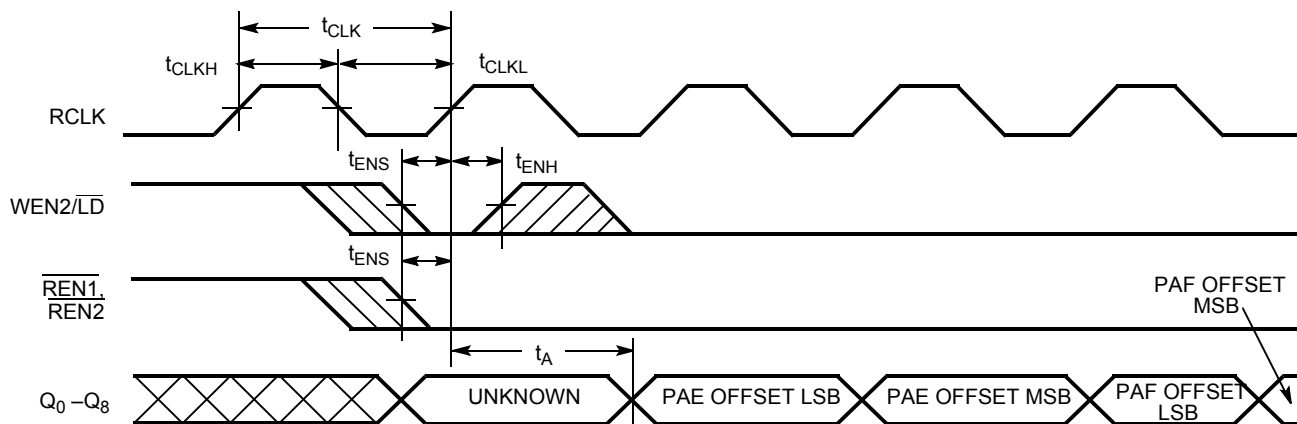
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
256 x 9 Low Voltage Synchronous FIFO				
15	CY7C4201V-15AXC	A32	32-Pin Pb-Free Thin Quad Flatpack	
512 x 9 Low Voltage Synchronous FIFO				
15	CY7C4211V-15AI	A32	32-Pin Thin Quad Flatpack	Industrial
	CY7C4211V-15AXI	A32	32-Pin Pb-Free Thin Quad Flatpack	
1K x 9 Low Voltage Synchronous FIFO				
15	CY7C4221V-15AC	A32	32-Pin Thin Quad Flatpack	Commercial
4K x 9 Low Voltage Synchronous FIFO				
15	CY7C4241V-15AXC	A32	32-Pin Pb-Free Thin Quad Flatpack	Commercial
8K x 9 Low Voltage Synchronous FIFO				
15	CY7C4251V-15AXC	A32	32-Pin Pb-Free Thin Quad Flatpack	Commercial
25	CY7C4251V-25AXC	A32	32-Pin Pb-Free Thin Quad Flatpack	Commercial

Package Diagrams

Figure 16. 32-Pin TQFP (7X7X1.0 mm)

DIMENSIONS ARE IN MILLIMETERS

51-85063 *C

[+] Feedback
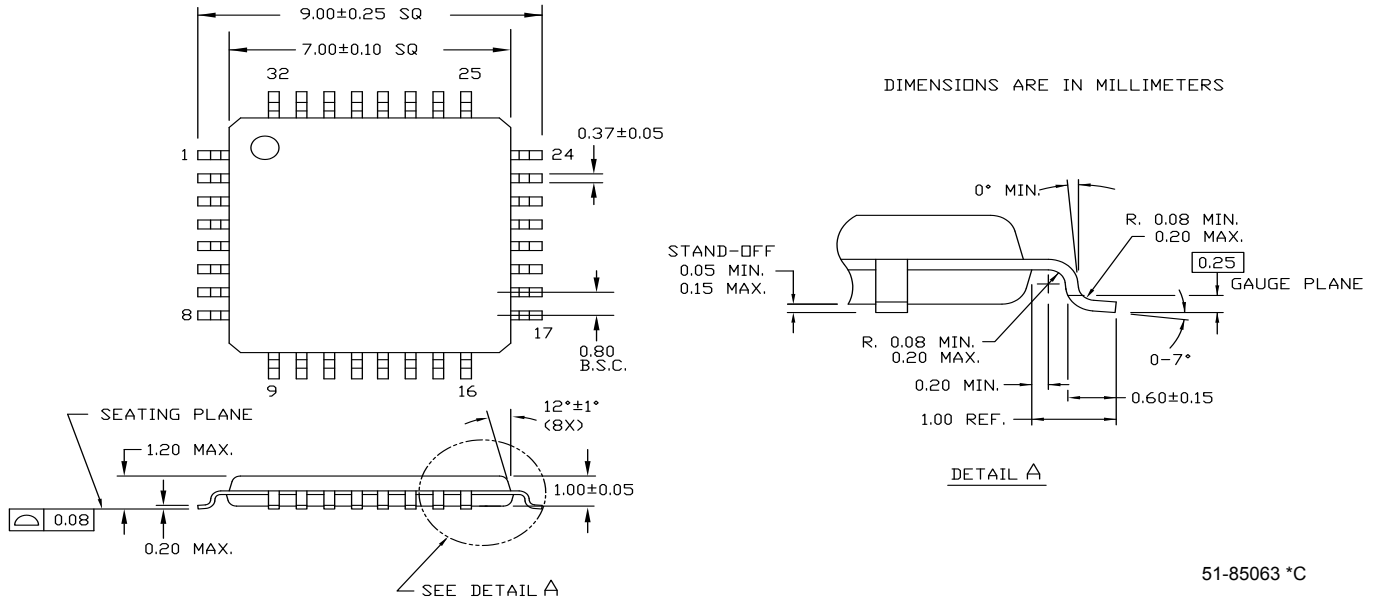
Figure 17. 32-Pin PLCC (.453X.553) in

DIMENSIONS IN INCHES $\frac{\text{MIN.}}{\text{MAX.}}$

51-85002 *C

[+] Feedback
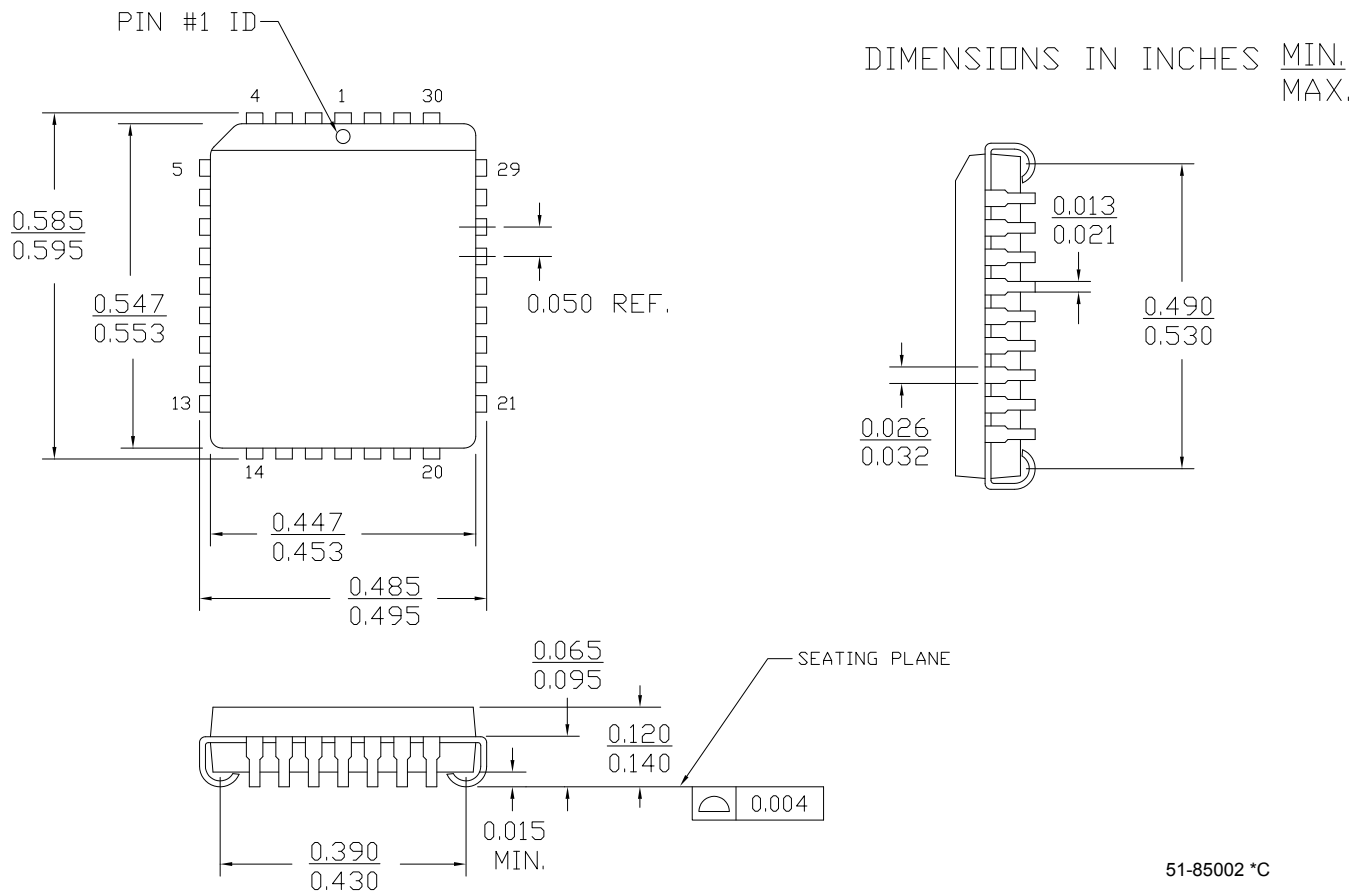
Document History Page

Document Title: CY7C4201V/4211V/4221V/CY7C4241V/4251V Low Voltage 256/512/1K/4K/8K x 9 Synchronous FIFOs **Document Number: 38-06010**				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	106471	09/10/01	SZV	Change from Spec number: 38-00622 to 38-06010
*A	127857	08/25/03	FSG	Fixed empty flag timing diagram Fixed switching waveform diagram typo
*B	384573	See ECN	ESH	Added Pb-Free logo to top of front page Inserted industrial temperature range into operating range Added parts CY7C4251V-25AXC, CY7C4251V-15AXC, CY7C4241V-15AXC, CY7C4241V-15JXC, CY7C4241V-25XC, CY7C4231V-25AXC, CY7C4221V-15AI, CY7C4211V-15AXI, CY7C4201V-15AXC to ordering information.
*C	2896039	03/19/2010	RAME	Added Contents Updated package diagrams Removed inactive parts from Ordering information table Removed references to CY7C4421V and CY7C4231V parts Updated links in Sales, Solutions and Legal Information

Sales, Solutions, and Legal Information

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