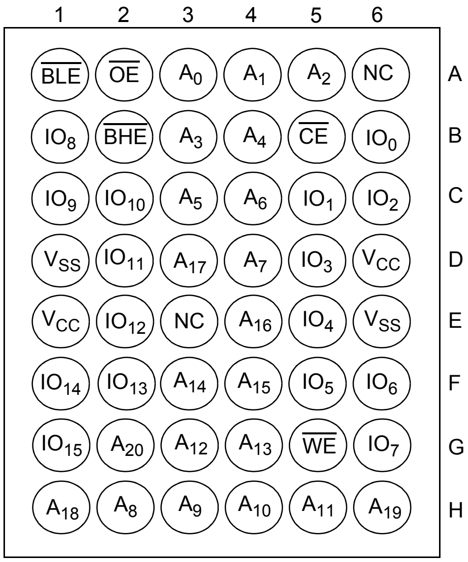
Contents

Selection Guide

Description	-12	Unit
Maximum Access Time	12	ns
Maximum Operating Current	250	mA
Maximum CMOS Standby Current	50	mA

Pin Configuration

Figure 1. 48-ball FBGA [1]



	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	IO_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}$	IO_0
C	IO_9	IO_{10}	A_5	A_6	IO_1	IO_2
D	V_{SS}	IO_{11}	A_{17}	A_7	IO_3	V_{CC}
E	V_{CC}	IO_{12}	NC	A_{16}	IO_4	V_{SS}
F	IO_{14}	IO_{13}	A_{14}	A_{15}	IO_5	IO_6
G	IO_{15}	A_{20}	A_{12}	A_{13}	$\overline{WE}$	IO_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{19}

Note

[1] NC pins are not connected to the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND [2] ....–0.3 V to +4.6 V

DC Voltage Applied to Outputs in High Z State [2]................................. –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [2] .... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... > 2001 V
(MIL-STD-883, Method 3015)

Latch up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-12		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	Min V_{CC}, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW Voltage	Min V_{CC}, I_{OL} = 8.0 mA	–	0.4	V
V_{IH} [2]	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL} [2]	Input LOW Voltage		–0.3	0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_{IN} \leq V_{CC}$	–1	+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_{OUT} \leq V_{CC}$, Output Disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, f = f_{max} = 1/t_{RC}, I_{OUT} = 0 mA CMOS levels	–	250	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{max}	–	60	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3 V, $V_{IN} \geq V_{CC}$ – 0.3 V, or $V_{IN} \leq$ 0.3 V, f = 0, V_{CC} = $V_{CC(max)}$	–	50	mA

Capacitance

Parameter[3]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	16	pF
C_{OUT}	I/O Capacitance		20	pF

Thermal Resistance

Parameter[3]	Description	Test Conditions	48-ball FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	24.72	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		5.79	°C/W

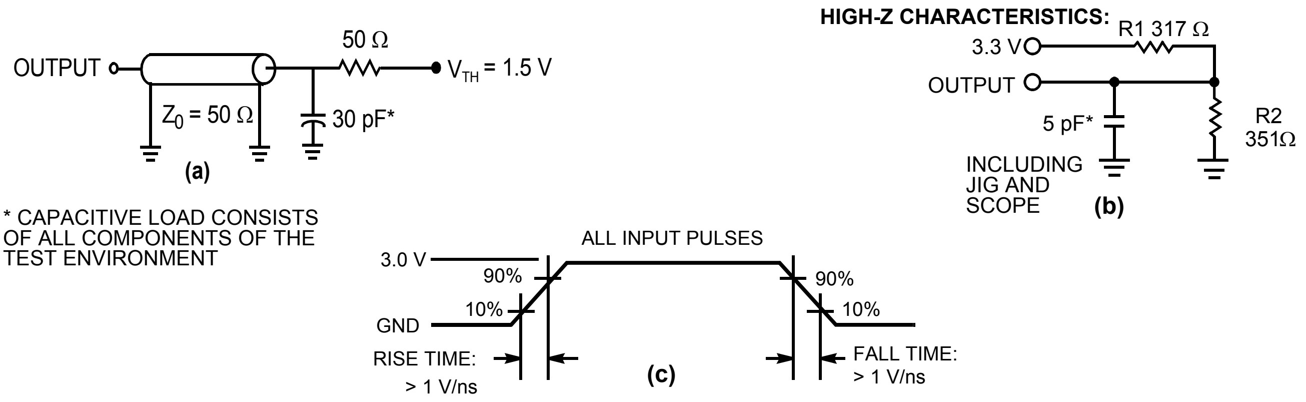
Notes

[2] $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 1 V for pulse durations of less than 20 ns.

[3] Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



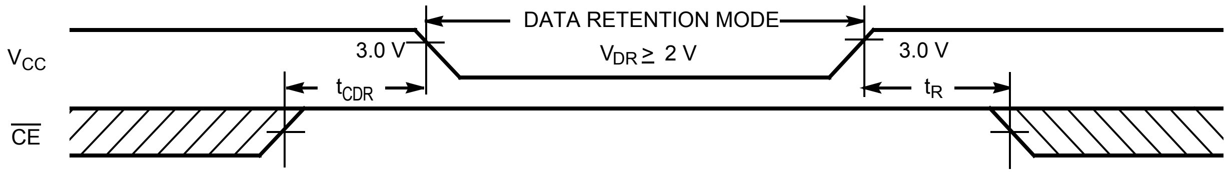
* CAPACITIVE LOAD CONSISTS OF ALL COMPONENTS OF THE TEST ENVIRONMENT

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention		2	–	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = 2$ V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	50	mA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0	–	–	ns
t_R[6]	Operation Recovery Time		t_{RC}	–	–	ns

Figure 3. Data Retention Waveform



Notes

4. Valid SRAM operation does not occur until the power supplies reach the minimum operating V_{DD} (3.0 V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins to include reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.

AC Switching Characteristics

Over the Operating Range [7]

Parameter	Description	-12		Unit
		Min	Max	
Read Cycle				
t_{power}	$V_{CC(typ)}$ to the first access [8]	100	–	µs
t_{RC}	Read Cycle Time	12	–	ns
t_{AA}	Address to Data Valid	–	12	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid	–	12	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid	–	7	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z [9]	1	–	ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z [9]	–	7	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z [9]	3	–	ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z [9]	–	7	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power Up [10]	0	–	ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power Down [10]	–	12	ns
t_{DBE}	Byte Enable to Data Valid	–	7	ns
t_{LZBE}	Byte Enable to Low Z [9]	1	–	ns
t_{HZBE}	Byte Disable to High Z [9]	–	7	ns
Write Cycle [11, 12]				
t_{WC}	Write Cycle Time	12	–	ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	9	–	ns
t_{AW}	Address Setup to Write End	9	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	9	–	ns
t_{SD}	Data Setup to Write End	7	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z [9]	3	–	ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z [9]	–	7	ns
t_{BW}	Byte Enable to End of Write	9	–	ns

Notes

[7] Test conditions are based on signal transition time of 3 ns or less and timing reference levels of 1.5 V and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part (a) of Figure 2 on page 5, unless specified otherwise.

[8] t_{power} is the minimum amount of time that the power supply must be at typical V_{CC} values until the first memory access can be performed.

[9] t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE} and t_{LZOE}, t_{LZCE}, t_{LZWE}, t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 2 on page 5. Transition is measured at ±200 mV from steady-state voltage.

[10] These parameters are guaranteed by design and are not tested.

[11] The internal memory write time is defined by the overlap of $\overline{\text{CE}}$, $\overline{\text{WE}} = V_{IL}$. Chip enables must be active and $\overline{\text{WE}}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing must be referenced to the leading edge of the signal that terminates the write.

[12] The minimum write cycle time for Write Cycle 2 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [13, 14]

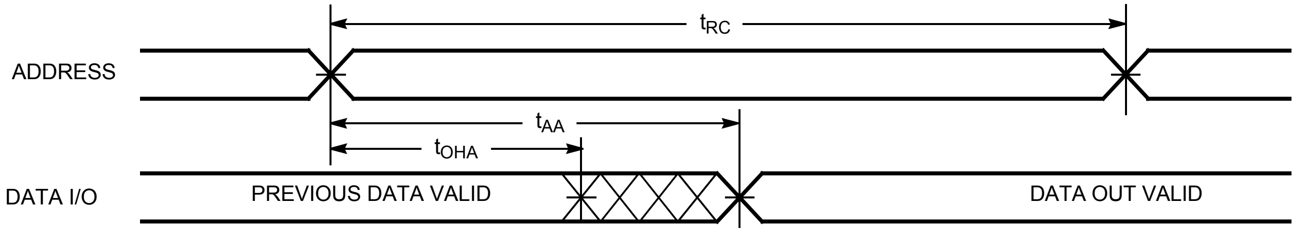
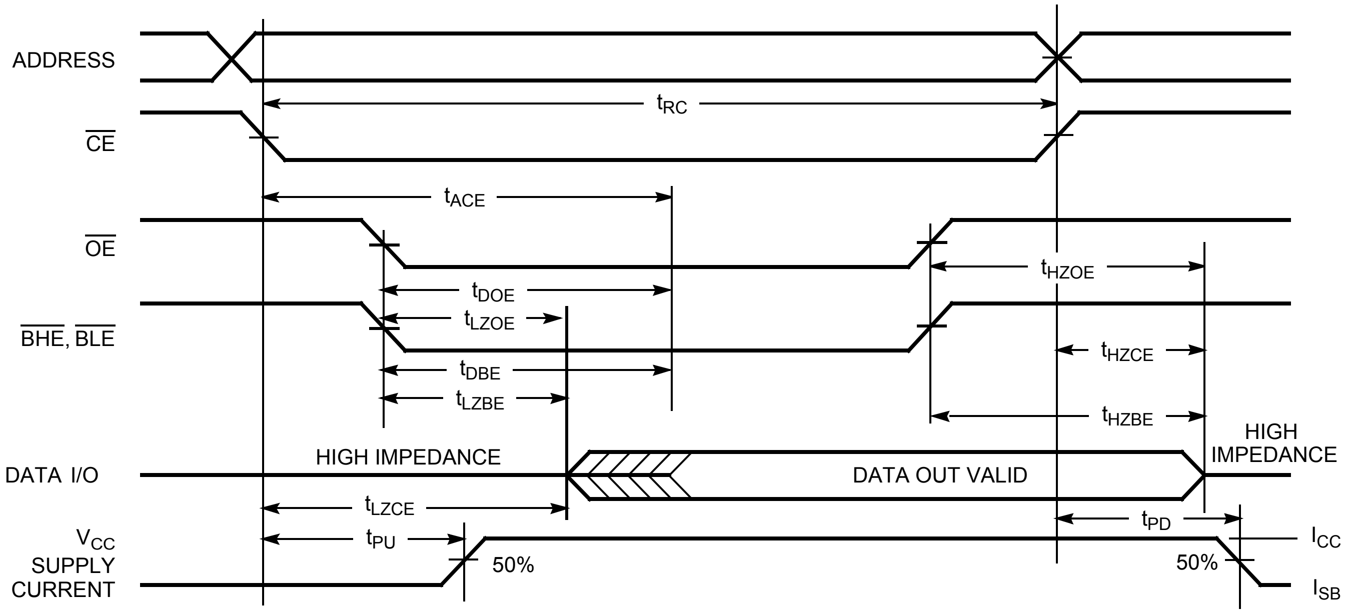


Figure 5. Read Cycle 2 ($\overline{OE}$ Controlled) [14, 15]



Notes

13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ or $\overline{BHE}$ or both = V_{IL}.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

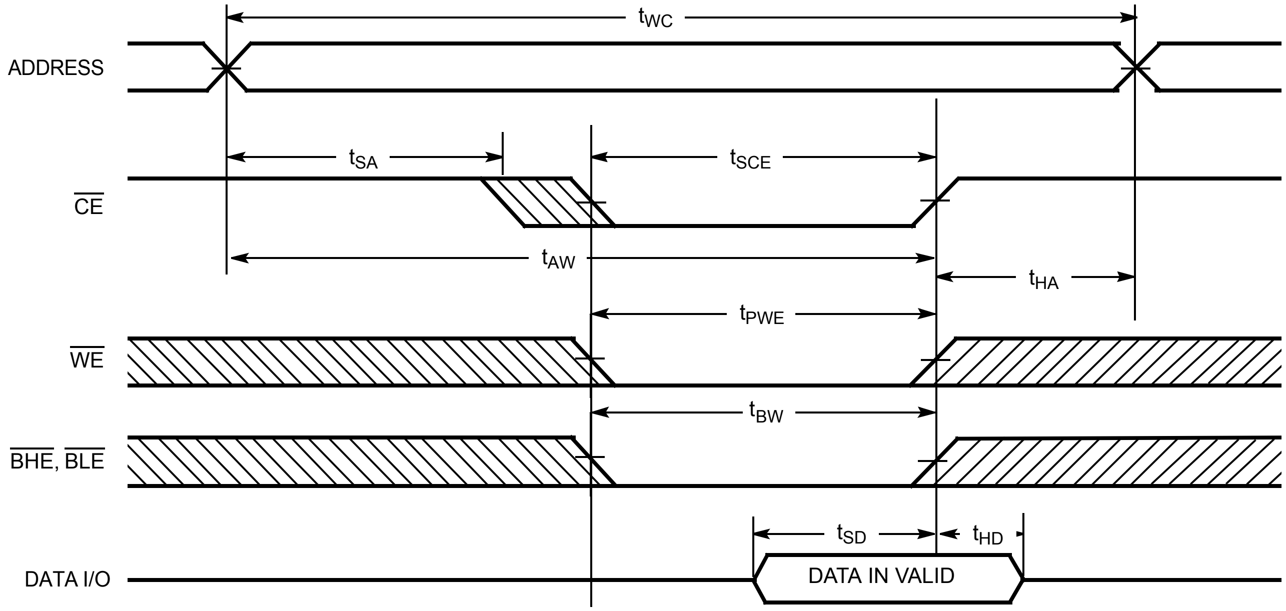


Figure 6. Write Cycle 1 ($\overline{CE}$ Controlled) [16, 17]

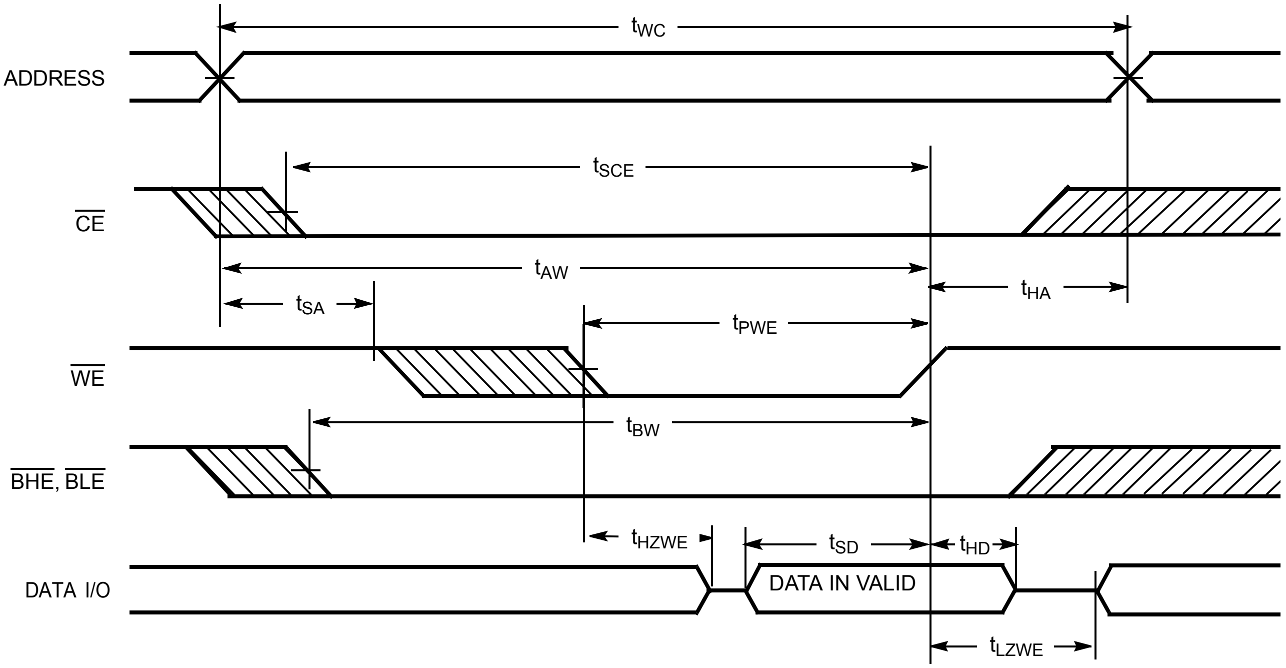


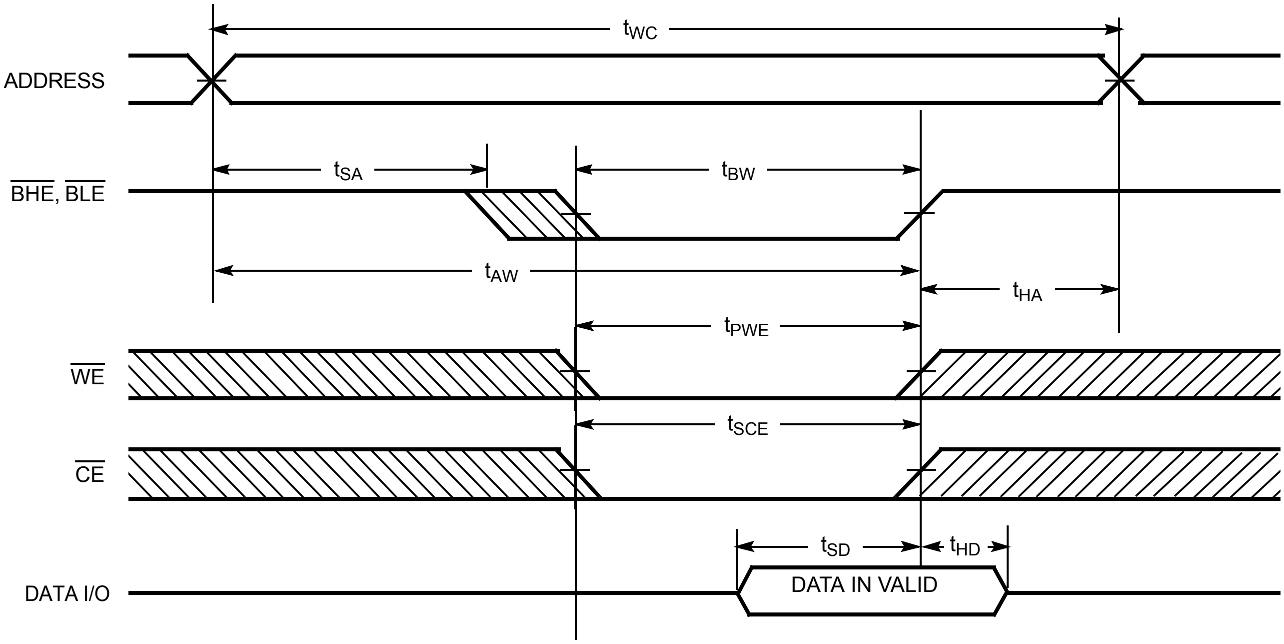
Figure 7. Write Cycle 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [16, 17]

Notes

16. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$, $\overline{BLE}$ or both = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms *(continued)*

Figure 8. Write Cycle 3 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–IO_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1071DV33-12BAXI	51-85191	48-ball FBGA (8 × 9.5 × 1.2 mm) (Pb-free)	Industrial

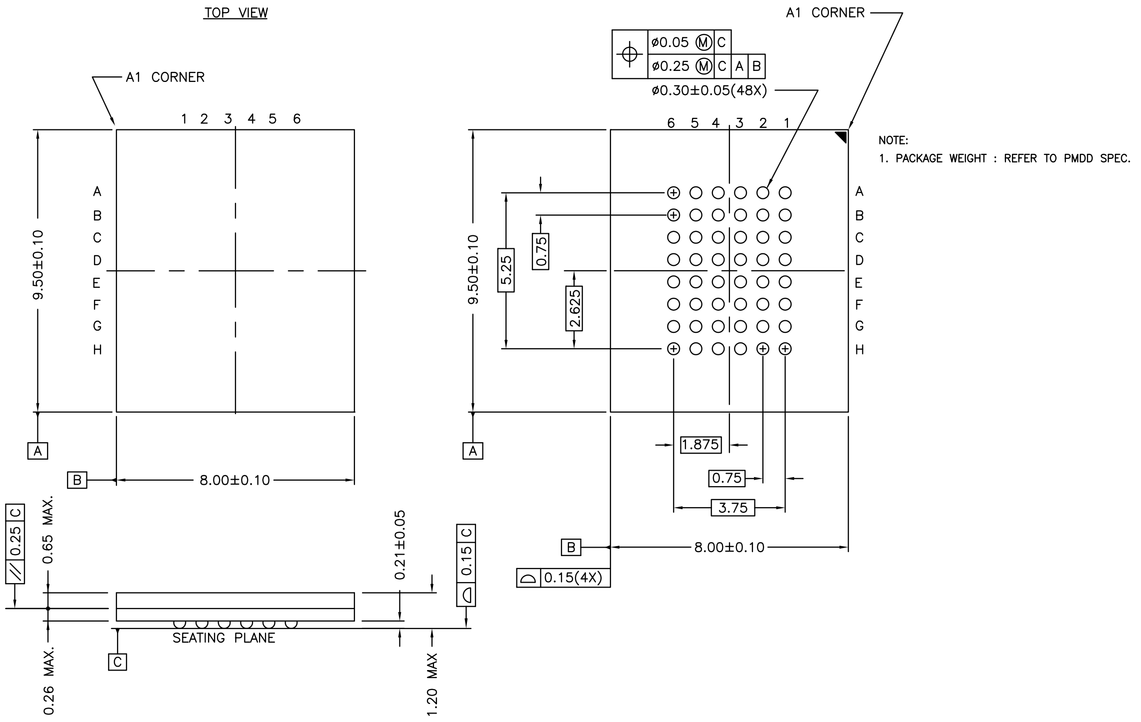
Ordering Code Definitions

CY 7 C 1 07 1 D V33 - 12 BA X I

Temperature Range:
I = Industrial
Pb-free
Package Type:
BA = 48-ball FBGA
Speed: 12 ns
V33 = Voltage range (3 V to 3.6 V)
D = C9, 90 nm Technology
1 = Data width × 16-bits
07 = 32-Mbit density
1 = Fast Asynchronous SRAM family
Technology Code: C = CMOS
7 = SRAM
CY = Cypress

Package Diagram

Figure 9. 48-ball FBGA (8 × 9.5 × 1.2 mm) BA48J Package Outline, 51-85191



NOTE:
1. PACKAGE WEIGHT : REFER TO PMDD SPEC.

51-85191 *C

Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
FPBGA	fine-pitch ball grid array
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
Document Title: CY7C1071DV33, 32-Mbit (2 M × 16) Static RAM **Document Number: 001-12063**				
**	605460	See ECN	VKN	New Data sheet
*A	1192183	See ECN	VKN / KKVTMP	Removed CE_2 feature Updated block diagram Changed I_{CC} spec from 160 mA to 225 mA Changed C_{IN} spec from 8 pF to 10 pF Changed C_{OUT} spec from 10 pF to 12 pF Changed t_{BW} spec from 8 ns to 9 ns
*B	2711136	05/29/2009	VKN / PYRS	Added 10 ns speed bin In 12 ns speed bin, changed I_{SB1} from 70 to 60 mA and I_{SB2} from 60 to 50 mA Changed C_{IN} from 8 pF to 16 pF and C_{OUT} from 10 pF to 20 pF Changed Θ_{JA} from 28.37 °C/W to 24.72 °C/W Removed 119-Ball PBGA package Added 48-Ball FBGA package
*C	2759408	09/03/2009	VKN / AESA	Removed 10ns speed Marked thermal specs as “TBD” Changed t_{DOE}, t_{HZOE}, t_{HZCE}, t_{DBE}, t_{HZBE}, t_{HZWE} specs from 6 ns to 7ns Added -12B2XI part (Dual CE option)
*D	2813370	11/23/2009	VKN	Changed I_{CC} spec from 225 mA to 250 mA.
*E	2925803	04/30/2010	VKN / AESA	Converted from Preliminary to Final Removed Dual CE option from the data sheet Updated links in Sales, Solutions, and Legal Information
*F	3109063	12/13/2010	AJU	Added Ordering Code Definitions.
*G	3132969	01/11/2011	AJU	Added Acronyms and Units of Measure. Changed all instances of IO to I/O. Updated in new template.
*H	3268861	05/28/2011	AJU	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”).
*I	3411360	10/17/2011	TAVA	Updated Features. Updated DC Electrical Characteristics. Updated Switching Waveforms. Updated Package Diagram.
*J	4573215	11/18/2014	TAVA	Added related documentation hyperlink in page 1. Updated Figure 9 in Package Diagram (spec 51-85191 *B to *C).

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2007-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

All products and company names mentioned in this document may be the trademarks of their respective holders.

Downloaded from Arrow.com.