

CY62138FV30 MoBL[®]

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Pin Configuration

Figure 1. 36-ball VFBGA (Top View) [1]

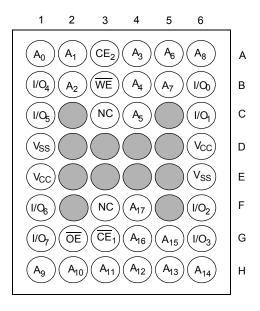


Figure 3. 32-pin TSOP I (Top View)

Figure 2. 32-pin SOIC/TSOP II (Top View)

Figure 4. 32-pin STSOP (Top View)

$\begin{array}{c c} A_{11} & & & \\ A_{12} & & & \\ A_{13} & & & \\ \hline \\ WE & & & \\ WE & & $	STSOP Top View (not to scale)	$\begin{array}{c c} 24 & \overline{OE} \\ 23 & \overline{A_{10}} \\ 22 & \overline{OE}_1 \\ 21 & UO_7 \\ 20 & UO_6 \\ 19 & UO_6 \\ 19 & UO_4 \\ 17 & UO_3 \\ 16 & \overline{OO_1} \\ 15 & UO_1 \\ 14 & UO_1 \\ 13 & UO_0 \\ 12 & \overline{A_0} \\ 11 & \overline{A_1} \\ 10 & \overline{A_2} \\ 9 & \overline{A_3} \end{array}$
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Product Portfolio

							F	ower Di	ssipatio	n		
Product Range		V _{CC} Range (V)		Speed	Operating I _{CC} (mA)			N)	Standby I _{SB2}			
FIGULE	Kange			Kange		(ns)	f = 1	MHz	f = 1	: max	(μ	A)
		Min	Typ ^[2]	Мах		Typ ^[2]	Max	Тур [2]	Мах	Тур [2]	Max	
CY62138FV30LL	Industrial / Automotive-A	2.2	3.0	3.6	45	1.6	2.5	13	18	1	5	

Notes

1. NC pins are not connected on the die.

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.

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Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	–65 °C to +150 °C
Ambient temperature with power applied	–55 °C to +125 °C
Supply voltage to ground potential	–0.3 V to 3.9 V
DC voltage applied to outputs in High Z State ^[3, 4]	–0.3 V to 3.9 V

DC input voltage ^[3, 4]	–0.3 V to 3.9 V
Output current into outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC} ^[5]
CY62138FV30LL	Industrial / Automotive-A		2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Deveneter	Description	Test Conditions	45 ns (Ind	Unit		
Parameter	Description	Test Conditions	Min	Тур ^[6]	Max	Unit
V _{OH}	Output HIGH voltage	I _{OH} = -0.1 mA	2.0	-	-	V
		I _{OH} = −1.0 mA, V _{CC} ≥ 2.70 V	2.4	-	-	V
V _{OL}	Output LOW voltage	I _{OL} = 0.1 mA	-	-	0.4	V
		I _{OL} = 2.1 mA, V _{CC} ≥ 2.70 V		-	0.4	V
V _{IH}	Input HIGH voltage	V _{CC} = 2.2 V to 2.7 V	1.8	-	V _{CC} + 0.3 V	V
		V _{CC} = 2.7 V to 3.6 V	2.2	-	V _{CC} + 0.3 V	V
V _{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V For BGA package	-0.3	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-0.3	-	0.8	V
		V _{CC} = 2.2 V to 3.6 V For other packages	s –0.3	-	0.6	V
I _{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	-	+1	μA
I _{OZ}	Output leakage current	$GND \leq V_O \leq V_{CC}$, output disabled	-1	-	+1	μA
I _{CC}	V _{CC} Operating supply current	$f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CCmax}$	-	13	18	mA
		f = 1 MHz I _{OUT} = 0 mA, CMOS levels	-	1.6	2.5	
I _{SB1} ^[7]	Automatic CE Power-down current–CMOS inputs	$\label{eq:cellson} \begin{split} \overline{CE}_1 &\geq V_{CC} - 0.2 \text{ V or } CE_2 \leq 0.2 \text{ V}, \\ V_{IN} &\geq V_{CC} - 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V}, \\ f &= f_{max} \text{ (address and data only),} \\ f &= 0 \text{ (OE, and WE), } V_{CC} = 3.60 \text{ V} \end{split}$	-	1	5	μΑ
I _{SB2} ^[7]	Automatic CE Power-down current–CMOS inputs	$\label{eq:cell} \begin{split} \overline{CE}_1 &\geq V_{CC} - 0.2 \text{ V or } CE_2 \leq 0.2 \text{ V}, \\ V_{IN} &\geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V}, \\ f &= 0, \ V_{CC} = 3.60 \text{ V} \end{split}$	-	1	5	μΑ

Notes

- Notes
 3. V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
 4. V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 5. Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
 6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
 7. Chip enables (CE₁ and CE₂) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

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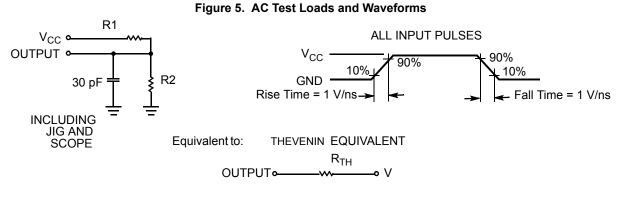
Capacitance

Parameter ^[8]	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = V_{CC(typ.)}$	10	pF
C _{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter ^[8]	Description	Test Conditions	32-pin SOIC	36-ball VFBGA	32-pin TSOP II	32-pin STSOP	32-pin TSOP I	Unit
Θ_{JA}		Still air, soldered on a 3 × 4.5 inch, two layer printed circuit	44.53	38.49	44.16	59.72	50.19	°C/W
ΘJC	Thermal resistance (Junction to Case)	board	24.05	17.66	11.97	15.38	14.59	°C/W

AC Test Loads and Waveforms



Parameter	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

8. Tested initially and after any design or process changes that may affect these parameters.

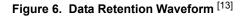


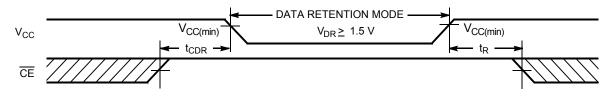
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ ^[9]	Max	Unit
V _{DR}	V _{CC} for data retention			1.5	-	-	V
I _{CCDR} ^[10]	Data retention current	$\begin{split} V_{CC} &= 1.5 \text{ V}, \overline{CE}_1 \geq V_{CC} - 0.2 \text{ V} \\ \text{or } CE_2 \leq 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V} \\ \text{or } V_{IN} \leq 0.2 \text{ V} \end{split}$	Industrial / Automotive-A	-	1	4	μΑ
t _{CDR} ^[11]	Chip deselect to data retention time			0	-	-	ns
t _R ^[12]	Operation recovery time			45	_	_	ns

Data Retention Waveform





Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25$ °C. 10. Chip enables (\overline{CE}_1 and CE_2) must be at CMOS level to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating. 11. Tested initially and after any design or process changes that may affect these parameters. 12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \ge 100 \, \mu$ s or stable at $V_{CC(min)} \ge 100 \, \mu$ s. 13. CE is the logical combination of \overline{CE}_1 and \overline{CE}_2 . When \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or \overline{CE}_2 is HIGH.



Switching Characteristics

Over the Operating Range

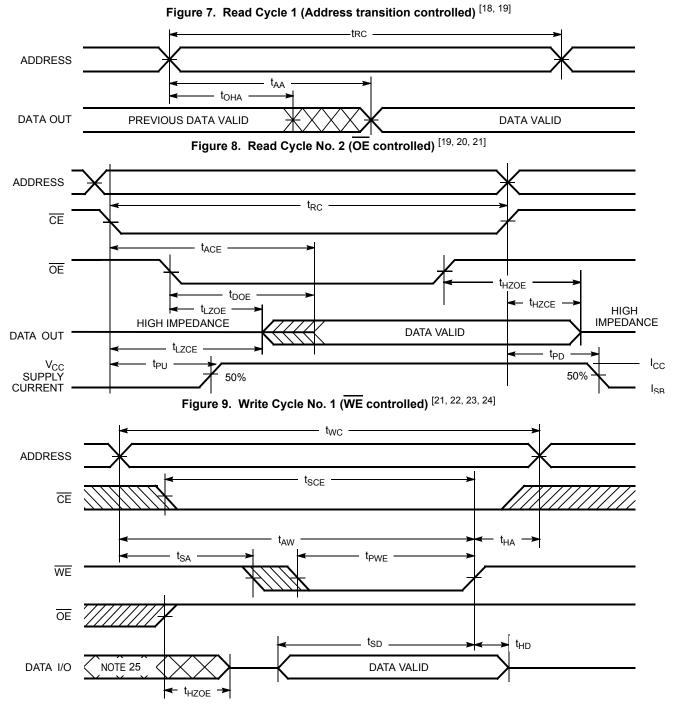
Parameter ^[14]	Description	45 ns (Industrial/ Automotive-A)		Unit
		Min	Мах	
Read Cycle				
t _{RC}	Read cycle time	45	-	ns
t _{AA}	Address to data valid	-	45	ns
t _{OHA}	Data hold from address change	10	-	ns
t _{ACE}	CE ₁ LOW and CE ₂ HIGH to data valid	-	45	ns
t _{DOE}	OE LOW to data valid	-	22	ns
t _{LZOE}	OE LOW to Low Z ^[15]	5	-	ns
t _{HZOE}	OE HIGH to High Z ^[15, 16]	-	18	ns
t _{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[15]	10	_	ns
t _{HZCE}	\overline{CE}_1 HIGH or CE_2 LOW to High Z ^[15, 16]	-	18	ns
t _{PU}	\overline{CE}_1 LOW and CE_2 HIGH to Power-up	0	-	ns
t _{PD}	\overline{CE}_1 HIGH or CE_2 LOW to Power-down	-	45	ns
Write Cycle [17]			
t _{WC}	Write cycle time	45	-	ns
t _{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	35	_	ns
t _{AW}	Address setup to write end	35	_	ns
t _{HA}	Address hold from write end	0	_	ns
t _{SA}	Address setup to Write Start	0	_	ns
t _{PWE}	WE pulse Width	35	_	ns
t _{SD}	Data setup to write end	25	_	ns
t _{HD}	Data hold from write end 0 –		_	ns
t _{HZWE}	WE LOW to High Z ^[15, 16]	-	18	ns
t _{LZWE}	WE HIGH to Low Z ^[15]	10	_	ns

Notes

- Notes
 14. Test conditions for all parameters other than tristate parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} as shown in the AC Test Loads and Waveforms on page 5.
 15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZCE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
 16. t_{HZCE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enters a high impedance state.
 17. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.



Switching Waveforms



Notes

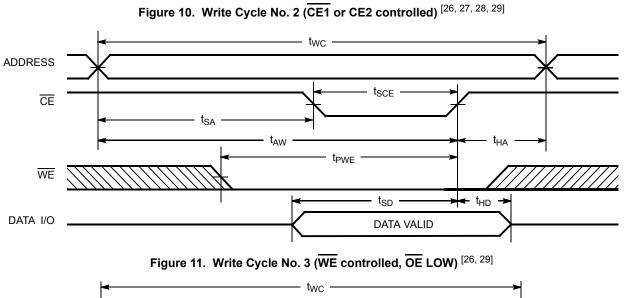
18. <u>The</u> device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.

- 20. Address valid before or similar to \overline{CE}_1 transition LOW and CE_2 transition HIGH.
- 21. CE is the logical combination of CE₁ transition ECe₂ when CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH. 22. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, and CE₂ = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write. 23. Data I/O is high impedance if $\overrightarrow{OE} = V_{IH}$. 24. If \overrightarrow{CE}_1 goes HIGH or CE₂ goes LOW simultaneously with \overrightarrow{WE} HIGH, the output remains in high impedance state.
- 25. During this period, the I/Os are in output state. Do not apply input signals.

^{19.} WE is HIGH for read cycle.



Switching Waveforms (continued)



ADDRESS t_{SCE} CE t_{AW} t_{HA} t_{PWE} WE t_{SD} t_{HD} NOTE 30 DATA VALID DATA I/O t_{HZWE} t_{LZWE} -

Truth Table

CE ₁	CE ₂	WE	OE	Inputs/Outputs	Mode	Power
Н	X ^[31]	Х	Х	High Z	Deselect/Power-down	Standby (I _{SB})
X ^[31]	L	Х	Х	High Z	Deselect/Power-down	Standby (I _{SB})
L	Н	Н	L	Data out	Read	Active (I _{CC})
L	Н	Н	Н	High Z	Output disabled	Active (I _{CC})
L	Н	L	Х	Data in	Write	Active (I _{CC})

Notes

26. CE is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and \underline{CE}_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH. 27. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write. 28. Data I/O is high impedance if $\overline{OE} = V_{IH}$. 29. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains iin high impedance state.

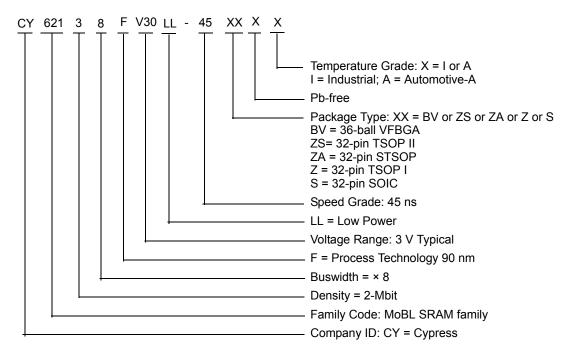
30. During this period, the *I*/Os are in output state. Do not apply input signals. 31. The 'X' (Don't care) state for the Chip enables (\overline{CE}_1 and \overline{CE}_2) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138FV30LL-45BVXI	51-85149	36-ball VFBGA (Pb-free)	Industrial
	CY62138FV30LL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
	CY62138FV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	
	CY62138FV30LL-45ZXI	51-85056	32-pin TSOP I (Pb-free)	
	CY62138FV30LL-45SXI	51-85081	32-pin SOIC (Pb-free)	
	CY62138FV30LL-45ZAXA	51-85094	32-pin STSOP (Pb-free)	Automotive-A

Ordering Code Definitions





Package Diagrams

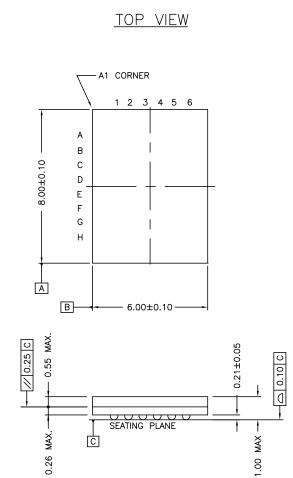
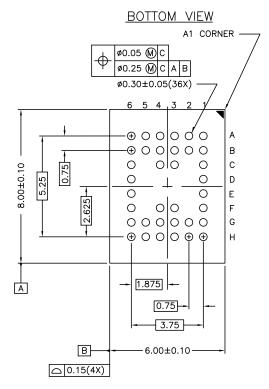


Figure 12. 36-ball VFBGA (6 × 8 × 1.0 mm) BV36A, 51-85149



51-85149 *D





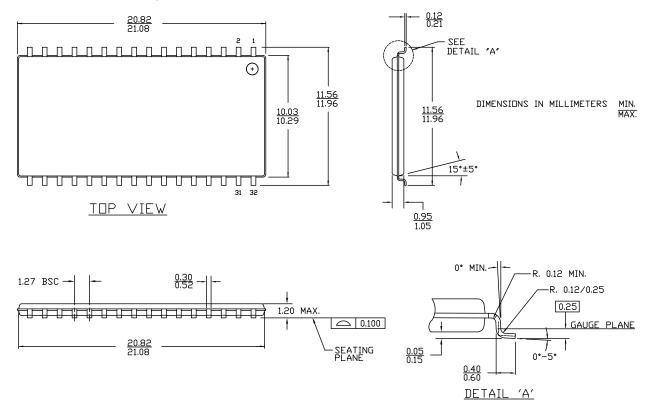


Figure 13. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32, 51-85095

51-85095 *B





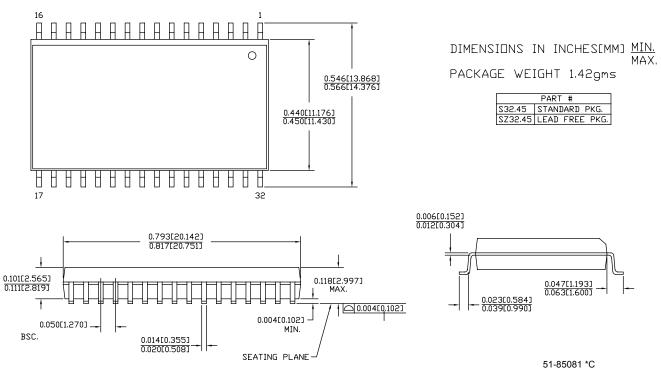


Figure 14. 32-pin Molded SOIC (450 Mil) S32.45/SZ32.45, 51-85081





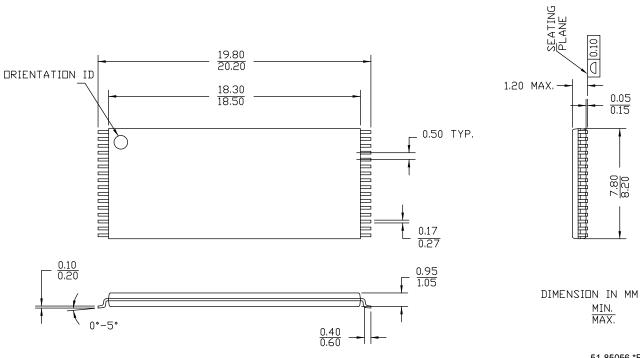


Figure 15. 32-pin TSOP I (8 × 20 ×1.0 mm) Z32, 51-85056

51-85056 *F





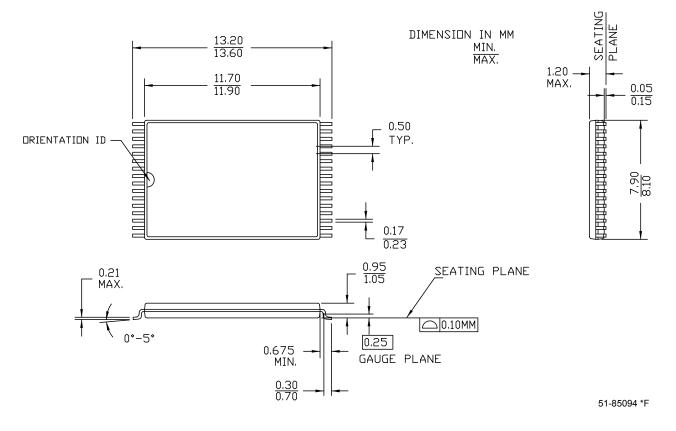


Figure 16. 32-pin STSOP (8 × 13.4 × 1.2 mm) ZA32, 51-85094





Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SOIC	small-outline integrated circuit
SRAM	static random access memory
STSOP	small thin small outline package
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
μA	micro Amperes
μS	micro seconds
mA	milli Amperes
mm	milli meter
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farads
V	Volts
W	Watts





Document History Page

Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	463660	See ECN	NXR	New data sheet
*A	467351	See ECN	NXR	Added 32-pin TSOP II package, 32 pin TSOP I and 32 pin STSOP packages Changed ball A3 from NC to CE_2 in 36-ball FBGA pin out
*В	566724	See ECN	NXR	Converted from Preliminary to Final Corrected typo in 32 pin TSOP II pin configuration diagram on page #2 (changed pin 24 from CE ₁ to OE and pin 22 from CE to CE ₁) Changed the I _{CC(max)} value from 2.25 mA to 2.5 mA for test condition f=1 MHz Changed the I _{SB2(typ)} value from 0.5 μ A to 1 μ A Changed the I _{SB2(max)} value from 2.5 μ A to 5 μ A Changed the I _{SB2(max)} value from 0.5 μ A to 1 μ A and I _{CCDR(max)} value from 2.5 μ A to 4 μ A
*C	797956	See ECN	VKN	Added 32-pin SOIC package Updated VIL spec for SOIC, TSOP-II, TSOP-I, and STSOP packages on Electrical characteristics table
*D	809101	See ECN	VKN	Corrected typo in the Ordering Information table
*E	940341	See ECN	VKN	Added footnote #7 related to I _{SB2} and I _{CCDR}
*F	2769239	09/25/09	VKN/AESA	Included Automotive-A information
*G	3055119	10/12/2010	RAME	Updated and converted all tablenotes into Footnote Added Acronyms and Units of Measure table Added Updated All Package Diagrams. Updated datasheet as per new template.
*H	3061313	10/15/2010	RAME	Minor changes: Corrected "IO" to "I/O"
*	3078557	11/04/2010	RAME	Corrected 55 C to -55C in Ambient Temperature with Power applied in Maximum Ratings Section
*J	3235744	04/20/2011	RAME	Removed the note "For best practice recommendations, refer to the Cypress application Note "System Design Guidelines" at http://www.cypress.com " in page 1 and its reference in Functional Description. Updated Package Diagrams.
*K	3285093	06/16/2011	RAME	Updated in new template.



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