

Pin Definition^[1, 2]

Pin	Name	I/O	Description
6	CLKINT	I	True Clock Input. Low Voltage Differential True Clock Input.
7	CLKINC	I	Complementary Clock Input. Low Voltage Differential Complementary Clock Input.
22	FBINC	I	Feedback Complementary Clock Input. Differential Input Connect to FBOUTC for accessing the PLL.
23	FBINT	Ι	Feedback True Clock Input. Differential Input Connect to FBOUTT for accessing the PLL.
3,12,17,26	YT(0:3)	0	True Clock Outputs. Differential Outputs.
2,13,16,27	YC(0:3)	0	Complementary Clock Outputs. Differential Outputs.
19	FBOUTT	0	Feedback True Clock Output . Differential Outputs. Connect to FBINT for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.
20	FBOUTC	0	Feedback Complementary Clock Output . Differential Outputs. Connect to FBINC for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships.
24	PWRDWN	Ι	Control input to turn device in the power-down mode.
4,8,11,18,21,25	VDDQ		2.5V Power Supply for Output Clock Buffers.2.5V Nominal.
9	AVDD		2.5V Power Supply for PLL. 2.5V Nominal.
1,5,14,15,28	GND		Ground
10	AGND		Analog Ground. 2.5V Analog Ground.

Zero-delay Buffer

When used as a zero-delay buffer the CY2SSTV855 will likely be in a nested clock tree application. For these applications the CY2SSTV855 offers a differential clock input pair as a PLL reference. The CY2SSTV855 then can lock onto the reference and translate with near zero delay to low-skew outputs. For normal operation, the external feedback differential input, FBINT/C, is connected to the feedback output, FBOUTT/C. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When AVDD is strapped LOW, the PLL is turned off and bypassed for test purposes.

Function Table

Inputs				Outputs				
AVDD	PWRDWN	CLKINT	CLKINC	YT(0:3)	YC(0:3)	FBOUTT	FBOUTC	PLL
GND	Н	L	Н	L	Н	L	Н	BYPASSED/OFF
GND	Н	Н	L	Н	L	Н	L	BYPASSED/OFF
2.5V	Н	L	Н	L	Н	L	Н	On
2.5V	Н	Н	L	Н	L	Н	L	On
2.5V	Х	< 20 MHz	< 20 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Off

Notes:

1. PU = internal pull-up.

2. A bypass capacitor $(0.1\mu F)$ should be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.



CY2SSTV855

Differential Parameter Measurement Information



CY2SSTV855

Differential Parameter Measurement Information (continued)

Absolute Maximum Conditions^[3]

Input Voltage Relative to V _{SS} :	V _{SS} – 0.3V
Input Voltage Relative to V _{DDQ} or AV _{DD} :	V _{DD} + 0.3V
Storage Temperature:	65°C to + 150°C
Operating Temperature:	–40°C to +85°C
Maximum Power Supply:	3.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

 $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications	$(AV_{DD} = V_{DDQ})$	= 2.5V ± 5%, T _A =	= –40°C to +85°C) ^[4]
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Parameter	Description	Conditions	Min.	Тур.	Max.	Unit
V _{ID}	Differential Input Voltage ^[5]	CLKINT, FBINT	0.36		V _{DDQ} + 0.6	V
V _{IX}	Differential Input Crossing Voltage ^[6]	CLKTIN, FBINT	(V _{DDQ} /2)- 0.2	V _{DDQ} /2	(V _{DDQ} /2) + 0.2	V
I _{IN}	Input Current	$V_{IN} = 0V \text{ or } V_{IN} = V_{DDQ}, CLKINT, FBINT$	-10	-	10	μA
I _{OL}	Output Low Current	V _{DDQ} = 2.375V, V _{OUT} = 1.2V	26	35	-	mA
I _{OH}	Output High Current	V _{DDQ} = 2.375V, V _{OUT} = 1V	-18	-32	-	mA
V _{OL}	Output Low Voltage	V _{DDQ} = 2.375V, I _{OL} = 12 mA		-	0.6	V
V _{OH}	Output High Voltage	V _{DDQ} = 2.375V, I _{OH} = -12 mA	1.7	-	-	V
V _{OUT}	Output Voltage Swing ^[7]		1.1	-	$V_{DDQ} - 0.4$	V
V _{OC}	Output Crossing Voltage ^[8]		(V _{DDQ} /2) – 0.2	V _{DDQ} /2	(V _{DDQ} /2) + 0.2	V
I _{OZ}	High-Impedance Output Current	$V_{O} = GND \text{ or } V_{O} = V_{DDQ}$	-10		10	μΑ
I _{DDQ}	Dynamic Supply Current ^[9]	V _{DDQ} = 170 MHz	-	235	300	mA
I _{DD}	PLL Supply Current	AV _{DD} only	_	9	12	mA
Cin	Input Pin Capacitance		_	4	_	pF

AC Electrical Specifications (AV_{DD} = V_{DDQ} = 2.5V±5%, T_A = -40°C to +85°C)^[10, 11]

Parameter	Description	Conditions	Min.	Тур.	Max.	Unit
f _{CLK}	Operating Clock Frequency	$AV_{DD} = 2.5V \pm 0.2V$	60		170	MHz
t _{DC}	Input Clock Duty Cycle ^[12]		40		60	%
t _{LOCK}	Maximum PLL lock Time				100	μs
t _{SL(O)}	Output Clocks Slew Rate	20% to 80% of VOD	1		2	V/ns
t _{PZL} , t _{PZH}	Output Enable Time (all outputs) ^[13]			30		ns
t _{PLZ} , t _{PHZ}	Output Disable Time (all outputs) ^[13]			10		ns
t _{CCJ}	Cycle to Cycle Jitter	f > 66 MHz	-100		100	ps
t _{JITT(H-PER)}	Half-period jitter	f > 66 MHz	-100		100	ps

Notes:

3. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

4. Unused inputs must be held HIGH or LOW to prevent them from floating.

5. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.

6. Differential cross-point input voltage is expected to track V_{DDQ} and is the voltage at which the differential signals must be crossing.

7. For load conditions see Figure 6.

8. The value of V_{OC} is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120Ω resistor. See Figure 6.

9. All outputs switching loaded with 16 pF in 60Ω environment. See Figure 6.

10. Parameters are guaranteed by design and characterization. Not 100% tested in production.

11. PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30 kHz and 33.3 kHz with a downspread of -0.5%

12. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{WH}/t_C, where the cycle time t_C decreases as the frequency goes up.

13. Refers to transition of non-inverting output.

14. All differential input and output terminals are terminated with 120Ω/16 pF as shown in Figure 6.

AC Electrical Specifications (AV_{DD} = V_{DDQ} = 2.5V±5%, T_A = -40°C to +85°C)^[10, 11] (continued)

Parameter	Description	Conditions	Min.	Тур.	Max.	Unit
t _{PLH}	Low-to-High Propagation Delay, CLKINT to YT[0:3]		1.5	3.5	6	ns
t _{PHL}	High-to-Low Propagation Delay, CLKINT to YT[0:3]		1.5	3.5	6	ns
t _{SK(0)}	Any Output to Any Output Skew ^[14]		-	-	100	ps
t _(Ø)	Static Phase Offset ^[14]		-450	-	450	ps
t _{D(Ø)}	Dynamic Phase Offset	f > 66 MHz	-350	_	350	ps

Ordering Information

Part Number	Package Type	Product Flow	
CY2SSTV855ZC	28-pin TSSOP	Commercial, 0° to 70°C	
CY2SSTV855ZCT	28-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C	
CY2SSTV855ZI	28-pin TSSOP	Industrial, –40° to 85°C	
CY2SSTV855ZIT	28-pin TSSOP – Tape and Reel	Industrial,–40° to 85°C	
Lead Free			
CY2SSTV855ZXC	28-pin TSSOP	Commercial, 0° to 70°C	
CY2SSTV855ZXCT	28-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C	
CY2SSTV855ZXI	28-pin TSSOP	Industrial, –40° to 85°C	
CY2SSTV855ZXIT	28-pin TSSOP – Tape and Reel	Industrial,–40° to 85°C	

Package Drawing and Dimensions

28-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z28.173

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