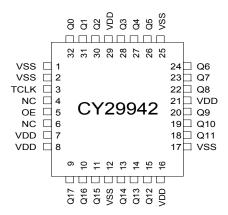


# **Pin Configuration**

Figure 1. 32-pin TQFP pinout



# **Pin Descriptions**

Pin	Name	I/O	Description
3	TCLK	Input	External reference/Test clock input. Weak internal pull-down resistor.
5	OE	Input	Output enable. When HIGH, all outputs are enabled. When set LOW, the outputs are at high impedance. Weak internal pull-up resistor.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	Output	Clock outputs
7, 8, 16, 21, 29	VDD		2.5 V or 3.3 V power supply
1, 2, 12, 17, 25	VSS		Ground
4, 6	NC		No connection

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## **Absolute Maximum Ratings**

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested. [1]

Maximum input voltage relative to $V_{SS}\!\!:$ $V_{SS}\!-0.3~V$
Maximum input voltage relative to $V_{DD}$ : $V_{DD}$ + 0.3 $V$
Storage temperature: –65 °C to 150 °C
Operating temperature:40 °C to 85 °C
Maximum ESD protection

Maximum power supply:5.5	i۷
Maximum input current:±20 n	nΑ

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, I/O voltages should be constrained to the range:

$$V_{SS} < V_{I/O} < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

## **DC Electrical Specifications**

 $V_{DD}$  = 3.3 V ± 5% or 2.5 V ± 5% over the specified temperature range.

Parameter	Description	Conditions	Min	Тур	Max	Unit
V <sub>IL</sub>	Input low voltage		V <sub>SS</sub>	-	0.8	V
V <sub>IH</sub>	Input high voltage		2.0	_	V <sub>DD</sub>	V
I <sub>IL</sub>	Input low current <sup>[2]</sup>		-	_	-200	μA
I <sub>IH</sub>	Input high current <sup>[2]</sup>		_	_	200	μA
V <sub>OL</sub>	Output low voltage <sup>[3]</sup>	I <sub>OL</sub> = 20 mA	-	-	0.5	V
V <sub>OH</sub>	Output high voltage <sup>[3]</sup>	$I_{OH}$ = -20 mA, $V_{DD}$ = 3.3 V	2.4	-	-	V
		I <sub>OH</sub> = –16 mA, V <sub>DD</sub> = 2.5 V	2.0	-	-	V
$I_{DDQ}$	Quiescent supply current	OE = V <sub>SS</sub>	-	5	7	mA
I <sub>DD</sub>	Dynamic supply current	V <sub>DD</sub> = 3.3 V, Outputs at 150 MHz, CL = 15 pF	_	285	_	mA
		$V_{DD}$ = 3.3 V, Outputs at 200 MHz, CL = 15 pF	_	335	_	mA
		$V_{DD}$ = 2.5 V, Outputs at 150 MHz, CL = 15 pF	_	200	_	mA
		$V_{DD}$ = 2.5 V, Outputs at 200 MHz, CL = 15 pF	_	240	_	mA
Z <sub>out</sub>	Output impedance	V <sub>DD</sub> = 3.3 V	8	12	16	Ω
		V <sub>DD</sub> = 2.5 V	10	15	20	Ω
C <sub>in</sub>	Input capacitance		_	4	_	pF

### **Thermal Resistance**

Parameter [4]	Description	Test Conditions	32-pin TQFP	Unit
$\theta_{JA}$	,	Test conditions follow standard test methods and procedures for measuring thermal impedance, in	67	°C/W
$\theta_{JC}$	Thermal resistance (junction to case)	accordance with EIA/JESD51.	28	°C/W

#### Notes

- 1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
- 2. Inputs have pull-up/pull-down resistors that effect input current.
- 3. Driving series or parallel terminated 50  $\!\Omega$  (or 50  $\!\Omega$  to V  $\!DD/2$  ) transmission lines.
- 4. These parameters are guaranteed by design and are not tested.

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## **AC Electrical Specifications**

 $V_{DD}$  = 3.3 V ±5% or 2.5 V ±5% over the specified temperature range  $^{[5]}$ 

Parameter	Description	Conditions	Min	Тур	Max	Unit
Fmax	Input frequency		_	-	200	MHz
tpd	TTL_CLK to Q delay <sup>[6, 7]</sup>	V <sub>DD</sub> = 3.3 V	1.8	3.3	3.8	ns
		V <sub>DD</sub> = 2.5 V	2.3	3.8	4.4	ns
DC	Output duty cycle <sup>[6, 7, 8]</sup>	Measured at V <sub>DD</sub> /2	45	-	55	%
tsk(0)	Output-to-output skew <sup>[6, 7]</sup>		_	110	200	ps
tskew(pp)	Part-to-part skew <sup>[9]</sup>	V <sub>DD</sub> = 3.3 V	_	-	1.0	ns
		V <sub>DD</sub> = 2.5 V	_	-	1.3	ns
tskew(pp)	Part-to-part skew <sup>[10]</sup>		_	-	600	ps
tr/tf	Output clocks rise/fall time <sup>[6, 7]</sup>	0.8 V to 2.0 V, V <sub>DD</sub> = 3.3 V; 0.5 V to 1.8 V, V <sub>DD</sub> = 2.5 V	0.2	_	1.1	ns

#### Notes

- 5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
  6. Outputs driving 50 Ω transmission lines.
  7. See Figure 2.

- 8. 50% input duty cycle.9. Across temperature and voltage ranges, includes output skew.10. For a specific temperature and voltage, includes output skew.

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Figure 2. LVCMOS\_CLK CY29942 Test Reference for  $V_{CC}$  = 3.3 V and  $V_{CC}$  = 2.5 V

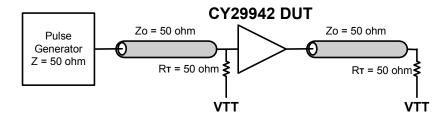


Figure 3. LVCMOS Propagation Delay (tpd) Test Reference

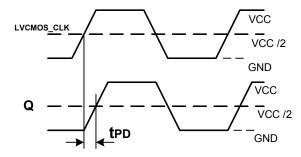


Figure 4. Output Duty Cycle (DC)

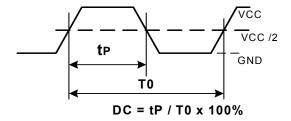
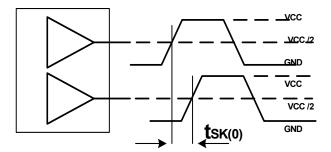


Figure 5. Output-to-Output Skew tsk(0)



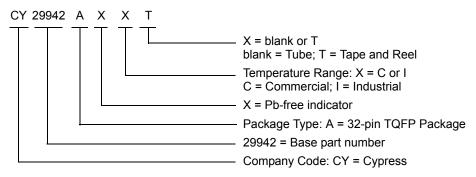
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# **Ordering Information**

Part Number	Package Type	Production Flow
Pb-free		
CY29942AXI	32-pin TQFP	Industrial, –40 °C to 85 °C
CY29942AXIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to 85 °C
CY29942AXC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY29942AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to 70 °C

### **Ordering Code Definitions**

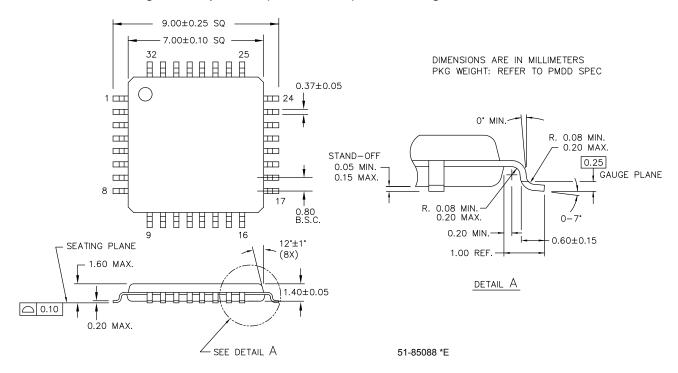


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## **Package Drawing and Dimensions**

Figure 6. 32-pin TQFP (7 × 7 × 1.4 mm) A3214 Package Outline, 51-85088





# **Acronyms**

Acronym	Description
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor-Transistor Logic
OE	Output Enable
PLL	Phase-Locked Loop
TQFP	Thin Quad Flat Pack

## **Document Conventions**

### **Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
MHz	megahertz
μΑ	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

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# **Document History Page**

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	111095	BRK	02/07/02	New data sheet.
*A	116777	HWT	08/14/02	Added a Commercial Temp. Range in the Ordering Information
*B	122876	RBI	12/21/02	Add power up requirements to maximum rating information.
*C	334117	RGL	See ECN	Added Lead-free devices Added typical value for output-output skew
*D	2761988	KVM	09/10/09	Ordering Information table: fixed typo and removed obsolete CY29942ACT. Changed Lead-free to Pb-free.
*E	2899304	BASH / CXQ	03/25/2010	Removed CY29942AC part from Ordering Information. Updated package diagram.
*F	3034172	CXQ	09/21/2010	Changed spec title. Updated format of "Features", changed wording in "Functional Description". Removed note 1, added info into Table 1 directly. Removed reference to multiple supplies, power supply sequencing from Absolute Maximum Ratings. Removed reference to $V_{DDC}$ from AC/DC Electrical Specs tables. Added condition OE = $V_{SS}$ for $I_{DDQ}$ in DC Electrical Specs table. Fixed formatting in AC/DC Electrical specs tables. Changed $t_{SKEW}$ to $t_{SK(0)}$ to match Figure 6. Added Ordering Code Definitions. Added Acronyms and Units of Measure sections. Minor edits.
*G	3548252	PURU	03/12/2012	Changed LQFP to TQFP throughout document.
*H	4149208	CINM	10/07/2013	Updated Package Drawing and Dimensions: spec 51-85088 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*	4586288	CINM	12/03/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end Updated Ordering Information: Removed the prune part numbers CY29942AI and CY29942AIT.
*J	5258930	PSR	05/04/2016	Added Thermal Resistance. Updated to new template.
*K	5500790	PAWK	10/28/2016	Sunset Review - No content change.
*L	5972824	AESATMP8	11/21/2017	Updated logo and Copyright.

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