Pinouts

Figure 1. CY2309NZ - 16 SOIC-Top View

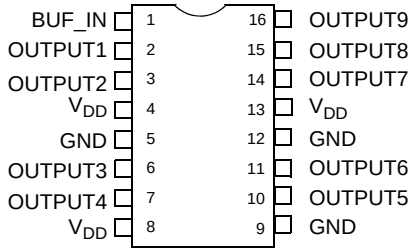


Table 1. Pin Description for CY2309NZ

Pin	Signal	Description
4, 8, 13	V_{DD}	3.3V Digital Voltage Supply
5, 9, 12	GND	Ground
1	BUF_IN	Input Clock
2, 3, 6, 7, 10, 11, 14, 15, 16	OUTPUT [1:9]	Outputs

Maximum Ratings

Supply Voltage to Ground Potential.....–0.5V to +7.0V

DC Input Voltage (Except REF) .....–0.5V to V_{DD} + 0.5V

DC Input Voltage REF .....–0.5V to 7V

Storage Temperature .....–65°C to +150°C

Junction Temperature ..... 150°C

Static Discharge Voltage (per MIL-STD-883, Method 3015) .....>2,000V

Operating Conditions for Commercial and Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	(Ambient Operating Temperature) Commercial	0	70	°C
	(Ambient Operating Temperature) Industrial	–40	85	°C
C_L	Load Capacitance, Fout < 100 MHz		30	pF
	Load Capacitance,100 MHz < Fout < 133.33 MHz		15	pF
C_{IN}	Input Capacitance		7	pF
BUF_IN, OUTPUT [1:9]	Operating Frequency	DC	133.33	MHz
t_{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for Commercial and Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage[1]			0.8	V
V_{IH}	Input HIGH Voltage[1]		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA		0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = –8 mA	2.4		V
I_{DD}	Supply Current	Unloaded outputs at 66.66 MHz		32	mA

Notes
1. BUF_IN input has a threshold voltage of V_{DD}/2.
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.

Switching Characteristics for Commercial and Industrial Temperature Devices[3]

Parameter	Name	Description	Min	Typ.	Max	Unit
	Duty Cycle[2] = $t_2 \div t_1$	Measured at 1.4V	40.0	50.0	60.0	%
t_3	Rise Time[2]	Measured between 0.8V and 2.0V			1.50	ns
t_4	Fall Time[2]	Measured between 0.8V and 2.0V			1.50	ns
t_5	Output to Output Skew[2]	All outputs equally loaded			250	ps
t_6	Propagation Delay, BUF_IN Rising Edge to OUTPUT Rising Edge[2]	Measured at $V_{DD}/2$	1	5	9.2	ns

Switching Waveforms

Figure 2. Duty Cycle Timing

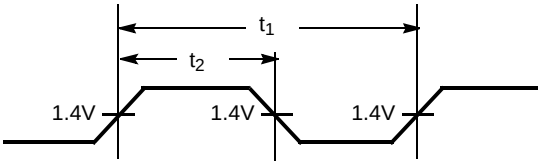


Figure 3. All Outputs Rise/Fall Time

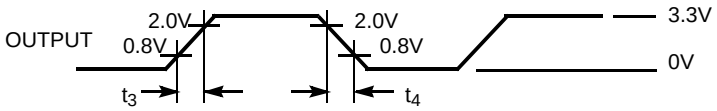


Figure 4. Output-Output Skew

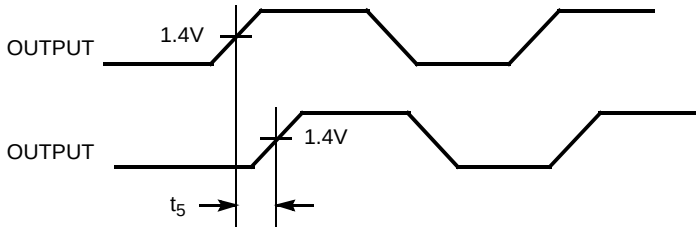
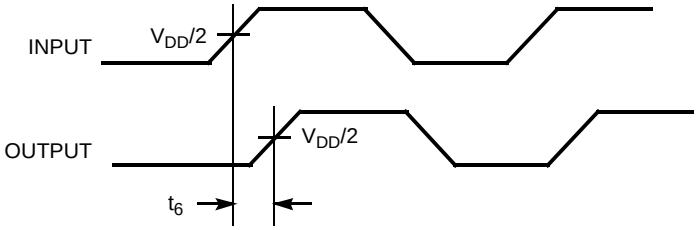
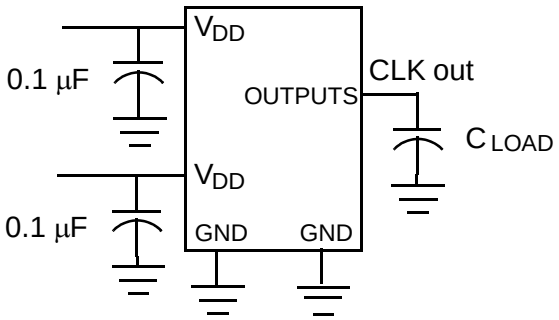


Figure 5. Input-Output Propagation Delay



Note
3. All parameters specified with loaded outputs.

Test Circuits

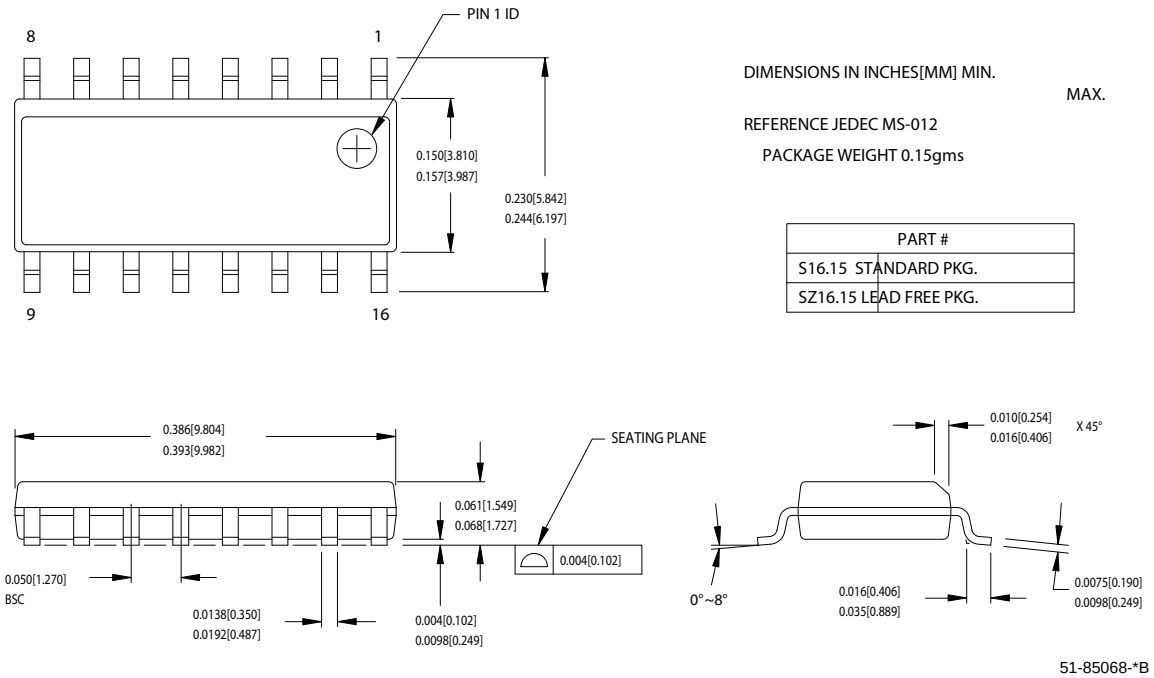


Ordering Information

Ordering Code	Package Type	Operating Range
CY2309NZSC–1H[4]	16-pin 150-mil SOIC	Commercial
CY2309NZSC–1HT[4]	16-pin 150-mil SOIC – Tape and Reel	Commercial
Pb-free		
CY2309NZSXC–1H	16-pin 150-mil SOIC	Commercial
CY2309NZSXC–1HT	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309NZSXI-1H	16-pin 150-mil SOIC	Industrial
CY2309NZSXI-1HT	16-pin 150-mil SOIC – Tape and Reel	Industrial

Package Diagram

Figure 6. 16-Pin (150-Mil) SOIC S16



Note
4. Not recommended for new designs.

Document History Page

Document Title: CY2309NZ Nine-Output 3.3V Buffer Document Number: 38-07182				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	111858	DSG	12/09/01	Change from Spec number: 38-00709 to 38-07182
*A	121834	RBI	12/14/02	Power-up requirements added to Operating Conditions Information
*B	130563	SDR	10/23/03	Added industrial operating temperature to operating conditions
*C	212991	RGL/GGK	03/30/04	Updated the propagation delay T_6 spec to 9.2 ns in the Switching Characteristics table
*D	270149	RGL	10/04/04	Added Lead-free devices Replaced 8.7ns Input/Output Delay to 1ns Input/Output Delayin the features section
*E	2568533	AESA	09/23/08	Updated template. Added Note “Not recommended for new designs.” Changed "SDRAM [1:9]" to "OUTPUT [1:9]" in Operating Conditions table. Removed part number CY2309NZSI–1H and CY2309NZSI–1HT.

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