

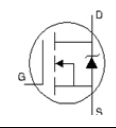
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/°C	Reference to 25°C , $I_D = 5mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.2	3.9	$m\Omega$	$V_{GS} = 10V, I_D = 110A$ ④
		—	3.3	4.1		$V_{GS} = 4.5V, I_D = 94A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Trans conductance	250	—	—	S	$V_{DS} = 25V, I_D = 110A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
R_G	Internal Gate Resistance	—	2.0	—	Ω	

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

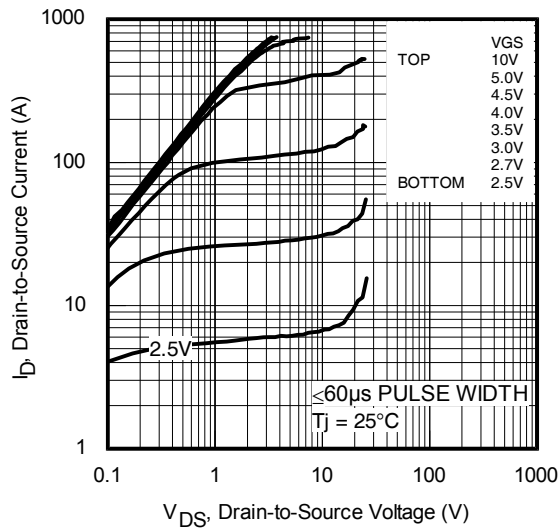
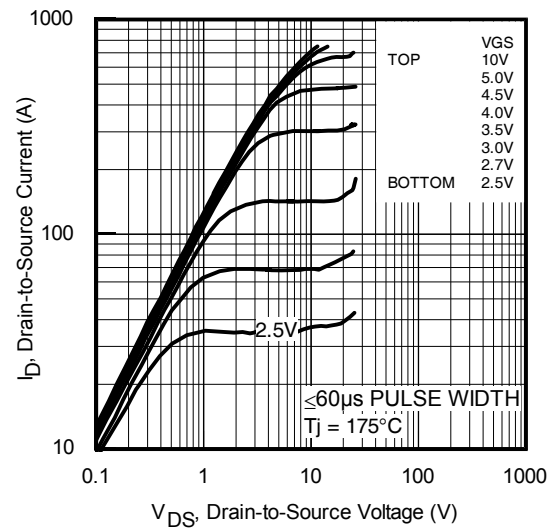
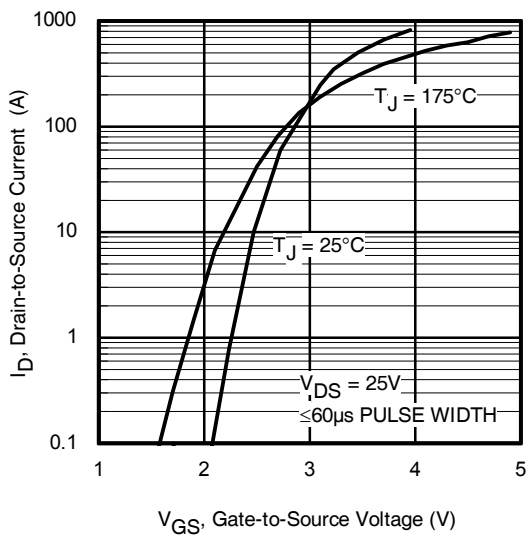
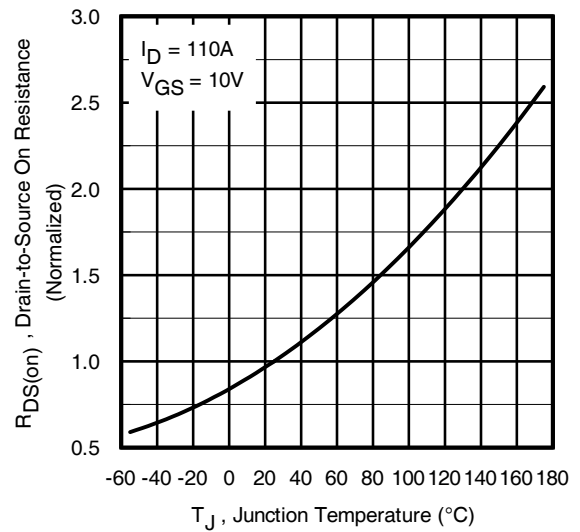
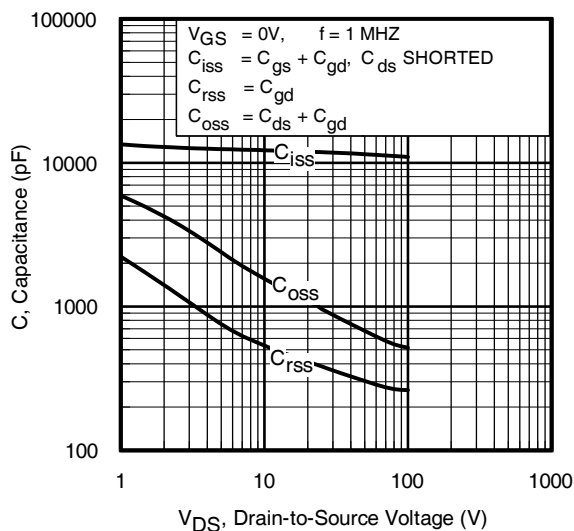
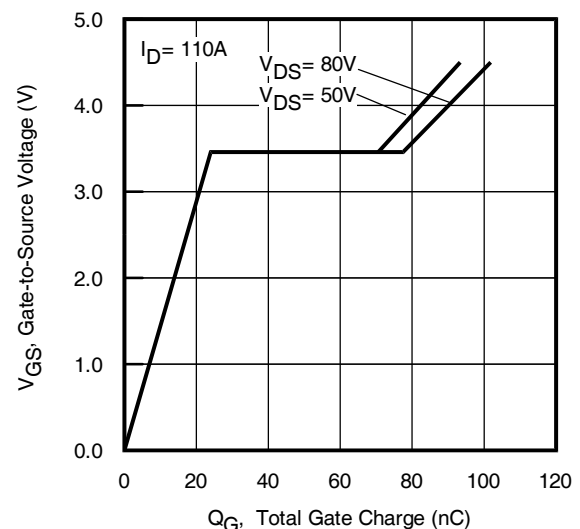
Q_g	Total Gate Charge	—	93	140	nC	$I_D = 110A$ $V_{DS} = 50V$ $V_{GS} = 4.5V$ ④
Q_{gs}	Gate-to-Source Charge	—	27	—		
Q_{gd}	Gate-to-Drain Charge	—	43	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	50	—	ns	$V_{DD} = 65V$ $I_D = 110A$ $R_G = 2.7\Omega$ $V_{GS} = 4.5V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	53	—		
t_r	Rise Time	—	160	—		
$t_{d(off)}$	Turn-Off Delay Time	—	110	—		
t_f	Fall Time	—	87	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0MHz$ $V_{GS} = 0V, V_{DS} = 0V$ to $80V$ ⑥ $V_{GS} = 0V, V_{DS} = 0V$ to $80V$ ⑤
C_{iss}	Input Capacitance	—	11490	—		
C_{oss}	Output Capacitance	—	680	—		
C_{rss}	Reverse Transfer Capacitance	—	300	—		
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	760	—		
$C_{oss\ eff.(TR)}$	Effective Output Capacitance (Time Related)	—	1170	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	190	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	750		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 110A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	53	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 85V$ $T_J = 125^\circ\text{C}$ $I_F = 110A,$ $di/dt = 100A/\mu s$ ④
		—	63	—		
Q_{rr}	Reverse Recovery Charge	—	99	—	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
		—	155	—		
I_{RRM}	Reverse Recovery Current	—	3.3	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.05mH$, $R_G = 25\Omega$, $I_{AS} = 110A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ $I_{SD} \leq 110A$, $di/dt \leq 1520A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss\ eff. (TR)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $C_{oss\ eff. (ER)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R_θ is measured at T_J approximately 90°C .
- ⑨ $R_{\theta JC}$ value shown is at time zero.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

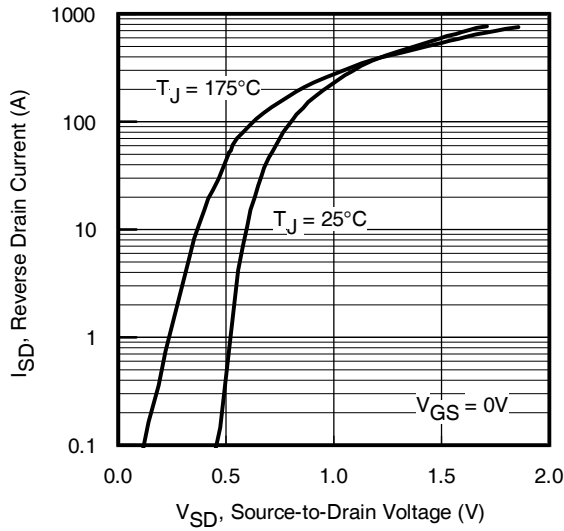


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

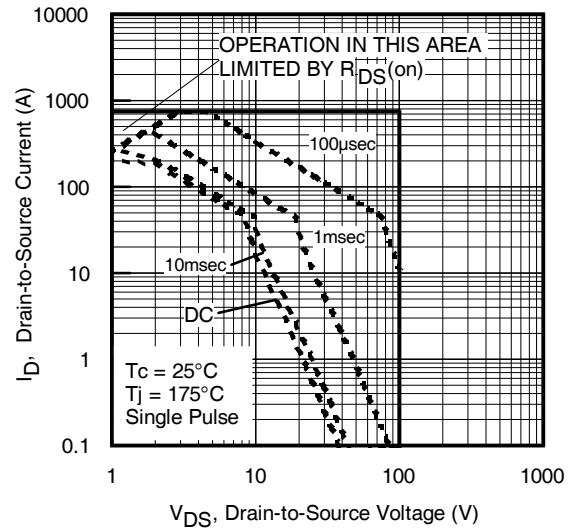


Fig 8. Maximum Safe Operating Area

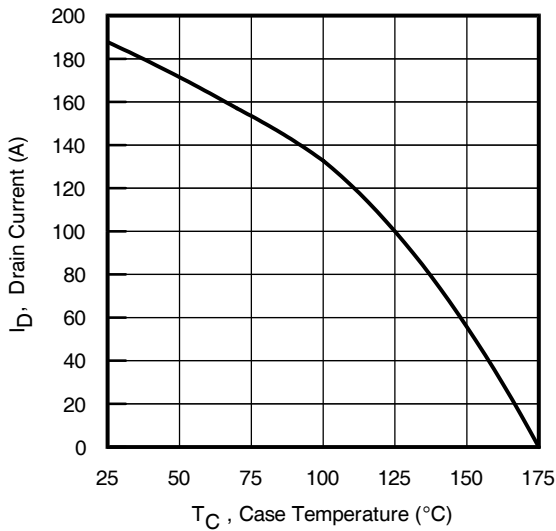


Fig 9. Maximum Drain Current vs. Case Temperature

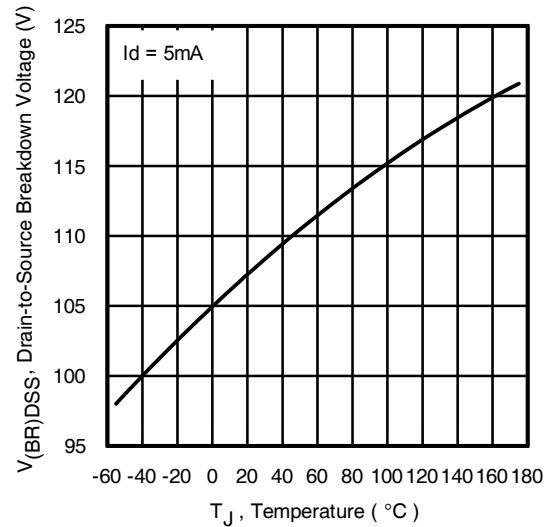


Fig 10. Drain-to-Source Breakdown Voltage

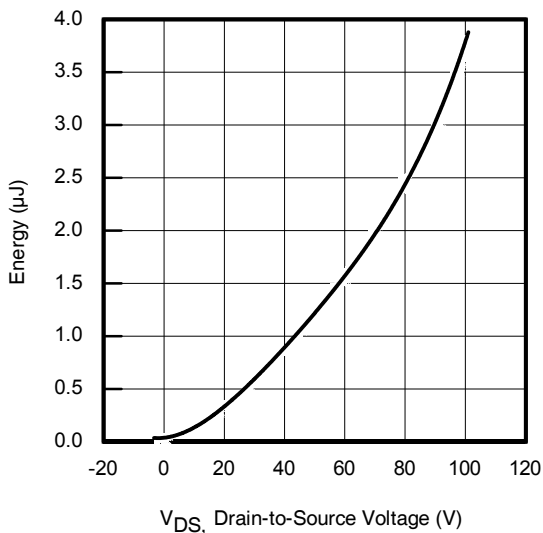


Fig 11. Typical Coss Stored Energy

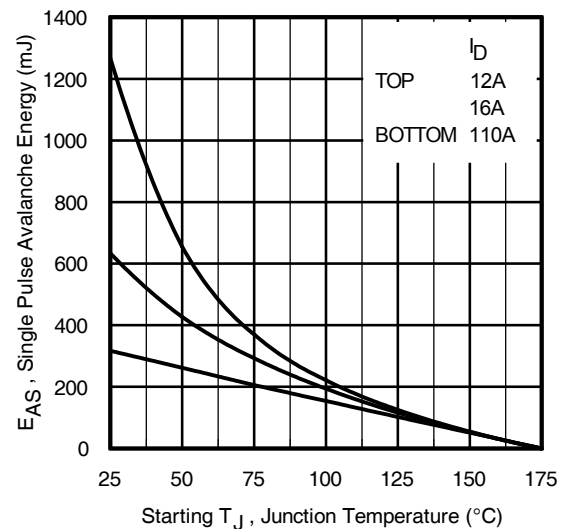


Fig 12. Maximum Avalanche Energy vs. Drain Current

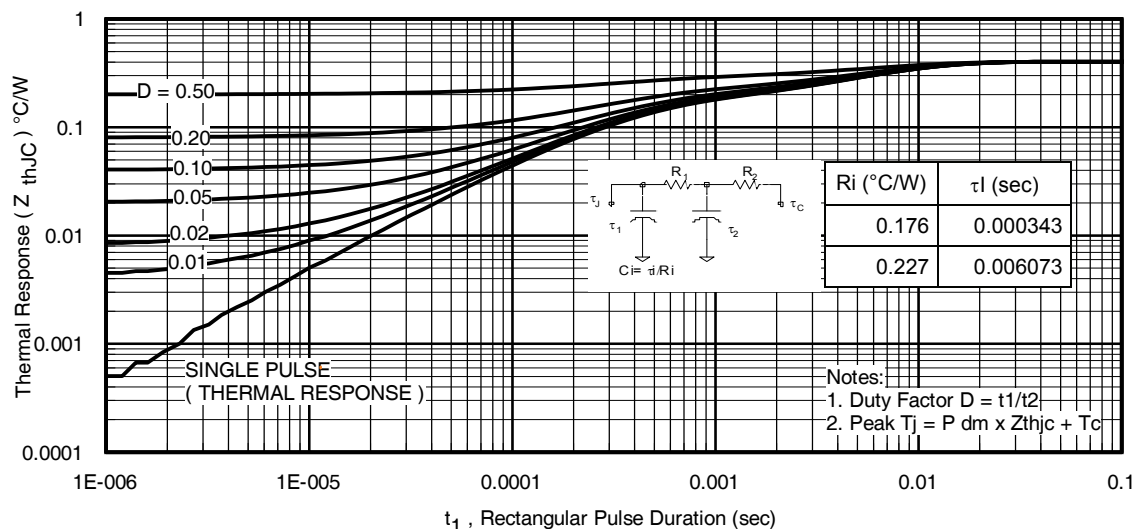


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

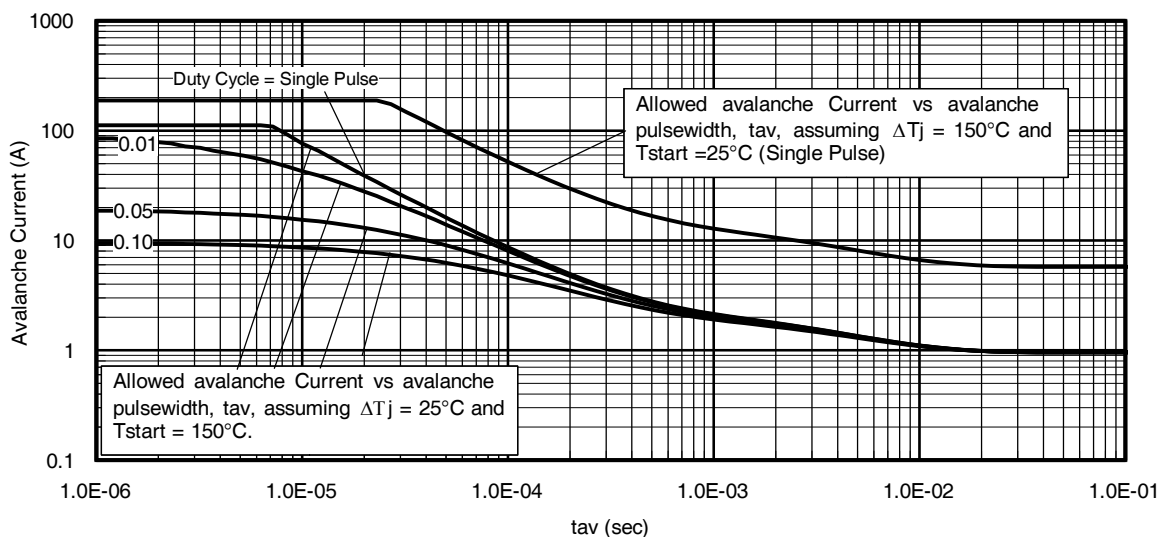
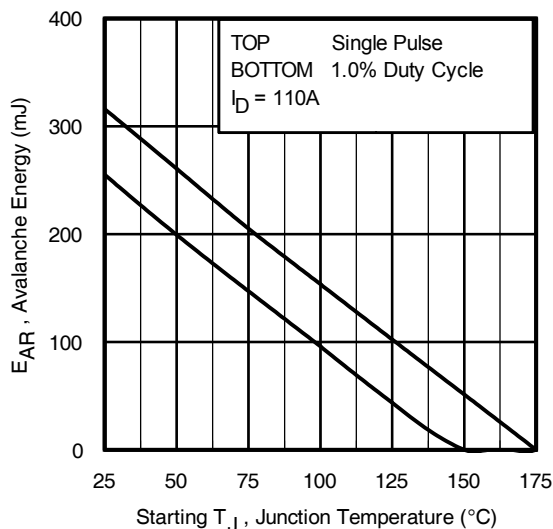


Fig 14. Avalanche Current vs. Pulse width



Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

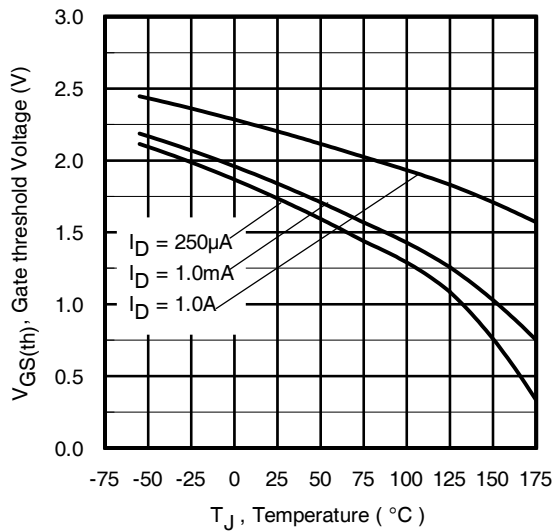
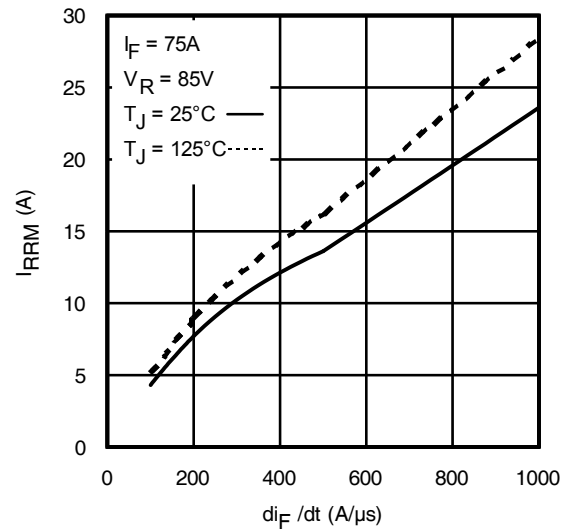
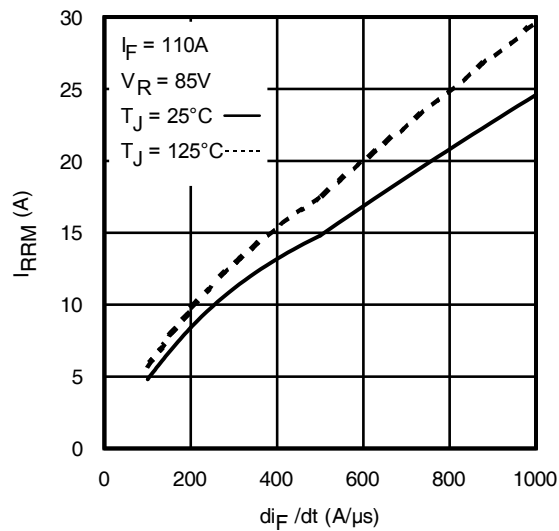
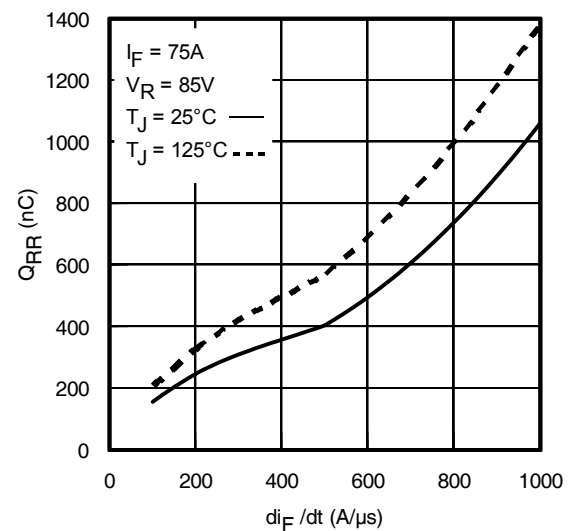
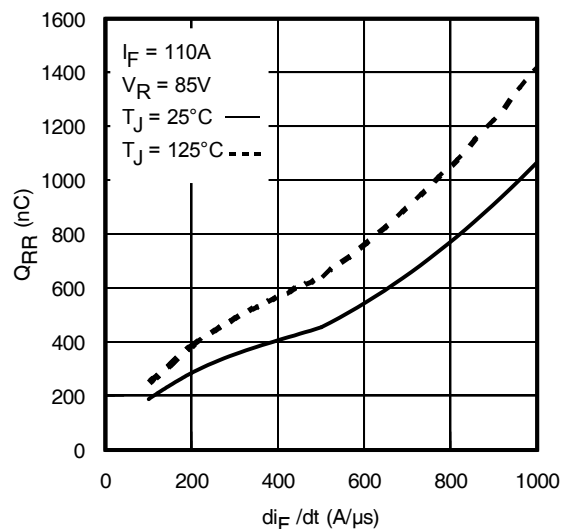
- Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
- Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
- Equation below based on circuit and waveforms shown in Figures 18a, 18b.
- $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- I_{av} = Allowable avalanche current.
- ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

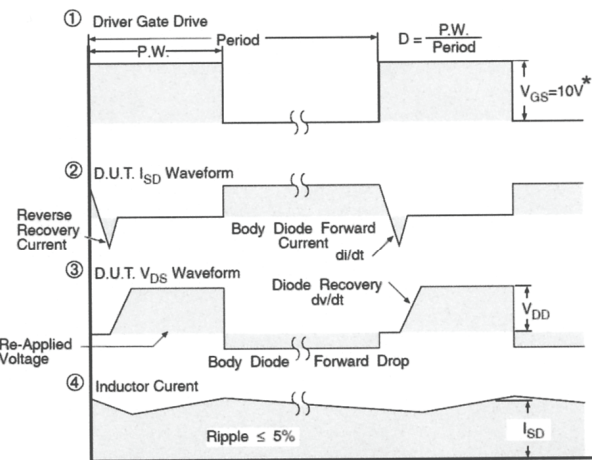
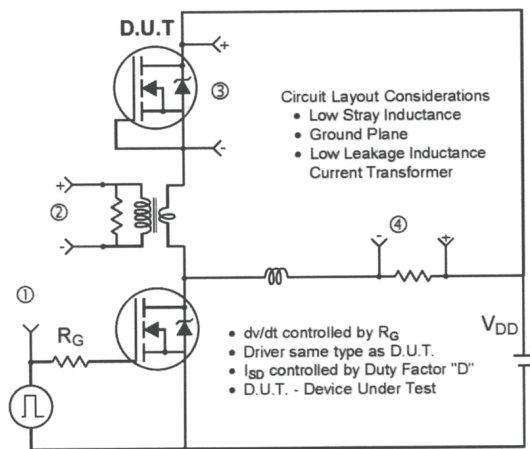
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature


Fig. 16. Threshold Voltage vs. Temperature

Fig. 17 - Typical Recovery Current vs. di_F/dt

Fig. 18 - Typical Recovery Current vs. di_F/dt

Fig. 19 - Typical Stored Charge vs. di_F/dt

Fig. 20 - Typical Stored Charge vs. di_F/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

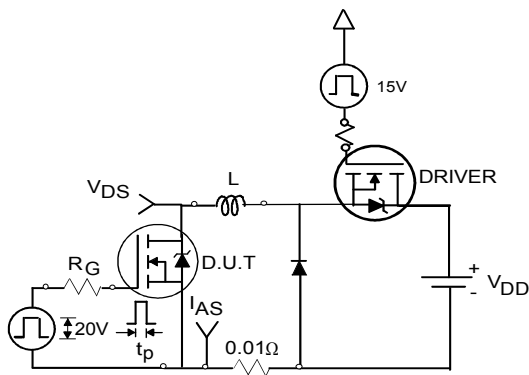


Fig 22a. Unclamped Inductive Test Circuit

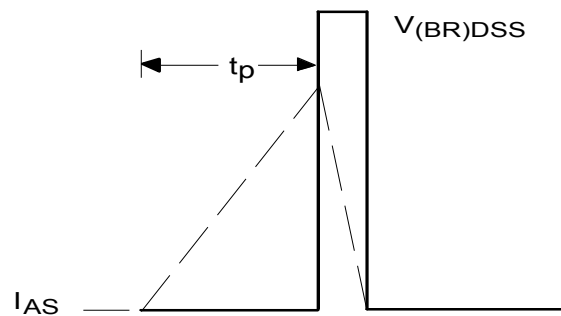


Fig 22b. Unclamped Inductive Waveforms

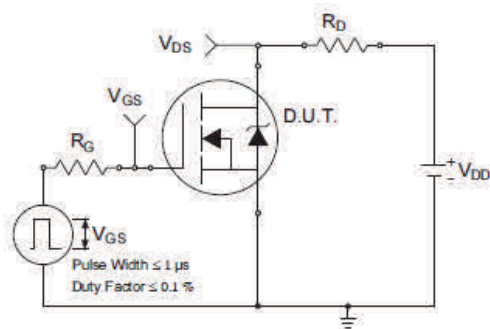


Fig 23a. Switching Time Test Circuit

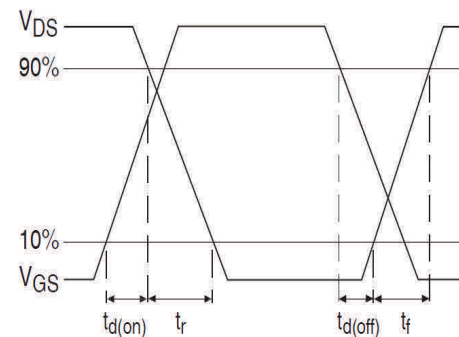


Fig 23b. Switching Time Waveforms

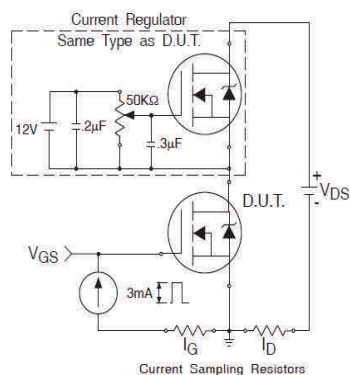


Fig 24a. Gate Charge Test Circuit

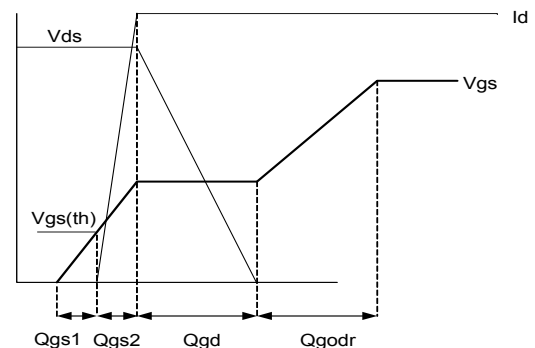
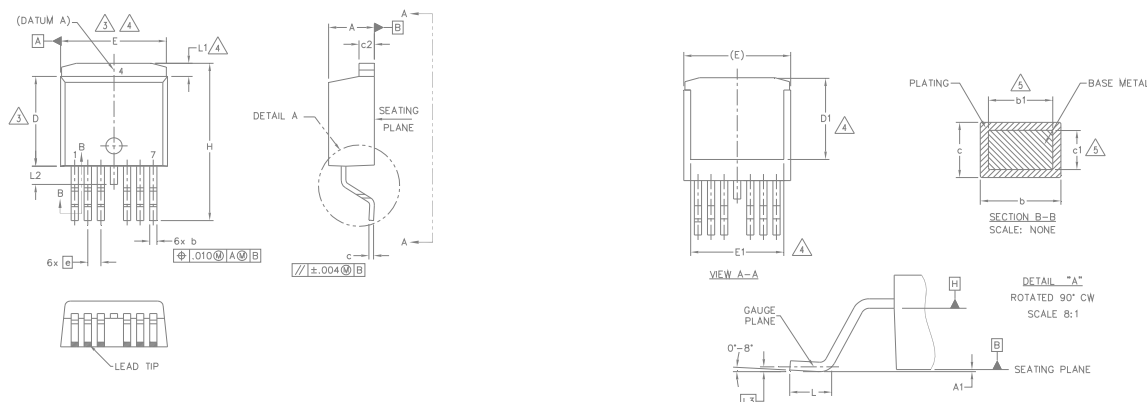


Fig 24b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline (Dimensions are shown in millimeters (inches))

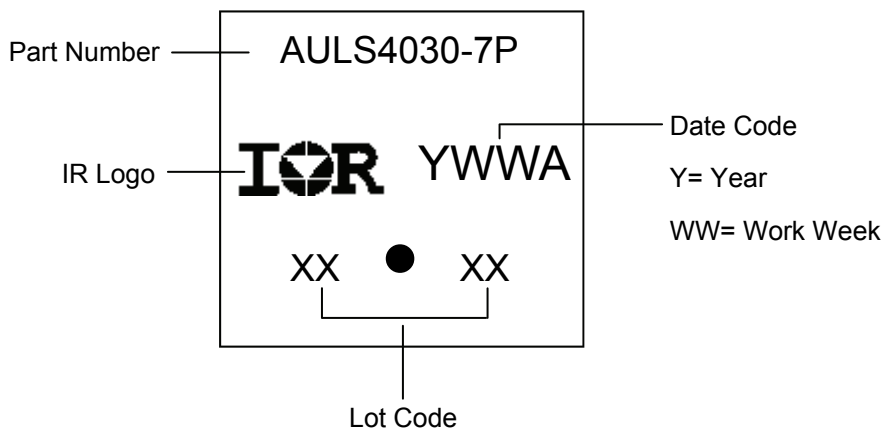


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	3,4
D	8.38	9.65	.330	.380	
D1	6.86	7.42	.270	.292	
E	9.65	10.54	.380	.415	
E1	6.22	8.48	.245	.334	
e	1.27 BSC		.050 BSC		4
H	14.61	15.88	.575	.625	4
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

D²Pak - 7 Pin Part Marking Information

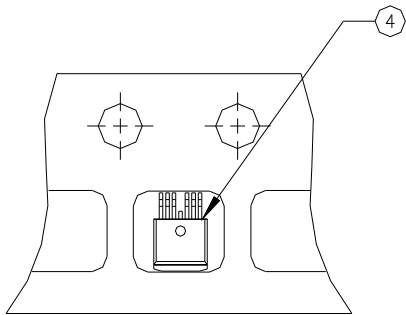


D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

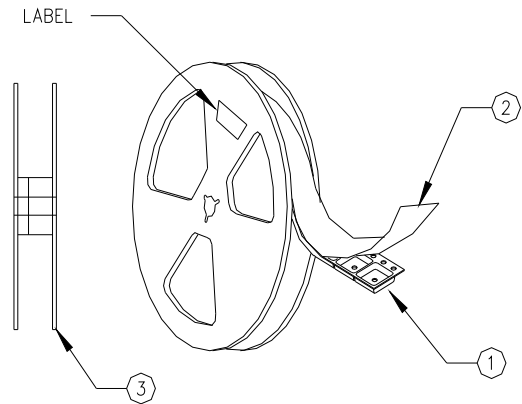
1. TAPE AND REEL.

- 1.1 REEL SIZE 13 INCH DIAMETER.
- 1.2 EACH REEL CONTAINING 800 DEVICES.
- 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
- 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
- 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
- 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.



2. LABELLING (REEL AND SHIPPING BAG).

- 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
- 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
- 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
- 2.4 QUANTITY:
- 2.5 VENDOR CODE: IR
- 2.6 LOT CODE:
- 2.7 DATE CODE:



Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D ² -Pak 7 Pin	MSL1
ESD	Machine Model	Class M4 (+/- 800V) [†] AEC-Q101-002	
	Human Body Model	Class H3A (+/- 6000V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
03/03/2014	- Added "Logic Level Gate Drive" bullet in the features section on page 1 - Updated data sheet with new IR corporate template
04/02/2014	- Updated package outline and part marking on page 8 & 9 - Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 6.
11/06/2015	- Updated datasheet with corporate template - Corrected ordering table on page 1.
10/10/2017	Corrected typo error on part marking on page 8.

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