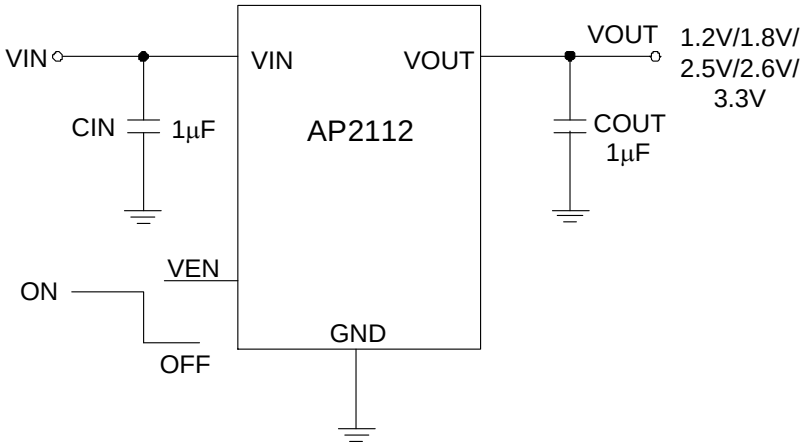
Typical Applications Circuit (Note 4)

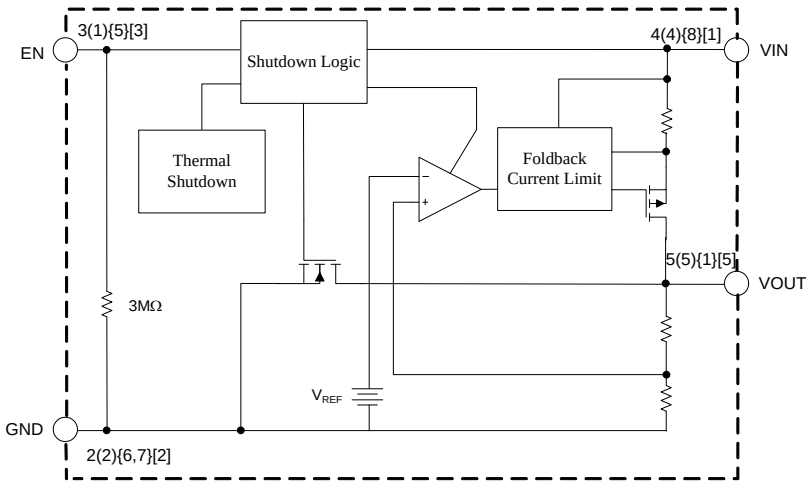


Note 4: It is recommended to use X7R or X5R dielectric capacitor if 1.0μF ceramic capacitor is selected as input/output capacitors.

Pin Descriptions

Pin Number			Pin Name	Function
SOT25	SOT89-5	SO-8		
1	4	8	VIN	Input Voltage
2	2	6, 7	GND	GND
3	3 (R5)	5	EN	Chip Enable, H – normal work, L – shutdown output
	1 (R5A)			
—	1 (R5)	2, 3, 4	NC	No Connection
	3 (R5A)			
5	5	1	VOUT	Output Voltage

Functional Block Diagram



A (B){C}[D]
A: SOT89-5 (R5)
B: SOT89-5 (R5A)
C: SO-8
D: SOT25

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Absolute Maximum Ratings (Note 5)

Symbol	Parameter	Rating		Unit
V_{CC}	Power Supply Voltage	6.5		V
T_J	Operating Junction Temperature Range	+150		°C
T_{STG}	Storage Temperature Range	-65 to +150		°C
T_{LEAD}	Lead Temperature (Soldering, 10 Seconds)	+260		°C
θ_{JA}	Thermal Resistance (Junction to Ambient)(No Heatsink)	SOT25	184	°C/W
		SO-8	114	
		SOT89-5	120	
—	ESD (Machine Model)	400		V
—	ESD (Human Body Model)	4000		V

Note 5: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	2.5	6.0	V
T_A	Ambient Operation Temperature Range	-40	+85	°C

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Electrical Characteristics

AP2112-1.2 Electrical Characteristics (@V_{IN} = 2.5V, C_{IN} = 1.0µF (Ceramic), C_{OUT} = 1.0µF (Ceramic), Typical T_A = +25°C, unless otherwise specified (Note 6))

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OUT}	Output Voltage	V_{IN} = 2.5V, 1mA ≤ I_{OUT} ≤ 30mA		V_{OUT} *98.5%	1.2	V_{OUT} *101.5%	V
$I_{OUT(MAX)}$	Maximum Output Current	V_{IN} = 2.5V, V_{OUT} = 1.182V to 1.218V		600	—	—	mA
$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	Load Regulation	V_{IN} = 2.5V, 1mA ≤ I_{OUT} ≤ 600mA		-1	0.2	1	%/A
$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	Line Regulation	2.5V ≤ V_{IN} ≤ 6V, I_{OUT} = 30mA		-0.1	0.02	0.1	%/V
V_{DROP}	Dropout Voltage	I_{OUT} = 10mA		—	1000	1300	mV
		I_{OUT} = 300mA		—	1000	1300	
		I_{OUT} = 600mA		—	1000	1300	
I_Q	Quiescent Current	V_{IN} = 2.5V, I_{OUT} = 0mA		—	55	80	µA
I_{STD}	Standby Current	V_{IN} = 2.5V, V_{EN} in OFF mode		—	0.01	1.0	µA
PSRR	Power Supply Rejection Ratio	Ripple 0.5Vp-p V_{IN} = 2.5V, I_{OUT} = 100mA	f = 100Hz	—	65	—	dB
			f = 1kHz	—	65	—	
$(\Delta V_{OUT}/V_{OUT})/\Delta T$	Output Voltage Temperature Coefficient	I_{OUT} = 30mA T_A = -40°C to +85°C		—	±100	—	ppm/°C
I_{SHORT}	Short Current Limit	V_{OUT} = 0V		—	50	—	mA
V_{NOISE}	RMS Output Noise	No Load, 10Hz ≤ f ≤ 100kHz		—	50	—	μV_{RMS}
V_{IH}	V_{EN} High Voltage	Enable logic high, regulator on		1.5	—	6.0	V
V_{IL}	V_{EN} Low Voltage	Enable logic low, regulator off		0	—	0.4	
t_S	Start-up Time	No Load		—	20	—	µs
R_{PD}	EN Pull Down Resistor	—		—	3.0	—	MΩ
R_{DCHG}	V_{OUT} Discharge Resistor	Set EN pin at Low		—	60	—	Ω
T_{OTSD}	Thermal Shutdown Temperature	—		—	+160	—	°C
T_{HYOTSD}	Thermal Shutdown Hysteresis	—		—	+25	—	
θ_{JC}	Thermal Resistance (Junction to Case)	SOT25		—	96	—	°C/W
		SO-8		—	75	—	
		SOT89-5		—	47	—	

Note 6: Production testing at T_A = +25°C. Over temperature specifications guaranteed by design only.

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Electrical Characteristics (Cont.)

AP2112-1.8 Electrical Characteristics (@V_{IN} = 2.8V, C_{IN} = 1.0µF (Ceramic), C_{OUT} = 1.0µF (Ceramic), Typical T_A = +25°C, unless otherwise specified (Note 6))

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OUT}	Output Voltage	V_{IN} = 2.8V, 1mA ≤ I_{OUT} ≤ 30mA		V_{OUT} *98.5%	1.8	V_{OUT} *101.5%	V
$I_{OUT(MAX)}$	Maximum Output Current	V_{IN} = 2.8V, V_{OUT} = 1.773V to 1.827V		600	—	—	mA
$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	Load Regulation	V_{OUT} = 1.8V, V_{IN} = V_{OUT}+1V, 1mA ≤ I_{OUT} ≤ 600mA		-1	0.2	1	%/A
$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	Line Regulation	2.8V ≤ V_{IN} ≤ 6V, I_{OUT} = 30mA		-0.1	0.02	0.1	%/V
V_{DROP}	Dropout Voltage	I_{OUT} = 10mA		—	500	700	mV
		I_{OUT} = 300mA		—	500	700	
		I_{OUT} = 600mA		—	500	700	
I_Q	Quiescent Current	V_{IN} = 2.8V, I_{OUT} = 0mA		—	55	80	µA
I_{STD}	Standby Current	V_{IN} = 2.8V, V_{EN} in OFF mode		—	0.01	1.0	µA
PSRR	Power Supply Rejection Ratio	Ripple 0.5Vp-p V_{IN} = 2.8V, I_{OUT} = 100mA	f = 100Hz	—	65	—	dB
			f = 1kHz	—	65	—	
$(\Delta V_{OUT}/V_{OUT})/\Delta T$	Output Voltage Temperature Coefficient	I_{OUT} = 30mA T_A = -40°C to +85°C		—	±100	—	ppm/°C
I_{SHORT}	Short Current Limit	V_{OUT} = 0V		—	50	—	mA
V_{NOISE}	RMS Output Noise	No Load, 10Hz ≤ f ≤ 100kHz		—	50	—	μV_{RMS}
V_{IH}	V_{EN} High Voltage	Enable logic high, regulator on		1.5	—	6.0	V
V_{IL}	V_{EN} Low Voltage	Enable logic low, regulator off		0	—	0.4	
t_S	Start-up Time	No Load		—	20	—	µs
R_{PD}	EN Pull Down Resistor	—		—	3.0	—	MΩ
R_{DCHG}	V_{OUT} Discharge Resistor	Set EN pin at Low		—	60	—	Ω
T_{OTSD}	Thermal Shutdown Temperature	—		—	+160	—	°C
T_{HYOTSD}	Thermal Shutdown Hysteresis	—		—	+25	—	
θ_{JC}	Thermal Resistance (Junction to Case)	SOT25		—	96	—	°C/W
		SO-8		—	75	—	
		SOT89-5		—	47	—	

Note 6: Production testing at T_A = +25°C. Over temperature specifications guaranteed by design only.

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Electrical Characteristics (Cont.)

AP2112-2.5 Electrical Characteristics (@V_{IN} = 3.5V, C_{IN} = 1.0µF (Ceramic), C_{OUT} = 1.0µF (Ceramic), Typical T_A = +25°C, unless otherwise specified (Note 6))

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OUT}	Output Voltage	V_{IN} = 3.5V, 1mA ≤ I_{OUT} ≤ 30mA		V_{OUT} *98.5%	2.5	V_{OUT} *101.5%	V
$I_{OUT(MAX)}$	Maximum Output Current	V_{IN} = 3.5V, V_{OUT} = 2.463V to 2.537V		600	—	—	mA
$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	Load Regulation	V_{OUT} = 2.5V, V_{IN} = V_{OUT}+1V, 1mA ≤ I_{OUT} ≤ 600mA		-1	0.2	1	%/A
$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	Line Regulation	3.5V ≤ V_{IN} ≤ 6V, I_{OUT} = 30mA		-0.1	0.02	0.1	%/V
V_{DROP}	Dropout Voltage	I_{OUT} = 10mA		—	5	8	mV
		I_{OUT} = 300mA		—	125	200	
		I_{OUT} = 600mA		—	250	400	
I_Q	Quiescent Current	V_{IN} = 3.5V, I_{OUT} = 0mA		—	55	80	µA
I_{STD}	Standby Current	V_{IN} = 3.5V, V_{EN} in OFF mode		—	0.01	1.0	µA
PSRR	Power Supply Rejection Ratio	Ripple 0.5Vp-p, V_{IN} = 3.5V, I_{OUT} = 100mA	f = 100Hz	—	65	—	dB
			f = 1KHz	—	65	—	
$(\Delta V_{OUT}/V_{OUT})/\Delta T$	Output Voltage Temperature Coefficient	I_{OUT} = 30mA, T_A = -40°C to +85°C		—	±100	—	ppm/°C
I_{SHORT}	Short Current Limit	V_{OUT} = 0V		—	50	—	mA
V_{NOISE}	RMS Output Noise	No Load, 10Hz ≤ f ≤ 100kHz		—	50	—	μV_{RMS}
V_{IH}	V_{EN} High Voltage	Enable logic high, regulator on		1.5	—	6.0	V
V_{IL}	V_{EN} Low Voltage	Enable logic low, regulator off		0	—	0.4	
t_S	Start-up Time	No Load		—	20	—	µs
R_{PD}	EN Pull Down Resistor	—		—	3.0	—	MΩ
R_{DCHG}	V_{OUT} Discharge Resistor	Set EN pin at Low		—	60	—	Ω
T_{OTSD}	Thermal Shutdown Temperature	—		—	+160	—	°C
T_{HYOTSD}	Thermal Shutdown Hysteresis	—		—	+25	—	
θ_{JC}	Thermal Resistance (Junction to Case)	SOT25		—	96	—	°C/W
		SO-8		—	75	—	
		SOT89-5		—	47	—	

Note 6: Production testing at T_A = +25°C. Over temperature specifications guaranteed by design only.

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Electrical Characteristics (Cont.)

AP2112-2.6 Electrical Characteristics (@V_{IN} = 3.6V, C_{IN} = 1.0µF (Ceramic), C_{OUT} = 1.0µF (Ceramic), Typical T_A = +25°C, unless otherwise specified (Note 6))

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OUT}	Output Voltage	V_{IN} = 3.6V, 1mA ≤ I_{OUT} ≤ 30mA		V_{OUT} *98.5%	2.6	V_{OUT} *101.5%	V
$I_{OUT(MAX)}$	Maximum Output Current	V_{IN} = 3.6V, V_{OUT} = 2.561V to 2.639V		600	—	—	mA
$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	Load Regulation	V_{OUT} = 2.6V, V_{IN} = V_{OUT}+1V, 1mA ≤ I_{OUT} ≤ 600mA		-1	0.2	1	%/A
$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	Line Regulation	3.6V ≤ V_{IN} ≤ 6V, I_{OUT} = 30mA		-0.1	0.02	0.1	%/V
V_{DROP}	Dropout Voltage	I_{OUT} = 10mA		—	5	8	mV
		I_{OUT} = 300mA		—	125	200	
		I_{OUT} = 600mA		—	250	400	
I_Q	Quiescent Current	V_{IN} = 3.6V, I_{OUT} = 0mA		—	55	80	µA
I_{STD}	Standby Current	V_{IN} = 3.6V, V_{EN} in OFF mode		—	0.01	1.0	µA
PSRR	Power Supply Rejection Ratio	Ripple 0.5Vp-p, V_{IN} = 3.6V, I_{OUT} = 100mA	f = 100Hz	—	65	—	dB
			f = 1kHz	—	65	—	
$(\Delta V_{OUT}/V_{OUT})/\Delta T$	Output Voltage Temperature Coefficient	I_{OUT} = 30mA, T_A = -40°C to +85°C		—	±100	—	ppm/°C
I_{SHORT}	Short Current Limit	V_{OUT} = 0V		—	50	—	mA
V_{NOISE}	RMS Output Noise	No Load, 10Hz ≤ f ≤ 100kHz		—	50	—	μV_{RMS}
V_{IH}	V_{EN} High Voltage	Enable logic high, regulator on		1.5	—	6.0	V
V_{IL}	V_{EN} Low Voltage	Enable logic low, regulator off		0	—	0.4	
t_S	Start-up Time	No Load		—	20	—	µs
R_{PD}	EN Pull Down Resistor	—		—	3.0	—	MΩ
R_{DCHG}	V_{OUT} Discharge Resistor	Set EN pin at Low		—	60	—	Ω
T_{OTSD}	Thermal Shutdown Temperature	—		—	+160	—	°C
T_{HYOTSD}	Thermal Shutdown Hysteresis	—		—	+25	—	
θ_{JC}	Thermal Resistance (Junction to Case)	SOT25		—	96	—	°C/W
		SO-8		—	75	—	
		SOT89-5		—	47	—	

Note 6: Production testing at T_A = +25°C. Over temperature specifications guaranteed by design only.

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Electrical Characteristics (Cont.)

AP2112-3.3 Electrical Characteristics (@V_{IN} = 4.3V, C_{IN} = 1.0µF (Ceramic), C_{OUT} = 1.0µF (Ceramic), Typical T_A = +25°C, unless otherwise specified (Note 6))

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OUT}	Output Voltage	V_{IN} = 4.3V, 1mA ≤ I_{OUT} ≤ 30mA		V_{OUT} *98.5%	3.3	V_{OUT} *101.5%	V
$I_{OUT(MAX)}$	Maximum Output Current	V_{IN} = 4.3V, V_{OUT} = 3.251V to 3.350V		600	—	—	mA
$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	Load Regulation	V_{IN} = 4.3V, 1mA ≤ I_{OUT} ≤ 600mA		-1	0.2	1	%/A
$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	Line Regulation	4.3V≤ V_{IN} ≤ 6V, I_{OUT} = 30mA		-0.1	0.02	0.1	%/V
V_{DROP}	Dropout Voltage	I_{OUT} = 10mA		—	5	8	mV
		I_{OUT} = 300mA		—	125	200	
		I_{OUT} = 600mA		—	250	400	
I_Q	Quiescent Current	V_{IN} = 4.3V, I_{OUT} = 0mA		—	55	80	µA
I_{STD}	Standby Current	V_{IN} = 4.3V, V_{EN} in OFF mode		—	0.01	1.0	µA
PSRR	Power Supply Rejection Ratio	Ripple 0.5Vp-p V_{IN} = 4.3V, I_{OUT} = 100mA	f = 100Hz	—	65	—	dB
			f = 1kHz	—	65	—	
$(\Delta V_{OUT}/V_{OUT})/\Delta T$	Output Voltage Temperature Coefficient	I_{OUT} = 30mA T_A = -40°C to +85°C		—	±100	—	ppm/°C
I_{SHORT}	Short Current Limit	V_{OUT} = 0V		—	50	—	mA
V_{NOISE}	RMS Output Noise	No Load, 10Hz ≤ f ≤ 100kHz		—	50	—	μV_{RMS}
V_{IH}	V_{EN} High Voltage	Enable logic high, regulator on		1.5	—	6.0	V
V_{IL}	V_{EN} Low Voltage	Enable logic low, regulator off		0	—	0.4	
t_S	Start-up Time	No Load		—	20	—	µs
R_{PD}	EN Pull Down Resistor	—		—	3.0	—	MΩ
R_{DCHG}	V_{OUT} Discharge Resistor	Set EN pin at Low		—	60	—	Ω
T_{OTSD}	Thermal Shutdown Temperature	—		—	+160	—	°C
T_{HYOTSD}	Thermal Shutdown Hysteresis	—		—	+25	—	
θ_{JC}	Thermal Resistance (Junction to Case)	SOT25		—	96	—	°C/W
		SO-8		—	75	—	
		SOT89-5		—	47	—	

Note 6: Production testing at T_A = +25°C. Over temperature specifications guaranteed by design only.

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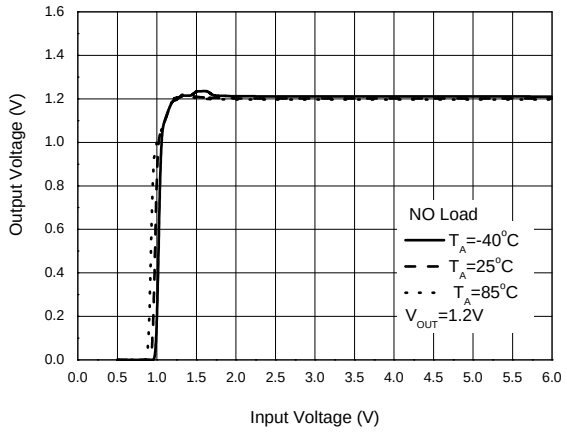
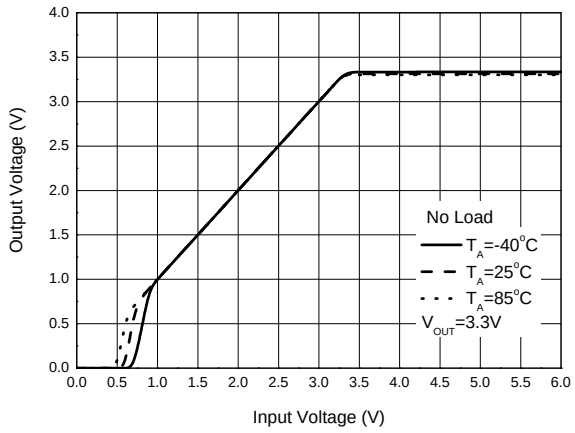
Performance Characteristics

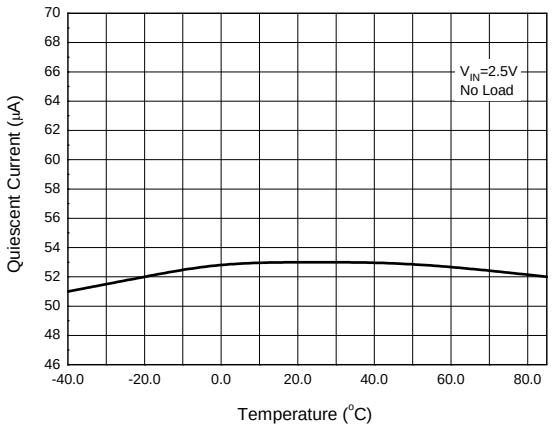
Output Voltage vs. Input Voltage



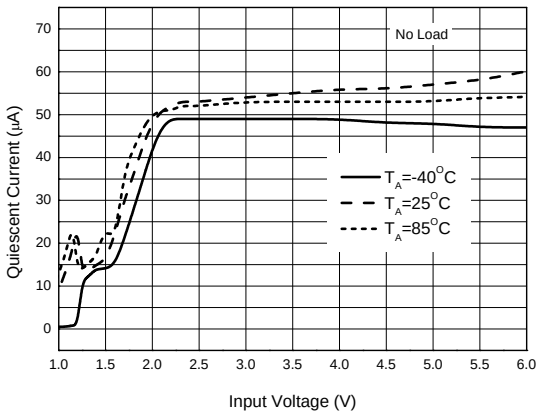
Output Voltage vs. Input Voltage



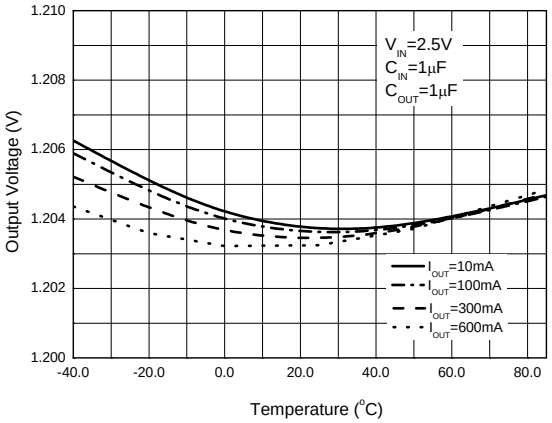
Quiescent Current vs. Temperature



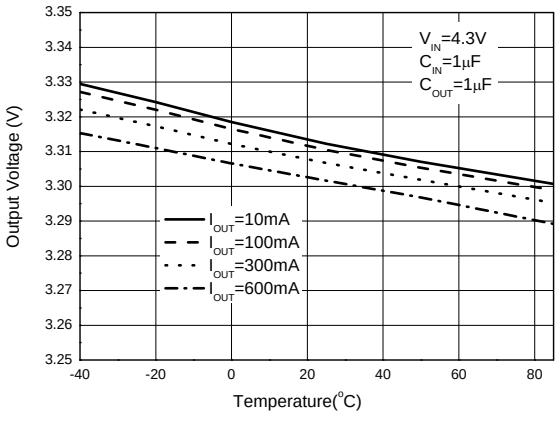
Quiescent Current vs. Input Voltage



Output Voltage vs. Temperature



Output Voltage vs. Temperature



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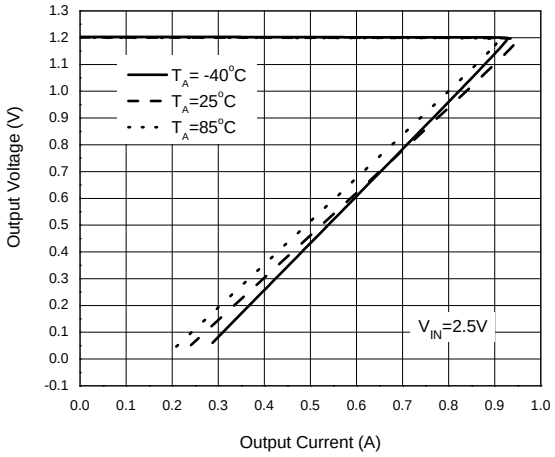
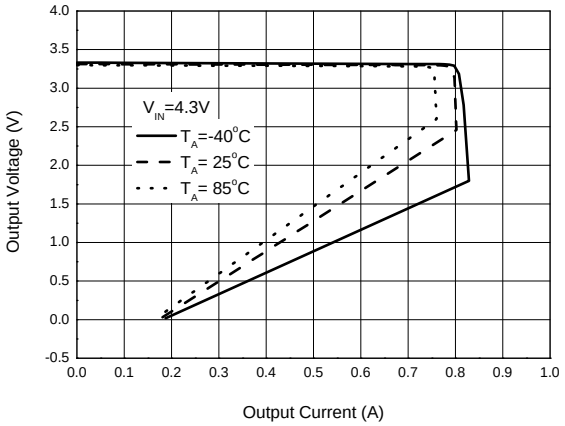
Performance Characteristics (Cont.)

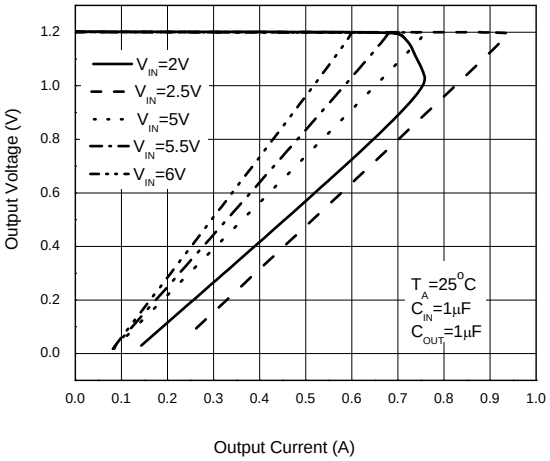
Output Voltage vs. Output Current



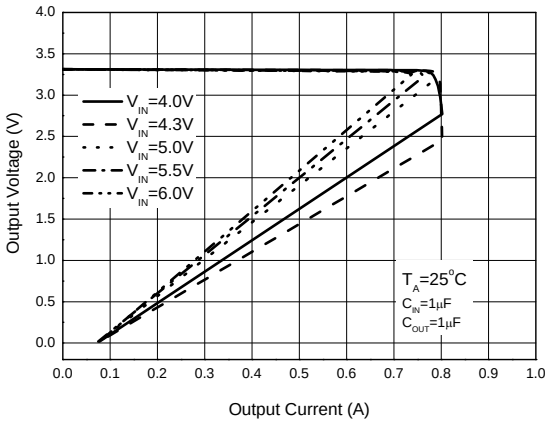
Output Voltage vs. Output Current



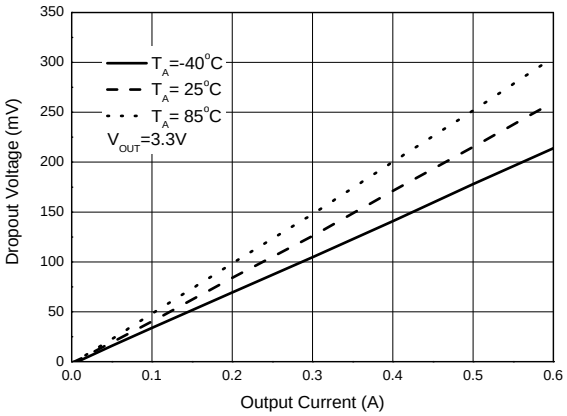
Output Voltage vs. Output Current



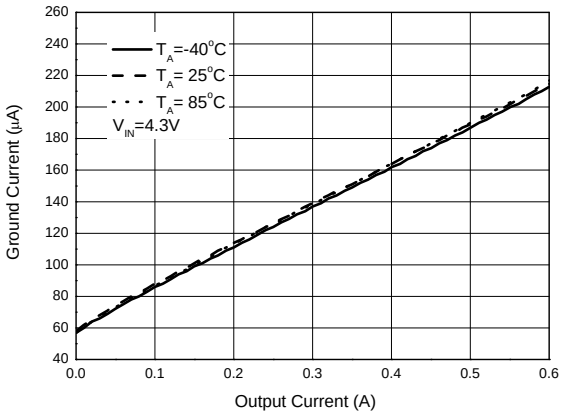
Output Voltage vs. Output Current



Dropout Voltage vs. Output Current



Ground Current vs. Output Current



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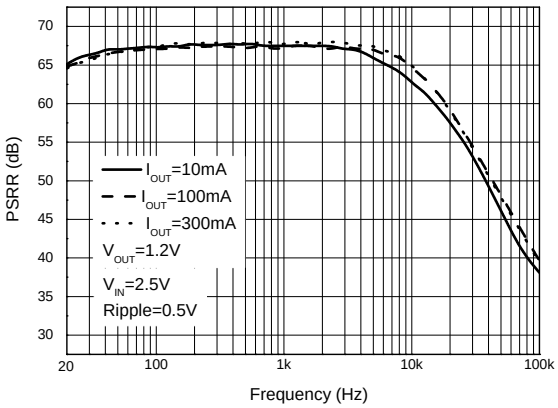
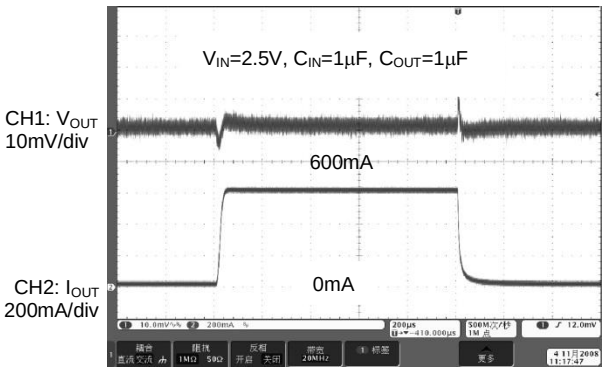
Performance Characteristics (Cont.)

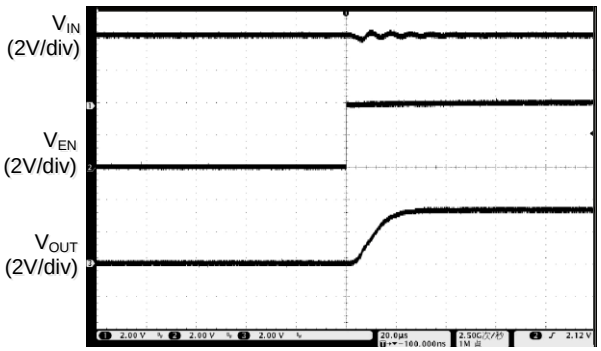
PSRR vs. Frequency



Load Transient

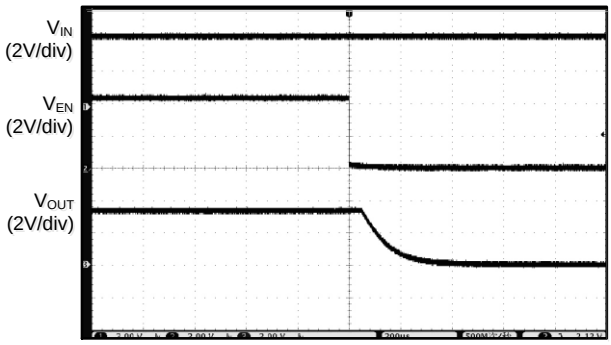


Enable On



20μs/div

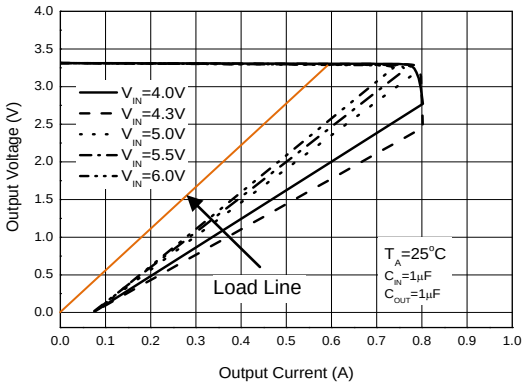
Enable Off



200μs/div

Application Note

In some unusual applications where a current load could be present at the output before the part is enabled the fold back current limiting may prevent the part from starting. Applications with multiple supplies or negative supplies need to be evaluated for this possibility. Product testing where a current source is applied before the part is enabled could be another area of concern. With a normal load as shown below there is no interference of the fold back current limiting circuit.



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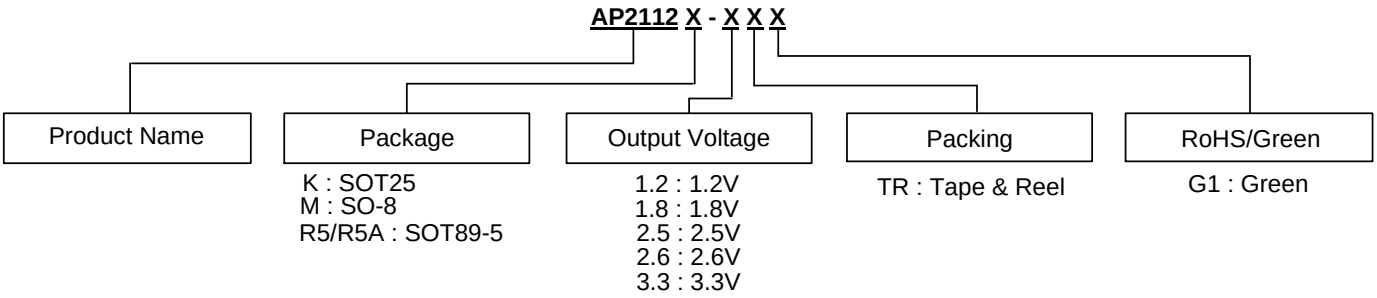
Ordering Information



Package	Temperature Range	Condition	Part Number	Marking ID	Packing
SOT25	-40 to +85°C	1.2V	AP2112K-1.2TRG1	G3L	3000/7”/Tape & Reel
		1.8V	AP2112K-1.8TRG1	G3M	3000/7”/Tape & Reel
		2.5V	AP2112K-2.5TRG1	G3N	3000/7”/Tape & Reel
		2.6V	AP2112K-2.6TRG1	G5N	3000/7”/Tape & Reel
		3.3V	AP2112K-3.3TRG1	G3P	3000/7”/Tape & Reel
SO-8	-40 to +85°C	1.2V	AP2112M-1.2TRG1	2112M-1.2G1	4000/13”/Tape & Reel
		1.8V	AP2112M-1.8TRG1	2112M-1.8G1	4000/13”/Tape & Reel
		2.5V	AP2112M-2.5TRG1	2112M-2.5G1	4000/13”/Tape & Reel
		2.6V	AP2112M-2.6TRG1	2112M-2.6G1	4000/13”/Tape & Reel
		3.3V	AP2112M-3.3TRG1	2112M-3.3G1	4000/13”/Tape & Reel
SOT89-5	-40 to +85°C	1.2V(R5)	AP2112R5-1.2TRG1	G37D	1000/7”/Tape & Reel
		1.8V(R5)	AP2112R5-1.8TRG1	G37E	1000/7”/Tape & Reel
		2.5V(R5)	AP2112R5-2.5TRG1	G37F	1000/7”/Tape & Reel
		2.6V(R5)	AP2112R5-2.6TRG1	G13F	1000/7”/Tape & Reel
		3.3V(R5)	AP2112R5-3.3TRG1	G37G	1000/7”/Tape & Reel
SOT89-5	-40 to +85°C	1.2V(R5A)	AP2112R5A-1.2TRG1	G33C	1000/7”/Tape & Reel
		1.8V(R5A)	AP2112R5A-1.8TRG1	G33E	1000/7”/Tape & Reel
		2.5V(R5A)	AP2112R5A-2.5TRG1	G28G	1000/7”/Tape & Reel
		2.6V(R5A)	AP2112R5A-2.6TRG1	G13E	1000/7”/Tape & Reel
		3.3V(R5A)	AP2112R5A-3.3TRG1	G28H	1000/7”/Tape & Reel

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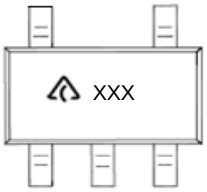
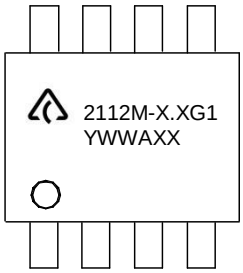
Marking Information

(1) SOT25



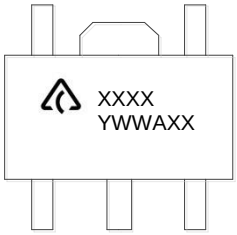
: Logo
XXX : Marking ID (See Ordering Information)

(2) SO-8



First line: Logo and Marking ID
Second line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch Number

(3) SOT89-5



First Line: Logo and Marking ID
Second line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch Number

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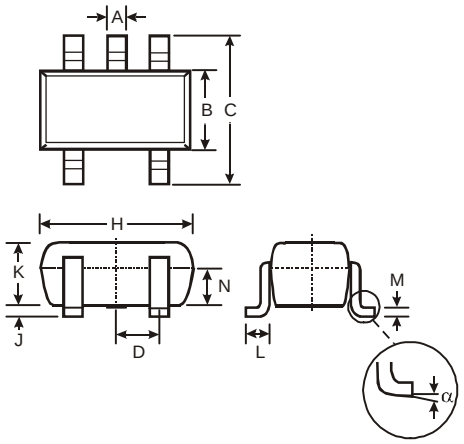
Package Outline Dimensions (Previously identified as SOT-23-5 for this product)

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT25

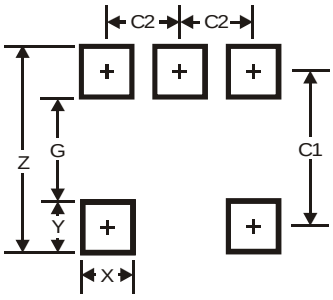


SOT25			
Dim	**Min**	**Max**	**Typ**
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	-	-	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT25



Dimensions	Value
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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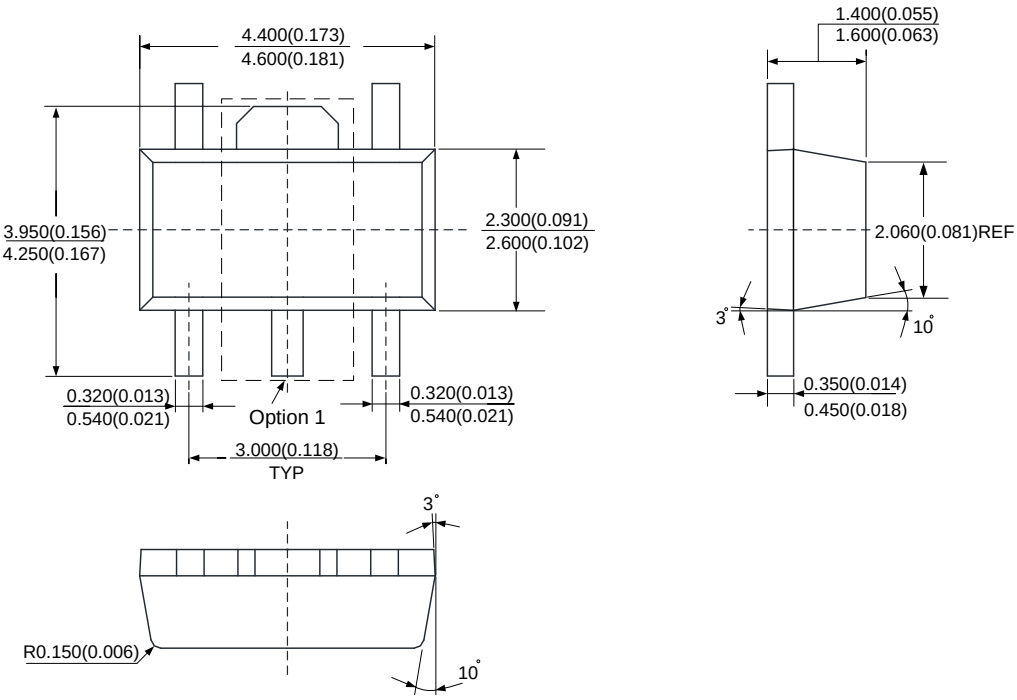
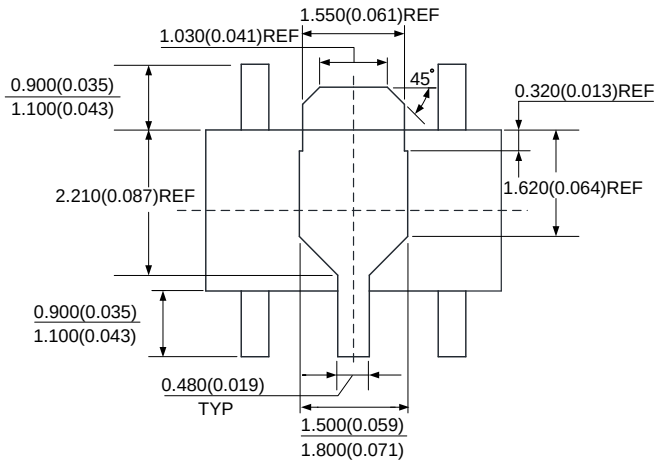
Package Outline Dimensions (All dimensions in mm.) (Previously identified as SOT-89-5 for this product)

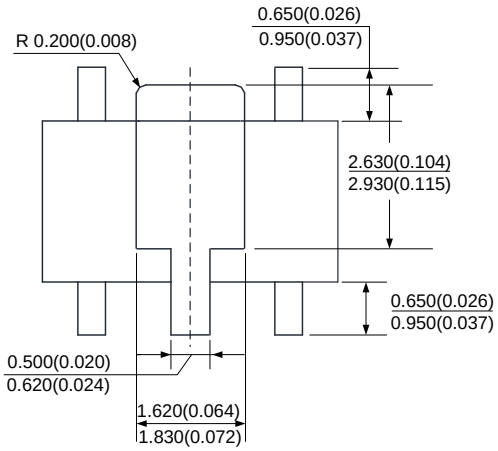
SOT89-5



Option 1



Option 2



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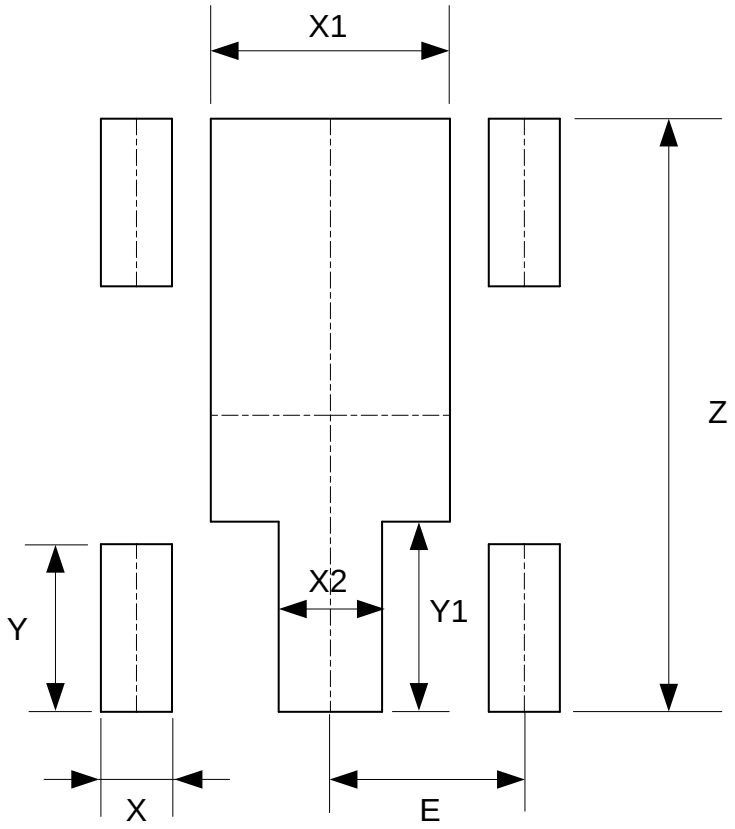
Suggested Pad Layout (Previously identified as SOT-89-5 for this product)

SOT89-5



Dimensions	Z (mm)/(inch)	X (mm)/(inch)	X1 (mm)/(inch)	X2 (mm)/(inch)	Y (mm)/(inch)	Y1 (mm)/(inch)	E (mm)/(inch)
Value	4.600/0.181	0.550/0.022	1.850/0.073	0.800/0.031	1.300/0.051	1.475/0.058	1.500/0.059

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Package Outline Dimensions (Previously identified as SOIC-8 for this product)

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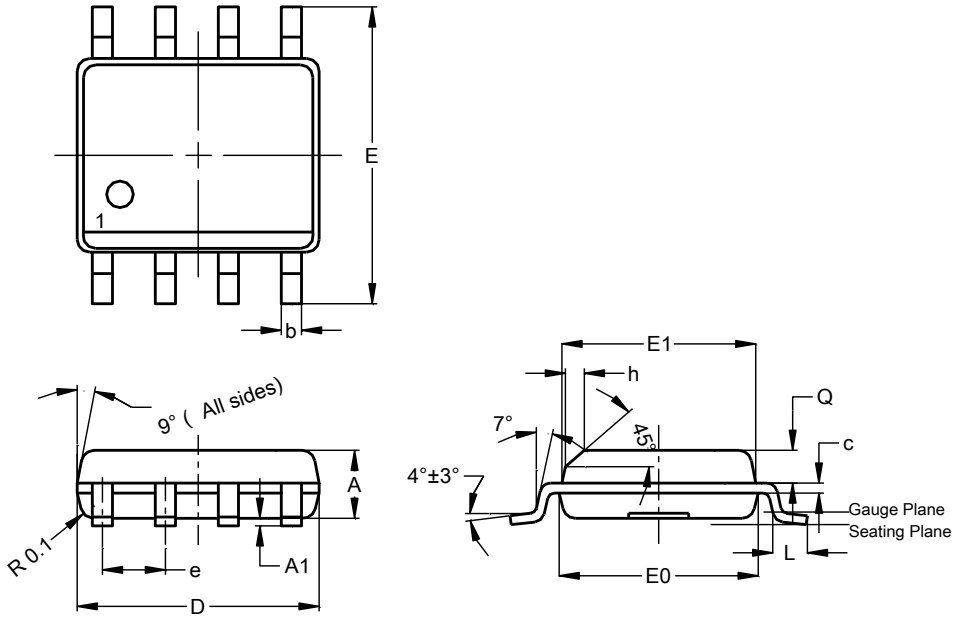
SO-8

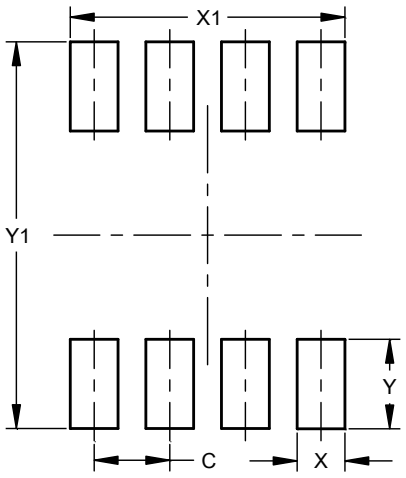


SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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