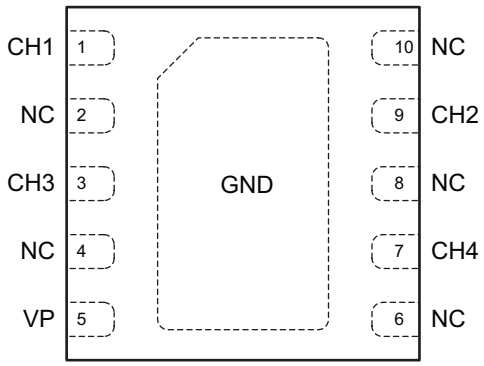
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8304ADI	-40 °C to +85 °C	2.6 mm x 2.6 mm DFN-10	Green Product

AOS Green Products (with "L" suffix) use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



DFN-10
(Top View)

Pin Number	Description
1, 3, 7, 9	Input/Output lines
2, 4, 6, 8, 10	No connection
5	VP
Center Tab	Ground

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VP – GND	3.3 V
Peak Pulse Current (I_{PP}), t_P = 8/20 µs	25 A
Peak Power Dissipation (8 x 20 µs@ 25 °C)	400 W
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating per IEC61000-4-2, Contact(1)	±30 kV
ESD Rating per IEC61000-4-2, Air(1)	±30 kV
ESD Rating per Human Body Model(2)	±30 kV

Notes:
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40 °C to +85 °C

Electrical Characteristics

T_A = 25°C unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40 °C to +85 °C.

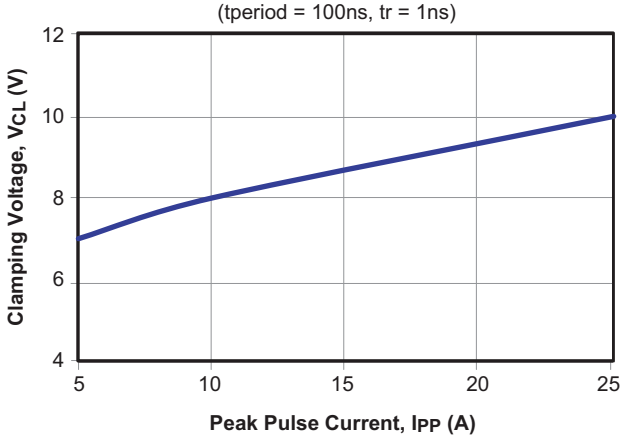
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Between pin 5 and GND[4]			3.3	V
I_R	Reverse Leakage Current	V_{RWM} = 3.3 V, between pins 5 and GND			**5**	µA
V_{BR}	Reverse Breakdown Voltage	V_{BR} = 1 mA	**3.5**		**5.6**	V
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 5 A, tp = 100 ns, any I/O pin to Ground[3][6][8]			 7.00 -3.00	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 10 A, tp = 100 ns, any I/O pin to Ground[3][6][8]			 8.00 -4.00	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 25 A, tp = 100 ns, any I/O pin to Ground[3][6][8]			 10.00 -5.00	 V V
C_j	Junction Capacitance	V_R = 0 V, f = 1 MHz, any I/O pin to Ground[3][7] V_R = 0 V, f = 1 MHz, between I/O pins[3][7]		 1.25	5 	pF pF
		V_R = 0 V, f = 1 MHz, any I/O pin to Ground[3][6] V_R = 0 V, f = 1 MHz, between I/O pins[3][6]		5 2.5	6 	pF pF

Notes:

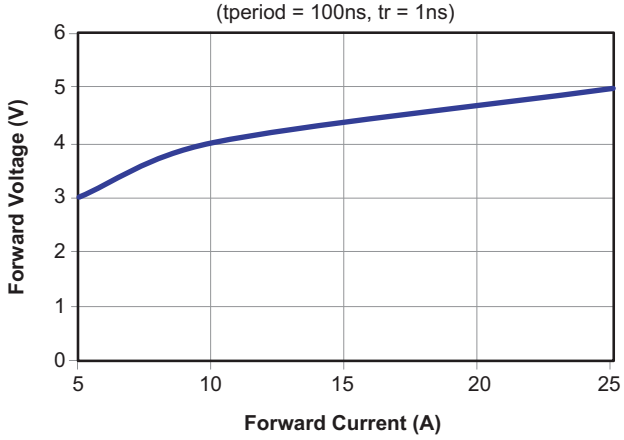
3. These specifications are guaranteed by design.
4. The working peak reverse voltage, V_{RWM}, should be equal to or greater than the DC or continuous peak operating voltage level.
5. V_{BR} is measured at the pulse test current I_T.
6. Measurements performed with no external capacitor on VP (pin 5 floating).
7. Measurements performed with VP biased to 3.3 Volts.
8. Measurements performed using a 100 ns Transmission Line Pulse (TLP) system.

Typical Performance Characteristics

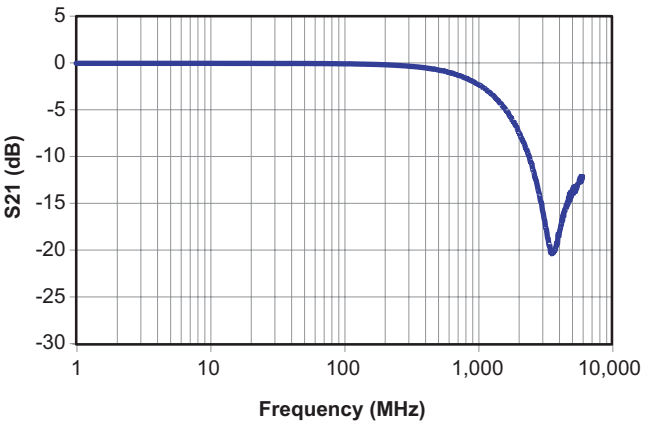
Clamping Voltage vs. Peak Pulse Current
(tperiod = 100ns, tr = 1ns)



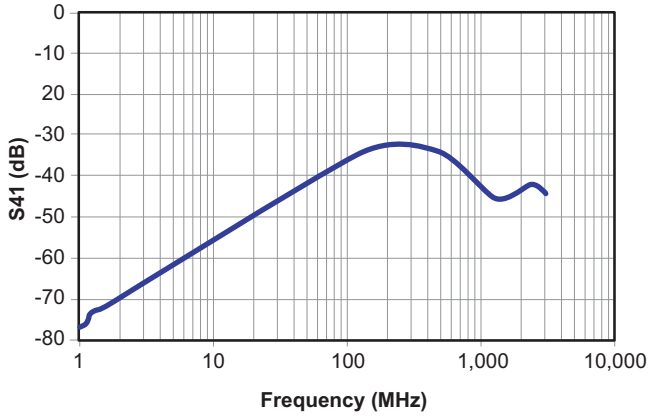
Forward Voltage vs. Forward Current
(tperiod = 100ns, tr = 1ns)



I/O – Gnd Insertion Loss (S21) vs. Frequency



Analog Crosstalk (I/O–I/O) vs. Frequency



Application Information

The AOZ8304A TVS is design to protect four data lines from fast damaging transient over-voltage by clamping the over-voltage to a reference. When the transient on a protected data line exceeds the reference voltage, the steering diode is forward bias and conducts harmful ESD transients away from the sensitive circuitry under protection.

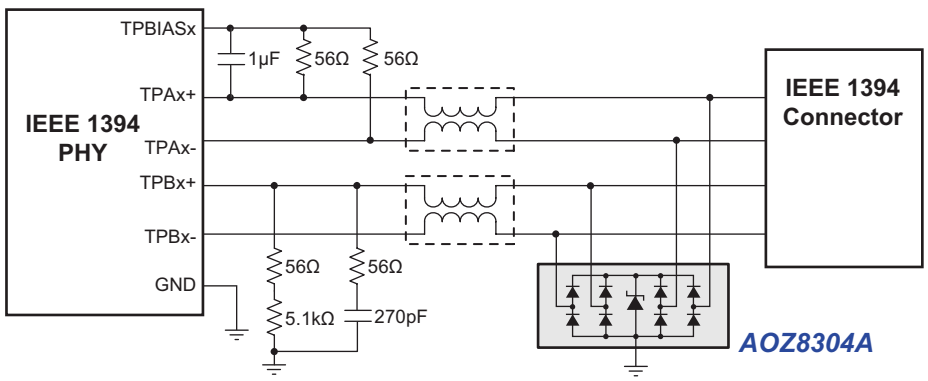
PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8304A devices should be located as close as possible to the noise source. The placement of the AOZ8304A devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8304A devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8304A device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced.

Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design. The AOZ8304A low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

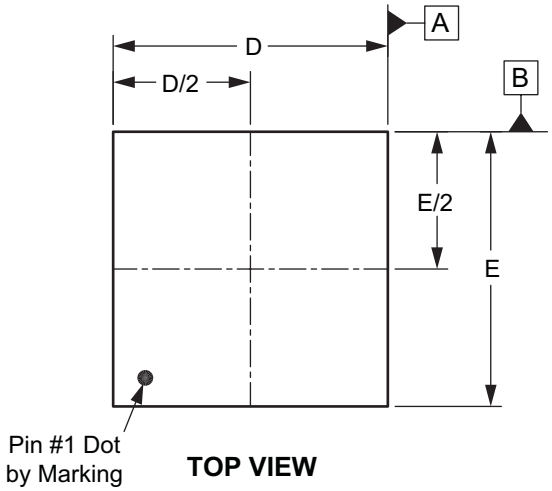
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the I/O terminals or connectors to restrict transient coupling.
2. Fill unused portions of the PCB with ground plane.
3. Minimize the path length between the TVS and the protected line.
4. Minimize all conductive loops including power and ground loops.
5. The ESD transient return path to ground should be kept as short as possible.
6. Never run critical signals near board edges.
7. Use ground planes whenever possible.
8. Avoid running critical signal traces (clocks, resets, etc.) near PCB edges.
9. Separate chassis ground traces from components and signal traces by at least 4 mm.
10. Keep the chassis ground trace length-to-width ratio < 5:1 to minimize inductance.
11. Protect all external connections with TVS diodes.

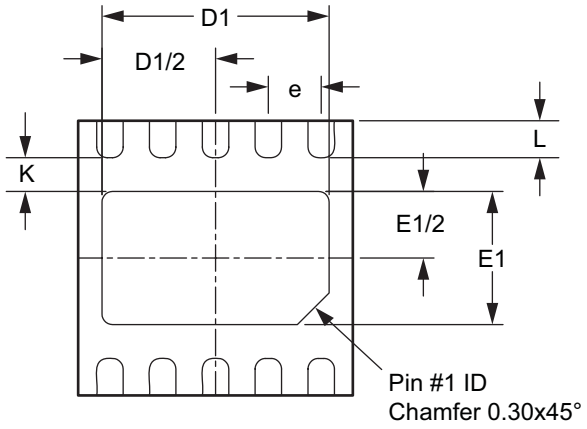


IEEE1394 Port Connection

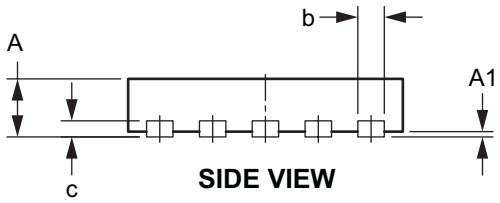
Package Dimensions, DFN 2.6 x 2.6, 10L



TOP VIEW



BOTTOM VIEW



SIDE VIEW

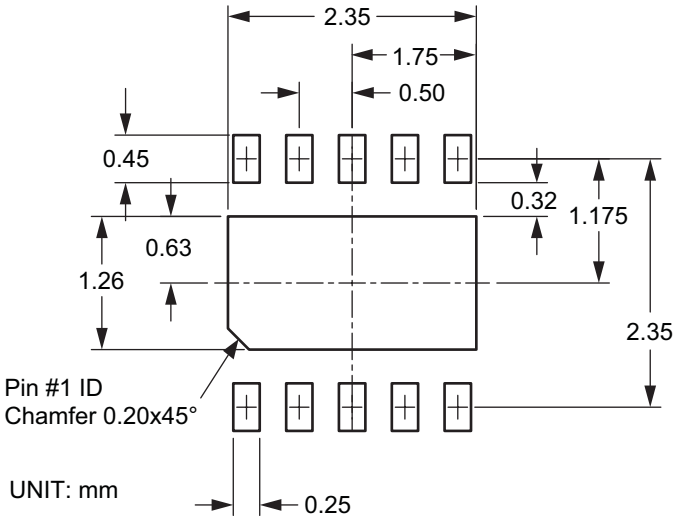
Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.00	—	0.05
b	0.20	0.25	0.30
c		0.152 REF.	
D	2.55	2.60	2.65
D1	2.10	2.15	2.20
E	2.55	2.60	2.65
E1	1.21	1.26	1.31
e		0.50 BSC	
K		0.32 REF	
L	0.30	0.35	0.40

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.020	0.022	0.024
A1	0.000	—	0.002
b	0.008	0.010	0.012
c		0.006 REF.	
D	0.100	0.102	0.104
D1	0.083	0.085	0.087
E	0.100	0.102	0.104
E1	0.048	0.050	0.052
e		0.050 BSC	
K		0.013 BSC	
L	0.012	0.014	0.016

RECOMMENDED LAND PATTERN

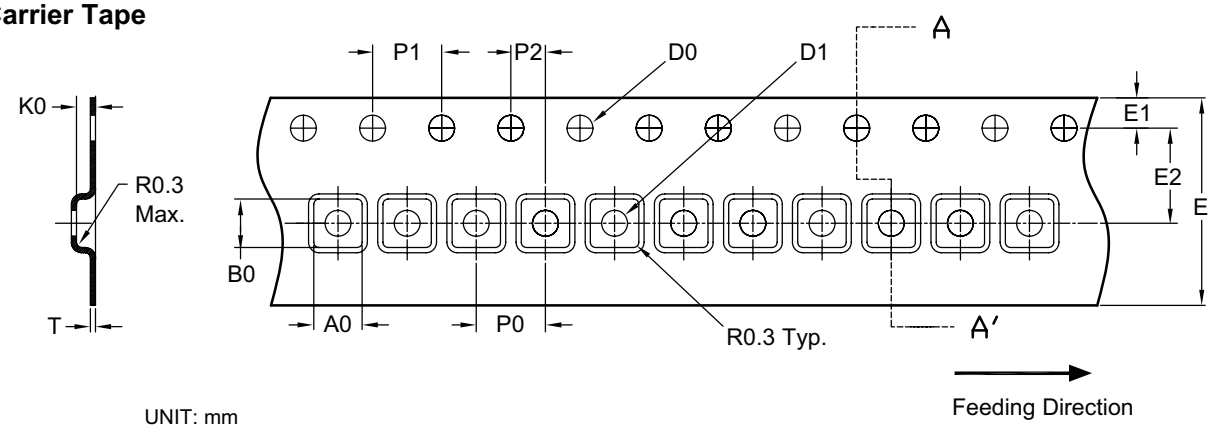


Note:

1. Controlling dimension is millimeter. Coverted inch dimensions are not necessarily exact

Tape and Reel Dimensions, DFN 2.6 x 2.6, 10L

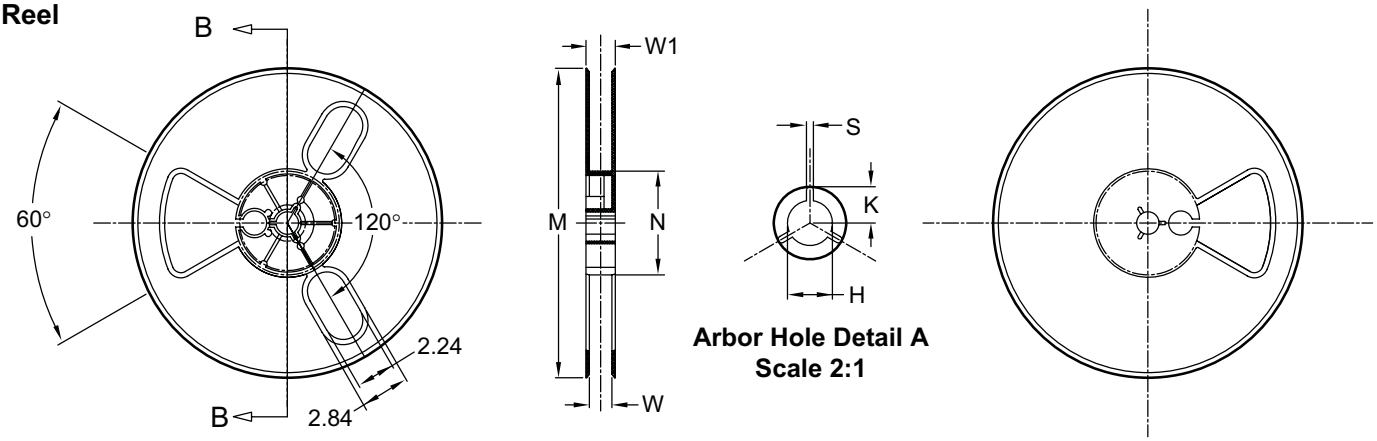
Carrier Tape



UNIT: mm

Package	T	B0	A0	K0	D0	D1	E	E1	E2	P0	P1	P2
DFN 2.6x2.6	0.30 ±0.05	2.80 ±0.10	2.80 ±0.10	1.10 ±0.10	ø1.50 +0.1/-0.0	ø1.50 Min.	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05

Reel

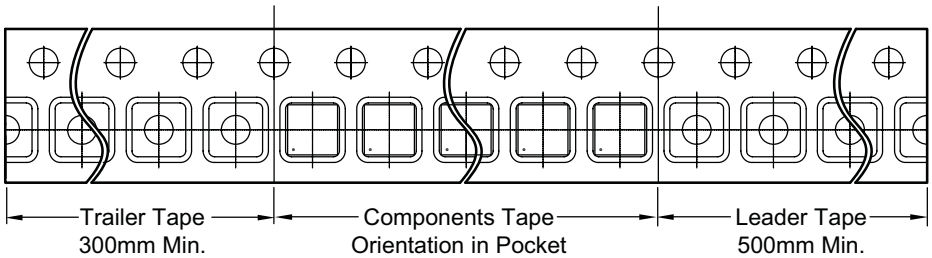


Back View | **Section B-B** | **Arbor Hole Detail A Scale 2:1** | **Front View**

UNIT: mm

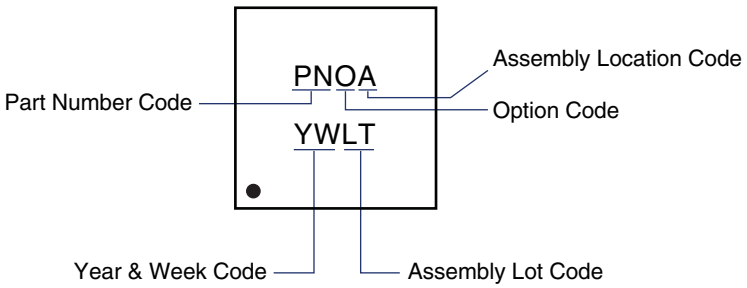
Tape Size	Reel Size	M	N	W	W1	H	K	S
12mm	ø180	ø179 ±1.0	60 ±0.5	13 ±0.5	17.0	ø13.0 ±0.2	10.5 ±0.25	2.0 ±0.2

Leader / Trailer & Orientation



Part Marking

AOZ8304ADI
(DFN-10)



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Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.