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REVISION HISTORY

8/12—Rev. 0 to Rev. A

Changed Storage Temperature from −65°C to +150°C to −40°C to +85°C 8

7/11—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

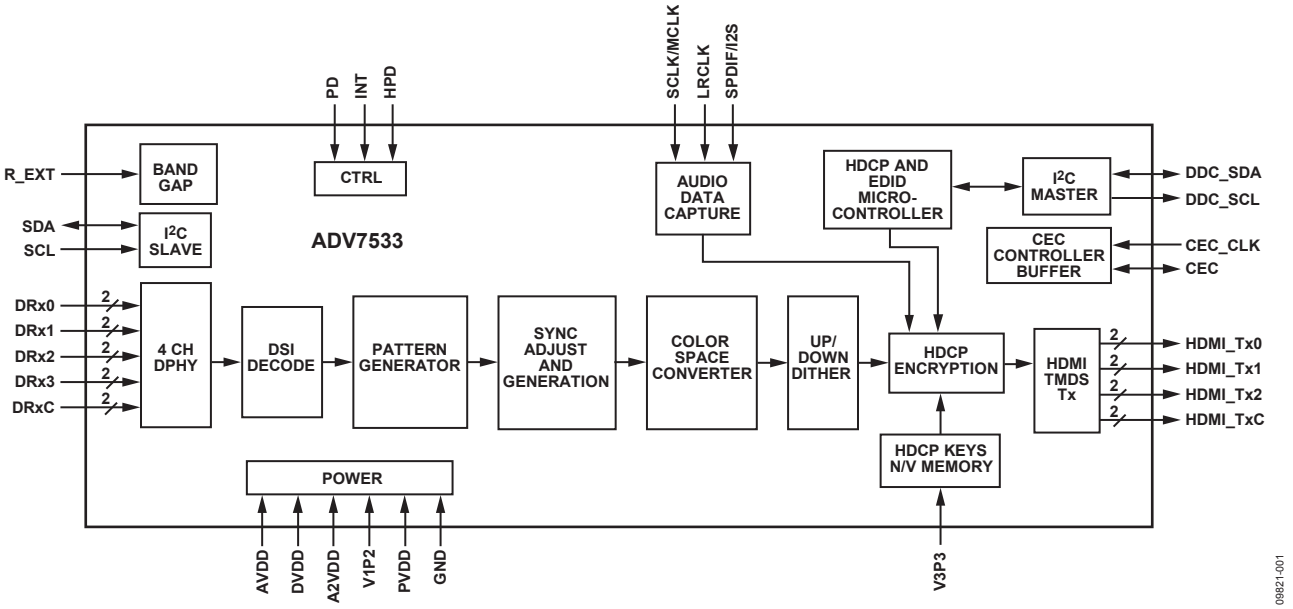

Figure 1.

SPECIFICATIONS

Table 1. Electrical Specifications

Parameter	Conditions	Temp	Test Level[1]	ADV7533BCBZ Min	Typ	Max	Unit
DIGITAL INPUTS							
Data Inputs—Audio, CEC_CLK							
Input Voltage, High (V_{IH})		Full	VI	1.4		3.5	V
Input Voltage, Low (V_{IL})		Full	VI	−0.3		+0.7	V
Input Capacitance		25°C	VIII		1.0	1.5	pF
I^2C Lines (SDA, SCL)							
Input Voltage, High (V_{IH})		Full	VI	1.3		5.5	V
Input Voltage, Low (V_{IL})		Full	VI	−0.3		+0.6	V
I^2C Lines (DDCSDA, DDCSCL)							
Input Voltage, High (V_{IH})	Default values	Full	VI	1.3		5.5	V
Input Voltage, Low (V_{IL})		Full	VI	−0.3		+0.6	V
Input Voltage, High (V_{IH})	Programmable optional values	Full	IV	3.5		5.5	V
Input Voltage, Low (V_{IL})		Full	IV	−0.5		+1.2	V
CEC							
Input Voltage, High (V_{IH})		Full	VI	2.0			V
Input Voltage, Low (V_{IL})		Full	VI			0.6	V
Output Voltage, High (V_{OH})		Full	VI	2.5		3.63	V
Output Voltage, Low (V_{OL})		Full	VI	−0.3		+0.6	V
HPD							
Input Voltage, High (V_{IH})		Full	VI	1.3		5.5	V
Input Voltage, Low (V_{IL})		Full	VI	−0.3		+0.6	V
DIGITAL OUTPUTS—INT							
Output Voltage, Low (V_{OL})	Load = 5 pF	Full	VI			0.4	V
THERMAL CHARACTERISTICS							
Thermal Resistance							
θ_{JC} Junction-to-Case		Full	V		20		°C/W
θ_{JA} Junction-to-Ambient		Full	V		43		°C/W
Ambient Temperature		Full	V	−10	+25	+85	°C
DC SPECIFICATIONS							
Input Leakage Current, I_{IL}		25°C	VI	−1		+1	µA
POWER SUPPLY							
1.8 V Supply Voltage (DV_{DD}, AV_{DD}, $A2V_{DD}$, PV_{DD})		Full	IV	1.71	1.8	1.9	V
V1P2 = (1.2 V)		Full	IV	1.14	1.2	1.26	V
V1P2 = (1.8 V)		Full	IV	1.71	1.8	1.9	V
Supply Voltage Noise Limit							
DVDD —Digital I/O Pad Logic		Full	IV			64	mV rms
AVDD—HDMI Analog Core		Full	IV			64	mV rms
V1P2—HDMI/DSI Digital Core							
1.2 V		Full	IV			43	mV rms
1.8 V		Full	Iv			64	mV rms
A2VDD—MIPI DPHY		Full	IV			64	mV rms
PVDD—HDMI PLL	Refer to Figure 2	Full	IV				mV rms
3.3 V Supply Voltage (V3P3)		Full	IV	3.15	3.30	3.45	V
3.3 V Supply Voltage Noise Limit		Full	IV			64	mV rms
Power-Down Current		25°C	VI		15		µA
Operating Current							
DVDD	I/O pads (30 bits at 720p)	Full	IV		6		mA

Parameter	Conditions	Temp	Test Level[1]	ADV7533BCBZ Min	Typ	Max	Unit
AVDD	HDMI analog core (24 bits at 720p)	Full	IV		11		mA
V1P2 (1.2 V)	HDMI/DSI digital core (DSI 30 bits/HDMI 24 bits at 720p)	Full	IV		39		mA
A2VDD	MIPI DPHY (30 bits/three lanes/720p)	Full	IV		12		mA
PVDD	HDMI PLL (24 bits at 720p)	Full	IV		11		mA
V3P3—HDMI/HDCP Memory	HDMI HDCP memory	Full	IV		0.3		mA
Transmitter Total Power	720p, 30-bit DSI in; 720p, 36-bit HDMI out; typical random pattern with CSC enabled, HDCP enabled, audio enabled						
V1P2 = 1.2 V		Full	IV		120	154	mW
V1P2 = 1.8 V		Full	VI			204	mW
AC SPECIFICATIONS							
TMDS Output Clock Frequency		25°C	IV	20		112	MHz
TMDS Output Clock Duty Cycle		25°C	IV	48		52	%
TMDS Differential Swing		25°C	VII	800	1000	1200	mV
Differential Output Timing							
Low-to-High Transition Time		25°C	VII	75	175		ps
High-to-Low Transition Time		25°C	VII	75	175		ps
AUDIO AC TIMING[2]							
SCLK Duty Cycle							
When N = Even Number		Full	IV	40	50	60	%
When N = Odd Number		Full	IV	49	50	51	%
I^2S, S/PDIF Setup, t_{ASU}		Full	IV	2			ns
I^2S, S/PDIF Hold Time, t_{AHLD}		Full	IV	2			ns
LRCLK Setup Time, t_{ASU}		Full	IV	2			ns
LRCLK Hold Time, t_{AHLD}		Full	IV	2			ns
CEC							
CEC_CLK Frequency[3]		Full	VIII	3	12	100	MHz
CEC_CLK Accuracy		Full	VIII	−2		+2	%
CEC_CLK Duty Cycle		Full	VIII	40		60	%
I^2C INTERFACE							
SCL Clock Frequency		Full	VIII			400[4]	kHz
SDA Setup Time, t_{DSU}		Full	VIII	100			ns
SDA Hold Time, t_{DHO}		Full	VIII	100			ns
Setup for Start, t_{STASU}		Full	VIII	0.6			µs
Hold Time for Start, t_{STAH}		Full	VIII	0.6			µs
Setup for Stop, t_{STOSU}		Full	VIII	0.6			µs
Bus Free Between Stop and Start, t_{BUF}		Full	VIII	1.3			µs
SCL High, t_{HIGH}		Full	VIII	0.6			µs
SCL Low, t_{LOW}		Full	VIII	1.3			µs

[1] See the Explanation of Test Levels section.
[2] 12 MHz crystal for default register settings.
[3] Only applies to S/PDIF if external MCLK is used.
[4] I^2C data rates of 100 KHz and 400 KHz are supported.

The power supply noise sensitivity of the ADV7533 is frequency dependent. Therefore, the maximum noise limit for the PVDD is specified in mV rms vs. frequency (see Figure 2).

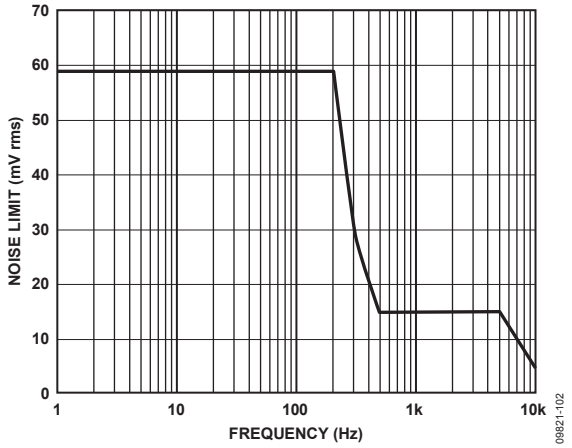

Figure 2. PVDD Maximum Noise Limit

MIPI/DSI SPECIFICATIONS

Unless noted, timing and levels comply with MIPI DPHY standards.

Table 2. DSI High Speed (HS) Specifications

				ADV7533			
Parameters	**Symbol**	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
DC SPECIFICATIONS							
DSI Input Common Mode Voltage	V_{CMRX}	25°C	VII	70		330	mV
DSI Input High Threshold	V_{IDTH}	25°C	VII			70	mV
DSI Input Low Threshold	V_{IDTL}	25°C	VII	−70			mV
DSI Single-Ended Input High Voltage	V_{IHHS}	25°C	VII			460	mV
DSI Single-Ended Input Low Voltage	V_{ILHS}	25°C	VII	−40			mV
DSI Single-Ended Threshold for Termination Enable	$V_{TERM-EN}$	25°C	VII			450	mV
Differential Input Impedance	Z_{ID}	25°C	VII	80	100	125	Ω
AC SPECIFICATIONS							
Single Channel Data Rate		25°C	IV	200		800	Mbps
Data to Clock Setup Time	t_{SETUP}	25°C	VII	0.15			UI_{INST}
Data to Clock Hold Time	t_{HOLD}	25°C	VII	0.15			UI_{INST}
DSI Clock Duty Cycle		25°C	VII	45	50	55	%
Common-Mode Interference Beyond 450 MHz	$\Delta V_{CMRX(HF)}$	25°C	VII			100	mV
Common-Mode Interference 50 MHz to 450 MHz	$\Delta V_{CMRX(LF)}$	25°C	VII	−50		+50	mV
Common-Mode Termination	C_{CM}	25°C	VII			60	pF

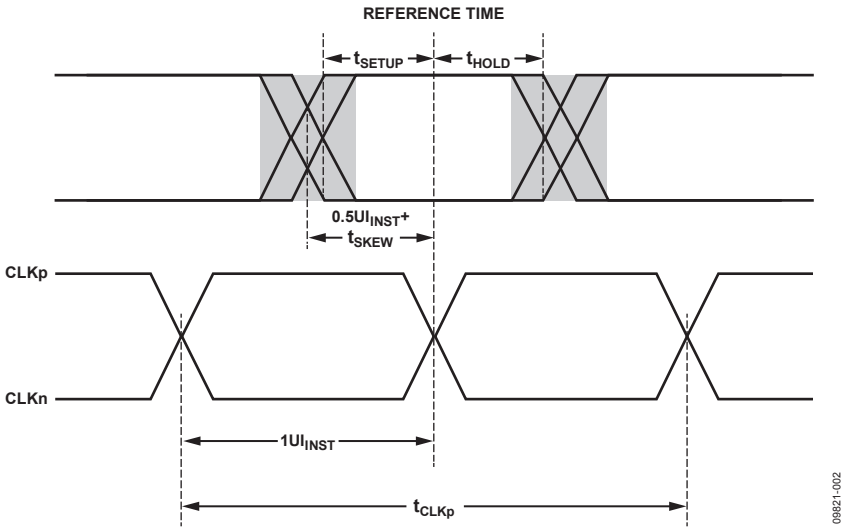

Figure 3. DSI Data to Clock Timing Definitions

Table 3. DSI Low Power Specifications

Parameter	Symbol	Temp	Test Level	Min	Typ	Max	Unit
DC SPECIFICATIONS							
Logic 1 Input Voltage	V_{IH}	25°C	VII	880			mV
Logic 0 Input Voltage, Not in ULP State	V_{IL}	25°C	VII			550	mV
Input Hysteresis	V_{HYST}	25°C	VII	25			mV
AC SPECIFICATIONS							
Input Pulse Rejection	E_{SPIKE}	25°C	VII			300	V × ps
Minimum Pulse Width Response	T_{MIN-RX}	25°C	VII	20			ns
Peak Interference Amplitude	V_{INT}	25°C	VII			200	mV
Interference Frequency	f_{INT}	25°C	VII	450			MHz

Table 4. DSI Pin Specifications

		ADV7533					
Parameter	Conditions	Temp	Test Level	Min	Typ	Max	Unit
DC SPECIFICATIONS							
Pin Signal Voltage Range	V_{PIN}	25°C	VII	−50		+1350	mV
Pin Leakage Current	I_{LEAK}	25°C	VII	−10		+10	µA
Ground Shift	V_{GNDSH}	25°C	VII	−50		+50	mV
Transient Pin Voltage Level	V_{PIN}(absmax)	25°C	VII	−0.15		+1.45	V
Maximum Transient Time Above V_{PIN} (Max) or Below V_{PIN} (Min)	T_{VPIN}(absmax)	25°C	VII			20	ns

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Digital Inputs—I²C (DDCSDA, DDCSCL, SDA, SCL) and HPD	5.5 V to −0.3 V
Digital Inputs—MIPI/DSI	1.8 V
Digital Inputs—Video/Audio Inputs, CEC_IO, CEC_CLK	3.63 V to −0.3 V
Digital Output Current	20 mA
Operating Temperature Range	−10°C to +85°C
Storage Temperature Range	−40°C to +85°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

EXPLANATION OF TEST LEVELS

I 100% production tested.
II 100% production tested at 25°C and sample tested at specified temperatures.
III Sample tested only.
IV Parameter is guaranteed by design and characterization testing.
V Parameter is a typical value only.
VI 100% production tested at 25°C; guaranteed by design and characterization testing.
VII Limits defined by HDMI specification; guaranteed by design and characterization testing.
VIII Parameter is guaranteed by design.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

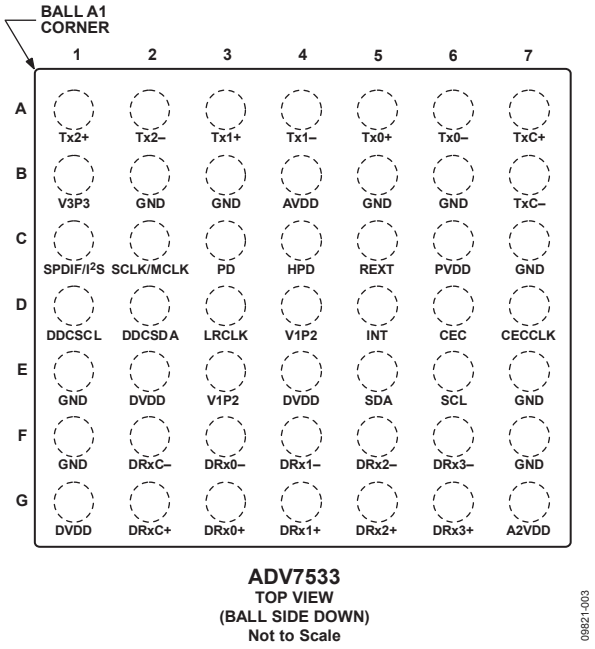

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
F6, G6	DRx3–/DRx3+	I	MIPI/DSI Differential Pair for Lane 3. Unused channel should be connected to ground.
F5, G5	DRx2–/DRx2+	I	MIPI/DSI Differential Pair for Lane 2. Unused channel should be connected to ground.
F4, G4	DRx1–/DRx1+	I	MIPI/DSI Differential Pair for Lane 1.
F3, G3	DRx0–/DRx0+	I	MIPI/DSI Differential Pair for Lane 0.
F2, G2	DRxC–/DRxC+	I	MIPI/DSI Differential Clock.
C3	PD	I	Power-Down. Programmable polarity is determined at power-up. The I^2C address and the PD polarity are set by the PD pin state when the supplies are applied to the ADV7533. Internally pulled up for 1; if 0 desired, pull down to ground with a 2 kΩ resistor. Supports typical CMOS logic levels from 1.8 V up to 3.3 V.
C5	R_EXT	I	Sets internal reference currents. Place a 1 KΩ resistor (1% tolerance) between this pin and ground.
C4	HPD	I	Hot Plug Detect Signal. Indicates to the interface whether the receiver is connected. 1.8 V to 5.0 V CMOS logic level.
C1	SPDIF/I2S	I	S/PDIF or I^2S Audio Data Input. Represents the S/PDIF block or the two channels of audio available through I^2S. Supports typical CMOS logic levels from1.8 V to 3.3 V.
C2	SCLK/MCLK	I	Audio Clock. Supports typical CMOS logic levels from1.8 V to 3.3 V. Unused input should be connected to ground.
D3	LRCLK	I	Audio Left/Right Clock Input. Supports typical CMOS logic levels from1.8 V to 3.3 V. Unused input should be connected to ground.
B7, A7	TxC–/TxC+	O	Differential Clock Output. Differential clock output at pixel clock rate; TMDS logic level.
A2, A1	Tx2–/Tx2+	O	Differential Output Channel 2. Differential output of the red data at 10× the pixel clock rate; TMDS logic level.
A4, A3	Tx1–/Tx1+	O	Differential Output Channel 1. Differential output of the green data at 10× the pixel clock rate; TMDS logic level.
A6, A5	Tx0–/Tx0+	O	Differential Output Channel 0. Differential output of the blue data at 10× the pixel clock rate; TMDS logic level.
D5	INT	O	Interrupt. CMOS logic level. A 2 kΩ pull-up resistor to interrupt the microcontroller I/O supply is recommended. This is a low active signal.
B4	AVDD	P	1.8 V Power Supply for TMDS Outputs. Should be filtered and as quiet as possible.
D4, E3	V1P2	P	Digital Logic Supply (1.2 V or 1.8 V). Set to 1.2 V for lowest power consumption. Should be filtered and as quiet as possible.

Pin No.	Mnemonic	Type[1]	Description
G7	A2VDD	P	1.8 V Power Supply for MIPI/DPHY Input. Should be filtered and as quiet as possible.
E2, E4, G1	DVDD	P	1.8 V Power Supply for Digital and I/O Power Supply. Supply power to the digital logic and I/Os. Should be filtered and as quiet as possible.
C6	PVDD	P	1.8 V Power Supply for the PLL. Should be filtered and as quiet as possible. This supply is the most noise sensitive.
B1	V3P3	P	3.3 V programming pin for HDCP nonvolatile memory.
B2, B3, B5, B6, C7, E1, E7, F1, F7	GND	P	Ground for all domains.
E5	SDA	C	Serial Port Data I/O. Serves as the serial port data I/O slave for register access. Supports CMOS logic levels from 1.8 V to 3.3 V.
E6	SCL	C	Serial Port Data Clock. Serves as the serial port data clock slave for register access. Supports CMOS logic levels from 1.8 V to 3.3 V.
D2	DDCSDA	C	Serial Port Data I/O to Receiver. Serves as the master to the DDC bus. 5 V CMOS logic level.
D1	DDCSCL	C	Serial Port Data Clock to Receiver. Serves as the master clock for the DDC bus. 5 V CMOS logic level.
D6	CEC	I/O	CEC I/O. If unused, pin should be connected to ground.
D7	CEC_CLK	I	CEC External Clock. Can be from 3 MHz to 100 MHz. Settings default to 12 MHz. If unused, pin should be connected to ground.

[1] I = input, O = output, P = power supply, C = control.

APPLICATIONS INFORMATION

DESIGN RESOURCES

Analog Devices, Inc., offers the following design resources:

- Evaluation kits
- Reference design schematics
- Hardware and software guides
- Software driver reference code
- HDMI compliance pretest services

Other support documentation is available under the nondisclosure agreement (NDA) from ATV_VideoTx_Apps@analog.com.

Other references include the following:

EIA/CEA-861E, which describes audio and video infoframes as well as the E-EDID structure for HDMI. It is available from the Consumer Electronics Association (CEA).

The HDMI v.1.3, the defining document for HDMI Version 1.3, and the HDMI Compliance Test Specification Version 1.3 are available from HDMI Licensing, LLC.

OUTLINE DIMENSIONS

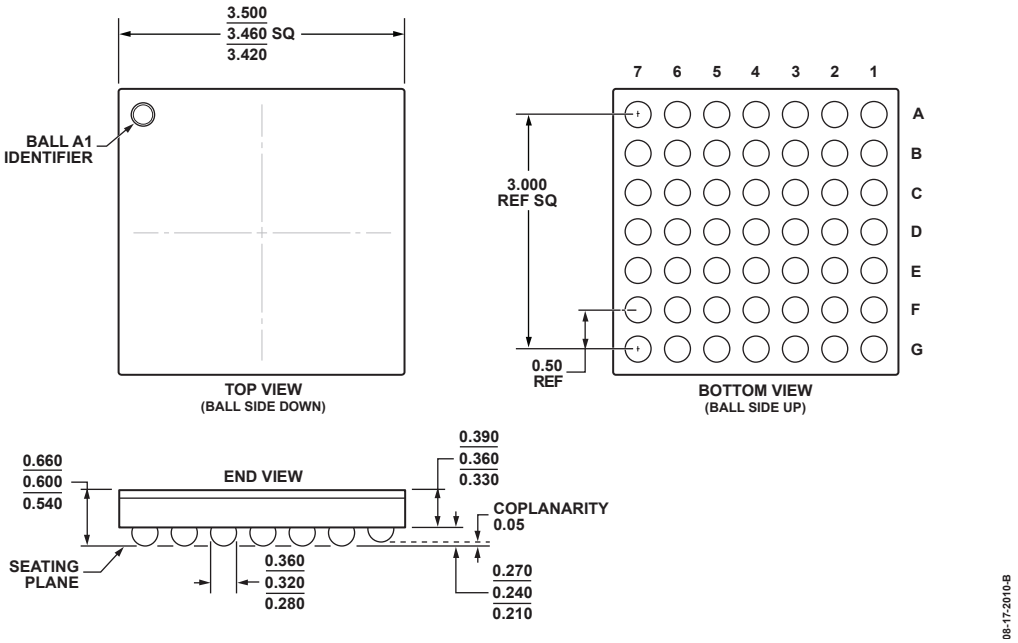

Figure 5. 49-Ball Wafer Level Chip Scale Package [WLCSP]
7 mm × 7 mm Body (CB-49-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADV7533BCBZ-RL	−10°C to +85°C	49-Ball Wafer Level Chip Scale Package [WLCSP]	CB-49-1
EVAL-ADV7533-SAZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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