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REVISION HISTORY

4/2004—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION

All voltages are relative to the respective ground; 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V; this does not apply to the ADuM1200W and ADuM1201W automotive grade products.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.60	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.25	mA	
ADuM1200 Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.1	1.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.3	5.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.3	2.0	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		10	13	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		2.8	3.4	mA	12.5 MHz logic signal freq.
ADuM1201 Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.8	1.1	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.8	1.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		2.8	3.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.8	3.5	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		6.3	8.0	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		6.3	8.0	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ (V_{DD1} or V_{DD2})
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1200/ADuM1201AR						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			1000	ns	
Maximum Data Rate[3]		1			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	50		150	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	
Change vs. Temperature			11		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			100	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		10		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM1200/ADuM1201BR						
Minimum Pulse Width[2]	PW			100	ns	
Maximum Data Rate[3]		10			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		50	ns	
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching				3		
Codirectional Channels[6]	t_{PSKCD}				ns	
Opposing Directional Channels[6]	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
ADuM1200/ADuM1201CR						
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		45	ns	
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching				3	ns	
Codirectional Channels[6]	t_{PSKCD}					
Opposing Directional Channels[6]	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output[7]	$\lvert CM_H \rvert$	25	35		kV/µs	$V_{Ix} = V_{DD1}$ or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\lvert CM_L \rvert$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Dynamic Supply Current per Channel[8]						
Input	$I_{DDI (D)}$		0.19		mA/Mbps	
Output	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1200 and ADuM1201 channel configurations.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V, 105°C OPERATION

All voltages are relative to the respective ground; 2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V; this does not apply to ADuM1200W and ADuM1201W automotive grade products.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.35	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.20	mA	
ADuM1200 Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.6	1.0	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.2	0.6	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		2.2	3.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		0.7	1.1	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		5.2	7.7	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		1.5	2.0	mA	12.5 MHz logic signal freq.
ADuM1201 Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.4	0.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.4	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		1.5	2.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.5	2.2	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		3.4	4.8	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		3.4	4.8	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ (V_{DD1} or V_{DD2})
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1200/ADuM1201AR						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			1000	ns	
Maximum Data Rate[3]		1			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	50		150	ns	
Pulse Width Distortion, $\|t_{PLH} − t_{PHL}\|$[4]	PWD			40	ns	
Change vs. Temperature			11		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			100	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		10		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM1200/ADuM1201BR						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			100	ns	
Maximum Data Rate[3]		10			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		60	ns	
Pulse Width Distortion, $\|t_{PLH} − t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			22	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			22	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	
ADuM1200/ADuM1201CR						
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		55	ns	
Pulse Width Distortion, $\|t_{PLH} − t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			16	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			16	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$ or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Dynamic Supply Current per Channel[8]						
Input	$I_{DDI (D)}$		0.10		mA/Mbps	
Output	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1200 and ADuM1201 channel configurations.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V, 105°C OPERATION

All voltages are relative to the respective ground; 5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V. 3 V/5 V operation: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5.0 V; or V_{DD1} = 5.0 V, V_{DD2} = 3.0 V; this does not apply to ADuM1200W and ADuM1201W automotive grade products.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions /Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$					
5 V/3 V Operation			0.50	0.6	mA	
3 V/5 V Operation			0.26	0.35	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$					
5 V/3 V Operation			0.11	0.20	mA	
3 V/5 V Operation			0.19	0.25	mA	
ADuM1200 Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.1	1.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.6	1.0	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.2	0.6	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.5	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			4.3	5.5	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.2	3.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			0.7	1.1	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.3	2.0	mA	5 MHz logic signal freq.
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$					
5 V/3 V Operation			10	13	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			5.2	7.7	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$					
5 V/3 V Operation			1.5	2.0	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			2.8	3.4	mA	12.5 MHz logic signal freq.
ADuM1201 Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			0.8	1.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.4	0.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.4	0.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.8	1.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BR and CR Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			2.8	3.5	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.5	2.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			1.5	2.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.8	3.5	mA	5 MHz logic signal freq.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions /Comments
25 Mbps (CR Grade Only)						
V_{DD1} Supply Current	$I_{DD1\ (25)}$					
5 V/3 V Operation			6.3	8.0	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			3.4	4.8	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2\ (25)}$					
5 V/3 V Operation			3.4	4.8	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			6.3	8.0	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	$0\ V \leq V_{IA}, V_{IB} \leq (V_{DD1}$ or $V_{DD2})$
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	V_{DD1} or V_{DD2}		V	$I_{Ox} = -20\ µA$, $V_{Ix} = V_{IxH}$
		(V_{DD1} or V_{DD2}) − 0.5	(V_{DD1} or V_{DD2}) − 0.2		V	$I_{Ox} = -4\ mA$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	$I_{Ox} = 20\ µA$, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	$I_{Ox} = 400\ µA$, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4\ mA$, $V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
ADuM1200/ADuM1201AR						$C_L = 15$ pF, CMOS signal levels
Minimum Pulse Width[2]	PW			1000	ns	
Maximum Data Rate[3]		1			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	50		150	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	
Change vs. Temperature			11		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			50	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		10		ns	
ADuM1200/ADuM1201BR						$C_L = 15$ pF, CMOS signal levels
Minimum Pulse Width[2]	PW			100	ns	
Maximum Data Rate[3]		10			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	15		55	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			22	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			22	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F					
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
ADuM1200/ADuM1201CR						$C_L = 15$ pF, CMOS signal levels
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		50	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F					
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions /Comments
For All Models						
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$ or V_{DD2}, $V_{CM} = 1000$ V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	$V_{Ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$					
5 V/3 V Operation			0.19		mA/ Mbps	
3 V/5 V Operation			0.10		mA/ Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$					
5 V/3 V Operation			0.03		mA/ Mbps	
3 V/5 V Operation			0.05		mA/ Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1200 and ADuM1201 channel configurations.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION

All voltages are relative to the respective ground; 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V; this applies to ADuM1200W and ADuM1201W automotive grade products.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.60	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.25	mA	
ADuM1200W, Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.1	1.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRZ and URZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.3	5.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.3	2.0	mA	5 MHz logic signal freq.
25 Mbps (URZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		10	13	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		2.8	3.4	mA	12.5 MHz logic signal freq.
ADuM1201W, Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.8	1.1	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.8	1.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRZ and URZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		2.8	3.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.8	3.5	mA	5 MHz logic signal freq.
25 Mbps (URZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		6.3	8.0	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		6.3	8.0	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ (V_{DD1} or V_{DD2})
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1200/ADuM1201WSRZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			1000	ns	
Maximum Data Rate[3]		1			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		150	ns	
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL}\rvert$[4]	PWD			40	ns	
Propagation Delay Skew[5]	t_{PSK}			100	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM1200/ADuM1201WTRZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			100	ns	
Maximum Data Rate[3]		10			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		50	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
ADuM1200/ADuM1201WURZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		45	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Dynamic Supply Current per Channel[8]						
Input	$I_{DDI (D)}$		0.19		mA/Mbps	
Output	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM1200W and ADuM1201W channel configurations.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V, 125°C OPERATION

All voltages are relative to the respective ground; 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V; this applies to ADuM1200W and ADuM1201W automotive grade products.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.35	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.20	mA	
ADuM1200W, Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.6	1.0	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.2	0.6	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRZ and URZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		2.2	3.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		0.7	1.1	mA	5 MHz logic signal freq.
25 Mbps (URZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		5.2	7.7	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		1.5	2.0	mA	12.5 MHz logic signal freq.
ADuM1201W, Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.4	0.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.4	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRZ and URZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		1.5	2.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.5	2.2	mA	5 MHz logic signal freq.
25 Mbps (URZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		3.4	4.8	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		3.4	4.8	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ (V_{DD1} or V_{DD2})
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1200/ADuM1201WSRZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			1000	ns	
Maximum Data Rate[3]		1			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		150	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	
Propagation Delay Skew[5]	t_{PSK}			100	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM1200/ADuM1201WTRZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			100	ns	
Maximum Data Rate[3]		10			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		60	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			22	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			22	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	
ADuM1200/ADuM1201WCR						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		55	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			16	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			16	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/μs	$V_{Ix} = V_{DD1}$, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Dynamic Supply Current per Channel[8]						
Input	$I_{DDI (D)}$		0.10		mA/Mbps	
Output	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM1200W and ADuM1201W channel configurations.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V, 125°C OPERATION

All voltages are relative to the respective ground; 5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. 3 V/5 V operation; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 5.0 V, V_{DD2} = 3.0 V; this applies to ADuM1200W and ADuM1201W automotive grade products.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.6	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.20	mA	
ADuM1200W, Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.1	1.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.2	0.6	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRZ and URZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.3	5.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		0.7	1.1	mA	5 MHz logic signal freq.
25 Mbps (URZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		10	13	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		1.5	2.0	mA	12.5 MHz logic signal freq.
ADuM1201W, Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.8	1.1	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.4	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRZ and URZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		2.8	3.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.5	2.2	mA	5 MHz logic signal freq.
25 Mbps (URZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		6.3	8.0	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		3.4	4.8	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ (V_{DD1} or V_{DD2})
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	V_{DD1} or V_{DD2}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	(V_{DD1} or V_{DD2}) − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1200/ADuM1201WSRZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			1000	ns	
Maximum Data Rate[3]		1			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	15		150	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	
Propagation Delay Skew[5]	t_{PSK}			50	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/ t_{PSKOD}			50	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM1200/ADuM1201WTRZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			100	ns	
Maximum Data Rate[3]		10			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	15		55	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			22	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			22	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	
ADuM1200/ADuM1201WURZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		50	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Dynamic Supply Current per Channel[8]						
Input	$I_{DDI (D)}$		0.19		mA/Mbps	
Output	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM1200W and ADuM1201W channel configurations.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 3 V/5 V, 125°C OPERATION

All voltages are relative to the respective ground; 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5.0 V; this applies to ADuM1200W and ADuM1201W automotive grade products.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.35	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.25	mA	
ADuM1200W, Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.6	1.0	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRZ and URZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		2.2	3.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.3	2.0	mA	5 MHz logic signal freq.
25 Mbps (URZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		5.2	7.7	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		2.8	3.4	mA	12.5 MHz logic signal freq.
ADuM1201W, Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.4	0.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.8	1.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRZ and URZ Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		1.5	2.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.8	3.5	mA	5 MHz logic signal freq.
25 Mbps (URZ Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (25)}$		3.4	4.8	mA	12.5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (25)}$		6.3	8.0	mA	12.5 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ (V_{DD1} or V_{DD2})
Logic High Input Threshold	V_{IH}	0.7 (V_{DD1} or V_{DD2})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD1} or V_{DD2})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	V_{DD1} or V_{DD2}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		(V_{DD1} or V_{DD2}) − 0.5	(V_{DD1} or V_{DD2}) − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1200/ADuM1201WSRZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			1000	ns	
Maximum Data Rate[3]		1			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	15		150	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			40	ns	
Propagation Delay Skew[5]	t_{PSK}			50	ns	
Channel-to-Channel Matching[6]	t_{PSKCD}/t_{PSKOD}			50	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM1200/ADuM1201WTRZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW			100	ns	
Maximum Data Rate[3]		10			Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	15		55	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			22	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			22	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
ADuM1200/ADuM1201WURZ						C_L = 15 pF, CMOS signal levels
Minimum Pulse Width[2]	PW		20	40	ns	
Maximum Data Rate[3]		25	50		Mbps	
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		50	ns	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	
Change vs. Temperature			5		ps/°C	
Propagation Delay Skew[5]	t_{PSK}			15	ns	
Channel-to-Channel Matching						
Codirectional Channels[6]	t_{PSKCD}			3	ns	
Opposing Directional Channels[6]	t_{PSKOD}			15	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	
For All Models						
Common-Mode Transient Immunity						
Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}$, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current per Channel[8]	$I_{DDI (D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel[8]	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 11 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM1200W and ADuM1201W channel configurations.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 8.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	$R_{I\text{-}O}$		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	$C_{I\text{-}O}$		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ_{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ_{JCO}		41		°C/W	

[1] The device is considered a 2-terminal device; Pin 1, Pin, 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM1200/ADuM1201 and ADuM1200W/ADuM1201W are approved by the organizations listed in Table 9; refer to Table 14 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 9.

UL	CSA	CQC	VDE
Recognized Under 1577 Component Recognition Program[1]	Approved under *CSA Component Acceptance Notice 5A*	Approved under CQC11-471543-2012	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single/Basic 2500 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 peak) maximum working voltage	Basic insulation per GB4943.1-2011	Reinforced insulation, 560 V peak
	Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Basic insulation, 400 V rms (588 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m	
File E214100	File 205078	File CQC14001114901	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM1200, ADuM1201, ADuM1200W, and ADuM1201W is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 sec (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM1200, ADuM1201, ADuM1200W, and ADuM1201W is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * and/or & marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 10.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. Note that the asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 11.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ second, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ seconds, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ seconds, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ seconds	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	160	mA
Side 2 Current		I_{S2}	170	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

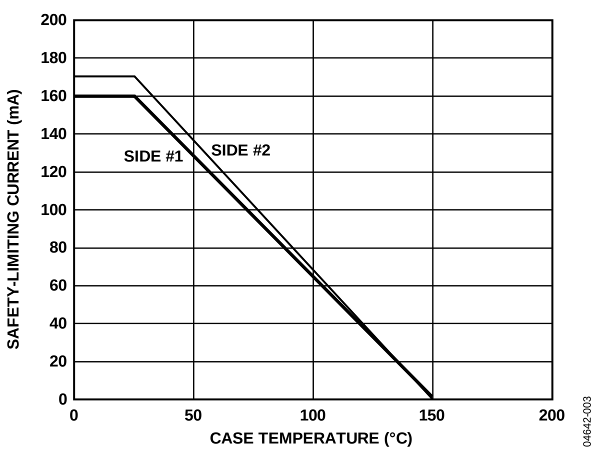


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 12.

Parameter	Rating
Operating Temperature (T_A)[1]	−40°C to +105°C
Operating Temperature (T_A)[2]	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1, 3]	2.7 V to 5.5 V
Supply Voltages (V_{DD1}, V_{DD2})[2, 3]	3.0 V to 5.5 V
Input Signal Rise and Fall Times	1.0 ms

[1] Does not apply to ADuM1200W and ADuM1201W automotive grade products.
[2] Applies to ADuM1200W and ADuM1201W automotive grade products.
[3] All voltages are relative to the respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

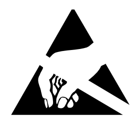
Table 13.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)[1]	−40°C to +105°C
Ambient Operating Temperature (T_A)[2]	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[3]	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[3, 4]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[3, 4]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin (I_O)[5]	−11 mA to +11 mA
Common-Mode Transients (CM_L, CM_H)[6]	−100 kV/μs to +100 kV/μs

[1] Does not apply to ADuM1200W and ADuM1201W automotive grade products.
[2] Applies to ADuM1200W and ADuM1201W automotive grade products.
[3] All voltages are relative to the respective ground.
[4] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[5] See Figure 3 for maximum rated current values for various temperatures.
[6] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 14. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

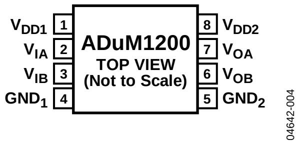


Figure 4. ADuM1200 Pin Configuration

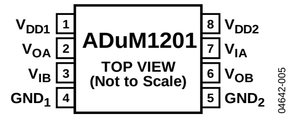


Figure 5. ADuM1201 Pin Configuration

Table 15. ADuM1200 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground Reference for Isolator Side 1.
5	GND_2	Ground 2. Ground Reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

Table 16. ADuM1201 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground Reference for Isolator Side 1.
5	GND_2	Ground 2. Ground Reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

Table 17. ADuM1200 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration.

Table 18. ADuM1201 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	H	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	H	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration.

TYPICAL PERFORMANCE CHARACTERISTICS

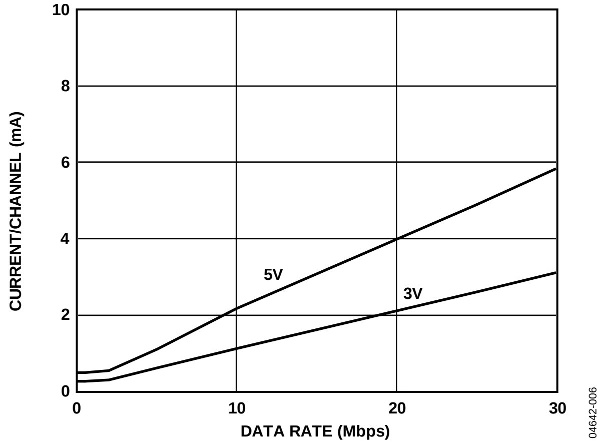


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

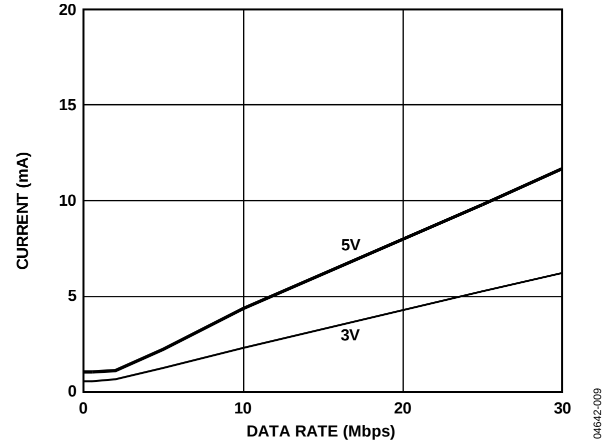


Figure 9. Typical ADuM1200 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

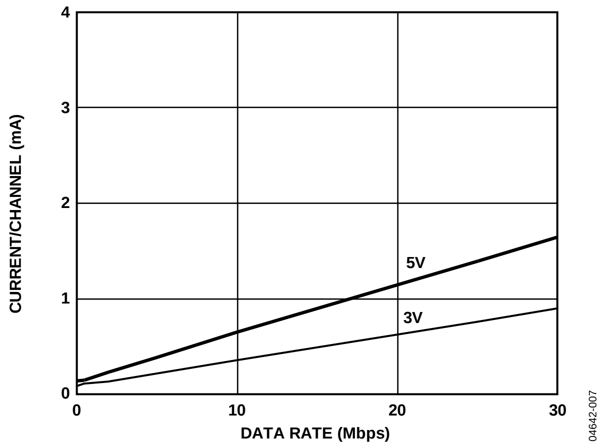


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

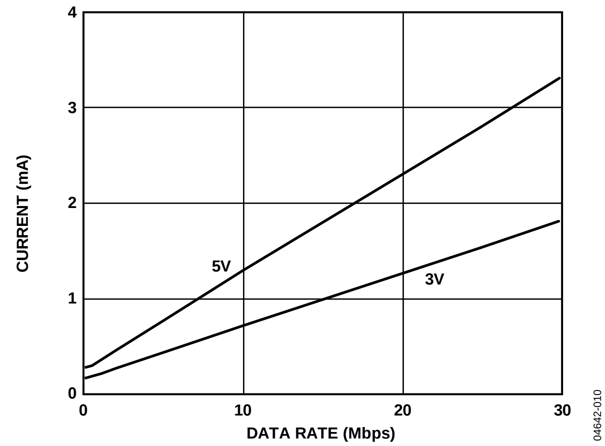


Figure 10. Typical ADuM1200 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

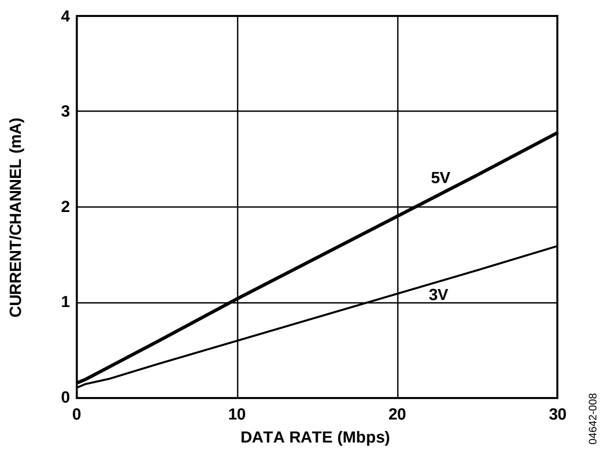


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

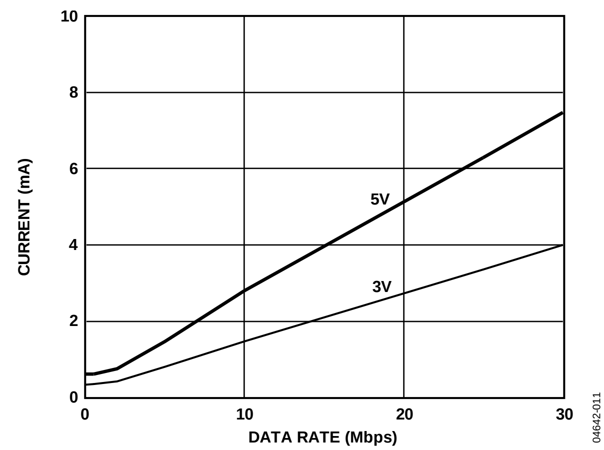


Figure 11. Typical ADuM1201 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM1200/ADuM1201 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins.

The capacitor value must be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

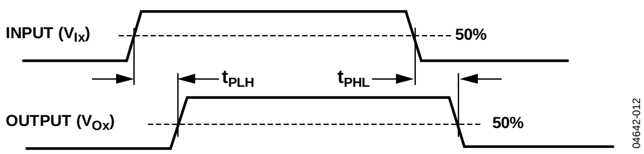


Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM1200/ADuM1201 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM1200/ADuM1201 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input send narrow (~1 ns) pulses to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than ~1 µs at the input, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 17 and Table 18) by the watchdog timer circuit.

The ADuM1200/ADuM1201 are extremely immune to external magnetic fields. The limitation on the magnetic field immunity of the ADuM1200/ADuM1201 is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The 3 V operating condition of the ADuM1200/ADuM1201 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\prod r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM1200/ADuM1201 and an imposed requirement that the induced voltage be 50% at most of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 13.

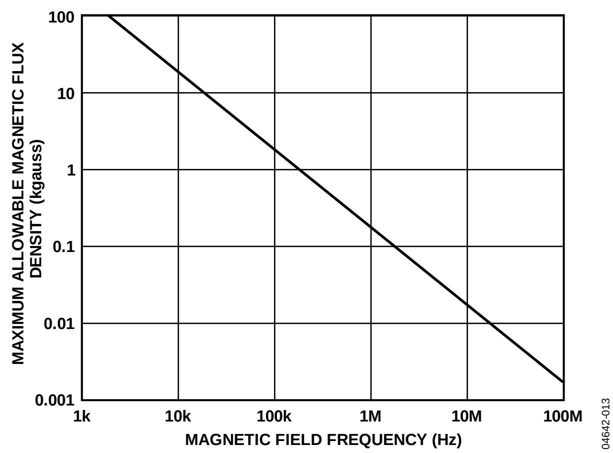


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and has the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1200/ADuM1201 transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. As seen, the ADuM1200/ADuM1201 are extremely immune and can be affected only by extremely large currents operating very close to the component at a high frequency. For the 1 MHz example, place a 0.5 kA current 5 mm away from the ADuM1200/ADuM1201 to affect the operation of the component.

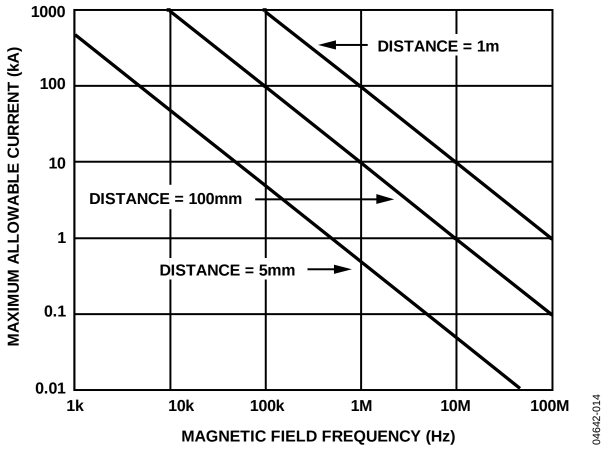


Figure 14. Maximum Allowable Current for Various Current-to-ADuM1200/ADuM1201 Spacings

Note that, at combinations of strong magnetic fields and high frequencies, any loops formed by PCB traces can induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM1200/ ADuM1201 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply currents, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 6 and Figure 7 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 11 provide total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM1200 and ADuM1201 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM1200/ADuM1201.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 14 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM1200/ADuM1201 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms, respectively.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages yet still achieves a 50-year service life. The working voltages listed in Table 14 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 is to be treated as a bipolar ac waveform, and the peak voltage is to be limited to the 50-year lifetime voltage value listed in Table 14.

Note that the voltage presented in Figure 16 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

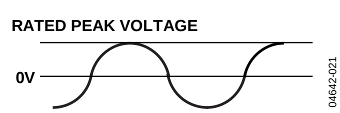


Figure 15. Bipolar AC Waveform

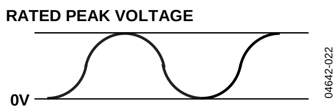


Figure 16. Unipolar AC Waveform

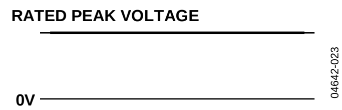


Figure 17. DC Waveform

OUTLINE DIMENSIONS

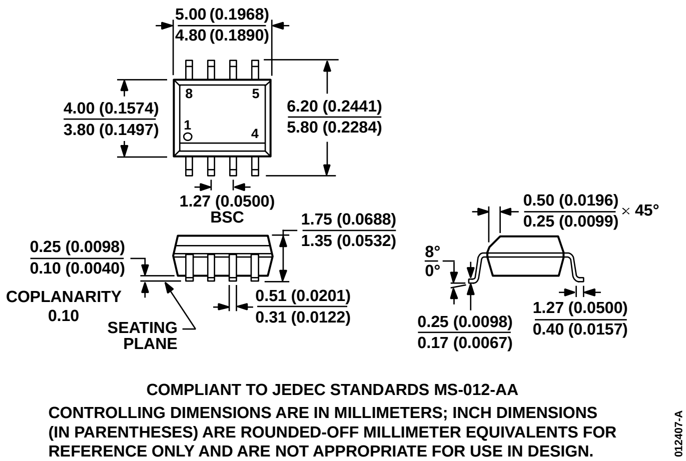


*Figure 18. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)*

ORDERING GUIDE

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Option[3]
ADuM1200AR	2	0	1	150	40	−40°C to +105°C	R-8
ADuM1200ARZ	2	0	1	150	40	−40°C to +105°C	R-8
ADuM1200ARZ-RL7	2	0	1	150	40	−40°C to +105°C	R-8
ADuM1200BR	2	0	10	50	3	−40°C to +105°C	R-8
ADuM1200BRZ	2	0	10	50	3	−40°C to +105°C	R-8
ADuM1200BRZ-RL7	2	0	10	50	3	−40°C to +105°C	R-8
ADuM1200CR	2	0	25	45	3	−40°C to +105°C	R-8
ADuM1200CRZ	2	0	25	45	3	−40°C to +105°C	R-8
ADuM1200CRZ-RL7	2	0	25	45	3	−40°C to +105°C	R-8
ADuM1200WSRZ	2	0	1	150	40	−40°C to +125°C	R-8
ADuM1200WSRZ-RL7	2	0	1	150	40	−40°C to +125°C	R-8
ADuM1200WTRZ	2	0	10	50	3	−40°C to +125°C	R-8
ADuM1200WTRZ-RL7	2	0	10	50	3	−40°C to +125°C	R-8
ADuM1200WURZ	2	0	25	45	3	−40°C to +125°C	R-8
ADuM1200WURZ-RL7	2	0	25	45	3	−40°C to +125°C	R-8
ADuM1201AR	1	1	1	150	40	−40°C to +105°C	R-8
ADuM1201AR-RL7	1	1	1	150	40	−40°C to +105°C	R-8
ADuM1201ARZ	1	1	1	150	40	−40°C to +105°C	R-8
ADuM1201ARZ-RL7	1	1	1	150	40	−40°C to +105°C	R-8
ADuM1201BR	1	1	10	50	3	−40°C to +105°C	R-8
ADuM1201BR-RL7	1	1	10	50	3	−40°C to +105°C	R-8
ADuM1201BRZ	1	1	10	50	3	−40°C to +105°C	R-8
ADuM1201BRZ-RL7	1	1	10	50	3	−40°C to +105°C	R-8
ADuM1201CR	1	1	25	45	3	−40°C to +105°C	R-8
ADuM1201CRZ	1	1	25	45	3	−40°C to +105°C	R-8
ADuM1201CRZ-RL7	1	1	25	45	3	−40°C to +105°C	R-8

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Option[3]
ADuM1201WSRZ	1	1	1	150	40	−40°C to +125°C	R-8
ADuM1201WSRZ-RL7	1	1	1	150	40	−40°C to +125°C	R-8
ADuM1201WTRZ	1	1	10	50	3	−40°C to +125°C	R-8
ADuM1201WTRZ-RL7	1	1	10	50	3	−40°C to +125°C	R-8
ADuM1201WURZ	1	1	25	45	3	−40°C to +125°C	R-8
ADuM1201WURZ-RL7	1	1	25	45	3	−40°C to +125°C	R-8

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] R-8 = 8-lead narrow-body SOIC_N.

AUTOMOTIVE PRODUCTS

The ADuM1200W/ADuM1201W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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