ADP3121

Dual Bootstrapped, 12 V MOSFET Driver with Output Disable

The ADP3121 is a dual, high voltage MOSFET driver optimized for driving two N−channel MOSFETs, the two switches in a non−isolated synchronous buck power converter. Each driver is capable of driving a 3000 pF load with a 20 ns propagation delay and a 15 ns transition time.

One of the drivers can be bootstrapped and is designed to handle the high voltage slew rate associated with floating high−side gate drivers. The ADP3121 includes overlapping drive protection to prevent shoot−through current in the external MOSFETs.

The $\overline{OD}$ pin shuts off both the high−side and the low−side MOSFETs to prevent rapid output capacitor discharge during system shutdown.

The ADP3121 is specified over the commercial temperature range of 0°C to 85°C and is available in 8−lead SOIC_N and 8−lead LFCSP packages.

Features

- All−In−One Synchronous Buck Driver
- Bootstrapped High−Side Drive
- One PWM Signal Generates Both Drives
- Anticross Conduction Protection Circuitry
- Overvoltage Protection
- $\overline{OD}$ for Disabling the Driver Outputs
- Meets CPU VR Requirement when Used with Flex−Mode™ Controller
- These are Pb−Free Devices

Typical Applications

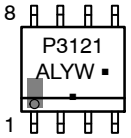
- Multiphase Desktop CPU Supplies
- Single Supply Synchronous Buck Converters

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

SO−8
D SUFFIX
CASE 751−07

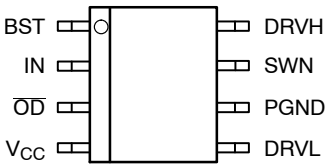


P3121A = Device Code
AL = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

LFCSP8
MN SUFFIX
CASE 932AF

L7Q = Device Code
# = Pb−Free Package
Y = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
ADP3121JRZ−RL	SOIC_N (Pb−Free)	2500/Tape & Reel
ADP3121JCPZ−RL	LFCSP_VD (Pb−Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

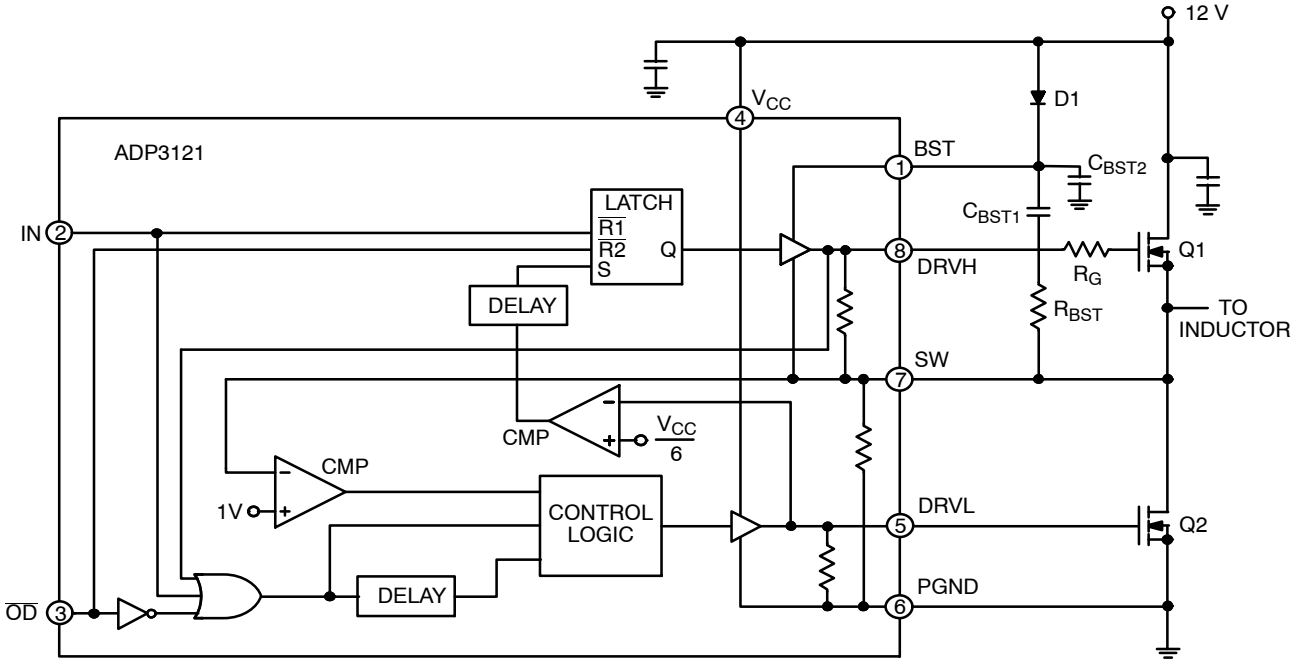


Figure 1. Block Diagram

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between the BST and SW pins holds this bootstrapped voltage for the high−side MOSFET while it is switching.
2	IN	Logic Level PWM Input. This pin has primary control of the drive outputs. In normal operation, pulling this pin low turns on the low−side driver; pulling it high turns on the high−side driver.
3	$\overline{OD}$	Output Disable. When low, this pin disables normal operation, forcing DRVH and DRVL low.
4	VCC	Input Supply. This pin should be bypassed to PGND with an ~1 μF ceramic capacitor.
5	DRVL	Synchronous Rectifier Drive. Output drive for the lower (synchronous rectifier) MOSFET.
6	PGND	Power Ground. This pin should be closely connected to the source of the lower MOSFET.
7	SW	Switch Node Connection. This pin is connected to the buck switching node, close to the upper MOSFET source. It is the floating return for the upper MOSFET drive signal. It is also used to monitor the switched voltage to prevent the lower MOSFET from turning on until the voltage is below ~1 V.
8	DRVH	Buck Drive. Output drive for the upper (buck) MOSFET.

MAXIMUM RATINGS

Rating	Value	Unit
θ_{JA}, SOIC_N 2−Layer Board 4−Layer Board	 123 90	°C/W
θ_{JA}, LFCSP_VD (Note 1) 4−Layer Board	 64.3	°C/W
Operating Ambient Temperature Range	0 to 85	°C
Junction Temperature Range	0 to 150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature Soldering (10 sec) Vapor Phase (60 sec) Infrared (15 sec)	 300 215 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Internally limited by thermal shutdown, 150°C min. 2−layer board, 1 in² Cu, 1 oz thickness. 60−180 seconds minimum above 237°C.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Pin Symbol	Pin Name	V_{max}	V_{min}
V_{CC}	Main supply voltage input	15 V	−0.3 V
GND	Ground	0 V	0 V
BST	Bootstrap Supply Voltage Input DC <200 ns BST to SW	 V_{CC} + 15 +35 +15	−0.3 V
SW	Switching Node (Bootstrap Supply Return) DC <200 ns	 +15 +25 V	 −5 V −10 V
DRVH	High−Side Driver Output DC <20 ns <200 ns	 BST + 0.3 V BST + 2.0 V BST + 0.3 V	 SW − 0.3 V SW − 2.0 V SW − 2.0 V
DRVL	Low−Side Driver Output DC <20 ns <200 ns	 V_{CC} + 0.3 V V_{CC} + 2.0 V V_{CC} + 0.3 V	 −0.3 V −2.0 V −2.0 V
IN	DRVH and DRVL Control Input	6.5 V	−0.3 V
$\overline{OD}$	Outside Disable	6.5 V	−0.3 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. All voltages are with respect to PGND except where noted.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, BST = 4.0 V to 26 V, T_A = 0°C to 85°C, unless otherwise noted) (Note 1)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage Range		V_{CC}	4.15		13.2	V
Supply Current	BST = 12 V, IN = 0 V	I_{SYS}		2.0	5.0	mA
$\overline{OD}$ INPUTS						
Input Voltage High			2.0			V
Input Voltage Low					0.8	V
Input Current			−1.0		+1.0	μA
Hysteresis			90	250		mV
PWM INPUTS						
Input Voltage High			2.0			V
Input Voltage Low					0.8	V
Input Current			−1.0		+1.0	μA
Hysteresis			90	250		mV
HIGH−SIDE DRIVER						
Output Resistance, Sourcing Current	BST − SW = 12 V; T_A = 25°C BST − SW = 12 V; T_A = 0°C to 85°C			 1.7	2.3 2.8	Ω
Output Resistance, Sinking Current	BST − SW = 12 V; T_A = 25°C BST − SW = 12 V; T_A = 0°C to 85°C			 1.7	2.3 2.8	Ω
Output Resistance, Unbiased	BST − SW = 0 V			10		kΩ
Transition Times	BST − SW = 12 V, C_{LOAD} = 3 nF, see Figure 4 BST − SW = 12 V, C_{LOAD} = 3 nF, see Figure 4	t_{rDRVH} t_{fDRVH}		20 20	32 30	ns
Propagation Delay Times	BST − SW = 12 V, C_{LOAD} = 3 nF 25°C ≤ T_A ≤ 85°C, see Figure 4	$t_{pdhDRVH}$	20	30	50	ns
	BST − SW = 12 V, C_{LOAD} = 3 nF, see Figure 4 See Figure 3 See Figure 3	$t_{pdlDRVH}$ $t_{pdl\overline{OD}}$ t_{pdhOD}		32 30 20	47 45 40	ns
SW Pull−Down Resistance	SW to PGND			10		kΩ
LOW−SIDE DRIVER						
Output Resistance, Sourcing Current	T_A = 25°C T_A = 0°C to 85°C			 1.8	2.4 2.8	Ω
Output Resistance, Sinking Current	T_A = 25°C T_A = 0°C to 85°C			 1.0	1.6 1.8	Ω
Output Resistance, Unbiased	V_{CC} = PGND			10		kΩ
Transition Times	C_{LOAD} = 3 nF, see Figure 4 C_{LOAD} = 3 nF, see Figure 4	t_{rDRVL} t_{fDRVL}		20 10	30 20	ns
Propagation Delay Times	C_{LOAD} = 3 nF, see Figure 4 C_{LOAD} = 3 nF, see Figure 4 See Figure 3 See Figure 3	$t_{pdhDRVL}$ $t_{pdlDRVL}$ $t_{pdl\overline{OD}}$ t_{pdhOD}	 100	15 17 37 180	35 32 52	ns
Timeout Delay	SW = 5.0 V SW = PGND		90 70	170 110		ns
Overvoltage Protection Threshold	IN = $\overline{OD}$ = 0 V, S_W = V_{CC}	$V_{SW(OVD)}$	1.5		3.5	V
UNDERVOLTAGE LOCKOUT						
UVLO Voltage		V_{CC} rising	1.5		3.0	V
Hysteresis				250		mV

1. ALL limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods

Theory of Operation

The ADP3121 is optimized for driving two N−channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high side and the low−side MOSFETs. Each driver is capable of driving a 3 nF load at speeds up to 500 kHz. A functional block diagram of ADP3121 is shown in Figure 1.

Low−Side Driver

The low−side driver is designed to drive a ground referenced N−channel MOSFET. The bias to the low−side driver is internally connected to the V_{CC} supply and PGND.

When the driver is enabled, the driver output is 180° out of phase with the PWM input. When the ADP3121 is disabled, the low−side gate is held low.

High−Side Driver

The high−side driver is designed to drive a floating N−channel MOSFET. The bias voltage for the high−side driver is developed by an external bootstrap supply circuit that is connected between the BST and SW pins.

The bootstrap circuit comprises Diode D1 and Bootstrap Capacitor C_{BST1}. C_{BST2} and R_{BST} are included to reduce the high−side gate drive voltage and to limit the switch node slew rate (called a Boot−Snap circuit). When the ADP3121 starts up, the SW pin is at ground, so the bootstrap capacitor charges up to V_{CC} through D1. When the PWM input goes high, the high−side driver begins to turn on the high−side MOSFET, Q1, by pulling charge out of C_{BST1} and C_{BST2}. As Q1 turns on, the SW pin rises up to V_{IN} and forces the BST pin to $V_{IN} + V_{C\ (BST)}$. This holds Q1 on because enough gate−to−source voltage is provided. To complete the cycle, Q1 is switched off by pulling the gate down to the voltage at the SW pin. When the low−side MOSFET, Q2, turns on, the SW pin is pulled to ground. This allows the bootstrap capacitor to charge up to V_{CC} again.

The output of the high−side driver is in phase with the PWM input. When the driver is disabled, the high−side gate is held low.

Overlap Protection Circuit

The overlap protection circuit prevents both of the main power switches, Q1 and Q2, from being on at the same time. This is done to prevent shoot−through currents from flowing through both power switches and the associated losses that can occur during their on/off transitions. The overlap protection circuit accomplishes this by adaptively controlling the delay from the Q1 turn−off to the Q2 turn−on, and by internally setting the delay from the Q2 turn−off to the Q1 turn−on.

To prevent the overlap of the gate drives during the Q1 turn−off and the Q2 turn−on, the overlap circuit monitors the voltage at the SW pin. When the PWM input signal goes low, Q1 begins to turn off (after propagation delay). Before Q2 can turn on, the overlap protection circuit makes sure that SW has first gone high and then waits for the voltage at the SW pin to fall from V_{IN} to 1 V. Once the voltage on the SW pin falls to 1.0 V, Q2 begins turn−on. If the SW pin has not gone high first, the Q2 turn−on is delayed by a fixed 150 ns. By waiting for the voltage on the SW pin to reach 1.0 V or for the fixed delay time, the overlap protection circuit ensures that Q1 is off before Q2 turns on, regardless of variations in temperature, supply voltage, input pulse width, gate charge, and drive current. If SW does not go below 1.0 V after 190 ns, DRVL turns on. This can occur if the current flowing in the output inductor is negative and flows through the high−side MOSFET body diode.

Overvoltage Protection

The ADP3121 includes an overvoltage protection (OVP) feature to protect the CPU from high voltages even before the main controller has enough V_{CC} to operate. The ADP3121 looks at the SW node during startup. If the voltage on SW is greater than the OVP threshold, DRVL is latched on and DRVH latched off. An OVP on the SW node will cause DRVL to go high and remain high.

To prevent false triggering of OVP, an input logic detection latch is set on the first occurrence of either IN or $\overline{OD}$ going high. If this second latch is set, then OVP is enabled. To clear the OVP or the input detected latch, V_{CC} must fall below UVLO.

Supply Capacitor Selection

For the supply input (V_{CC}) of the ADP3121, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents that are drawn. Use a 4.7 μF, low ESR capacitor. Multi−layer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size. Keep the ceramic capacitor as close as possible to the ADP3121.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and a diode, as shown in Figure 1. These components can be selected after the high−side MOSFET is chosen. The bootstrap capacitor must have a voltage rating that can handle twice the maximum supply voltage. A minimum 50 V rating is recommended. The capacitor values are determined by

$$C_{BST1} + C_{BST2} = 10 \times \frac{Q_{GATE}}{V_{GATE}} \qquad \text{(eq. 1)}$$

$$\frac{C_{BST1}}{C_{BST1} + C_{BST2}} = \frac{V_{GATE}}{V_{CC} - V_D} \qquad \text{(eq. 2)}$$

where:

Q_{GATE} is the total gate charge of the high−side MOSFET at V_{GATE}.

V_{GATE} is the desired gate drive voltage (usually in the range of 5.0 V to 10 V, 7.0 V being typical).

V_D is the voltage drop across D1.

Re−arranging Equation 1 and Equation 2 to solve for C_{BST1} yields:

$$C_{BST1} = 10 \times \frac{Q_{GATE}}{V_{CC} - V_D}$$

C_{BST2} can then be found by rearranging Equation 1.

$$C_{BST2} = 10 \times \frac{Q_{GATE}}{V_{GATE}} - C_{BST1}$$

For example, an NTD60N02 has a total gate charge of about 12 nC at V_{GATE} = 7.0 V. Using V_{CC} = 12 V and V_D = 0.1 V, then C_{BST1} = 12 nF and C_{BST2} = 6.8 nF. Good quality ceramic capacitors should be used.

R_{BST} is used to limit slew rate and minimize ringing at the switch node. It also provides peak current limiting through D1. An R_{BST} value of 1.5 Ω to 2.2 Ω is a good choice. The resistor needs to handle at least 250 mΩ due to the peak currents that flow through it.

A small signal diode can be used for the bootstrap diode due to the ample gate drive voltage supplied by V_{CC}. The bootstrap diode must have a minimum 15 V rating to withstand the maximum supply voltage. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX} \quad \text{(eq. 3)}$$

where f_{MAX} is the maximum switching frequency of the controller.

The peak surge current rating should be calculated by:

$$I_{F(PEAK)} = \frac{V_{CC} - V_D}{R_{BST}} \quad \text{(eq. 4)}$$

MOSFET Selection

When interfacing the ADP3121 to external MOSFETs, the designer should consider ways to make a robust design that minimizes stresses on both the driver and the MOSFETs. These stresses include exceeding the short time duration voltage ratings on the driver pins as well as the external MOSFET.

It is also highly recommended to use the Boot−Snap circuit to improve the interaction of the driver with the characteristics of the MOSFETs. If a simple bootstrap arrangement is used, make sure to include a proper snubber network on the SW node.

High−Side (Control) MOSFETs

A high−side, high speed MOSFET is usually selected to minimize switching losses (see the ADP3186 or ADP3188 data sheet for Flex−Mode controller details). This typically implies a low gate resistance and low input capacitance/charge device. Yet, a significant source lead inductance can also exist that depends mainly on the MOSFET package; it is best to contact the MOSFET vendor for this information.

The ADP3121 DRVH output impedance and the input resistance of the MOSFETs determine the rate of charge delivery to the internal capacitance of the gate. This determines the speed at which the MOSFETs turn on and off. However, because of potentially large currents flowing in the MOSFETs at the on and off times (this current is usually larger at turn−off due to ramping up of the output current in the output inductor), the source lead inductance generates a significant voltage when the high−side MOSFETs switch off. This creates a significant drain−source voltage spike across the internal die of the MOSFETs and can lead to a catastrophic avalanche. The mechanisms involved in this avalanche condition are referenced in literature from the MOSFET suppliers.

The MOSFET vendor should provide a rating for the maximum voltage slew rate at drain current around which this can be designed. Once this specification is obtained, determine the maximum current expected in the MOSFET by:

$$I_{MAX} = I_{DC}(\text{per phase}) + (V_{CC} - V_{OUT}) \times \frac{D_{MAX}}{f_{MAX} \times L_{OUT}} \quad \text{(eq. 5)}$$

where:

D_{MAX} is determined for the VR controller being used with the driver. This current is divided roughly equally between MOSFETs if more than one is used (assume a worst−case mismatch of 30% for design margin).

L_{OUT} is the output inductor value.

When producing the design, there is no exact method for calculating the dV/dt due to the parasitic effects in the external MOSFETs as well as the PCB. However, it can be measured to determine if it is safe. If it appears that the dV/dt is too fast, an optional gate resistor can be added between DRVH and the high−side MOSFETs. This resistor slows down the dV/dt, but it increases the switching losses in the high−side MOSFETs. The ADP3121 is optimally designed with an internal drive impedance that works with most MOSFETs to switch them efficiently, yet minimizes dV/dt. However, some high speed MOSFETs can require this external gate resistor depending on the currents being switched in the MOSFET.

Low−Side (Synchronous) MOSFETs

The low−side MOSFETs are usually selected to have a low on resistance to minimize conduction losses. This usually implies a large input gate capacitance and gate charge. The first concern is to make sure the power delivery from the ADP3121 DRVL does not exceed the thermal rating of the driver (see the ADP3186, ADP3188, or ADP3189 data sheets for Flex−Mode controller details).

The next concern for the low−side MOSFETs is to prevent them from being inadvertently switched on when the high−side MOSFET turns on. This occurs due to the drain−gate (Miller capacitance, also specified as C_{rss} capacitance) of the MOSFET. When the drain of the low−side MOSFET is switched to V_{CC} by the high−side turning on (at a dV/dt rate), the internal gate of the low−side MOSFET is pulled up by an amount roughly equal to $V_{CC} \times (C_{rss}/C_{iss})$. It is important to make sure this does not put the MOSFET into conduction.

Another consideration is the nonoverlap circuitry of the ADP3121 that attempts to minimize the nonoverlap period. During the state of the high−side turning off to low−side turning on, the SW pin is monitored (as well as the conditions of SW prior to switching) to adequately prevent overlap.

However, during the low−side turn−off to high−side turn−on, the SW pin does not contain information for determining the proper switching time, so the state of the DRVL pin is monitored to go below one sixth of V_{CC}; then, a delay is added. Due to the Miller capacitance and internal delays of the low−side MOSFET gate, ensure that the Miller−to−input capacitance ratio is low enough, and that the low−side MOSFET internal delays are not so large as to allow accidental turn−on of the low−side when the high−side turns on. Contact ON Semiconductor for an updated list of recommended low−side MOSFETs.

PC Board Layout Considerations

Use these general guidelines when designing printed circuit boards:

- Trace out the high current paths and use short, wide (>20 mil) traces to make these connections.
- Minimize trace inductance between DRVH and DRVL outputs and MOSFET gates.
- Connect the PGND pin of the ADP3121 as closely as possible to the source of the lower MOSFET.
- Locate the V_{CC} bypass capacitor as close as possible to the V_{CC} and PGND pins.
- Use vias to other layers, when possible, to maximize thermal conduction away from the IC.

Figure 2 shows an example of the typical land patterns based on the guidelines given previously. For more detailed layout guidelines for a complete CPU voltage regulator subsystem, refer to the PC Board Layout Considerations section of the ADP3188 data sheet.

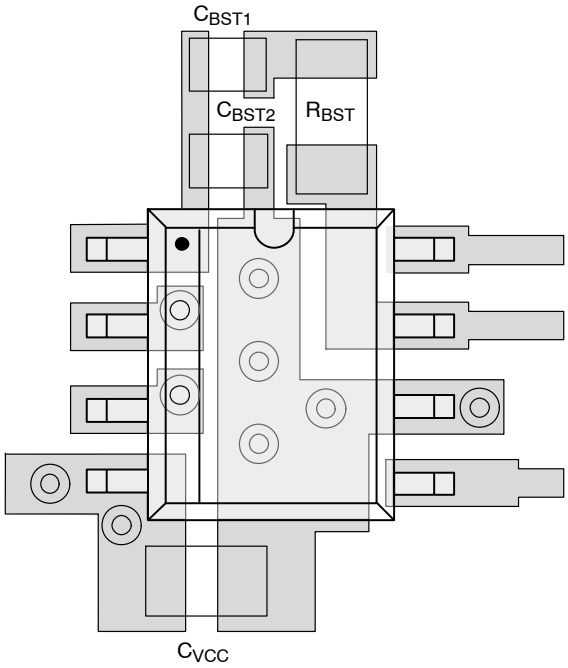


Figure 2. External Component Placement Example

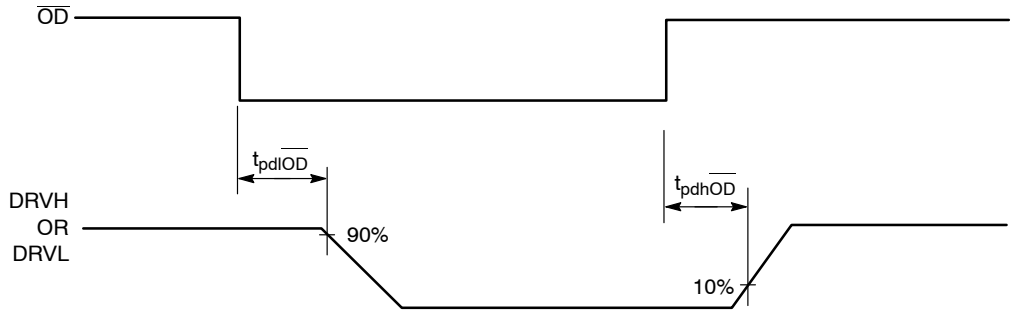


Figure 3. Output Disable Timing Diagram

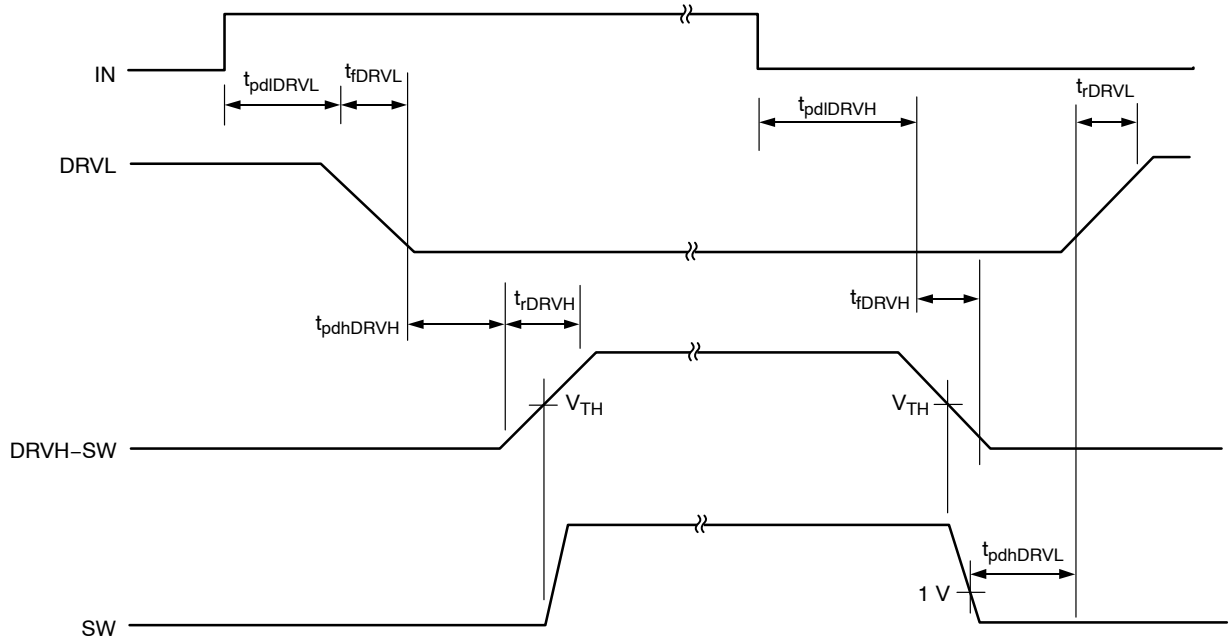
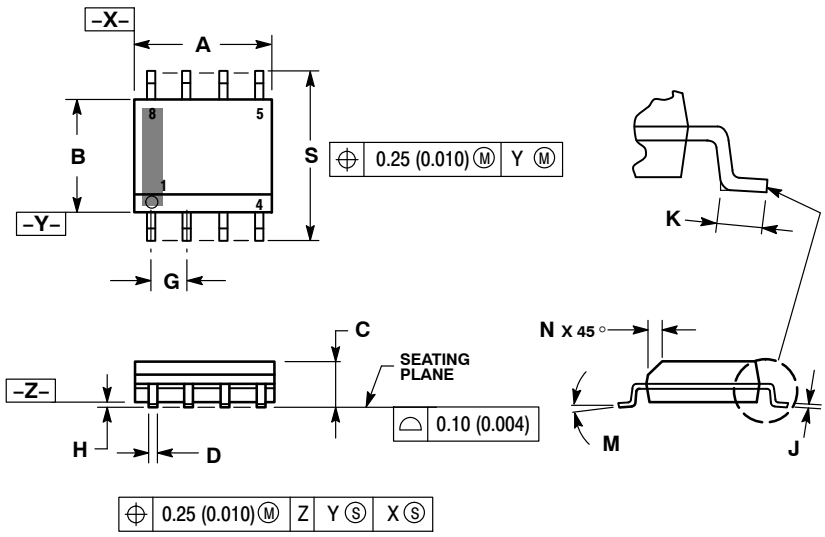


Figure 4. Timing Diagram

PACKAGE DIMENSIONS

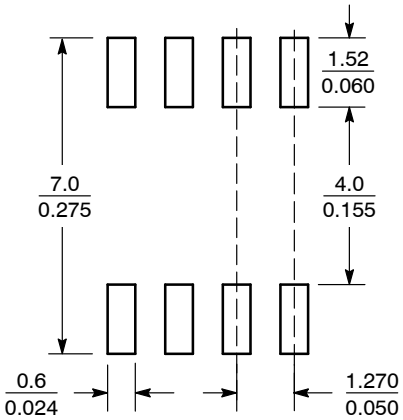
SOIC−8 NB
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

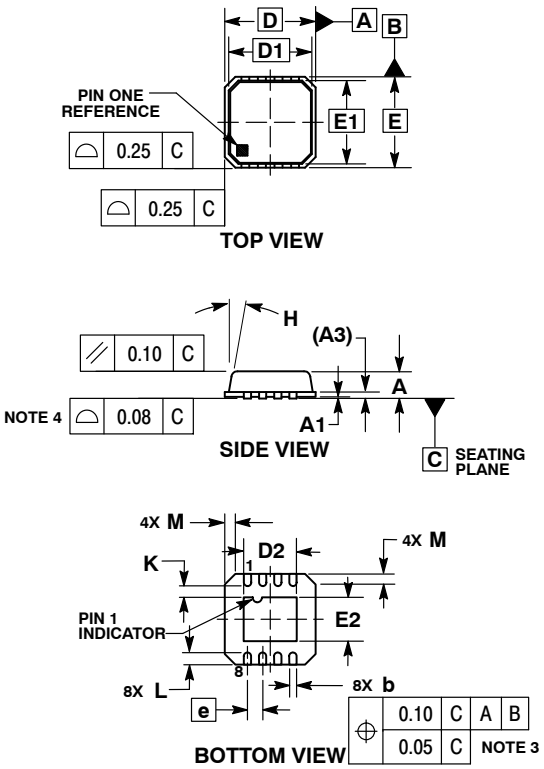


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

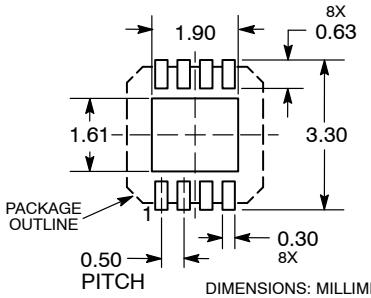
LFCSP8 3x3, 0.5P
CASE 932AF−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	0.90
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D1	2.75 BSC	
D2	1.59	1.89
E	3.00 BSC	
E1	2.75 BSC	
E2	1.30	1.60
e	0.50 BSC	
H	−−−	12°
K	0.20	−−−
L	0.30	0.50
M	−−−	0.60

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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For additional information, please contact your local Sales Representative

ADP3121/D