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10/08—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, V_{OUT} = 3.3 V, @ T_A = T_J = −40°C to +125°C for minimum/maximum specifications and T_A = 25°C for typical specifications, unless otherwise noted.[1]

Table 1.

Parameters	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range		2.3		5.5	V
Undervoltage Lockout Threshold	V_{IN} rising	2.15	2.20	2.25	V
	V_{IN} falling	2.10	2.14	2.20	V
OUTPUT CHARACTERISTICS					
Output Voltage Range		2.8		5.5	V
Feedback Impedance			450		kΩ
Feedback Voltage	ADP2503/ADP2504 adjustable output (PWM operation, no load)	490	500	510	mV
Output Voltage Initial Accuracy	ADP2503/ADP2504 fixed output (PWM operation, no load)	−2		+2	%
Load and Line Regulation	V_{IN} = 2.3 V to 3.6 V, I_{LOAD} = 0 mA to 500 mA, forced PWM mode			0.5	%
	V_{IN} = 2.3 V to 5.5 V, I_{LOAD} = 0 mA to 500 mA, forced PWM mode			0.6	%
CURRENT CHARACTERISTICS					
Quiescent Current (V_{IN})	I_{OUT} = 0 mA, V_{IN} = EN = 3.6 V, device not switching		38	50	µA
Shutdown Current	T_A = T_J = −40°C to +125°C		0.2	1	µA
SWITCH CHARACTERISTICS					
N-Channel Switches	V_{IN} = 3.6 V		150		mΩ
P-Channel Switches	V_{IN} = V_{OUT} = 3.6 V		150		mΩ
P-Channel Leakage	T_J = −40°C to +125°C			1	µA
Switch Current Limit					
ADP2504		1.3		2.0	A
ADP2503		1.0		1.4	A
Reverse Current Limit				1.1	A
OSCILLATOR AND STARTUP					
Oscillator Frequency		2.1	2.5	2.9	MHz
On Time PMOS1 (Buck Mode)	Minimum duty cycle = 30%	130			ns
On Time NMOS2 (Boost Mode)	Maximum duty cycle = 50% (×2)			200	ns
SYNC Clock Frequency		2.2		2.8	MHz
SYNC Clock Minimum Off Time		160			ns
LOGIC LEVEL CHARACTERISTICS					
EN, SYNC Input High Threshold		1.2			V
EN, SYNC Input Low Threshold				0.4	V
EN, SYNC Leakage Current	V_{EN} = V_{IN}, V_{SYNC} = V_{IN}	−1	+0.1	+1	µA
THERMAL CHARACTERISTICS					
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			25		°C

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN, VIN, SW1, SW2, VOUT, SYNC, EN, FB	−0.3 V to +6 V
PGND to AGND	−0.3 V to 0.3 V
Operating Ambient Temperature Range	−40°C to +125°C
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020
ESD Human Body Model	±2000 V
ESD Charged Device Model	±1500 V
ESD Machine Model	±100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

The ADP2503/ADP2504 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature (T_A) does not guarantee that the junction temperature (T_J) is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. T_J of the device is dependent on T_A, the power dissipation (P_D) of the device, and the junction-to-ambient thermal resistance (θ_{JA}) of the package. Maximum T_J is calculated from T_A and P_D using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

θ_{JA} of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inch × 3 inch circuit board. Refer to JEDEC JESD 51-9 for detailed information on the board construction.

THERMAL RESISTANCE

θ_{JA} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}	Unit
10-Lead LFCSP (QFN)	84	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

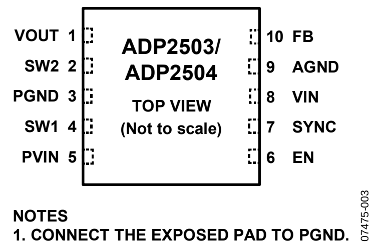

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT	Output of the ADP2503/ADP2504. Connect the output capacitor between VOUT and PGND.
2	SW2	Power Switch 2 Connection. This is the internal connection to the input PMOS and NMOS switches. Connect SW2 to the inductor with a short, wide track.
3	PGND	Power GND. Connect the input and output capacitors and the PGND pin to a PGND plane.
4	SW1	Power Switch 1 Connection. This is the internal connection to the output PMOS and NMOS switches. Connect SW1 to the inductor with a short, wide track.
5	PVIN	Power Input. This the input to the buck-boost power switches. Place a 10 µF capacitor between PVIN and PGND as close as possible to the ADP2503/ADP2504.
6	EN	Enable. Drive EN high to turn on the ADP2503/ADP2504. Bring EN low to put the device into shutdown mode.
7	SYNC	The SYNC pin permits the ADP2503/ADP2504 to operate in three different modes.
		Normal operation: with SYNC driven low, the ADP2503/ADP2504 operate at 2.5 MHz PWM mode for heavy and medium loads, and moves to power save mode (PSM) mode for light loads.
		Forced PWM operation: with SYNC driven high, the ADP2503/ADP2504 operate at fixed 2.5 MHz PWM mode for all load conditions.
		SYNC mode: to synchronize the ADP2503/ADP2504 switching to an external signal, drive this pin with a clock between 2.2 MHz and 2.8 MHz. The SYNC signal must have on and off times greater than 160 ns.
8	VIN	Analog Power Supply. This is the supply for the ADP2503/ADP2504 internal circuitry.
9	AGND	Analog Ground.
10	FB	Output Feedback. This is an input to the internal error amplifier and must be connected to VOUT on fixed output versions; for the adjustable model, this is the voltage feedback.
EP	Exposed pad	Connect the exposed pad to PGND.

TYPICAL PERFORMANCE CHARACTERISTICS

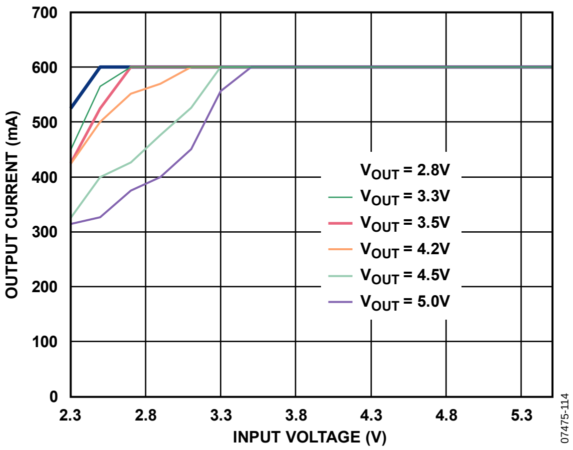

Figure 3. ADP2503 Output Current vs. Input Voltage

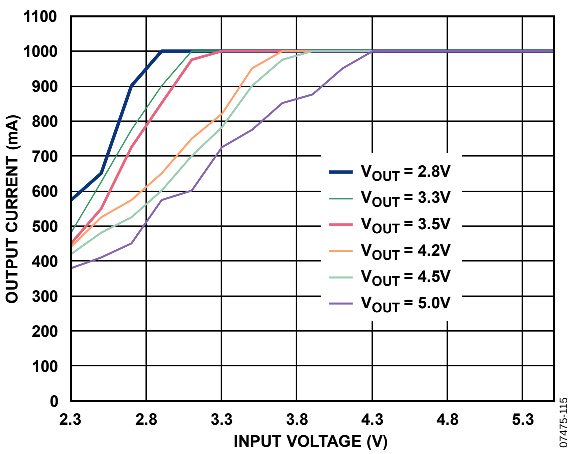

Figure 4. ADP2504 Output Current vs. Input Voltage

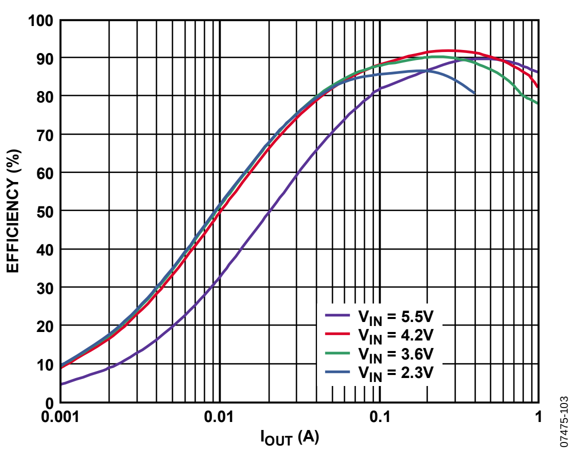

Figure 5. Efficiency vs. Output Current, PWM Mode (V_{OUT} = 5.0 V)

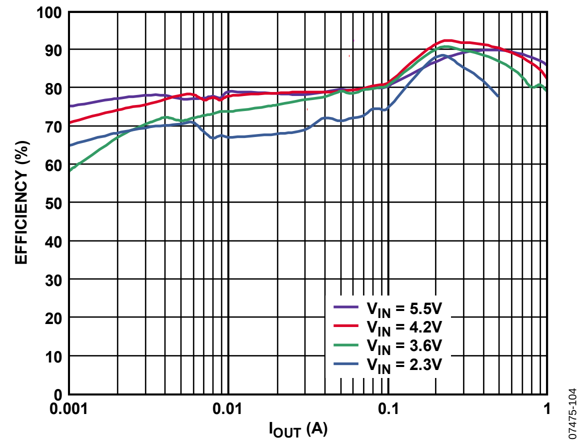

Figure 6. Efficiency vs. Output Current, PSM and PWM Mode (V_{OUT} = 5.0 V)

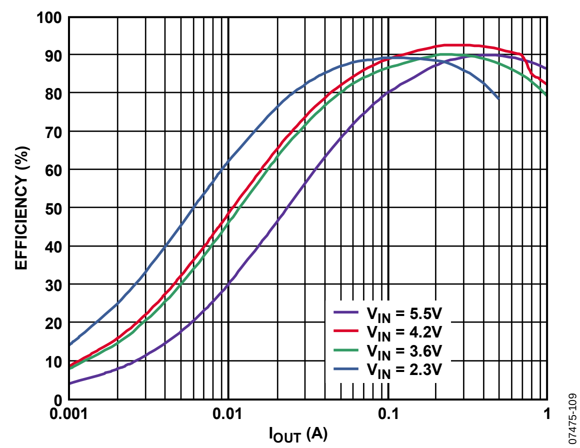

Figure 7. Efficiency vs. Output Current, PWM Mode (V_{OUT} = 3.3 V)

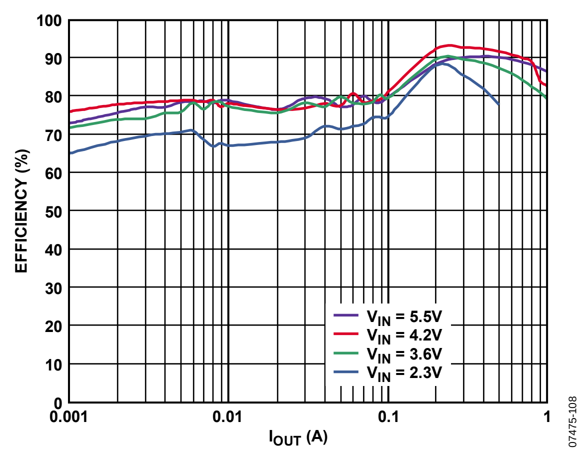

Figure 8. Efficiency vs. Output Current, PSM and PWM Mode (V_{OUT} = 3.3 V)

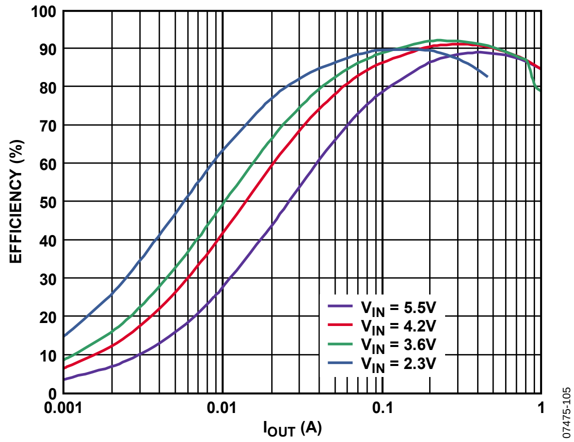

Figure 9. Efficiency vs. Output Current, PWM Mode (V_{OUT} = 2.8 V)

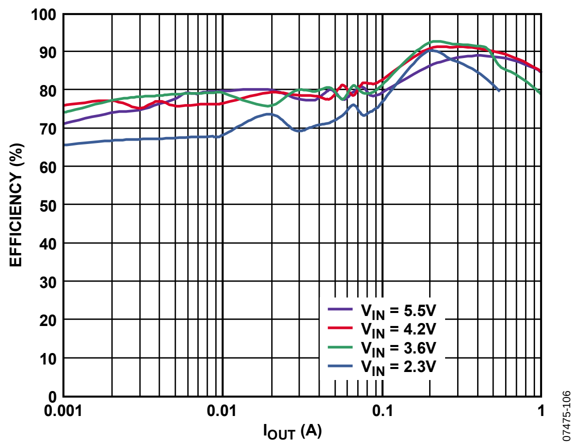

Figure 10. Efficiency vs. Output Current, PSM and PWM Mode (V_{OUT} = 2.8 V)

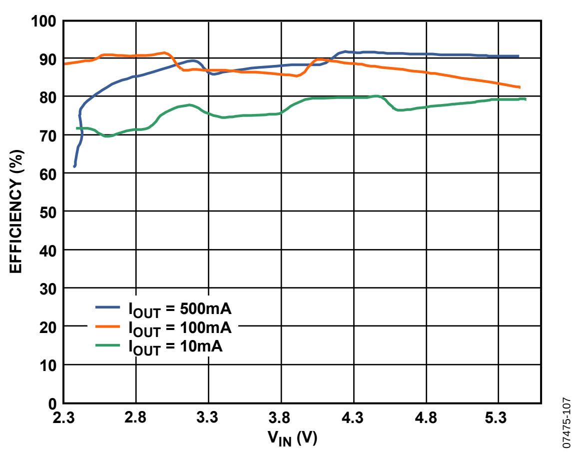

Figure 11. Efficiency vs. Input Voltage (V_{OUT} = 3.3 V)

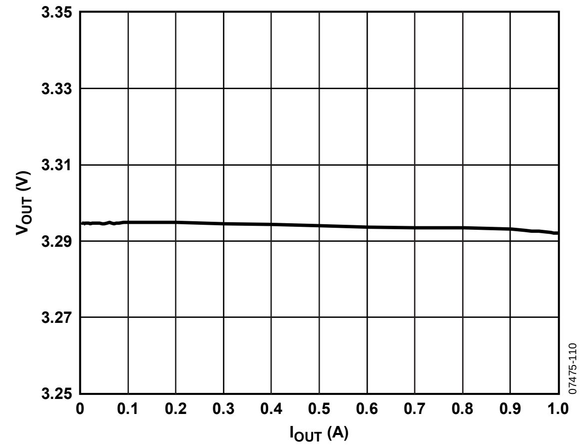

Figure 12. Load Regulation (V_{IN} = 3.6 V, V_{OUT} = 3.3 V)

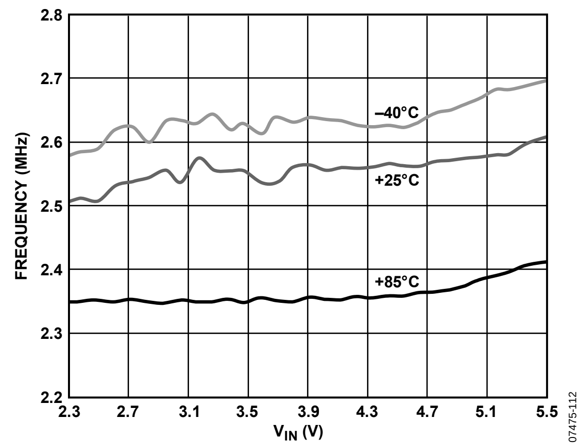

Figure 13. Frequency vs. Input Voltage Over Temperature (V_{OUT} = 3.3 V)

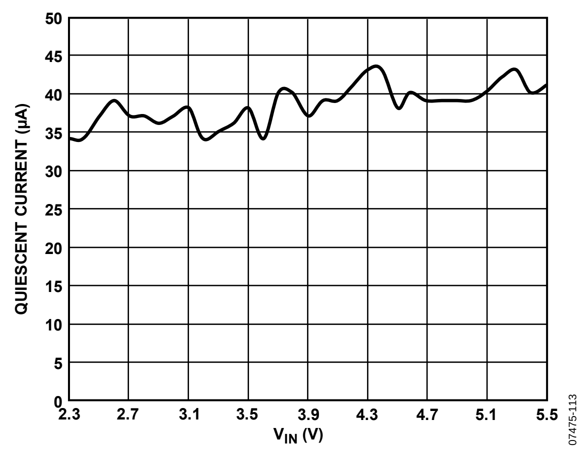

Figure 14. Quiescent Current vs. Input Voltage (V_{OUT} = 3.3 V)

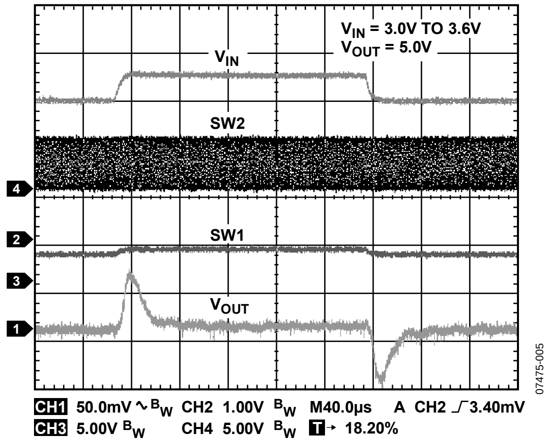

Figure 15. Line Transient, PWM Mode (V_{IN} = 3.0 V to 3.6 V, V_{OUT} = 5.0 V)

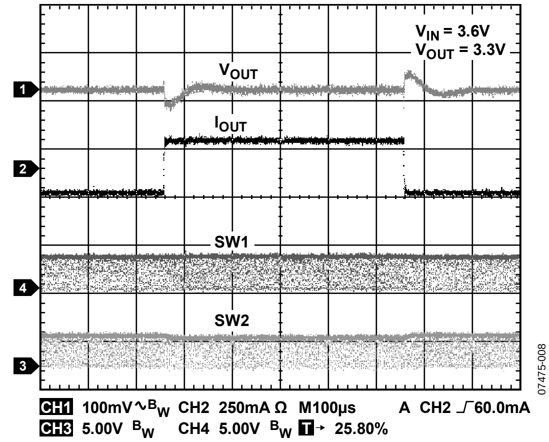

Figure 18. Load Transient (V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 350 mA)

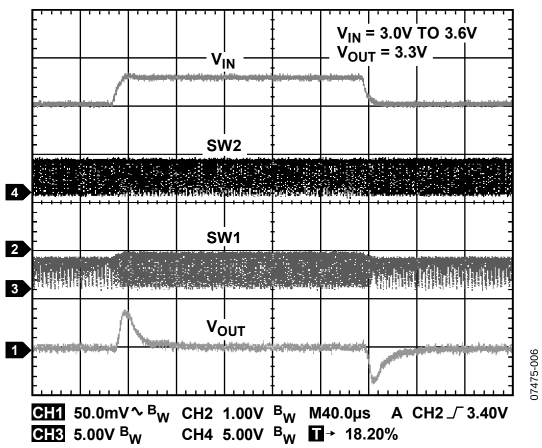

Figure 16. Line Transient, PWM Mode (V_{IN} = 3.0 V to 3.6 V, V_{OUT} = 3.3 V)

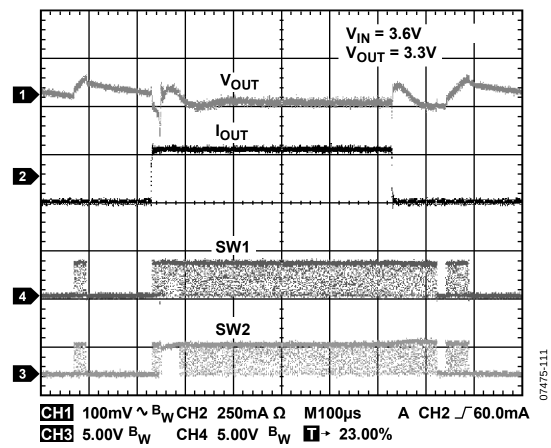

Figure 19. Load Transient (V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA to 300 mA)

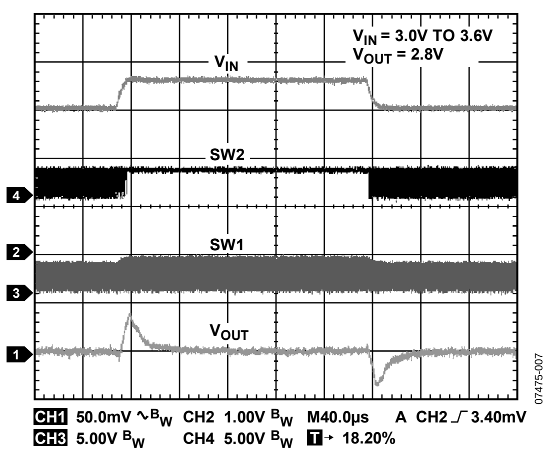

Figure 17. Line Transient, PWM Mode (V_{IN} = 3.0 V to 3.6 V, V_{OUT} = 2.8 V)

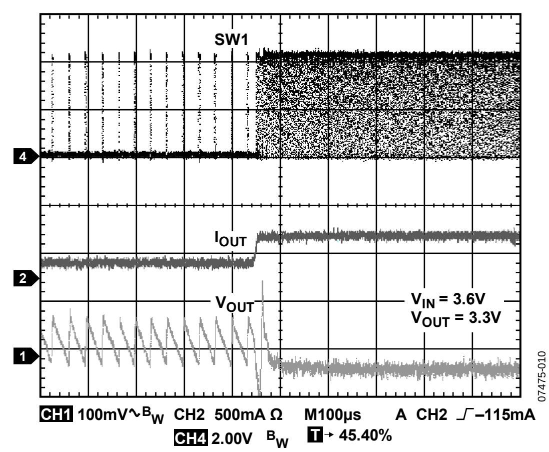

Figure 20. Mode Change by Load Transients, Load Rise (V_{IN} = 3.6 V, V_{OUT} = 3.3 V)

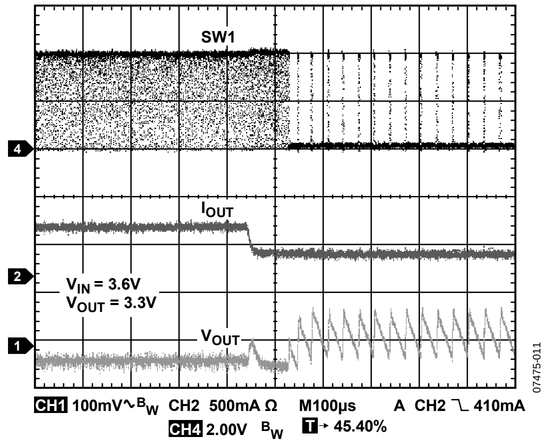

Figure 21. Mode Change by Load Transients, Load Fall (V_{OUT} = 3.3 V)

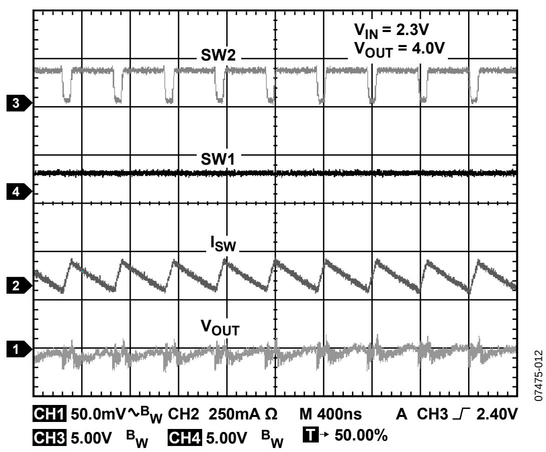

Figure 22. Typical PWM Switching Waveform, Boost Operation (V_{OUT} = 4.0 V)

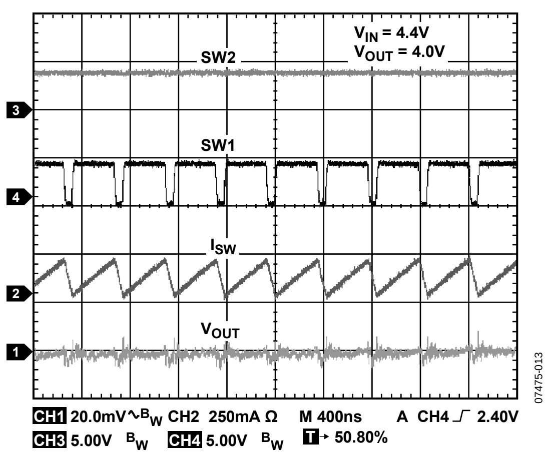

Figure 23. Typical PWM Switching Waveform, Buck Operation (V_{OUT} = 4.0 V)

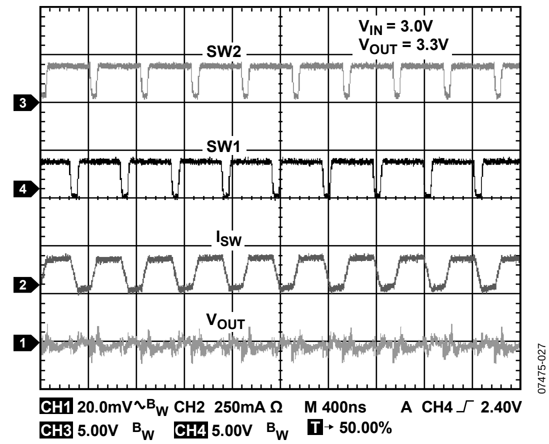

Figure 24. Typical PWM Switching Waveform, Buck-Boost Operation (V_{OUT} = 3.3 V)

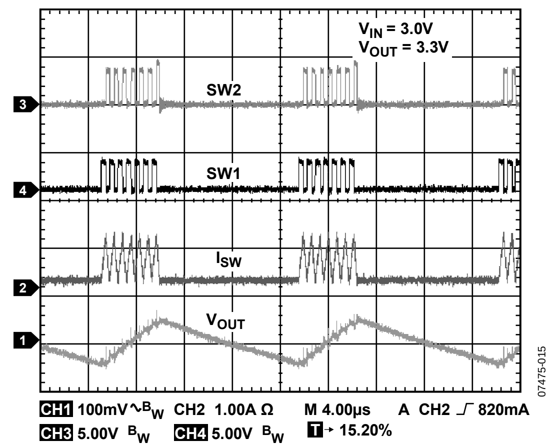

Figure 25. Typical PSM Switching Waveform, Buck-Boost Operation (V_{OUT} = 3.3 V)

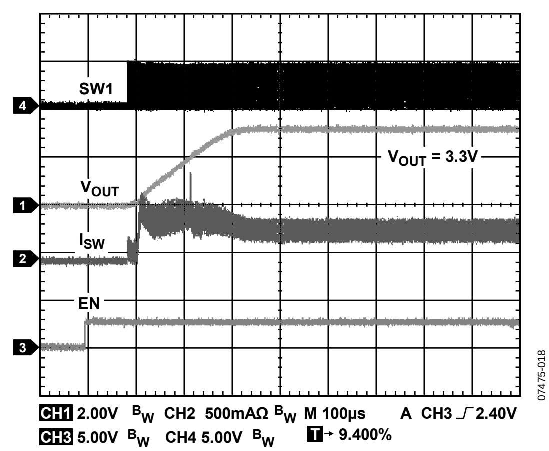

Figure 26. Startup into PWM Mode (V_{OUT} = 3.3 V, I_{OUT} = 300 mA)

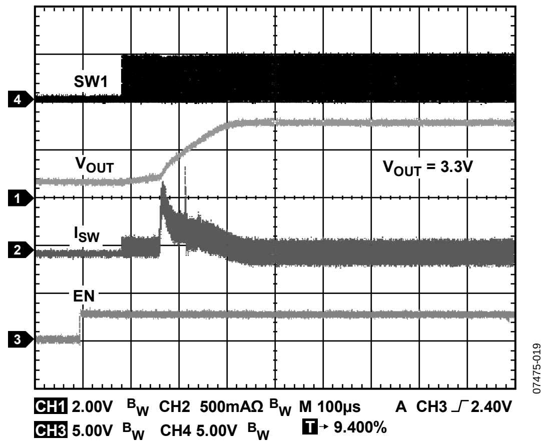

Figure 27. Startup into PWM Mode (V_{OUT} = 3.3 V, I_{OUT} = 10 mA)

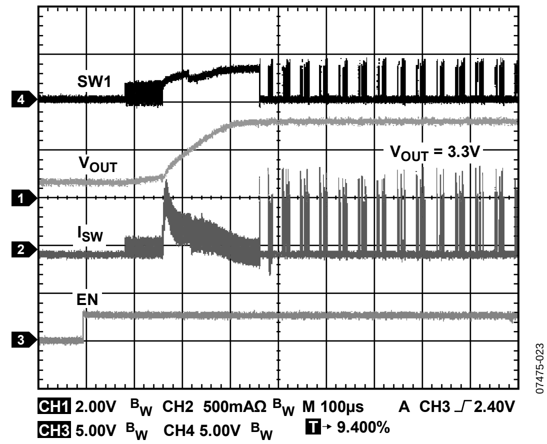

Figure 28. Startup into PSM Mode (V_{OUT} = 3.3 V, I_{OUT} = 10 mA)

THEORY OF OPERATION

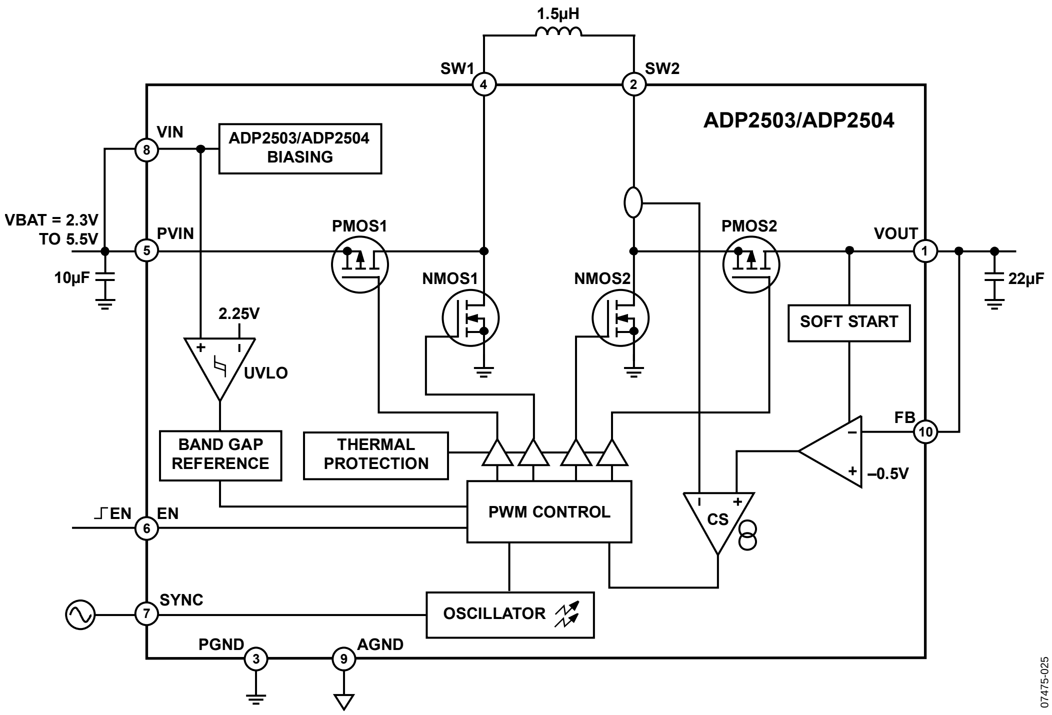

Figure 29. ADP2503/ADP2504 Block Diagram

The ADP2503/ADP2504 are synchronous average current-mode switching buck-boost regulators designed to maintain a fixed output voltage V_{OUT} from an input supply V_{IN} that can be greater than, equal to, or less than V_{OUT}. When V_{IN} is significantly greater than V_{OUT}, the device is in buck mode: PMOS2 is always active, NMOS2 is always off, and the PMOS1 and NMOS1 switches constitute a buck converter. When V_{IN} is significantly lower than V_{OUT}, the device is in boost mode: PMOS1 is always active, NMOS1 is always off, and the NMOS2 and PMOS2 switches constitute a boost converter. When V_{IN} is in the range [V_{OUT} ± 10%], the ADP2503/ADP2504 automatically enter the buck-boost mode. In buck-boost mode, the two operations, buck (PMOS1 and NMOS1 switching in antiphase) and boost (NMOS2 and PMOS2 switching in antiphase), take place at each period of the clock. This is aimed at maintaining the regulation and keeping a minimal current ripple in the inductor to guarantee good transient performances.

POWER SAVE MODE

When the SYNC pin is low, the ADP2503/ADP2504 can operate in power save mode (PSM). In this mode, when the load current becomes less than 75 mA nominally at V_{IN} = 3.6 V, the controller pulls up V_{OUT} and then halts the switching regime until V_{OUT} goes back to a restart value. Then V_{OUT} is pulled up again for a new cycle. This minimizes the switching losses at light load. When the load rises above 150 mA, the ADP2503/ADP2504 revert to fixed PWM mode. This results in about 75 mA of hysteresis between PSM and fixed PWM, preventing oscillations between these two modes.

SOFT START

When the ADP2503/ADP2504 are started, V_{OUT} is ramped from 0 V to its final programmed value in 200 µs (typical). This limits the inrush current to less than 600 mA for a nominal output capacitor of 20 µF. Because the V_{OUT} start-up slope is constant, the inrush current becomes larger if the output capacitor is made larger.

SYNC FUNCTION

When the SYNC pin is high, PSM is deactivated. The ADP2503/ADP2504 always operate in PWM using the internal oscillator. When the SYNC pin is switching in the 2.1 MHz to 2.9 MHz range, the regulator switching frequency slides to the frequency applied on SYNC and then locks on it. When the SYNC pin stops switching, the regulator switching frequency slides back to the internal oscillator frequency.

ENABLE

The device starts operation with soft start when the EN pin is brought high. Pulling the EN pin low forces the device into shutdown, with a typical shutdown current of 0.2 µA.

In this mode, the PMOS power switches are turned off, the NMOS power switches are turned on, and the control circuitry is not enabled. For proper operation, the EN pin must be terminated and must not be left floating.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the power switches under undefined conditions and, therefore, prevents deep discharge of the battery supply. V_{IN} must be greater than 2.25 V to enable the converter. During operation, if V_{IN} drops below 2.10 V, the ADP2503/ADP2504 are disabled until the supply exceeds the UVLO rising threshold.

THERMAL SHUTDOWN

When the junction temperature, T_J, exceeds 150°C typical, the device goes into thermal shutdown. In this mode, the power switches are turned off. The device resumes operation when the junction temperature again falls below 125°C typical.

SHORT-CIRCUIT PROTECTION

When the nominal inductor peak current value of 1.5 A is reached, the ADP2503/ADP2504 first switch off the NMOS2 transistor if it is active. If the current thereafter continues to increase by an extra amount of 200 mA, the PMOS1 transistor is also switched off. This operation is reversible when the short circuit stops. It allows the inductor current ripple to be minimized close to 1.5 A and, thus, the controller to restore V_{OUT} even if a high load current is maintained after the short circuit.

REVERSE CURRENT LIMIT

In case of a short circuit on V_{OUT} to a value greater than expected, the inductor current becomes negative (reverse current). The negative peak value is limited to 1.1 A by deactivating the PMOS2 switch.

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP2503/ADP2504 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and device count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

INDUCTOR SELECTION

The high 2.5 MHz switching frequency of the ADP2503/ADP2504 allows for minimal output voltage ripple, while minimizing inductor size and cost. Careful inductor selection also optimizes efficiency and reduces electromagnetic interference (EMI). The selection of the inductor value determines the inductor current ripple and loop dynamics.

$$\Delta I_L, peak\,(Buck) = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L}$$

$$\Delta I_L, peak\,(Boost) = \frac{(V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{V_{IN}}{f_{OSC} \times L}$$

where:
f_{OSC} is the switching frequency (typically 2.5 MHz).
L is the inductor value in henries.

A larger inductor value reduces the current ripple (and, therefore, the peak inductor current), but is physically larger in size with increased dc resistance. Inductor values between 1 μH and 1.5 μH are suggested. The maximum inductor value to ensure stability is 2.0 μH. For increased efficiency with the ADP2504, it is suggested that a 1.5 μH inductor be used.

The inductor peak current is at the maximum in boost mode. To determine the actual maximum inductor current in boost mode, estimate the input dc current.

$$I_{IN(MAX)} = I_{LOAD(MAX)} \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \frac{1}{\eta}$$

where η is efficiency (assume $\eta \approx 0.85$ to 0.90).

The saturation current rating of the inductor must be at least $I_{IN(MAX)} + \Delta I_{LOAD}/2$.

Ceramic multilayer inductors can be used with lower current designs for a reduced overall solution size and dc resistance (DCR). These are available in low profile packages. Care must be taken because these derate quickly as the inductor value is increased, especially at higher operating temperatures.

Ferrite core inductors have good core loss characteristics as well as reasonable dc resistance. A shielded ferrite inductor reduces the EMI generated by the inductor.

Table 5. Sample of Recommended Inductors

Vendor	Value (μH)	Device No.	DCR (mΩ)	I_{SAT} (A)	Dimensions L × W × H (mm)
Toko	1.2	DE2810C	55	1.7	2.8 × 2.8 × 1.0
Toko	1.5	DE2810C	60	1.5	2.8 × 2.8 × 1.0
Toko	1	MDT2520-CN	100	1.8	2.5 × 2 × 1.2
Murata	1	LQM2HP-G0	55	1.6	2.5 × 2 × 1
Murata	1.5	LQM2HP-G0	70	1.5	2.5 × 2 × 1
TDK	1.0	CPL2512T	90	1.5	2.5 × 1.5 × 1.2
TDK	1.5	CPL2512T	120	1.2	2.5 × 1.5 × 1.2
Coilcraft	1.0	LPS3010	85	1.7	3.0 × 3.0 × 0.9
Coilcraft	1.5	LPS3010	120	1.3	3.0 × 3.0 × 0.9
Taiyo Yuden	1.5	NR3015T1	40	1.5	3.0 × 3.0 × 1.5

Output Capacitor Selection

The output capacitor selection determines the output voltage ripple, transient response, and the loop dynamics of the ADP2503/ADP2504. The output voltage ripple for a given output capacitor is as follows:

$$\Delta V_{OUT}, peak\,(Buck) = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times 8 \times L \times (f_{OSC})^2 \times C_{OUT}}$$

$$\Delta V_{OUT}, peak\,(Boost) = \frac{I_{LOAD} \times (V_{OUT} - V_{IN})}{C_{OUT} \times V_{OUT} \times f_{OSC}}$$

If the ADP2503/ADP2504 are operating in buck mode, the worst-case voltage ripple occurs for the highest input voltage, V_{IN}. If the ADP2503/ADP2504 are operating in boost mode, the worst-case voltage ripple occurs for the lowest input voltage, V_{IN}.

The maximum voltage overshoot, or undershoot, is inversely proportional to the value of the output capacitor. To ensure stability and excellent transient response, it is recommended to use a minimum of 22 μF X5R 6.3 V or 2 × 10 μF X5R 6.3 V capacitors at the output. The effective capacitance (includes temperature and dc bias effects) needed for stability is 14 μF.

Table 6. Recommended Output Capacitors

Vendor	Value	Device No.	Dimensions L × W × H (mm)
Murata	2 × 10 µF, 6.3 V	GRM188R60J106ME47	1.6 × 0.8 × 0.8 (2)
TDK	2 × 10 µF, 6.3 V	C1608JB0J106K	1.6 × 0.8 × 0.8 (2)
Murata	22 µF, 6.3 V	GRM21BR60J226ME39	2 × 1.25 × 1.25
TDK	22 µF, 6.3 V	C2012X5R0J226M	2 × 1.25 × 1.25
TDK	22 µF, 10 V	C3216X5R1A226K	2 × 1.25 × 1.25
Murata	2 × 10 µF, 10 V	GRM21BR71A106KE51L	2 × 1.25 × 1.25 (2)

Input Capacitor Selection

The ADP2503/ADP2504 require an input capacitor to filter noise on the VIN pin, and provide the transient currents while maintaining constant input and output voltage. A 10 µF X5R/X7R ceramic capacitor rated for 6.3 V is the minimum recommended input capacitor. Increased input capacitance reduces the amplitude of the switching frequency ripple on the battery. Because of the dc bias characteristics of ceramic capacitors, a 0603, 6.3 V, X5R/X7R, 10 µF ceramic capacitor is preferable.

Table 7. Recommended Input Capacitors

Vendor	Value	Device No.	Dimensions L × W × H (mm)
Murata	10 µF, 6.3 V	GRM188R60J106ME47	1.6 × 0.8 × 0.8
TDK	10 µF, 6.3 V	C1608JB0J106K	1.6 × 0.8 × 0.8

OUTPUT VOLTAGE PROGRAMMING

The ADP2503/ADP2504 have an adjustable model where the output is programmed through an external resistor divider. The resistor divider is connected between VOUT and FB and between FB and GND; keep the combined total for the resistor divider close to 400 kΩ. The typical voltage reference (V_{REF}) is 500 mV and depending on the output voltage required, the following equation can be used to calculate the value of the resistors:

$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) \times V_{REF}$$

An example of the calculation for a required output voltage of 3.0 V follows.

$$3.0\text{ V} = \left(\frac{360\text{ k}\Omega}{60\text{ k}\Omega}\right) \times 0.5\text{ V}$$

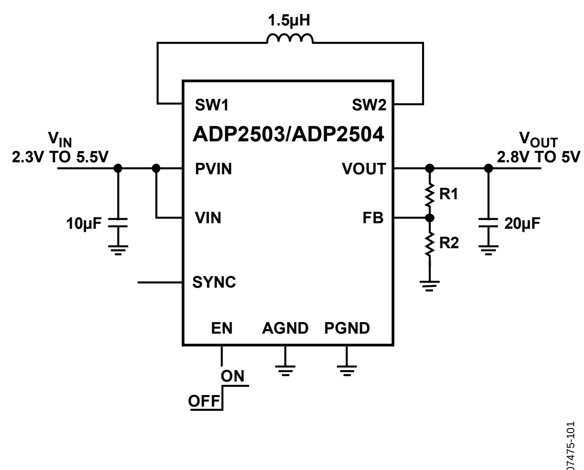

Figure 30. Typical Application Circuit for the Adjustable ADP2503/ADP2504

PCB LAYOUT GUIDELINES

Poor layout can affect ADP2503/ADP2504 performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following rules:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies and large tracks act like antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

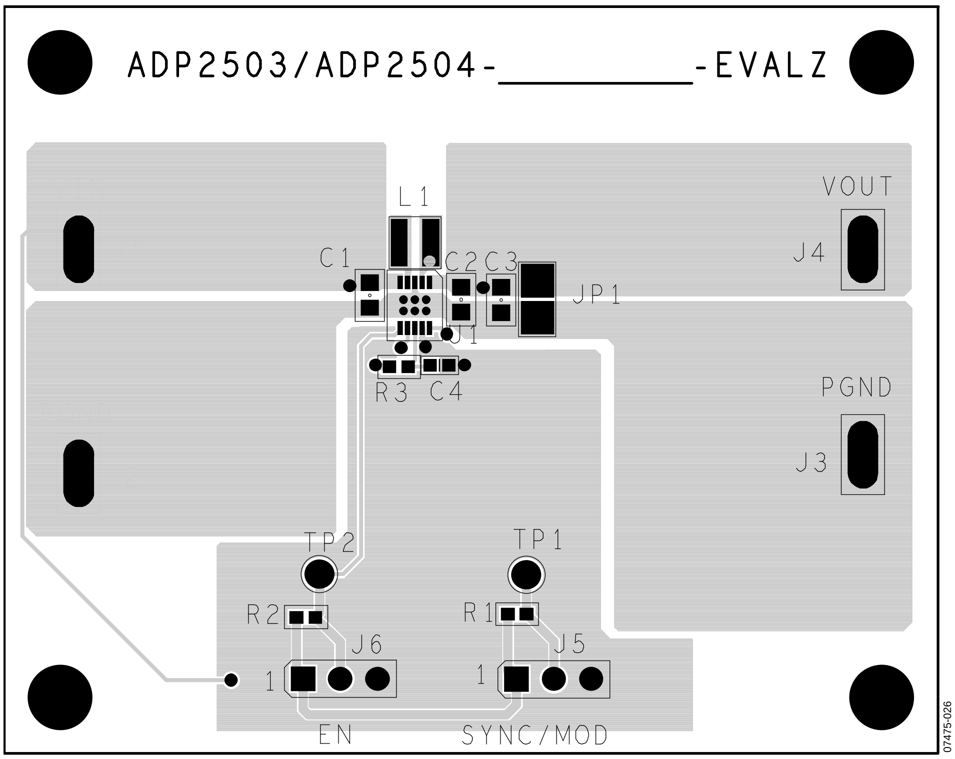

Figure 31. ADP2503/ADP2504 Evaluation Board for Fixed Output Voltages

OUTLINE DIMENSIONS

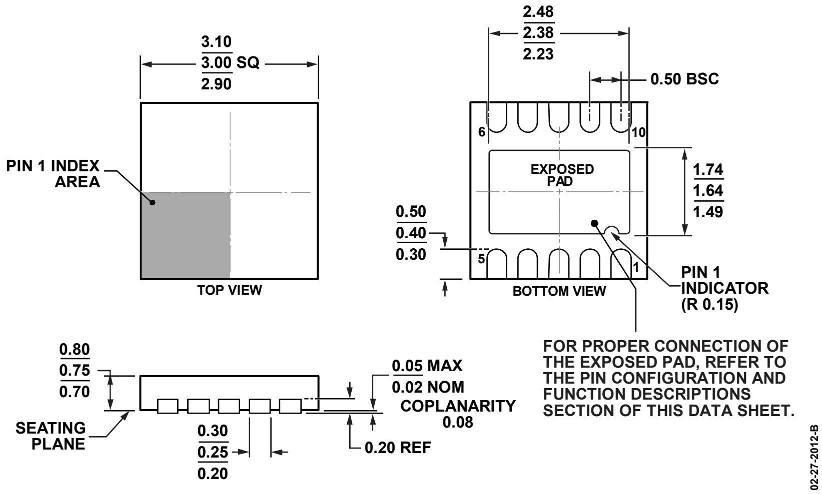

Figure 32. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Voltage	Max Current	Temperature Range	Package Description	Package Option	Branding
ADP2503ACPZ-2.8-R7	2.8 V	0.6 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	L9Y
ADP2503ACPZ-3.3-R7	3.3 V	0.6 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	L9Z
ADP2503ACPZ-3.5-R7	3.5 V	0.6 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LAP
ADP2503ACPZ-4.2-R7	4.2 V	0.6 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LA0
ADP2503ACPZ-4.5-R7	4.5 V	0.6 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LA1
ADP2503ACPZ-5.0-R7	5.0 V	0.6 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LA2
ADP2503ACPZ-R7	Adj	0.6 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LE7
ADP2504ACPZ-2.8-R7	2.8 V	1 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	L9T
ADP2504ACPZ-3.3-R7	3.3 V	1 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	L85
ADP2504ACPZ-3.5-R7	3.5 V	1 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LAN
ADP2504ACPZ-4.2-R7	4.2 V	1 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	L9U
ADP2504ACPZ-4.5-R7	4.5 V	1 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	L9V
ADP2504ACPZ-5.0-R7	5.0 V	1 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	L9W
ADP2504ACPZ-R7	Adj	1 A	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LE8
ADP2503CPZ-REDYKIT				Evaluation Board for Fixed Output Voltages, 3.3 V and 5.0 V		
ADP2504CPZ-REDYKIT				Evaluation Board for Fixed Output Voltages, 2.8 V and 5.0 V		
ADP2503-EVALZ				Evaluation Board		
ADP2504-EVALZ				Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] Redykit contains two evaluation boards with the stated output voltages plus three devices of each available fixed output voltage.