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REVISION HISTORY

8/09—Rev. B to Rev. C	
Updated Format.....	Universal
Changes to Table 1.....	3
Changes to Table 2.....	4
Updated Outline Dimensions	12
Changes to Ordering Guide	13

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $V_L = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter ¹	B Version			T Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C	−40°C to +125°C	+25°C	−55°C to +125°C		
ANALOG SWITCH							
Analog Signal Range	V _{SS} to V _{DD}			V _{SS} to V _{DD}			
R _{ON}	25			25		Ω typ	V _D = ±12.5 V, I _S = −10 mA
	35	45	45	35	45	Ω max	V _{DD} = +13.5 V, V _{SS} = −13.5 V
LEAKAGE CURRENTS							
Source Off Leakage, I _S (Off)	±0.1			±0.1		nA typ	V _{DD} = +16.5 V, V _{SS} = −16.5 V
Drain Off Leakage, I _D (Off)	±0.25	±5	±15	±0.25	±15	nA max	V _D = ±15.5 V, V _S = ∓15.5 V; see Figure 12
	±0.1			±0.1		nA typ	V _D = ±15.5 V, V _S = ∓15.5 V; see Figure 12
Channel On Leakage, I _D , I _S (On)	±0.75	±5	±30	±0.75	±30	nA max	V _S = V _D = ±15.5 V; see Figure 13
	±0.4			±0.4		nA typ	
	±0.75	±5	±30	±0.75	±30	nA max	
DIGITAL INPUTS							
Input High Voltage, V _{INH}	2.4			2.4		V min	
Input Low Voltage, V _{INL}	0.8			0.8		V max	
Input Current							
I _{INL} or I _{INH}	±0.005			±0.005		μA typ	V _{IN} = V _{INL} or V _{INH}
	±0.5			±0.5		μA max	
DYNAMIC CHARACTERISTICS ²							
t _{TRANSITION}	160	200	200	145	200	ns max	R _L = 300 Ω, C _L = 35 pF; V _{S1} = ±10 V, V _{S2} = ∓10 V; see Figure 14
Break-Before-Make Time Delay, t _D	30			30		ns typ	R _L = 300 Ω, C _L = 35 pF; V _{S1} = V _{S2} = ±10 V; see Figure 15
Off Isolation	5			5		ns min	
Channel-to-Channel Crosstalk	80			80		dB typ	R _L = 50 Ω, f = 1 MHz; see Figure 16
C _S (Off)	90			70		dB typ	R _L = 50 Ω, f = 1 MHz; see Figure 17
C _D , C _S (On)	6			6		pF typ	f = 1 MHz
	55			55		pF typ	f = 1 MHz
POWER REQUIREMENTS							
I _{DD}	0.0001			0.0001		μA typ	V _{DD} = +16.5 V, V _{SS} = −16.5 V
	1	2.5	2.5	1	2.5	μA max	V _{IN} = 0 V or 5 V
I _{SS}	0.0001			0.0001		μA typ	
	1	2.5	2.5	1	2.5	μA max	
I _L	0.0001			0.0001		μA typ	V _L = 5.5 V
	1	2.5	2.5	1	2.5	μA max	

¹ Temperature ranges are as follows: B Version: -40°C to $+125^\circ\text{C}$; T Version: -55°C to $+125^\circ\text{C}$.

² Guaranteed by design, not subject to production test.

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SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $V_L = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter ¹	B Version			T Version		Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C	–40°C to +125°C	+25°C	–55°C to +125°C		
ANALOG SWITCH							
Analog Signal Range			0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	40			40		Ω typ	$V_D = 3\text{ V}$, 8.5 V , $I_S = -10\text{ mA}$
		60	70		70	Ω max	$V_{DD} = 10.8\text{ V}$
LEAKAGE CURRENT							
Source OFF Leakage, I_S (Off)	± 0.1			± 0.1		nA typ	$V_{DD} = 13.2\text{ V}$
	± 0.25	± 5	± 15	± 0.25	± 15	nA max	$V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$;
Drain OFF Leakage, I_D (Off)	± 0.1			± 0.1		nA typ	see Figure 12
	± 0.75	± 5	± 30	± 0.75	± 30	nA max	$V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$;
Channel ON Leakage, I_D , I_S (On)	± 0.4			± 0.4		nA typ	see Figure 12
	± 0.75	± 5	± 30	± 0.75	± 30	nA max	$V_S = V_D = 12.2\text{ V}/1\text{ V}$; see Figure 13
DIGITAL INPUTS							
Input High Voltage, V_{INH}		2.4	2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8	0.8		0.8	V max	
Input Current							
I_{INL} or I_{INH}		± 0.005	± 0.005		± 0.005	μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.5	± 0.5		± 0.5	μA max	
DYNAMIC CHARACTERISTICS ²							
$t_{TRANSITION}$	180	250	250	170	250	ns max	$R_L = 300\Omega$, $C_L = 35\text{ pF}$; $V_{S1} = 0\text{ V}/8\text{ V}$, $V_{S2} = 8\text{ V}/0\text{ V}$; see Figure 14
Break-Before-Make Time Delay, t_D	60			60		ns typ	$R_L = 300\Omega$, $C_L = 35\text{ pF}$;
							$V_{S1} = V_{S2} = 8\text{ V}$; see Figure 15
Off Isolation	80			80		dB typ	$R_L = 50\Omega$, $f = 1\text{ MHz}$; see Figure 16
Channel-to-Channel Crosstalk	90			70		dB typ	$R_L = 50\Omega$, $f = 1\text{ MHz}$; see Figure 17
C_S (Off)	13			13		pF typ	$f = 1\text{ MHz}$
C_D , C_S (On)	65			65		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS							
I_{DD}	0.0001			0.0001		μA typ	$V_{DD} = 13.2\text{ V}$
	1	2.5	2.5	1	2.5	μA max	$V_{IN} = 0\text{ V}$ or 5 V
I_L	0.0001			0.0001		μA typ	$V_L = 5.5\text{ V}$
	1	2.5	2.5	1	2.5	μA max	

¹ Temperature ranges are as follows: B Version: –40°C to +125°C; T Version: –55°C to +125°C.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	$-0.3\text{ V to }+25\text{ V}$
V_{SS} to GND	$+0.3\text{ V to }-25\text{ V}$
V_L to GND	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$
Analog, Digital Inputs ¹	$V_{SS} - 2\text{ V to }V_{DD} + 2\text{ V}$ or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	100 mA
Operating Temperature Range	
Industrial (B Version)	$-40^\circ\text{C to }+125^\circ\text{C}$
Extended (T Version)	$-55^\circ\text{C to }+125^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	150°C
CERDIP Package, Power Dissipation	600 mW
θ_{JA} , Thermal Impedance	110°C/W
Lead Temperature, Soldering (10 sec)	300°C
PDIP Package, Power Dissipation	400 mW
θ_{JA} , Thermal Impedance	100°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	400 mW
θ_{JA} , Thermal Impedance	155°C/W
MSOP Package, Power Dissipation	315 mW
θ_{JA} , Thermal Impedance	205°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

¹Overvoltages at IN, S or D is clamped by internal diodes. Limit current to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

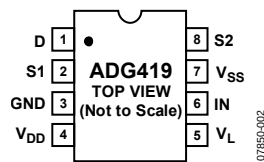


Figure 2. Pin Configuration

Table 4. Pin Function Description

Pin No.	Mnemonic	Description
1	D	Drain terminal. May be an input or an output.
2	S1	Source terminal. May be an input or an output.
3	GND	Ground (0 V) reference.
4	V _{DD}	Most positive power supply potential.
5	V _L	Logic power supply (5 V).
6	IN	Logic control input.
7	V _{SS}	Most negative power supply potential in dual-supply applications. In single-supply applications, it may be connected to GND.
8	S2	Source terminal. May be an input or an output.

Table 5. Truth Table

Logic	Switch 1	Switch 2
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

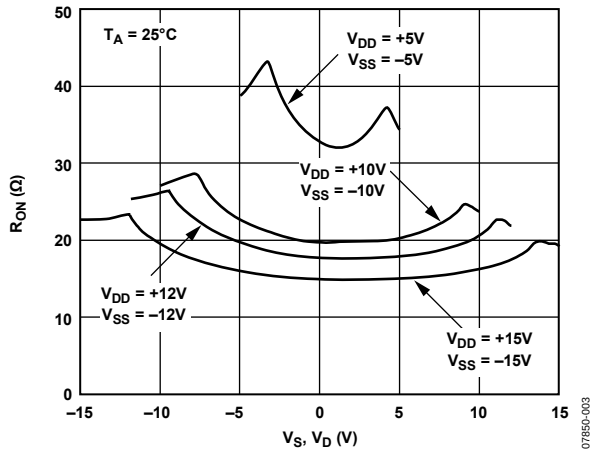


Figure 3. R_{ON} as a Function of V_D (V_S), Dual-Supply Voltage

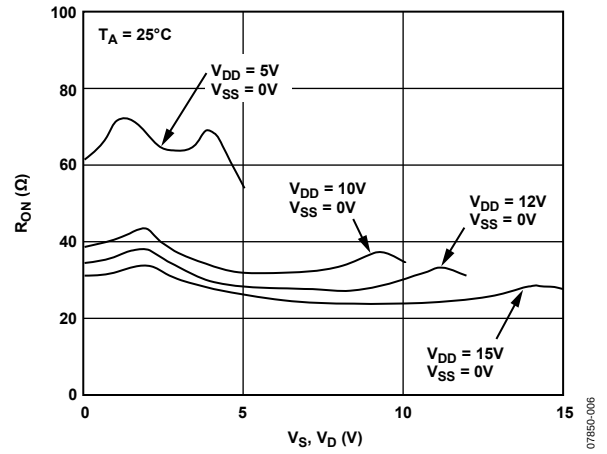


Figure 6. R_{ON} as a Function of V_D (V_S), Single-Supply Voltage

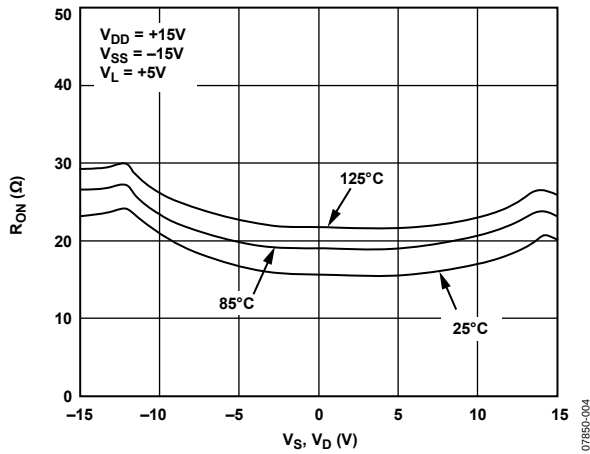


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

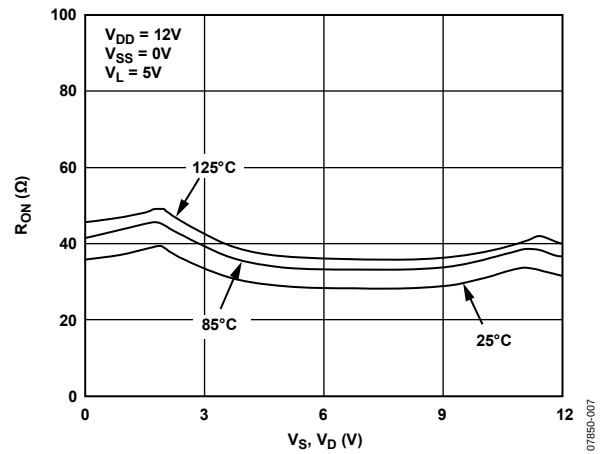


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures

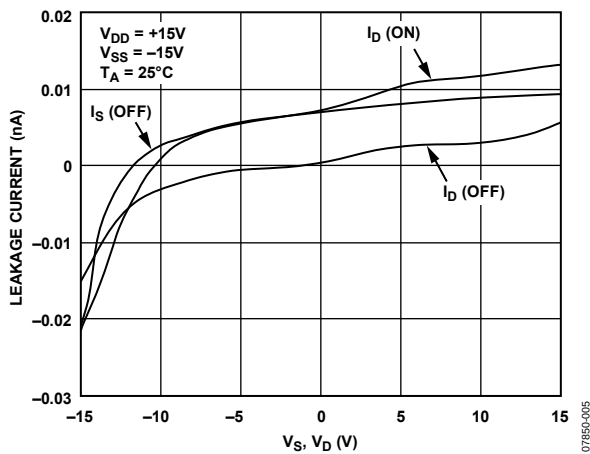


Figure 5. Leakage Currents as a Function of V_S (V_D)

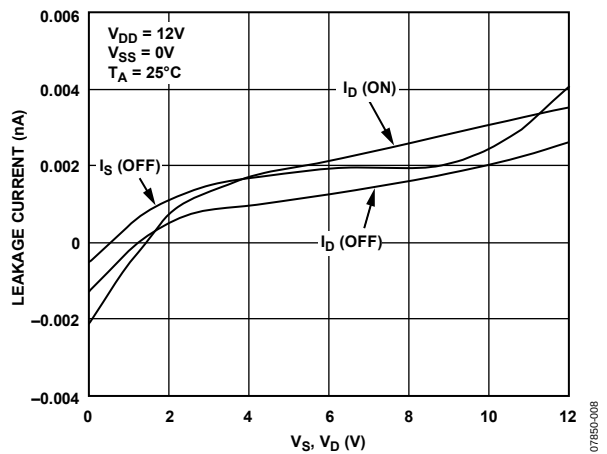


Figure 8. Leakage Currents as a Function of V_S (V_D)

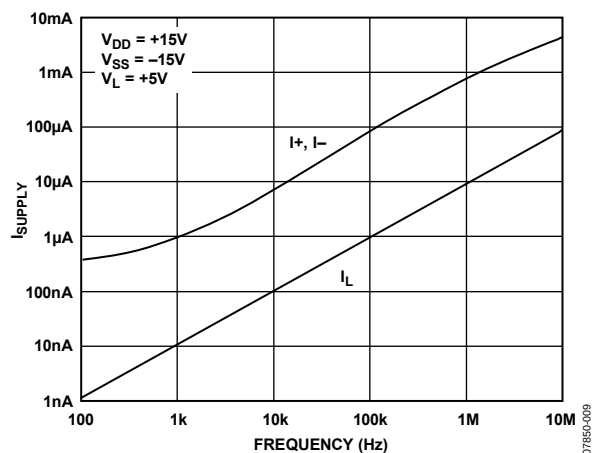


Figure 9. Supply Current (I_{SUPPLY}) vs. Input Switching Frequency

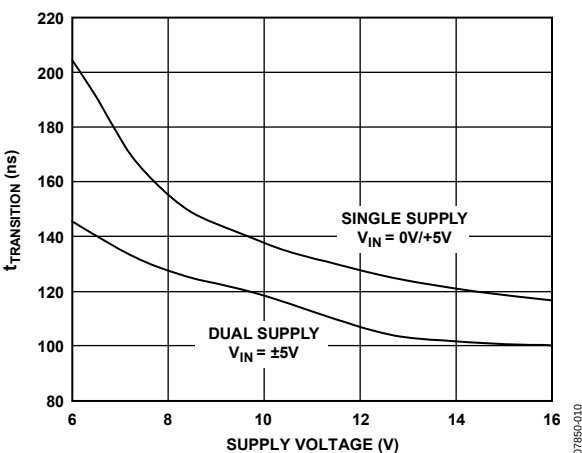


Figure 10. Transition Time ($t_{TRANSITION}$) vs. Power Supply Voltage

TEST CIRCUITS

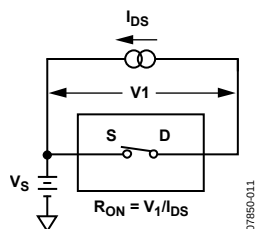


Figure 11. On Resistance

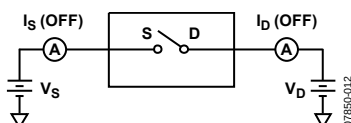


Figure 12. Off Leakage

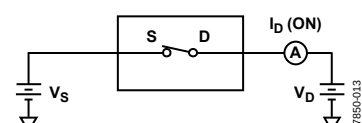


Figure 13. On Leakage

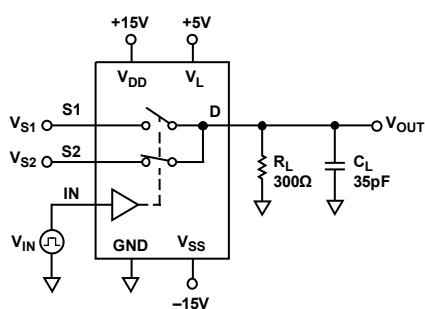


Figure 14. Transition Time, $t_{\text{TRANSITION}}$

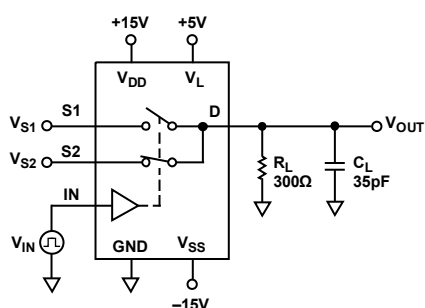
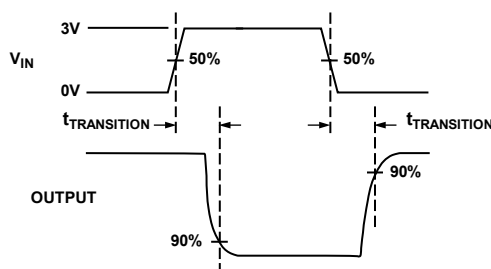
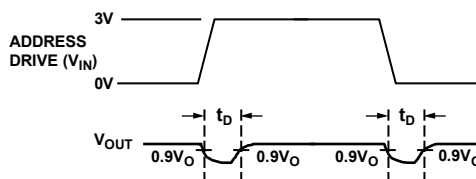


Figure 15. Break-Before-Make Time Delay, t_D



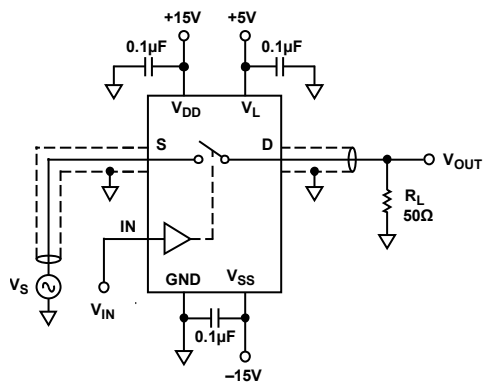
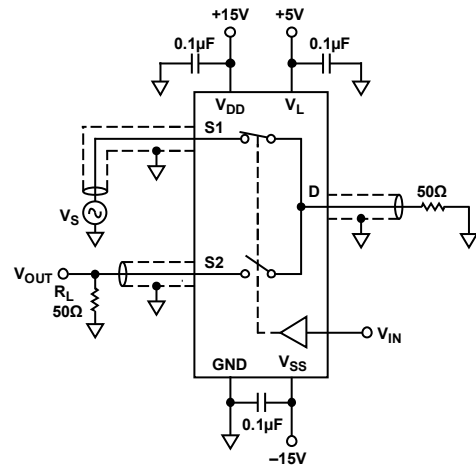


Figure 16. Off Isolation

071950-016



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \log |V_S/V_{OUT}|$$

Figure 17. Crosstalk

071950-017

TERMINOLOGY

V_{DD}

Most positive power supply potential.

V_{SS}

Most negative power supply potential in dual-supply applications.
In single-supply applications, it may be connected to GND.

V_L

Logic power supply (5 V).

GND

Ground (0 V) reference.

S

Source terminal. May be an input or an output.

D

Drain terminal. May be an input or an output.

IN

Logic control input.

R_{ON}

Ohmic resistance between D and S.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_D (V_S)

Analog voltage on terminals D, S.

C_S (Off)

Off switch source capacitance.

C_D, C_S (On)

On switch capacitance.

t_{TRANSITION}

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

Off time or on time measured between the 90% points of both switches when switching from one address state to the other.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off channel.

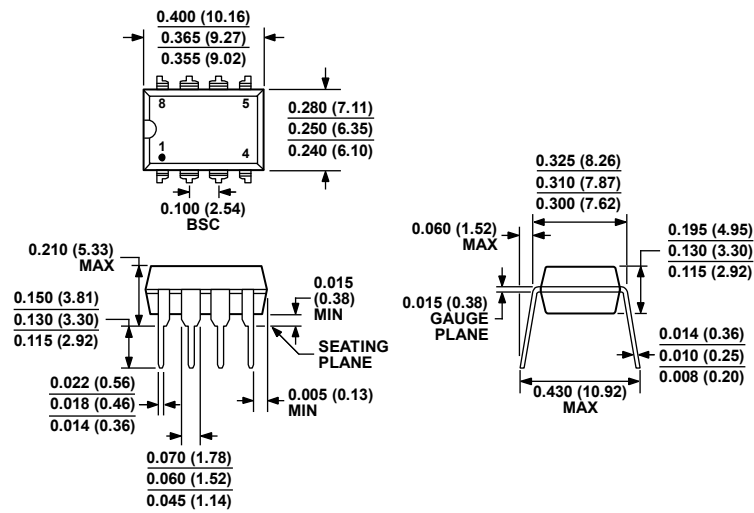
I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

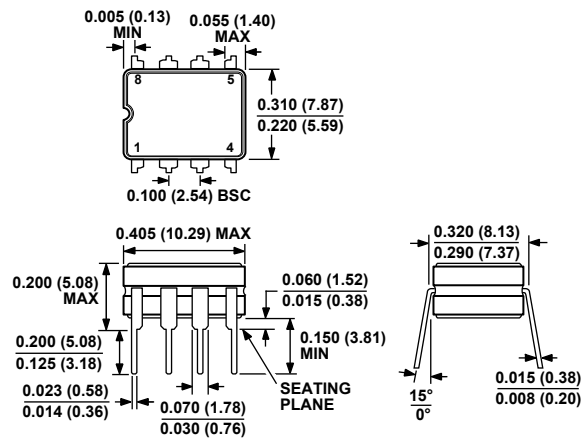
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 18. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)

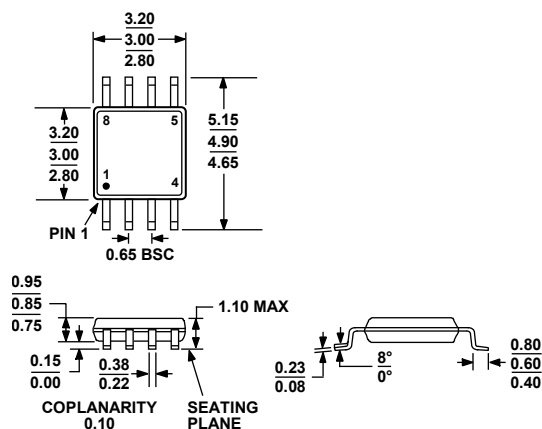
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)

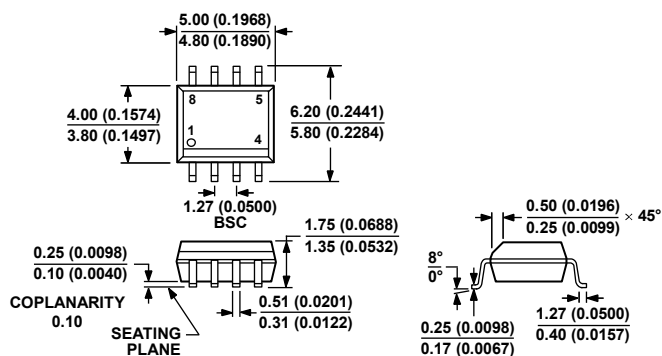
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 20. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 21. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG419BN	-40°C to +125°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
ADG419BNZ ¹	-40°C to +125°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
ADG419BR	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BR-REEL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BR-REEL7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ-REEL ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ-REEL7 ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRM	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRM-REEL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRM-REEL7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRMZ ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419BRMZ-REEL ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419BRMZ-REEL7 ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419TQ	-55°C to +125°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8	

¹ Z = RoHS Compliant Part, # denotes that RoHS compliant part is top or bottom marked.

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