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REVISION HISTORY

2/13—Rev. B to Rev. C

Removed TO-8 Package ... Universal
Changed Input Voltage Noise 13 nV/√Hz to 15 nV/√Hz and
Changes to General Description Section ... 1
Changes to Endnote 1, Table 1 ... 4
Added Operating Temperature Range, Table 2 ... 5
Deleted Using a Heat Sink Section ... 11
Updated Outline Dimensions ... 13
Added Ordering Guide ... 14

11/88—Rev. A to Rev. B

SPECIFICATIONS

T_A = 25°C and ±15 V dc, unless otherwise noted. All minimum and maximum specifications are guaranteed.

Table 1.

Parameter	Test Conditions/ Comments	AD841J			AD841K			AD841S[1]			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[2]			0.8	2.0		0.5	1.0		0.5	2.0	mV
	T_{MIN} – T_{MAX}			5.0			3.3		5.5		mV
Offset Drift			35			35			35		µV/°C
INPUT BIAS CURRENT			3.5	8		3.5	5		3.5	8	µA
	T_{MIN} – T_{MAX}			10			6			12	µA
Input Offset Current			0.1	0.4		0.1	0.2		0.1	0.4	µA
	T_{MIN} – T_{MAX}			0.5			0.3			0.6	µA
INPUT CHARACTERISTICS	Differential mode										
Input Resistance			200			200			200		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10	12		±10	12		±10	12		V
Common-Mode Rejection	V_{CM} = ±10 V	86	100		103	109		86	110		dB
	T_{MIN} – T_{MAX}	80			100			80			dB
INPUT VOLTAGE NOISE	f = 1 kHz		15			15			15		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		47			47			47		µV rms
OPEN-LOOP GAIN	V_{OUT} = ±10 V										
	R_{LOAD} ≥ 500 Ω	25	45		25	45		25	45		V/mV
	T_{MIN} – T_{MAX}	12			20			12			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 500 Ω										
	T_{MIN} – T_{MAX}	±10			±10			±10			V
Current	V_{OUT} = ±10 V	50			50			50			mA
OUTPUT RESISTANCE	Open loop		5			5			5		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p-p		40			40			40		MHz
Full Power Bandwidth[3]	V_{OUT} = 20 V p-p										
	R_{LOAD} ≥ 500 Ω	3.1	4.7		3.1	4.7		3.1	4.7		MHz
Rise Time[4]	A_V = –1		10			10			10		ns
Overshoot[4]	A_V = –1		10			10			10		%
Slew Rate[4]	A_V = –1	200	300		200	300		200	300		V/µs
Settling Time 10 V Step	A_V = –1										
	to 0.1%		90			00			90		ns
	to 0.01%		110			110			110		ns
OVERDRIVE RECOVERY	–Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.03			0.03			0.03		%
Differential Phase	f = 4.4 MHz		0.022			0.022			0.022		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			11	12		11	12		11	12	mA
	T_{MIN} – T_{MAX}			14			14			16	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	86	100		90	100		86	100		dB
	T_{MIN} – T_{MAX}	80			86			80			dB

Parameter	Test Conditions/ Comments	AD841J			AD841K			AD841S[1]			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TEMPERATURE RANGE											
Rated Performance[5]		0		70	0		70	−55		+125	°C

[1] Standard military drawing available: 5962-89641012A – (SE/883B).
[2] Input offset voltage specifications are guaranteed after 5 minutes at T_A = 25°C.
[3] Full power bandwidth = slew rate/2 π V_{PEAK}.
[4] Refer to Figure 22 to Figure 24.
[5] S grade T_{MIN} – T_{MAX} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_S)	±18 V
Internal Power Dissipation[1]	
PDIP (N-14)	1.5 W
CERDIP (Q-14)	1.3 W
Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Storage Temperature Range	
Q-14	−65°C to +150°C
N-14	−65°C to +125°C
Operating Temperature Range	
AD841J/AD841K	0°C to 70°C
AD841S	−55°C to +125°C
Junction Temperature	+175°C
Lead Temperature Range (Soldering 60 sec)	+300°C

[1] Maximum internal power dissipation is specified so that T_J does not exceed 175°C at an ambient temperature of 25°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Table 3.

Package Type	θ_{JC}	θ_{JA}	θ_{SA}	Unit
14-Lead CERDIP	35	110	38	°C/W
14-Lead PDIP	30	100		°C/W
20-Lead LCC	35	150		°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

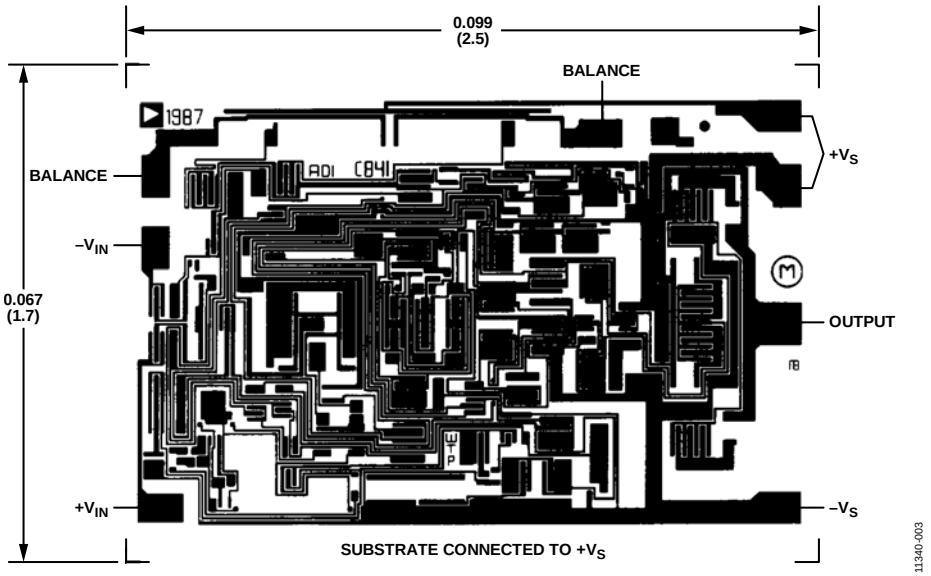


Figure 3. Metalization Photograph
Contact factory for latest dimensions
Dimensions shown in inches and (millimeters)

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C and V_S = ±15 V, unless otherwise noted.

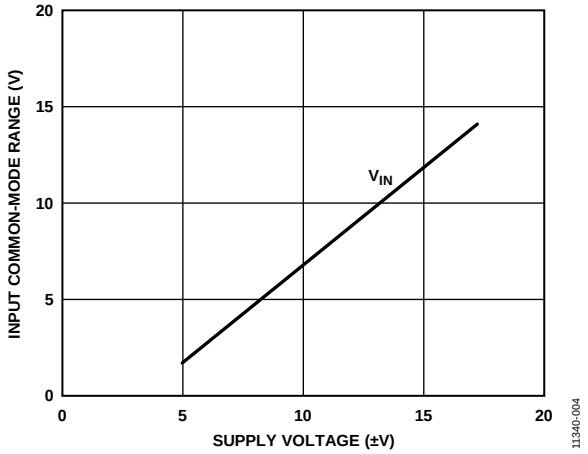


Figure 4. Input Common-Mode Range vs. Supply Voltage

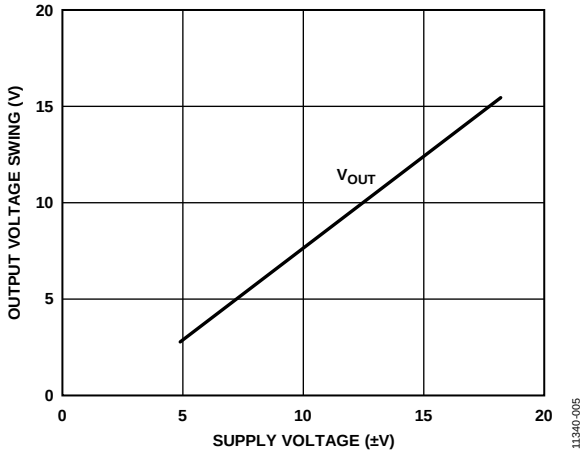


Figure 5. Output Voltage Swing vs. Supply Voltage

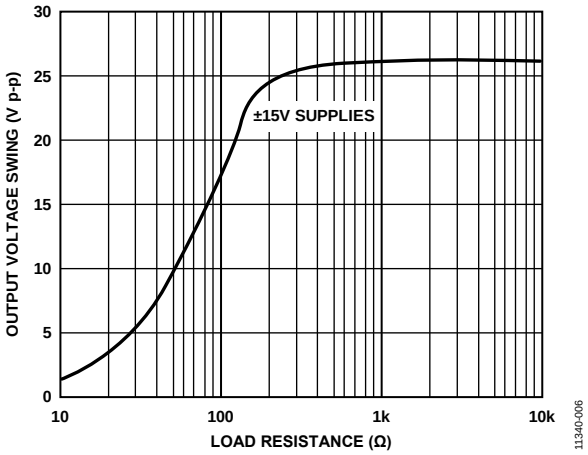


Figure 6. Output Voltage Swing vs. Load Resistance

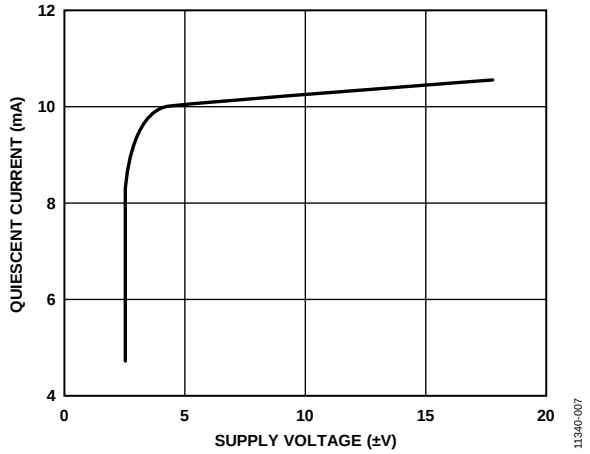


Figure 7. Quiescent Current vs. Supply Voltage

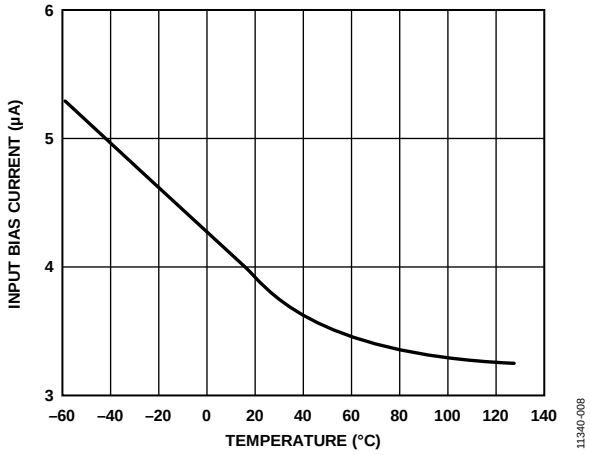


Figure 8. Input Bias Current vs. Temperature

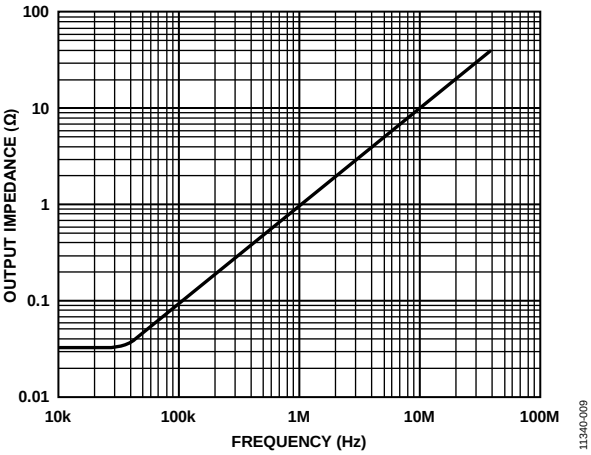


Figure 9. Output Impedance vs. Frequency

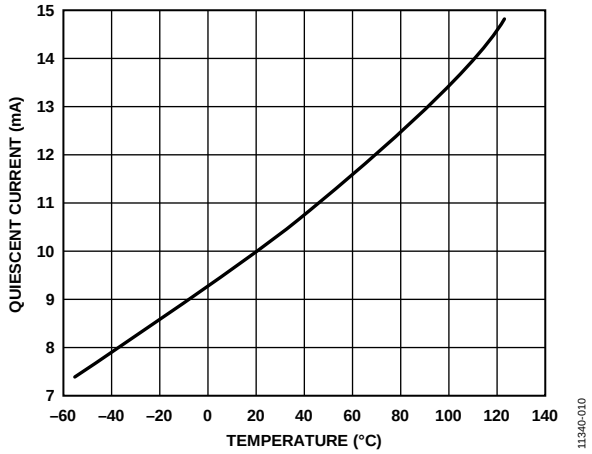


Figure 10. Quiescent Current vs. Temperature

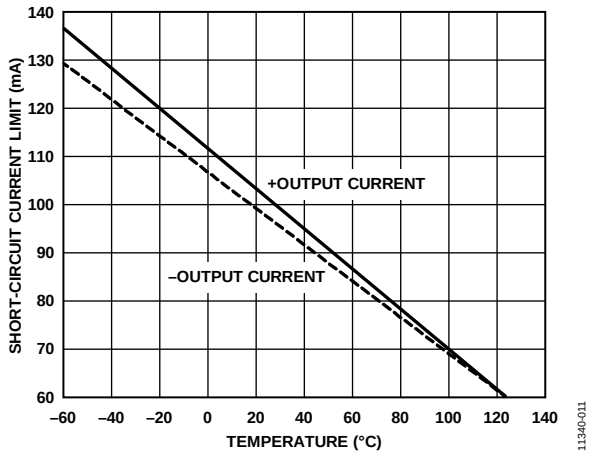


Figure 11. Short-Circuit Current Limit vs. Temperature

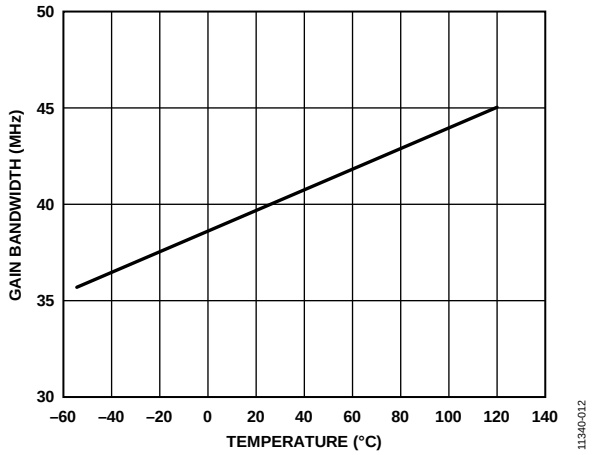


Figure 12. Gain Bandwidth Product vs. Temperature

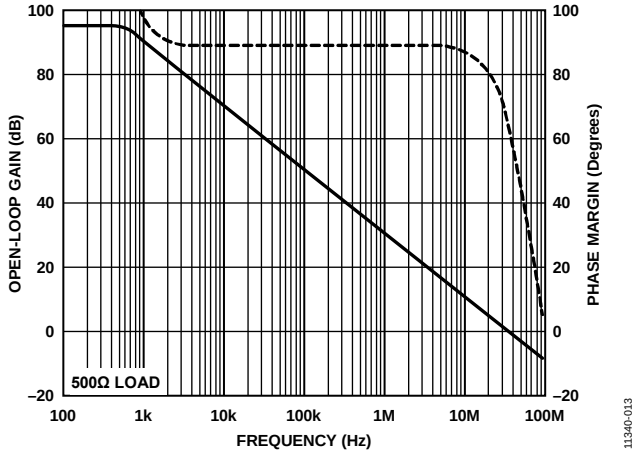


Figure 13. Open-Loop Gain and Phase Margin vs. Frequency

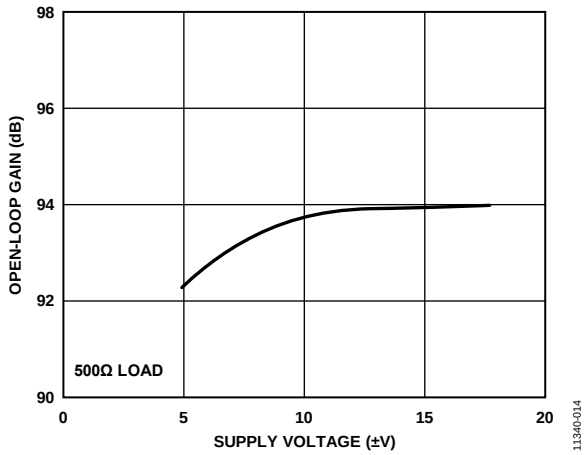


Figure 14. Open-Loop Gain vs. Supply Voltage

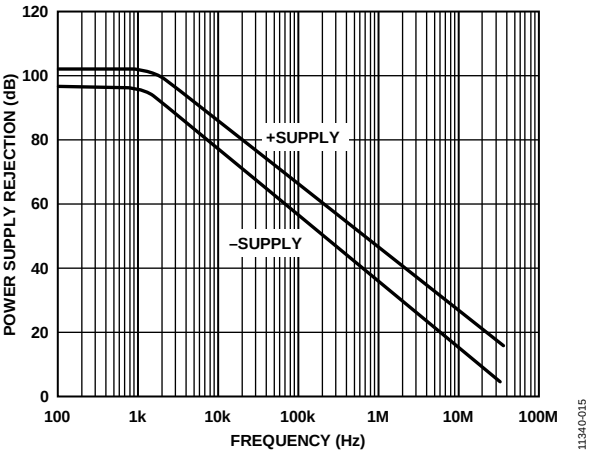


Figure 15. Power Supply Rejection vs. Frequency

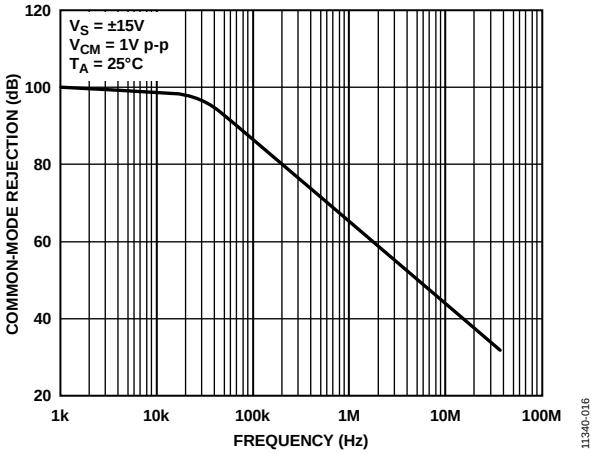


Figure 16. Common-Mode Rejection vs. Frequency

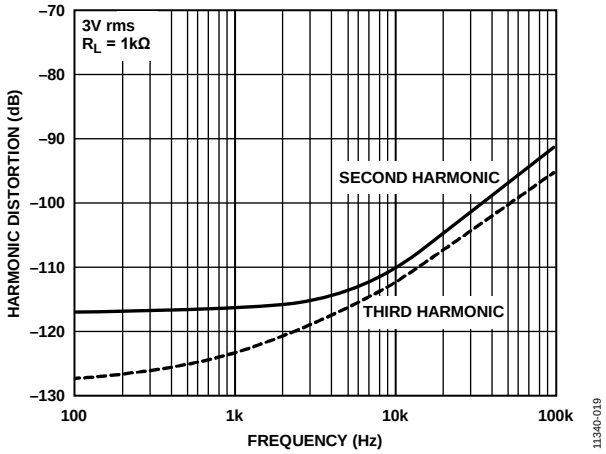


Figure 19. Harmonic Distortion vs. Frequency

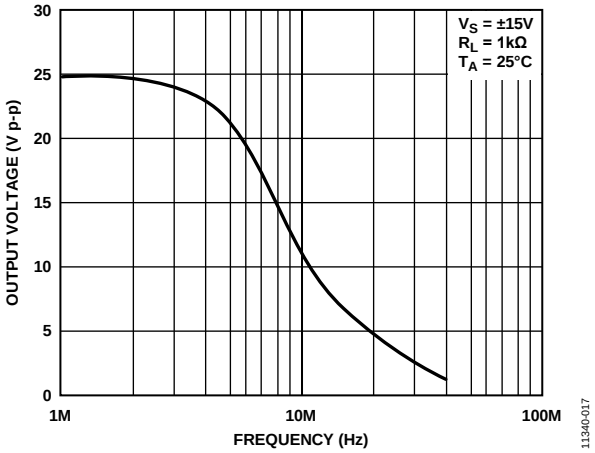


Figure 17. Large Signal Frequency Response

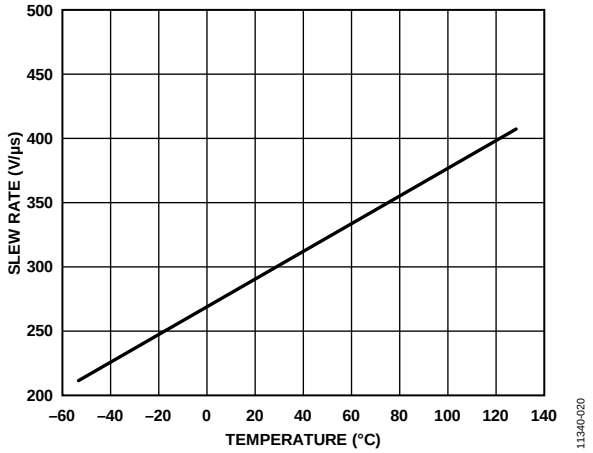


Figure 20. Slew Rate vs. Temperature

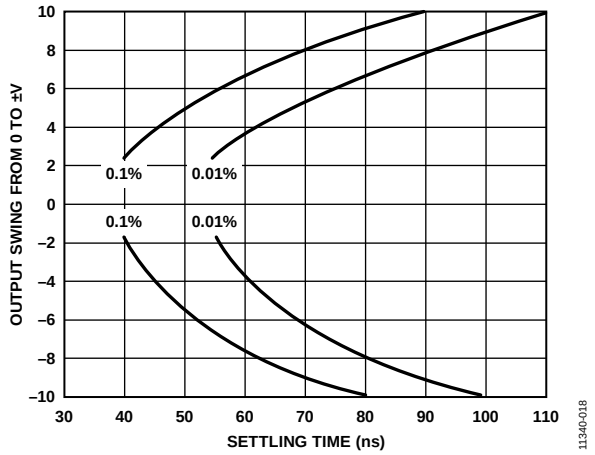


Figure 18. Output Swing and Error vs. Settling Time

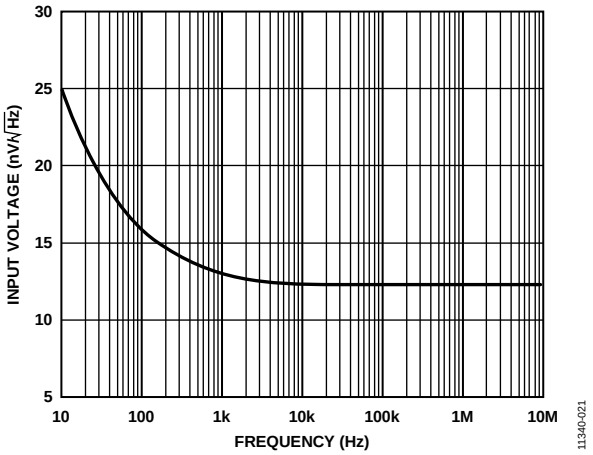


Figure 21. Input Voltage Noise Spectral Density

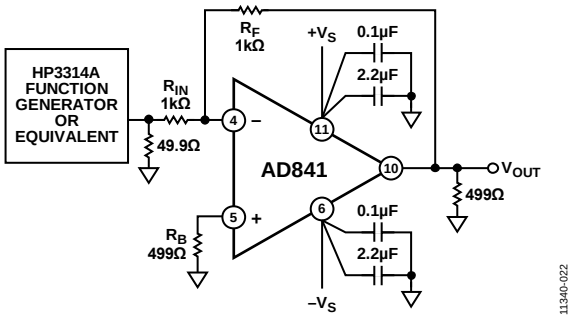


Figure 22. Inverting Amplifier Configuration (PDIP Pinout)

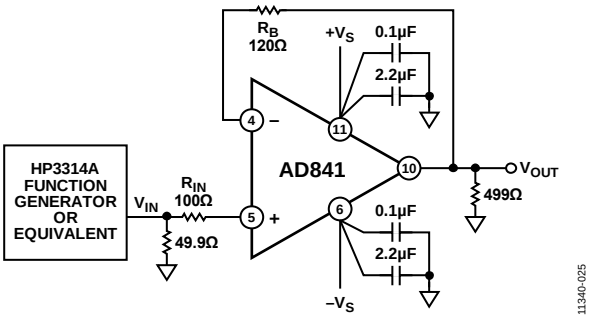


Figure 25. Unity-Gain Buffer Amplifier Configuration (PDIP Pinout)

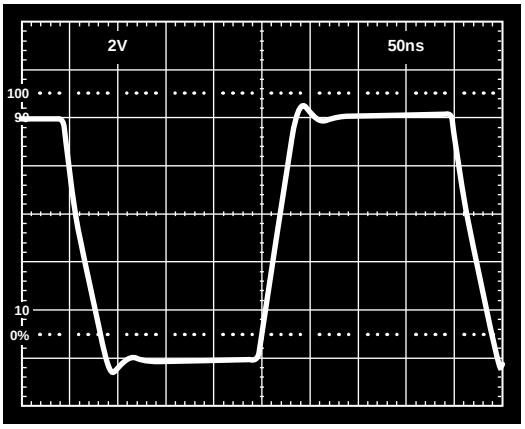


Figure 23. Inverter Large Signal Pulse Response

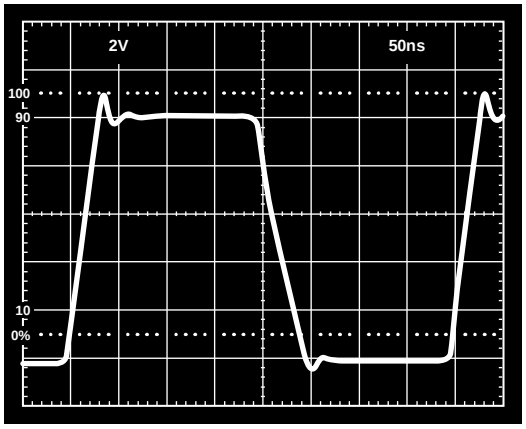


Figure 26. Buffer Large Signal Pulse Response

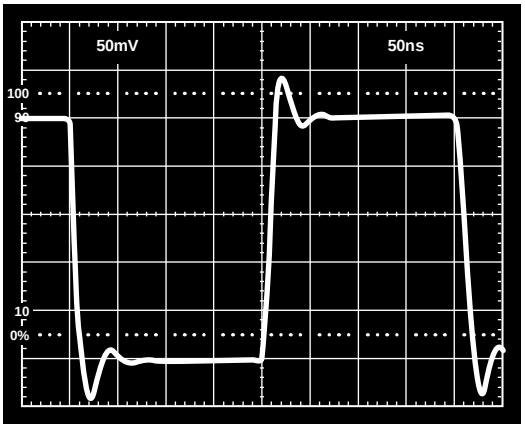


Figure 24. Inverter Small Signal Pulse Response

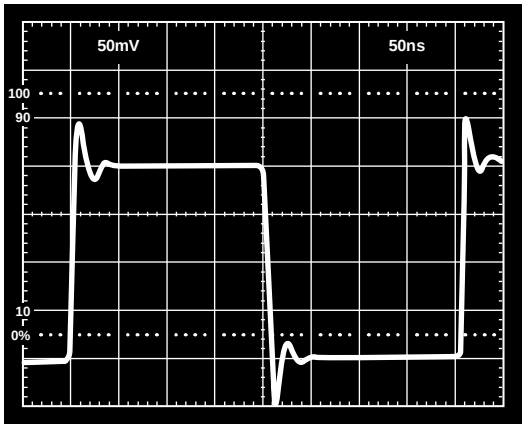


Figure 27. Buffer Small Signal Pulse Response

THEORY OF OPERATION

OFFSET NULLING

The input offset voltage of the AD841 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 28 can be used.

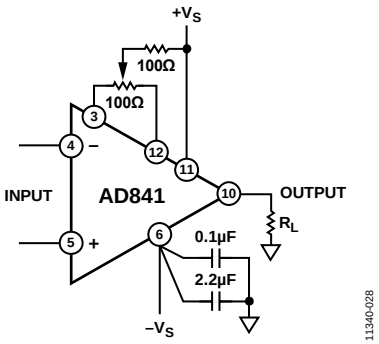


Figure 28. Offset Nulling (PDIP Pinout)

INPUT CONSIDERATIONS

An input resistor (R_{IN} in Figure 25) is recommended in circuits where the input to the AD841 is subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into the input.

For high performance circuits it is recommended that a resistor (R_B in Figure 22 and Figure 25) be used to reduce bias current errors by matching the impedance at each input. The output voltage error caused by the offset current is more than an order of magnitude less than the error present if the bias current error is not removed.

AD841 SETTLING TIME

Figure 29 and Figure 31 show the settling performance of the AD841 in the test circuit shown in Figure 30.

Settling time is defined as the interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components, which comprise settling time. They include

- Propagation delay through the amplifier
- Slewing time to approach the final output value
- The time of recovery from the overload associated with slewing
- Linear settling to within the specified error band

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

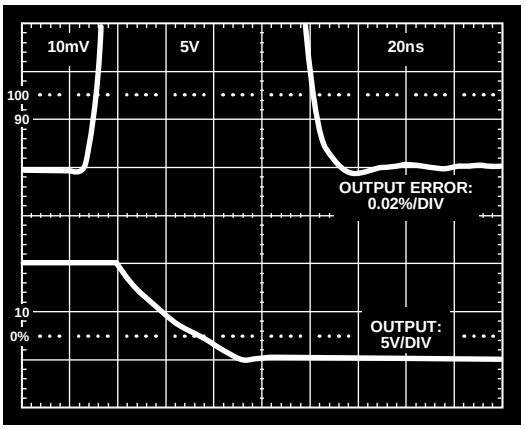


Figure 29. AD841 0.01% Settling Time

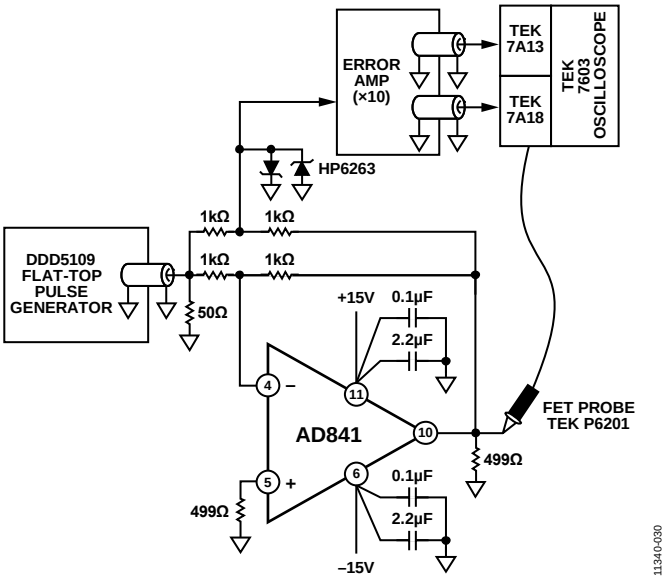


Figure 30. Settling Time Test Circuit

Measurement of the 0.01% settling in 110 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 500 Ω load. The input to the error amp is clamped to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 10, and it contains a gain vernier to fine trim the gain.

Figure 31 shows the long-term stability of the settling characteristics of the AD841 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

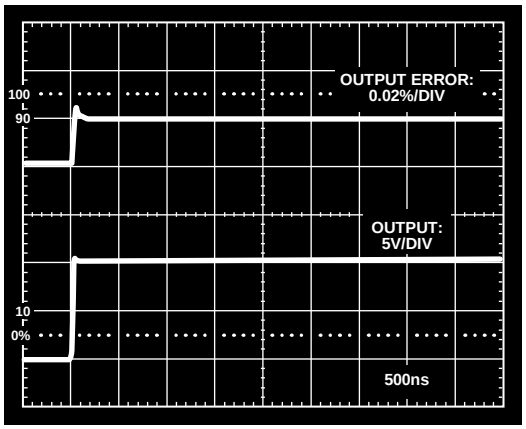


Figure 31. AD841 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD841, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Avoid sockets because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Bypass power supply leads to ground as close as possible to the amplifier pins. A 2.2 µF capacitor in parallel with a 0.1 µF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD841 is sensitive to capacitive loading. The AD841 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF (for a unity-gain follower). A resistor in series with the output can be used to decouple larger capacitive loads.

Figure 32 shows a typical configuration for driving a large capacitive load. The 51 Ω output resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low-pass filter formed by the 51 Ω resistor and the load capacitance, C_L.

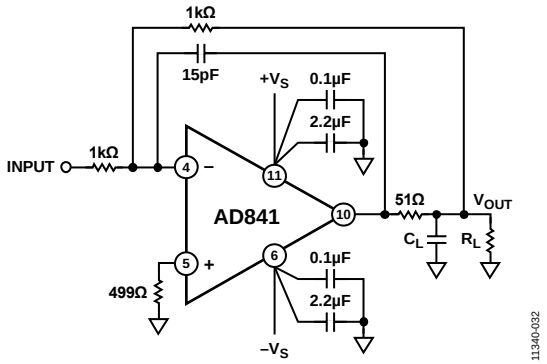


Figure 32. Circuit for Driving a Large Capacitive Load

TERMINATED LINE DRIVER

The AD841 functions very well as a high speed line driver of either terminated or unterminated cables. Figure 33 shows the AD841 driving a doubly terminated cable in a follower configuration. The AD841 maintains a typical slew rate of 300 V/µs, which means it can drive a ±10 V, 4.7 MHz signal or a ±3 V, 15.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor, R_{BT}, (also equal to the characteristic impedance of the cable) may be placed between the AD841 output and the cable to damp any stray signals caused by a mismatch between R_T and the cable's characteristic impedance. This results in a cleaner signal, but because half the output voltage is dropped across R_{BT}, the op amp must supply double the output signal required if there is no back termination. Therefore, the full power bandwidth is cut in half.

If termination is not used, cables appear as capacitive loads. If this capacitive load is large, it should be decoupled from the AD841 by a resistor in series with the output (see Figure 32).

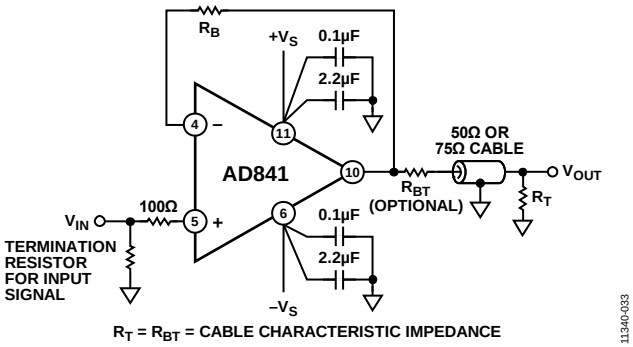


Figure 33. Line Driver Configuration

OVERDRIVE RECOVERY

Figure 34 shows the overdrive recovery capability of the AD841. Typical recovery time is 200 ns from negative overdrive and 700 ns from positive overdrive.

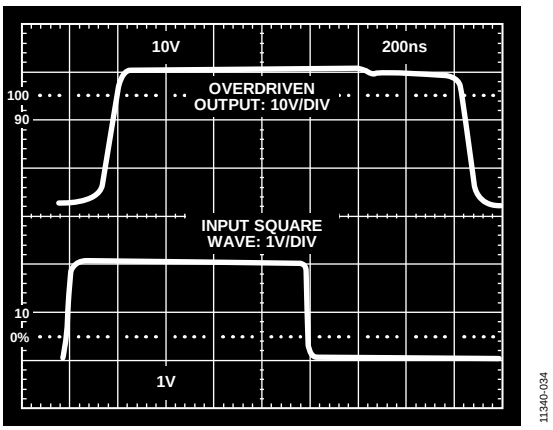


Figure 34. Overdrive Recovery

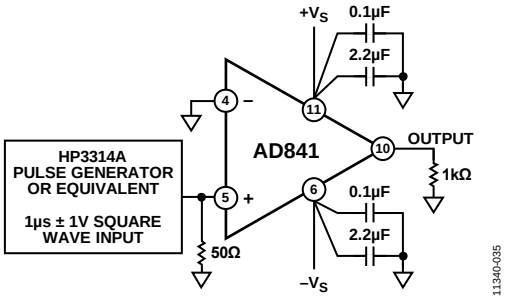
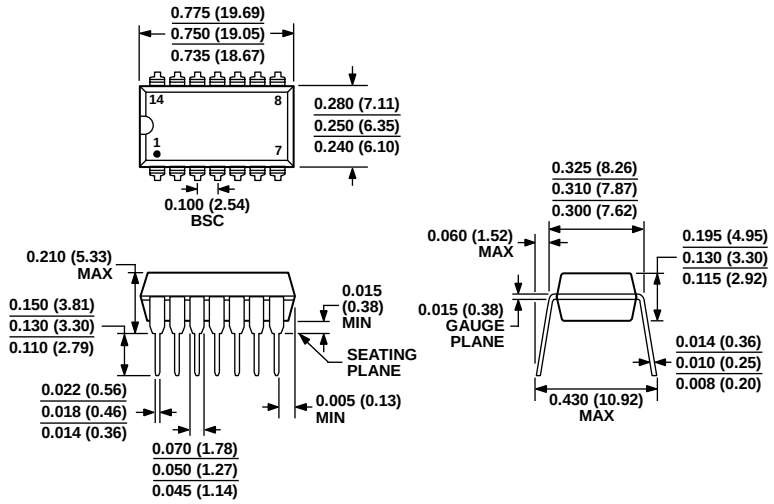


Figure 35. Overdrive Recovery Test Circuit

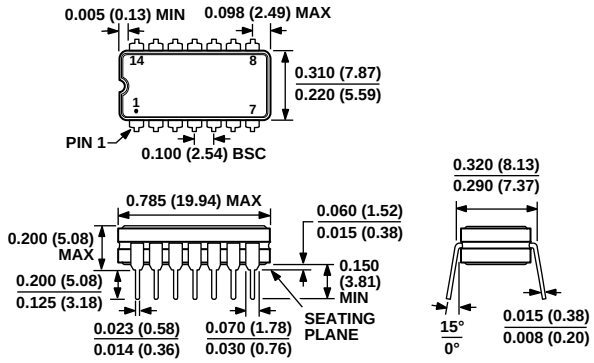
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 36. 14-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-14)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 37. 14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)
Dimensions shown in inches and (millimeters)

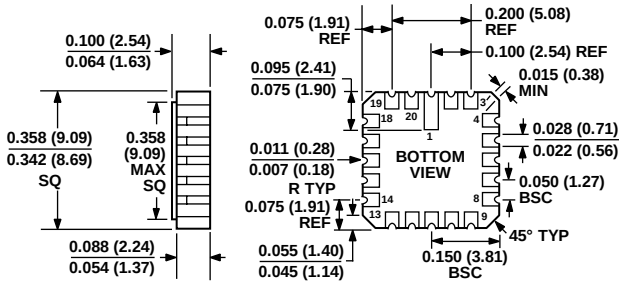


Figure 38. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20-1)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD841JNZ	0°C to +70°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD841KNZ	0°C to +70°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD841JCHIPS		Die	
AD841SCHIPS		Die	
AD841SE	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20-1
AD841SE/883B	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20-1
AD841SQ	−55°C to +125°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD841SQ/883B	−55°C to +125°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D11340-0-2/13(C)