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**6/15—Rev. B to Rev. C**

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**4/09—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 2.5 ± 10% V, $V_{DRIVE}$ = 2.25 V to 3.6 V, internal reference = 2.048 V, $f_{SCLK}$ = 80 MHz, $f_{SAMPLE}$ = 4.2 MSPS, $T_A$ = $T_{MIN}$ to $T_{MAX}$[1], unless otherwise noted.

**Table 2.**

| Parameter | AD7357B/AD7357Y Min | AD7357B/AD7357Y Typ | AD7357B/AD7357Y Max | AD7357WY Min | AD7357WY Typ | AD7357WY Max | Unit | Test Conditions/ Comments |
|---|---|---|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | | | | $f_{IN}$ = 500 kHz sine wave |
| Signal-to-Noise Ratio (SNR) | 74.5 | 76.5 | | 74.5 | 76.5 | | dB | |
| | | | | 74 | | | dB | −40°C to +25°C only |
| Signal-to-Noise and Distortion (SINAD)[2] | 74 | 76 | | 74 | 76 | | dB | |
| | | | | 73.5 | | | dB | −40°C to +25°C only |
| Total Harmonic Distortion (THD)[2] | | −83 | −80 | | −83 | −80 | dB | |
| | | | | | | −79 | | −40°C to +25°C only |
| Spurious Free Dynamic Range (SFDR) | | −85 | −82 | | −85 | −82 | dB | |
| | | | | | | −81 | dB | −40°C to +25°C only |
| Intermodulation Distortion (IMD)[2] | | | | | | | | fa = 1 MHz + 50 kHz, fb = 1 MHz − 50 kHz |
| Second-Order Terms | | −86 | | | −86 | | dB | |
| Third-Order Terms | | −79 | | | −79 | | dB | |
| ADC to ADC Isolation[2] | | −100 | | | −100 | | dB | $f_{IN}$ = 1 MHz, $f_{NOISE}$ = 100 kHz to 2.5 MHz |
| CMRR[2] | | −100 | | | −100 | | dB | $f_{NOISE}$ = 100 kHz to 2.5 MHz |
| SAMPLE-AND-HOLD | | | | | | | | |
| Aperture Delay | | | 3.5 | | | 3.5 | ns | |
| Aperture Delay Match | | | 40 | | | 40 | ps | |
| Aperture Jitter | | 16 | | | 16 | | ps | |
| Full Power Bandwidth | | | | | | | | |
| At 3 dB | | 110 | | | 110 | | MHz | |
| At 0.1 dB | | 77 | | | 77 | | MHz | At 0.1 dB |
| DC ACCURACY | | | | | | | | |
| Resolution | 14 | | | 14 | | | Bits | |
| Integral Nonlinearity (INL)[2] | | ±2 | ±3 | | ±2 | ±3 | LSB | |
| Differential Nonlinearity (DNL)[2] | | ±0.5 | ±0.99 | | ±0.5 | ±0.99 | LSB | Guaranteed no missed codes to 14 bits |
| Positive Full-Scale Error[2] | | | ±20 | | | ±20 | LSB | |
| Positive Full-Scale Error Match[2] | | | ±20 | | | ±20 | LSB | |
| Midscale Error[2] | | | 0/35 | | | 0/38 | LSB | |
| Midscale Error Match[2] | | | ±12 | | | ±15 | LSB | |
| Negative Full-Scale Error[2] | | | ±20 | | | ±20 | LSB | |
| Negative Full-Scale Error Match[2] | | | ±20 | | | ±20 | LSB | |
| ANALOG INPUT | | | | | | | | |
| Fully Differential Input Range ($V_{IN+}$ and $V_{IN}$−) | | | $V_{CM}$ ± $V_{REF}$/2 | | | $V_{CM}$ ± $V_{REF}$/2 | V | $V_{CM}$ = common-mode voltage; $V_{IN+}$ and $V_{IN-}$ must remain within GND and $V_{DD}$ |
| Common-Mode Voltage Range | 0.5 | | 1.6 | 0.5 | | 1.6 | V | The voltage around which $V_{IN+}$ and $V_{IN-}$ are centered |
| DC Leakage Current | | ±0.5 | ±5 | | ±0.5 | ±5 | µA | |
| Input Capacitance | | 32 | | | 32 | | pF | When in track mode |
| | | 8 | | | 8 | | pF | When in hold mode |

| Parameter | AD7357B/AD7357Y Min | Typ | Max | AD7357WY Min | Typ | Max | Unit | Test Conditions/ Comments |
|---|---|---|---|---|---|---|---|---|
| REFERENCE INPUT/OUTPUT | | | | | | | | |
| $V_{REF}$ Input Voltage Range | 2.048 + 0.1 | | $V_{DD}$ | 2.048 + 0.1 | | $V_{DD}$ | V | |
| $V_{REF}$ Input Current | | 0.3 | 0.45 | | 0.3 | 0.45 | mA | When in reference overdrive mode |
| $V_{REF}$ Output Voltage | 2.038 | | 2.058 | 2.038 | | 2.058 | V | ±2.048 V ± 0.5% maximum at $V_{DD}$ = 2.5 V ± 5% |
| | 2.043 | | 2.053 | 2.043 | | 2.053 | V | 2.048 V ± 0.25% maximum at $V_{DD}$ = 2.5 V ± 5% and 25°C |
| $V_{REF}$ Temperature Coefficient | | 6 | 20 | | 6 | 20 | ppm/°C | |
| $V_{REF}$ Long Term Stability | | 100 | | | 100 | | ppm | For 1000 hours |
| $V_{REF}$ Thermal Hysteresis | | 50 | | | 50 | | ppm | |
| $V_{REF}$ Noise | | 60 | | | 60 | | μV rms | |
| $V_{REF}$ Output Impedance | | 1 | | | 1 | | Ω | |
| LOGIC INPUTS | | | | | | | | |
| Input Voltage | | | | | | | | |
| High, $V_{INH}$ | 0.6 × $V_{DRIVE}$ | | | 0.6 × $V_{DRIVE}$ | | | V | |
| Low, $V_{INL}$ | | | 0.3 × $V_{DRIVE}$ | | | 0.3 × $V_{DRIVE}$ | V | |
| Input Current, $I_{IN}$ | | | ±1 | | | ±1 | μA | $V_{IN}$ = 0 V or $V_{DRIVE}$ |
| Input Capacitance, $C_{IN}$ | | 3 | | | 3 | | pF | |
| LOGIC OUTPUTS | | | | | | | | |
| Output Voltage | | | | | | | | |
| High, $V_{OH}$ | $V_{DRIVE}$ − 0.2 | | | $V_{DRIVE}$ − 0.2 | | | V | |
| Low, $V_{OL}$ | | | 0.2 | | | 0.2 | V | |
| Floating State Leakage Current | | | ±1 | | | ±1 | μA | |
| Floating State Output Capacitance | | 5.5 | | | 5.5 | | pF | |
| Output Coding | Straight binary | | | Straight binary | | | | |
| CONVERSION RATE | | | | | | | | |
| Conversion Time | $t_2$ + 15.5 × $t_{SCLK}$ | | | $t_2$ + 15.5 × $t_{SCLK}$ | | | ns | |
| Track-and-Hold Acquisition Time[2] | | | 33 | | | 33 | ns | Full-scale step input |
| Throughput Rate | | | 4.2 | | | 4.2 | MSPS | |
| POWER REQUIREMENTS | | | | | | | | |
| $V_{DD}$ | 2.25 | | 2.75 | 2.25 | | 2.75 | V | Nominal $V_{DD}$ = 2.5 V |
| $V_{DRIVE}$[3] | 2.25 | | 3.6 | 2.25 | | 3.6 | V | |
| $I_{TOTAL}$[4] | | | | | | | | Digital inputs = 0 V or $V_{DRIVE}$ |
| Normal Mode | | | | | | | | |
| Operational | | 14 | 20 | | 14 | 20 | mA | |
| Static | | 6 | 7.6 | | 6 | 7.6 | mA | SCLK on or off |
| Power-Down Mode | | | | | | | | |
| Partial | | 3.5 | 4.5 | | 3.5 | 4.5 | mA | SCLK on or off |
| Full | | 5 | 40 | | 5 | 40 | μA | SCLK on or off |

| Parameter | AD7357B/AD7357Y Min | Typ | Max | AD7357WY Min | Typ | Max | Unit | Test Conditions/ Comments |
|---|---|---|---|---|---|---|---|---|
| Power Dissipation | | | | | | | | |
| Normal Mode | | | | | | | | |
| Operational | | 36 | 59 | | 36 | 59 | mW | |
| Static | | 16 | 21 | | 16 | 21 | mW | SCLK on or off |
| Power-Down Mode | | | | | | | | |
| Partial | | 9.5 | 11.5 | | 9.5 | 11.5 | mW | SCLK on or off |
| Full | | 16 | 110 | | 16 | 110 | µW | SCLK on or off |

[1] Temperature ranges are as follows: AD7357Y: −40°C to +125°C; AD7357B (TSSOP): −40°C to +85°C; AD7357B (LFCSP): −40°C to +125°C; AD7357WY: −40°C to +125°C.
[2] See the Terminology section.
[3] The interface is functional with $V_{DRIVE}$ voltages down to 1.8 V. In this condition, the SCLK speed may need to be slowed down. See the access and hold times in the Timing Specifications section.
[4] $I_{TOTAL}$ is the total current flowing in $V_{DD}$ and $V_{DRIVE}$.

## TIMING SPECIFICATIONS

$V_{DD}$ = 2.5 V ± 10%, $V_{DRIVE}$ = 2.25 V to 3.6 V, internal reference = 2.048 V, $T_A$ = $T_{MAX}$ to $T_{MIN}$[1], unless otherwise noted.

**Table 3.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description |
|---|---|---|---|
| $f_{SCLK}$ | 500 | kHz min | |
| | 80 | MHz max | |
| $t_{CONVERT}$ | $t_2 + 15.5 \times t_{SCLK}$ | ns min | $t_{SCLK} = 1/f_{SCLK}$ |
| $t_{QUIET}$ | 5 | ns min | Minimum time between end of serial read and next falling edge of $\overline{CS}$ |
| $t_2$ | 5 | ns min | $\overline{CS}$ to SCLK setup time |
| $t_3$[2] | 6 | ns max | Delay from $\overline{CS}$ until $SDATA_A$ and $SDATA_B$ are three-state disabled |
| $t_4$[2, 3] | | | Data access time after SCLK falling edge |
| | 12.5 | ns max | 1.8 V ≤ $V_{DRIVE}$ < 2.25 V |
| | 11 | ns max | 2.25 V ≤ $V_{DRIVE}$ < 2.75 V |
| | 9.5 | ns max | 2.75 V ≤ $V_{DRIVE}$ < 3.3 V |
| | 9 | ns max | 3.3 V ≤ $V_{DRIVE}$ ≤ 3.6 V |
| $t_5$ | 5 | ns min | SCLK low pulse width |
| $t_6$ | 5 | ns min | SCLK high pulse width |
| $t_7$[2] | | | SCLK to data valid hold time |
| | 3.5 | ns min | 1.8 V ≤ $V_{DRIVE}$ < 2.75 V |
| | 3 | ns min | 2.75 V ≤ $V_{DRIVE}$ ≤ 3.6 V |
| $t_8$ | 9.5 | ns max | $\overline{CS}$ rising edge to $SDATA_A$, $SDATA_B$, high impedance |
| $t_9$ | 5 | ns min | $\overline{CS}$ rising edge to falling edge pulse width |
| $t_{10}$[2] | 4.5 | ns min | SCLK falling edge to $SDATA_A$, $SDATA_B$, high impedance |
| | 9.5 | ns max | SCLK falling edge to $SDATA_A$, $SDATA_B$, high impedance |
| Latency | 1 conversion latency | | |

[1] Temperature ranges are as follows: AD7357Y: −40°C to +125°C; AD7357B (TSSOP): −40°C to +85°C; AD7357B (LFCSP): −40°C to +125°C; AD7357WY: −40°C to +125°C.
[2] Specified with a load capacitance of 10 pF on $SDATA_A$ and $SDATA_B$.
[3] The time required for the output to cross 0.4 V or 2.4 V.

# ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to AGND, DGND, REFGND | −0.3 V to +3 V |
| $V_{DRIVE}$ to AGND, DGND, REFGND | −0.3 V to +5 V |
| $V_{DD}$ to $V_{DRIVE}$ | −5 V to +3 V |
| AGND to DGND to REFGND | −0.3 V to +0.3 V |
| Analog Input Voltages[1] to AGND | −0.3 V to VDD + 0.3 V |
| Digital Input Voltages[2] to DGND | −0.3 V to VDRIVE + 0.3V |
| Digital Output Voltages[3] to DGND | −0.3 V to VDRIVE + 0.3 V |
| Input Current to Any Pin Except Supplies[4] | ±10 mA |
| Operating Temperature Range | |
| AD7357Y | −40°C to +125°C |
| AD7357B (TSSOP) | −40°C to +85°C |
| AD7357B (LFCSP) | −40°C to +125°C |
| AD7357WY | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| TSSOP Package | |
| $\theta_{JA}$ Thermal Impedance | 143°C/W |
| $\theta_{JC}$ Thermal Impedance | 45°C/W |
| LFCSP Package | |
| $\theta_{JA}$ Thermal Impedance | 44°C/W |
| $\theta_{JC}$ Thermal Impedance | 22°C/W |
| Lead Temperature, Soldering | |
| Reflow Temperature (10 sec to 30 sec) | 255°C |
| ESD | 2 kV |

[1] Analog input voltages are $V_{INA+}$, $V_{INA-}$, $V_{INB+}$, $V_{INB-}$, $REF_A$, and $REF_B$.
[2] Digital input voltages are $\overline{CS}$ and SCLK.
[3] Digital output voltages are $SDATA_A$ and $SDATA_B$.
[4] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

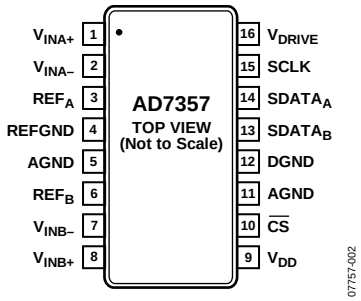



*Figure 2. Pin Configuration, TSSOP*

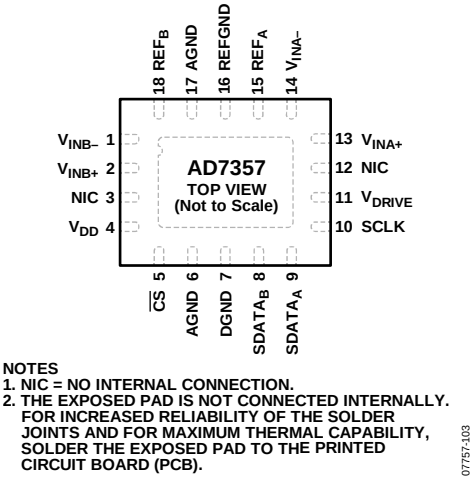



*Figure 3. Pin Configuration, LFCSP*

**Table 5. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| **TSSOP** | **LFCSP** | **Mnemonic** | **Description** |
| 1, 2 | 13, 14 | $V_{INA+}$, $V_{INA-}$ | Analog Inputs of ADC A. These analog inputs form a fully differential pair. |
| 3, 6 | 15, 18 | $REF_A$, $REF_B$ | Reference Decoupling Capacitor Pins. Decoupling capacitors are connected between these pins and the REFGND pin to decouple the reference buffer for each respective ADC. It is recommended to decouple each reference pin with a 10 µF capacitor. Provided that the output is buffered, take the on-chip reference from these pins and apply it externally to the rest of the system. The nominal internal reference voltage is 2.048 V and appears at these pins. These pins can also be overdriven by an external reference. The input voltage range for the external reference is 2.048 V + 100 mV to $V_{DD}$. |
| 4 | 16 | REFGND | Reference Ground. This is the ground reference point for the reference circuitry on the AD7357. Refer any external reference signal to this REFGND voltage. Decoupling capacitors must be placed between this pin and the $REF_A$ and $REF_B$ pins. |
| 5, 11 | 6, 17 | AGND | Analog Ground. This is the ground reference point for all analog circuitry on the AD7357. Refer all analog input signals to this AGND voltage. The AGND and DGND voltages must ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |
| 7, 8 | 1, 2 | $V_{INB-}$, $V_{INB+}$ | Analog Inputs of ADC B. These analog inputs form a fully differential pair. |
| 9 | 4 | $V_{DD}$ | Power Supply Input. The $V_{DD}$ range for the AD7357 is 2.5 V ± 10%. Decouple the supply to AGND with a 0.1 µF capacitor and a 10 µF tantalum capacitor. |
| 10 | 5 | $\overline{CS}$ | Chip Select. Active low, logic input. This input provides the dual function of initiating conversions on the AD7357 and framing the serial data transfer. |
| 12 | 7 | DGND | Digital Ground. This is the ground reference point for all digital circuitry on the AD7357. Connect this pin to the DGND plane of a system. The DGND and AGND voltages must ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |
| 13, 14 | 8, 9 | $SDATA_B$, $SDATA_A$ | Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. 16 SCLK falling edges are required to access the 14 bits of data from the AD7357. The data simultaneously appears on both data output pins from the simultaneous conversions of both ADCs. The data stream consists of two leading zeros, followed by the 14 bits of conversion data. The data is provided MSB first. If $\overline{CS}$ is held low for 18 SCLK cycles rather than 16, then two trailing zeros appear after the 14 bits of data. If $\overline{CS}$ is held low for an additional 18 SCLK cycles on either $SDATA_A$ or $SDATA_B$, the data from the other ADC follows on the $SDATA_x$ pins. This allows data from a simultaneous conversion on both ADCs to gather in serial format on either $SDATA_A$ or $SDATA_B$. |
| 15 | 10 | SCLK | Serial Clock. Logic input. A serial clock input provides the SCLK for accessing the data from the AD7357. This clock is also used as the clock source for the conversion process. |

| Pin No. | | | |
|---|---|---|---|
| **TSSOP** | **LFCSP** | **Mnemonic** | **Description** |
| 16 | 11 | $V_{DRIVE}$ | Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. This pin is decoupled to DGND. The voltage at this pin may be different than at $V_{DD}$. |
| Not applicable | 3, 12 | NIC | No Internal Connection. These pins are not connected internally. |
| Not applicable | | EPAD | Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and for maximum thermal capability, solder the exposed pad to the printed circuit board (PCB). |

# TYPICAL PERFORMANCE CHARACTERISTICS

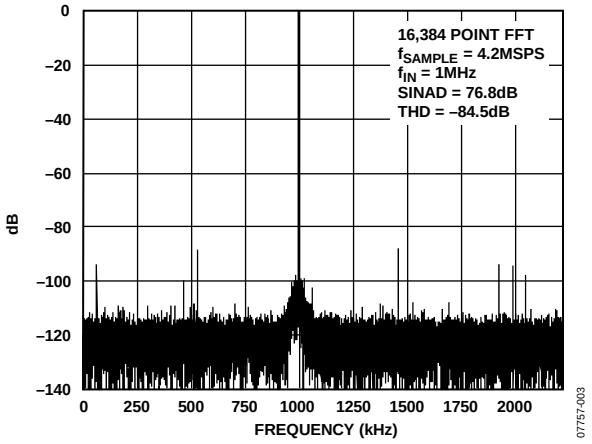



Figure 4. Typical FFT

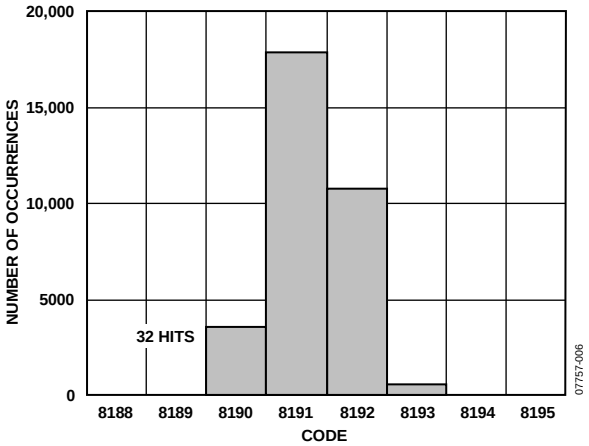



Figure 7. Histogram of Codes

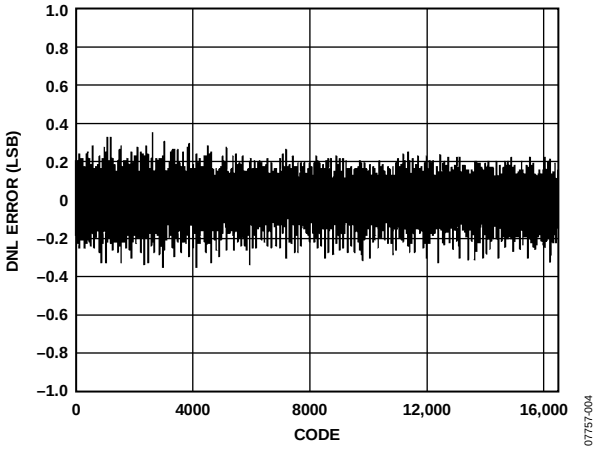



Figure 5. Typical DNL

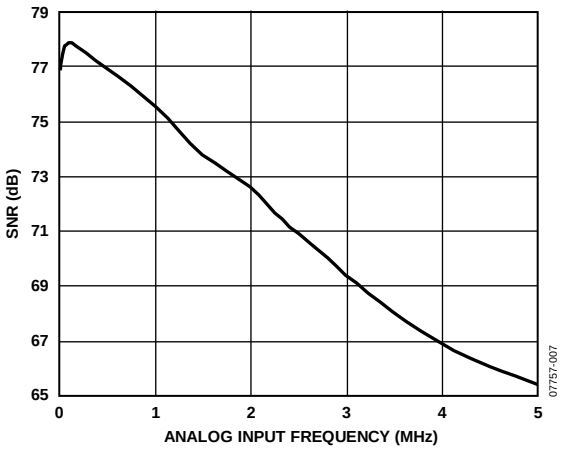



Figure 8. SNR vs. Analog Input Frequency

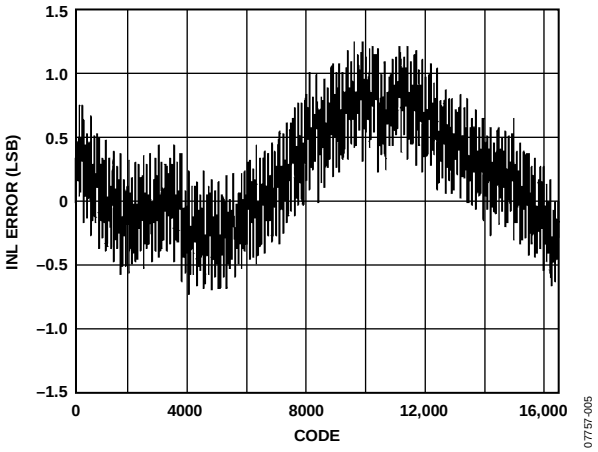



Figure 6. Typical INL

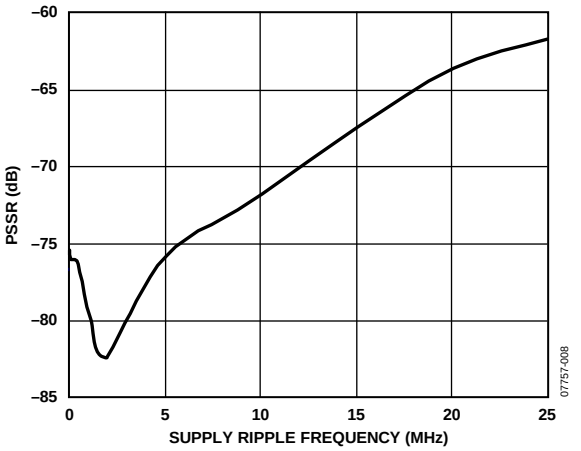



Figure 9. PSRR vs. Supply Ripple Frequency with No Supply Decoupling

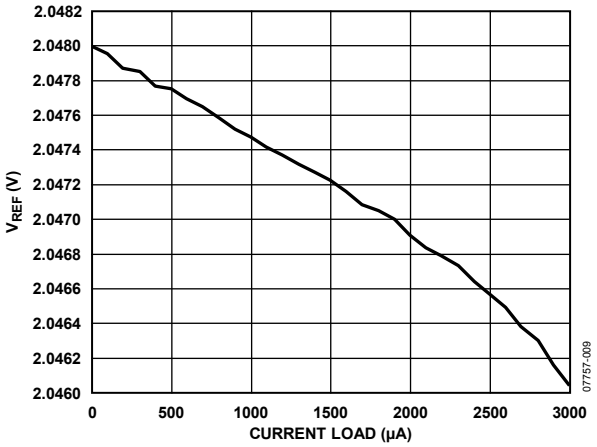



Figure 10. $V_{REF}$ vs. Reference Output Current Drive

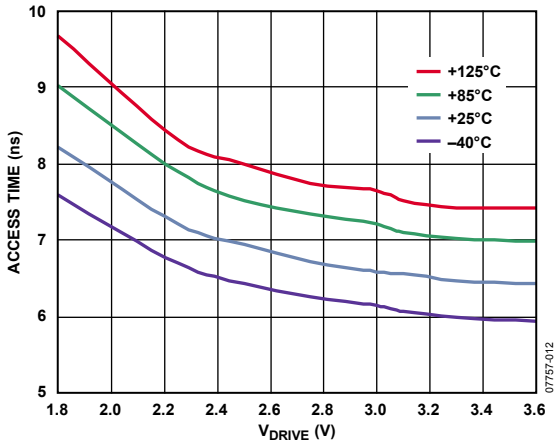



Figure 13. Access Time vs. $V_{DRIVE}$

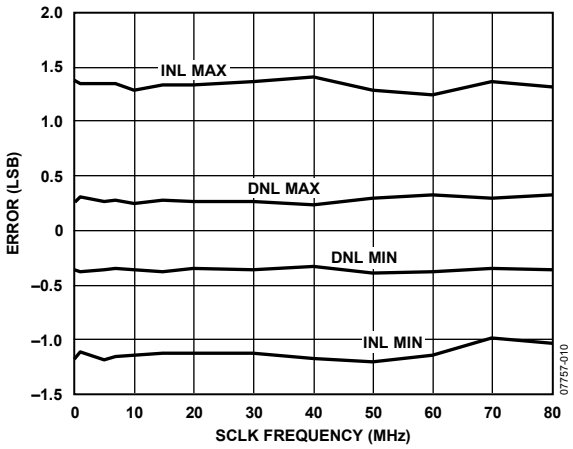



Figure 11. Linearity Error vs. SCLK Frequency

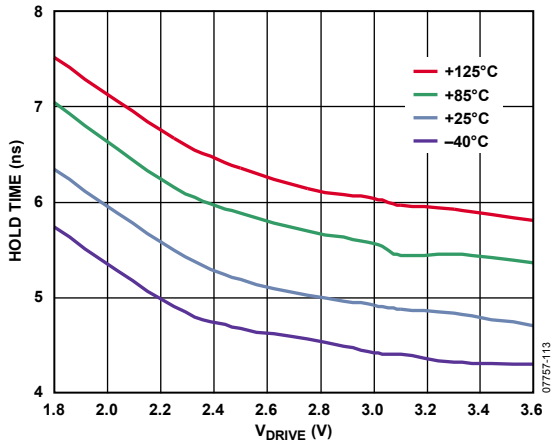



Figure 14. Hold Time vs. $V_{DRIVE}$

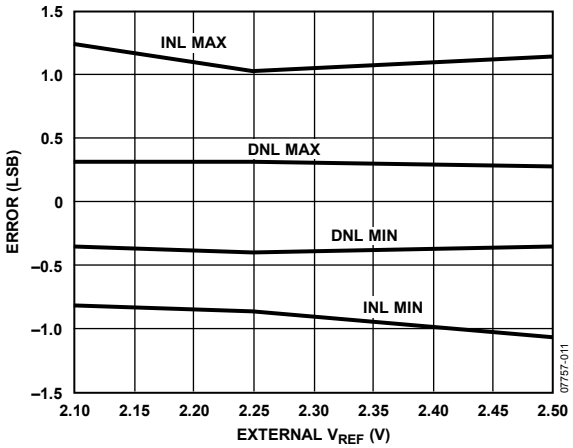



Figure 12. Linearity Error vs. External $V_{REF}$

# TERMINOLOGY

**Integral Nonlinearity (INL)**
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (1 LSB below the first code transition) and full scale (1 LSB above the last code transition).

**Differential Nonlinearity (DNL)**
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Negative Full-Scale Error**
Negative full-scale error is the deviation of the first code transition (00 … 000) to (00 … 001) from the ideal (that is, $-V_{REF}$ + 0.5 LSB) after the midscale error has been adjusted out.

**Negative Full-Scale Error Match**
Negative full-scale error match is the difference in negative full-scale error between the two ADCs.

**Midscale Error**
Midscale error is the deviation of the midscale code transition (011 … 111) to (100 … 000) from the ideal (that is, 0 V).

**Midscale Error Match**
Midscale error match is the difference in midscale error between the two ADCs.

**Positive Full-Scale Error**
Positive full-scale error is the deviation of the last code transition (111 … 110) to (111 … 111) from the ideal (that is, $V_{REF}$ − 1.5 LSB) after the midscale error has been adjusted out.

**Positive Full-Scale Error Match**
Positive full-scale error match is the difference in positive full-scale error between the two ADCs.

**ADC to ADC Isolation**
ADC to ADC isolation is a measure of the level of crosstalk between ADC A and ADC B. It is measured by applying a full-scale 1 MHz sine wave signal to one of the two ADCs and applying a full-scale signal of variable frequency to the other ADC. The ADC-to-ADC isolation is the ratio of the power of the 1 MHz signal on the converted ADC to the power of the noise signal on the other ADC that appears in the FFT. The noise frequency on the unselected channel varies from 100 kHz to 2.5 MHz.

**Power Supply Rejection Ratio (PSRR)**
PSRR is the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC VDD supply of the frequency, $f_S$. The frequency of the input varies from 5 kHz to 25 MHz.

$$PSRR\ (\text{dB}) = 10 \log(Pf/Pf_S)$$

where:
*Pf* is the power at frequency, f, in the ADC output.
$Pf_S$ is the power at frequency, $f_S$, in the ADC output.

**Common-Mode Rejection Ratio (CMRR)**
CMRR is the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of $V_{IN+}$ and $V_{IN-}$ of frequency, $f_S$, as follows:

$$CMRR\ (\text{dB}) = 10 \log(Pf/Pf_S)$$

where:
*Pf* is the power at frequency, f, in the ADC output.
$Pf_S$ is the power at frequency, $f_S$, in the ADC output.

**Track-and-Hold Acquisition Time**
The track-and-hold amplifier returns to track mode at the end of a conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of conversion.

**Signal-to-(Noise + Distortion) Ratio (SINAD)**
SINAD is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical SINAD for an ideal N-bit converter with a sine wave input is given by

$$SINAD = (6.02\ N + 1.76)\ \text{dB}$$

Thus, for a 12-bit converter, SINAD is 74 dB and for a 14-bit converter, SINAD is 86 dB.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7357, it is defined as

$$THD\ (\text{dB}) = -20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
$V_1$ is the rms amplitude of the fundamental.
$V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through the sixth harmonics.

**Peak Harmonic or Spurious Noise**
Peak harmonic or spurious noise is the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

**Intermodulation Distortion (IMD)**

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7357 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification (see Table 2), where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

**Thermal Hysteresis**

Thermal hysteresis is the absolute maximum change of the reference output voltage after the device is cycled through temperature from either

$T\_HYS+$ = 25°C to $T_{MAX}$ to 25°C

$T\_HYS-$ = 25°C to $T_{MIN}$ to 25°C

It is expressed in ppm using the following equation:

$$V_{HYS}(\text{ppm}) = \left| \frac{V_{REF}(25°\text{C}) - V_{REF}(T\_HYS)}{V_{REF}(25°\text{C})} \right| \times 10^6$$

where:

$V_{REF}(25°C)$ is $V_{REF}$ at 25°C.

$V_{REF}(T\_HYS)$ is the maximum change of $V_{REF}$ at T_HYS+ or T_HYS−.

# THEORY OF OPERATION

## CIRCUIT INFORMATION

The AD7357 is a high speed, dual, 14-bit, single-supply, successive approximation ADC. The device operates from a 2.5 V power supply and features throughput rates up to 4.2 MSPS.

The AD7357 contains two on-chip differential track-and-hold amplifiers, two successive approximation ADCs, and a serial interface with two separate data output pins. The device is housed in a 16-lead TSSOP package or an 18-lead LFCSP package, offering the user considerable space-saving advantages over alternative solutions.

The serial clock input accesses data from the device, but also provides the clock source for each successive approximation ADC. The AD7357 has an on-chip 2.048 V reference. If an external reference is desired, the internal reference can be overdriven with a reference value ranging from (2.048 V + 100 mV) to $V_{DD}$. If the internal reference is to be used elsewhere in the system, the reference output needs to be buffered first. The differential analog input range for the AD7357 is $V_{CM} \pm V_{REF}/2$.

The AD7357 features power-down options to allow power saving between conversions. The power-down options are implemented via the standard serial interface, as described in the Modes of Operation section.

## CONVERTER OPERATION

The AD7357 has two successive approximation ADCs, each based around two capacitive DACs. Figure 15 and Figure 16 show simplified schematics of one of these ADCs in acquisition and conversion phases, respectively. The ADC comprises control logic, an SAR, and two capacitive DACs. In Figure 15 (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays may acquire the differential signal on the input.

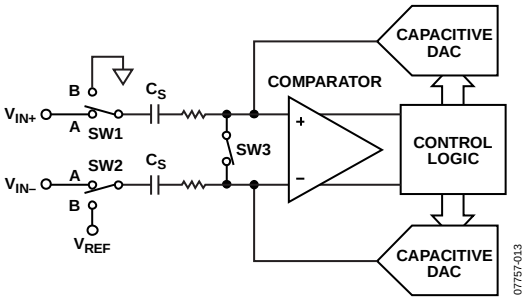



*Figure 15. ADC Acquisition Phase*

When the ADC starts a conversion (see Figure 16), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected when the conversion begins. The control logic and charge redistribution DACs add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete.

The control logic generates the ADC output code. The output impedances of the sources driving the $V_{IN+}$ and $V_{IN-}$ pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

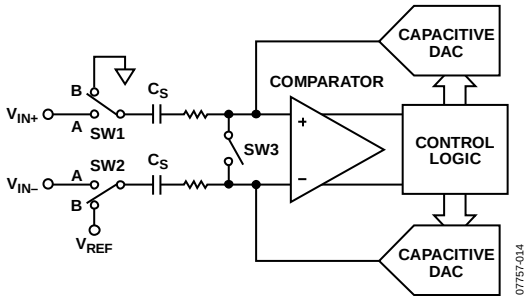



*Figure 16. ADC Conversion Phase*

## ANALOG INPUT STRUCTURE

Figure 17 shows the equivalent circuit of the analog input structure of the AD7357. The four diodes provide ESD protection for the analog inputs. Take care to ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the device.

The C1 capacitors in Figure 17 are typically 8 pF and can primarily be attributed to pin capacitance. The R1 resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 30 Ω. The C2 capacitors are the ADC sampling capacitors with a capacitance of 32 pF typically.

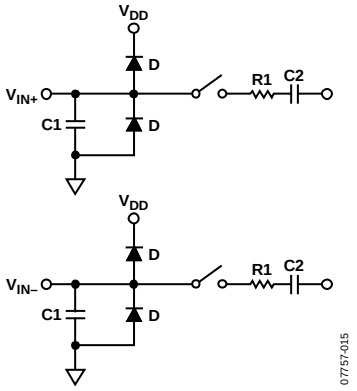



*Figure 17. Equivalent Analog Input Circuit*
*Conversion Phase—Switches Open, Track Phase—Switches Closed*

For ac applications, it is recommended to remove high frequency components from the analog input signal by the use of an RC low-pass filter on the analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input must be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and may necessitate the use of an input buffer amplifier. The choice of the operational amplifier is a function of the particular application.

When no amplifier drives the analog input, limit the source impedance to low values. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 18 shows a graph of the THD vs. the analog input signal frequency for various source impedances.

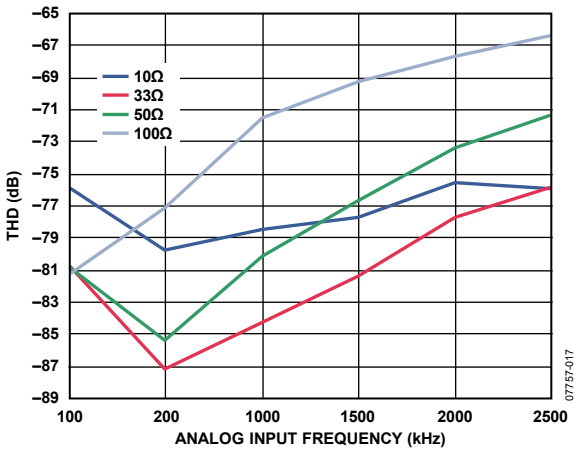



*Figure 18. THD vs. Analog Input Frequency for Various Source Impedances*

Figure 19 shows a graph of the THD vs. the analog input frequency while sampling at 4.2 MSPS. In this case, the source impedance is 33 Ω.

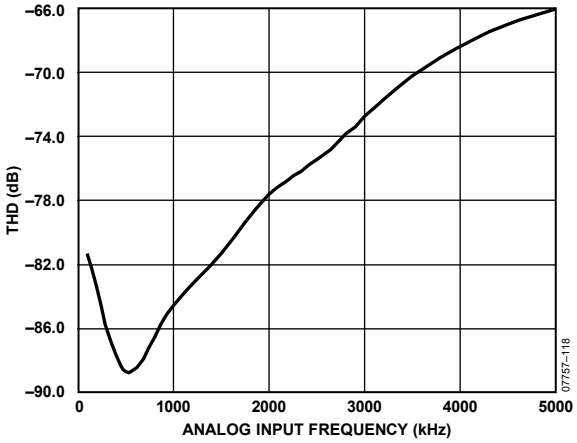



*Figure 19. THD vs. Analog Input Frequency*

## ANALOG INPUTS

Differential signals have some benefits over single-ended signals, including noise immunity based on the common-mode rejection of the device and improvements in distortion performance. Figure 20 defines the fully differential input of the AD7357.

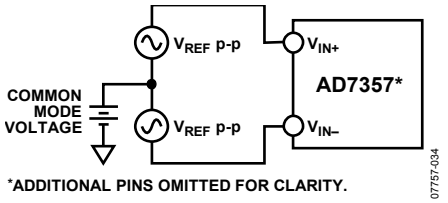



*Figure 20. Differential Input Definition*

The amplitude of the differential signal is the difference between the signals applied to the $V_{IN+}$ and $V_{IN-}$ pins in each differential pair ($V_{IN+} - V_{IN-}$). $V_{IN+}$ and $V_{IN-}$ are simultaneously driven by two signals each of amplitude $V_{REF}$ that are 180° out of phase. This amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ peak-to-peak regardless of the common mode (CM).

CM is the average of the two signals and is, therefore, the voltage on which the two inputs are centered.

$$CM = (V_{IN+} + V_{IN-})/2$$

This results in the span of each input being CM ± $V_{REF}$/2. This voltage must be set up externally. When setting up the CM, ensure that that $V_{IN+}$ and $V_{IN-}$ remain within GND/$V_{DD}$. When a conversion occurs, CM is rejected, resulting in a virtually noise free signal of amplitude $-V_{REF}$ to $+V_{REF}$ corresponding to the digital codes of 0 to 16,383.

## DRIVING DIFFERENTIAL INPUTS

Differential operation requires VIN+ and VIN− to be driven simultaneously with two equal signals that are 180° out of phase. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended to differential conversion.

### *Differential Amplifier*

An ideal method of applying differential drive to the AD7357 is to use a differential amplifier such as the AD8138. This device can be used as a single-ended to differential amplifier or as a differential to differential amplifier. The AD8138 also provides common-mode level shifting. Figure 21 shows how the AD8138 is used as a single-ended to differential amplifier. The positive and negative outputs of the AD8138 are connected to the respective inputs on the ADC via a pair of series resistors to minimize the effects of switched capacitance on the front end of the ADC.

The architecture of the AD8138 results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components.

If the source for the analog inputs used has zero impedance, all four resistors ($R_G1$, $R_G2$, $R_F1$, and $R_F2$) must be the same. If the source has a 50 Ω impedance and a 50 Ω termination, for example, increase the value of $R_G2$ by 25 Ω to balance this parallel impedance on the input and thus ensures that both the positive and negative analog inputs have the same gain. The outputs of the amplifier are perfectly matched balanced differential outputs of identical amplitude and are exactly 180° out of phase.

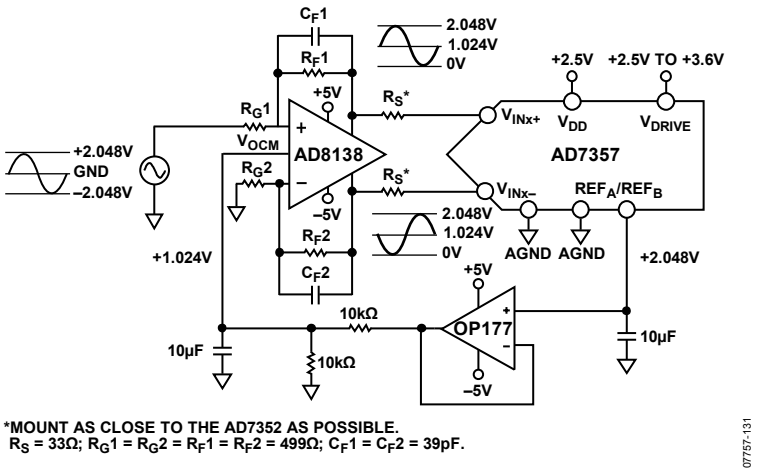
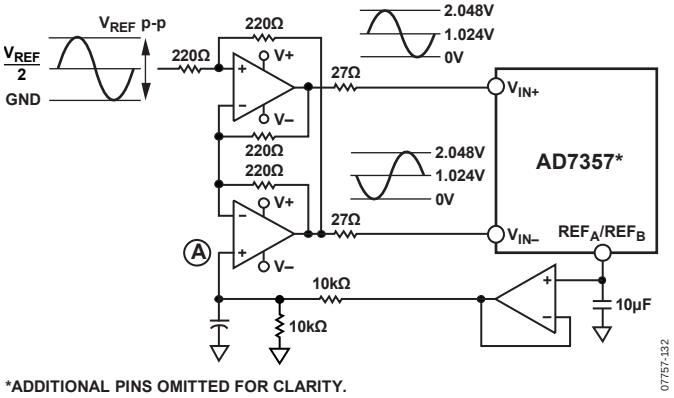



*Figure 21. Using the AD8138 as a Single-Ended to Differential Amplifier*

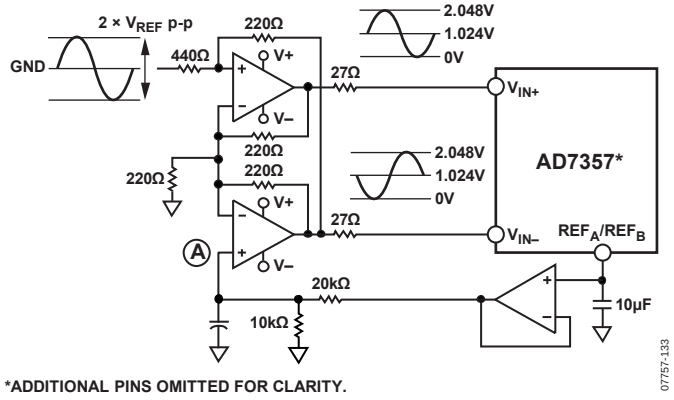
### *Operational Amplifier Pair*

An operational amplifier pair is used to directly couple a differential signal to one of the analog input pairs of the AD7357. The circuit configurations shown in Figure 22 and Figure 23 show how an operational amplifier pair can be used to convert a single-ended signal into a differential signal for a bipolar and unipolar input signal, respectively. The voltage applied to Point A sets up the common-mode voltage. In both diagrams, Point A is connected in some way to the reference. The AD8022 is a suitable dual operational amplifier that is used in this configuration to provide differential drive to the AD7357.




*ADDITIONAL PINS OMITTED FOR CLARITY.

*Figure 22. Dual Operational Amplifier Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal*




*ADDITIONAL PINS OMITTED FOR CLARITY.

*Figure 23. Dual Operational Amplifier Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal*

## VOLTAGE REFERENCE

The AD7357 allows the choice of a very low temperature drift internal voltage reference or an external reference. The internal 2.048 V reference of the AD7357 provides excellent performance and can be used in almost all applications.

When the internal reference is used, the reference voltage is present on the $REF_A$ and $REF_B$ pins. Decouple these pins to REFGND with 10 µF capacitors. The internal reference voltage can be used elsewhere in the system, provided it is buffered externally.

The $REF_A$ and $REF_B$ pins can also be overdriven with an external voltage reference if desired. The applied reference voltage can range from 2.048 V + 100 mV to $V_{DD}$. A common choice is to use an external 2.5 V reference such as the ADR441 or ADR431.

## ADC TRANSFER FUNCTION

The output coding for the AD7357 is straight binary. The designed code transitions occur at successive LSB values (such as 1 LSB or 2 LSB). The LSB size is $(2 \times V_{REF})/16,384$. The ideal transfer characteristic of the AD7357 is shown in Figure 24.

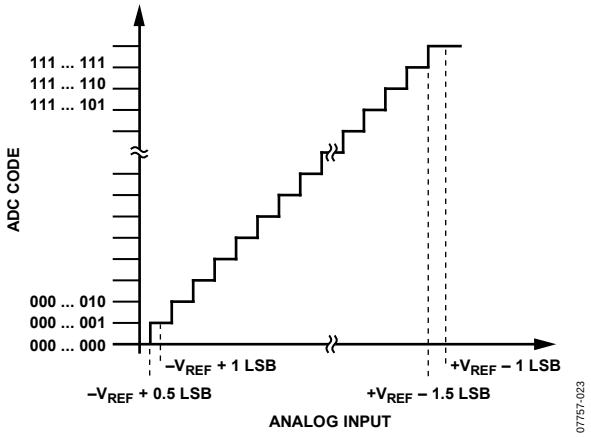



*Figure 24. Deal Transfer Characteristic*

# MODES OF OPERATION

The AD7357 mode of operation is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. After a conversion is initiated, the point at which $\overline{CS}$ is pulled high determines which power-down mode, if any, the device enters. Similarly, if already in a power-down mode, $\overline{CS}$ can control whether the device returns to normal operation or remains in a power-down mode. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation and throughput rate ratio for the differing application requirements.

## NORMAL MODE

Normal mode is intended for applications needing the fastest throughput rates. The user does not need to worry about any power-up times because the AD7357 remains fully powered at all times. Figure 25 shows the general diagram of the operation of the AD7357 in this mode.

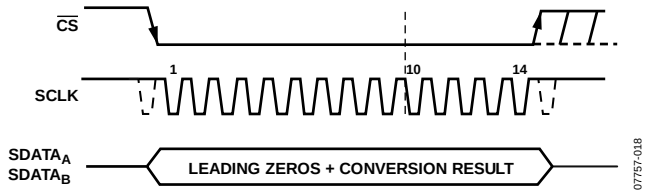



*Figure 25. Normal Mode Operation*

The conversion is initiated on the falling edge of $\overline{CS}$, as described in the Serial Interface section. To ensure that the device remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the 16th SCLK falling edge, the device remains powered up, but the conversion is terminated and $SDATA_A$ and $SDATA_B$ go back into three-state. To complete the conversion and access the conversion result for the AD7357, 16 serial clock cycles are required. SDATA lines do not return to three-state after 16 SCLK cycles have elapsed, but instead do so when $\overline{CS}$ is brought high again. If $\overline{CS}$ is left low for another 2 SCLK cycles, two trailing zeros are clocked out after the data. If $\overline{CS}$ is left low for a further 16 SCLK cycles, the result for the other ADC on board is also accessed on the same SDATA line as shown in Figure 32 (see the Serial Interface section).

When 32 SCLK cycles have elapsed, the SDATA line returns to three-state on the 32nd SCLK falling edge. If $\overline{CS}$ is brought high prior to this, the SDATA line returns to three-state at that point. Thus, $\overline{CS}$ may idle low after 32 SCLK cycles until it is brought high again sometime prior to the next conversion, if so desired, because the bus still returns to three-state upon completion of the dual result read.

When a data transfer is complete and $SDATA_A$ and $SDATA_B$ have returned to three-state, another conversion can be initiated after the quiet time, $t_{QUIET}$, has elapsed by bringing $\overline{CS}$ low again (assuming the required acquisition time has been allowed).

## PARTIAL POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion or a series of conversions can be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7357 is in partial power-down mode, all analog circuitry is powered down except for the on-chip reference and reference buffers.

To enter partial power-down mode, interrupt the conversion process by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK, as shown in Figure 26. When $\overline{CS}$ is brought high in this window of SCLKs, the device enters partial power-down mode, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and $SDATA_A$ and $SDATA_B$ go back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the device remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

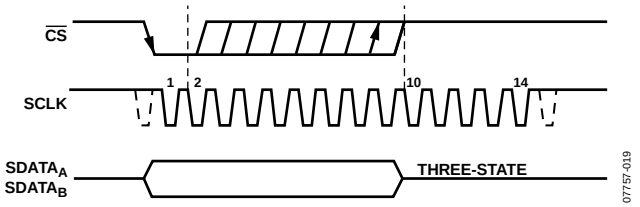



*Figure 26. Entering Partial Power-Down Mode*

To exit this mode of operation and to power up the AD7357 again, perform a dummy conversion. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device is fully powered up after approximately 200 ns elapses (or one full conversion), and valid data results from the next conversion, as shown in Figure 27. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the AD7357 again goes into partial power-down mode. This avoids accidental power-up due to glitches on the $\overline{CS}$ line. Although the device may begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$. If the AD7357 is already in partial power-down mode and $\overline{CS}$ is brought high between the second and 10th falling edges of SCLK, the device enters full power-down mode.

## FULL POWER-DOWN MODE

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, as power-up from a full power-down takes substantially longer than from a partial power-down. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and, thus, power-down. When the AD7357 is in full power-down, all analog circuitry is powered down. Full power-down is entered in a way that is similar to partial power-down, except that the timing sequence shown in Figure 26 must be executed twice. The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK. The device enters partial power-down mode at this point.

To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 28. When $\overline{CS}$ has been brought high in this window of SCLKs, the device completely powers down.

Note that it is not necessary to complete the 16 SCLK pulses after $\overline{CS}$ has been brought high to enter a power-down mode.

To exit full power-down mode and power up the AD7357, perform a dummy conversion, such as powering up from partial power-down. On the falling edge of $\overline{CS}$, the device begins to power up, as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The required power-up time must elapse before a conversion can be initiated, as shown in Figure 29.

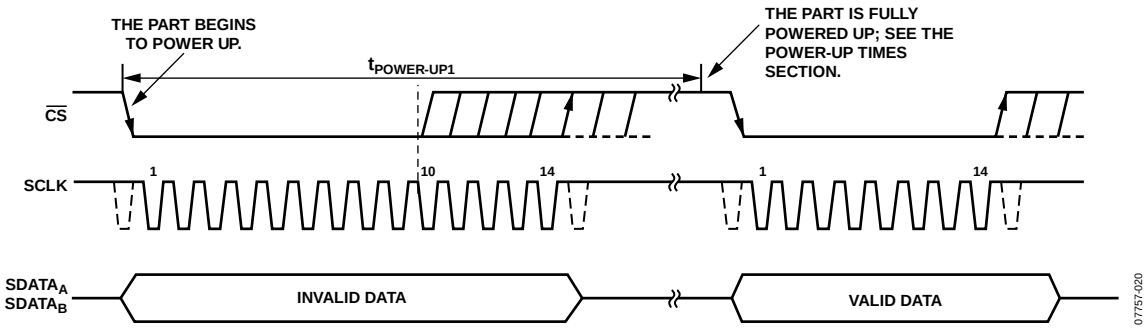



Figure 27. Exiting Partial Power-Down Mode

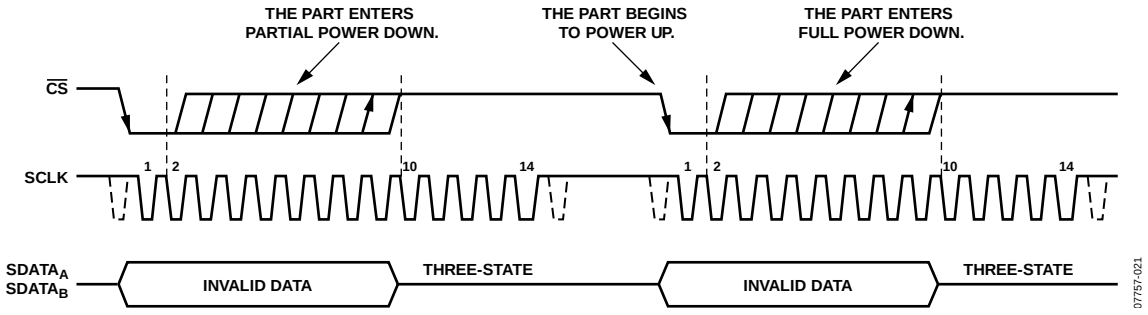



Figure 28. Entering Full Power-Down Mode

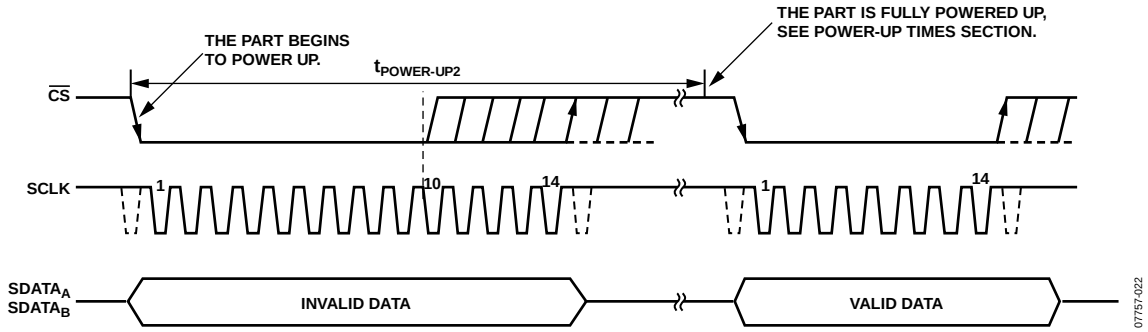



Figure 29. Exiting Full Power-Down Mode

## POWER-UP TIMES

The AD7357 has two power-down modes: partial power-down and full power-down. They are described in detail in the Partial Power-Down Mode section and the Full Power-Down Mode section. This section describes the power-up time required when coming out of either of these modes. Note that the power-up times apply with the recommended decoupling capacitors in place on the $REF_A$ and $REF_B$ pins.

To power up from partial power-down mode, one dummy cycle is required. The device is fully powered up after approximately 200 ns from the falling edge of $\overline{CS}$ has elapsed. As soon as the partial power-up time has elapsed, the ADC is fully powered up and the input signal is acquired properly. The quiet time, $t_{QUIET}$, must still be allowed from the point where the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$.

To power up from full power-down, allow approximately 6 ms from the falling edge of $\overline{CS}$, shown in Figure 29 as $t_{POWER-UP2}$.

Note that during power-up from partial power-down mode, the track-and-hold, which is in hold mode while the device is powered down, returns to track mode after the first SCLK edge that the device receives after the falling edge of $\overline{CS}$.

When power supplies are first applied to the AD7357, the ADC powers up in either of the power-down modes or in normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the device is fully powered up before attempting a valid conversion. Likewise, if the device is kept in partial power-down mode immediately after the supplies are applied, then initiate two dummy cycles. The first dummy cycle must hold $\overline{CS}$ low until after the 10th SCLK falling edge; in the second cycle, $\overline{CS}$ must be brought high between the second and 10th SCLK falling edges (see Figure 26).

Alternatively, if the device is placed into full power-down mode when the supplies are applied, three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th SCLK falling edge; the second and third dummy cycles place the device into full power-down mode (see Figure 28 and the Modes of Operation section).

## POWER vs. THROUGHPUT RATE

The power consumption of the AD7357 varies with the throughput rate. When using very slow throughput rates and as fast an SCLK frequency as possible, the various power-down options can be used to make significant power savings. However, the AD7357 quiescent current is low enough that even without using the power-down options, there is a noticeable variation in power consumption with sampling rate. This is true whether a fixed SCLK value is used or if it is scaled with the sampling rate. Figure 30 shows a plot of power vs. throughput rate when operating in normal mode for a fixed maximum SCLK frequency and an SCLK frequency that scales with the sampling rate. The internal reference is used for Figure 30.

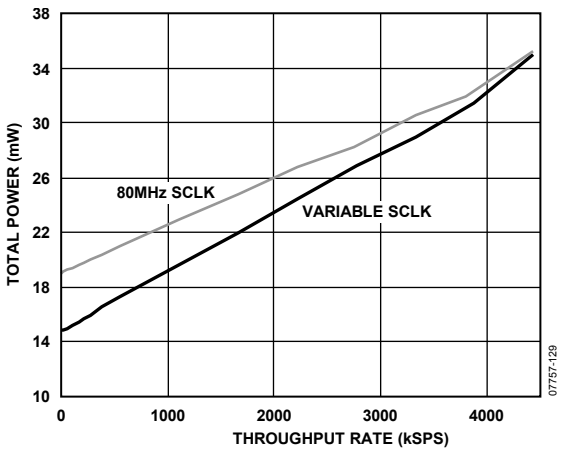



*Figure 30. Total Power vs. Throughput Rate*

# SERIAL INTERFACE

Figure 31 shows the detailed timing diagram for serial interfacing to the AD7357. The serial clock (SCLK) provides the conversion clock and controls the transfer of information from the AD7357 during conversion. There is a single sample delay in the result that is clocked out from the AD7357.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode. At this point, the analog input is sampled and the bus is taken out of three-state. The conversion is also initiated and requires a minimum of 16 SCLKs to complete. When 16 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge, as shown in Figure 31 at Point B. On the rising edge of $\overline{CS}$, the conversion is terminated and $SDATA_A$ and $SDATA_B$ go back into three-state. If $\overline{CS}$ is not brought high but is, instead, held low for an additional 16 SCLK cycles on $SDATA_A$, the data from the conversion on ADC B is output on $SDATA_A$.

Likewise, if $\overline{CS}$ is held low for an additional 16 SCLK cycles on $SDATA_A$, the data from the conversion on ADC A is output on $SDATA_B$ (see Figure 32). In this case, the SDATA line in use goes back into three-state on the 32nd SCLK falling edge or the rising edge of $\overline{CS}$, whichever occurs first.

A minimum of 16 SCLK cycles are required to perform the conversion process and to access data from one conversion on either data line of the AD7357. Note that the data accessed on $SDATA_A$ and $SDATA_B$ is the result of the previous conversion. $\overline{CS}$ going low provides the leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with a second leading zero. Thus, the first falling clock edge on the serial clock has the leading zero provided and clocks out the second leading zero. The 14-bit result then follows with the final bit in the data transfer valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge. In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge depending on the SCLK frequency. The first rising edge of SCLK after the $\overline{CS}$ falling edge has the second leading zero provided and the 15th rising SCLK edge has DB0 provided.

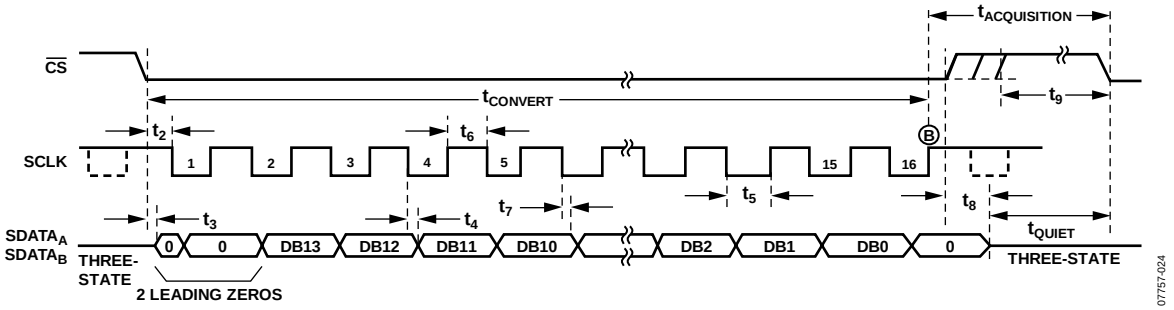



*Figure 31. Serial Interface Timing Diagram*

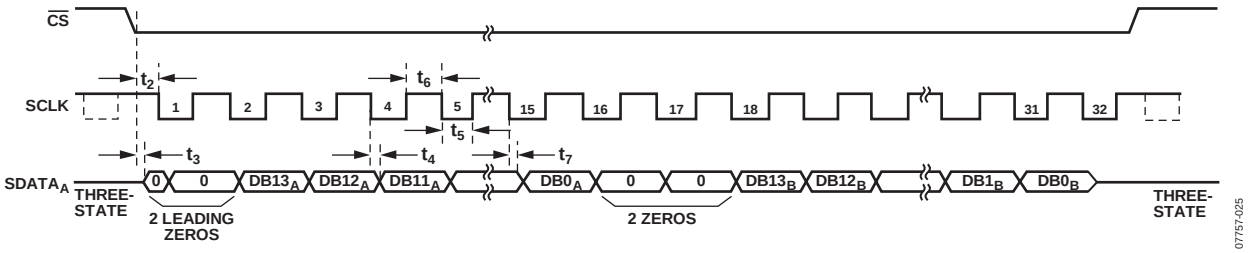



*Figure 32. Reading Data from Both ADCs on One SDATA Line with 32 SCLKs*

# APPLICATION SUGGESTIONS

## GROUNDING AND LAYOUT

The analog and digital supplies to the AD7357 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The PCB that houses the AD7357 must be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of easily separated ground planes.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. Sink the two AGND pins of the AD7357 in the AGND plane. Join the digital and analog ground plans in only one place. If the AD7357 is in a system where multiple devices require an AGND and DGND connection, still make the connection at one point only. Establish a star ground point as close as possible to the ground pins on the AD7357.

Avoid running digital lines under the device because this couples noise onto the die. Allow the analog ground planes to run under the AD7357 to avoid noise coupling. The power supply lines to the AD7357 must use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, shield fast switching signals, such as clocks with digital ground, and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, run traces on opposite sides of the board at right angles to each other. A microstrip technique is the best method, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is important; decouple all supplies with 10 µF tantalum capacitors parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, place them as close as possible to the device, ideally right up against the device. The 0.1 µF capacitor must have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to logic switching.

## EVALUATING THE AD7357 PERFORMANCE

The recommended layout for the AD7357 is outlined in evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the converter evaluation and development board (CED). The CED can be used in conjunction with the AD7357 evaluation board (as well as many other evaluation boards ending in the ED designator from Analog Devices, Inc.) to demonstrate and evaluate the ac and dc performance of the AD7357.

The software allows the user to perform ac (fast Fourier transform) and dc (linearity) tests on the AD7357. The software and documentation are on a CD that is shipped with the evaluation board.

# OUTLINE DIMENSIONS

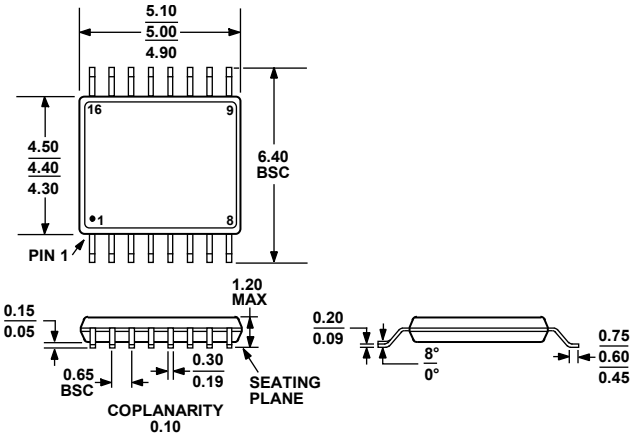



*Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-16)*
*Dimensions shown in millimeters*

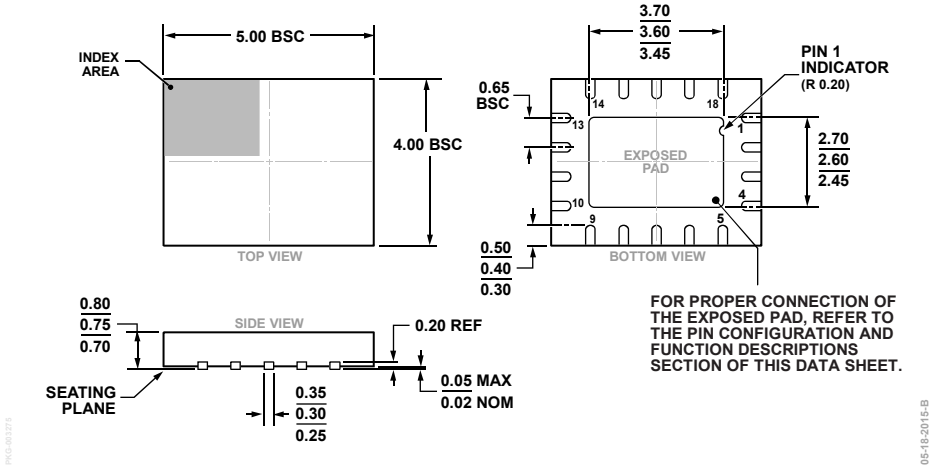



*Figure 34. 18-Lead Lead Frame Chip Scale Package [LFCSP_WQ]*
*5mm × 4 mm Body, Very Very Thin Quad*
*(CP-18-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2, 3, 4] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7357BCPZ | −40°C to +125°C | 18-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-18-1 |
| AD7357BCPZ-RL | −40°C to +125°C | 18-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-18-1 |
| AD7357BRUZ | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| AD7357BRUZ-500RL7 | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| AD7357BRUZ-RL | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| AD7357YRUZ | −40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| AD7357YRUZ-500RL7 | −40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| AD7357YRUZ-RL | −40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| AD7357WYRUZ | −40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| AD7357WYRUZ-RL | −40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| EVAL-AD7357EDZ | | Evaluation Board | |
| EVAL-CED1Z | | Converter Evaluation and Development Board | |

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] The EVAL-AD7357EDZ can be used as a standalone evaluation board or in conjunction with the EVAL-CED1Z board for evaluation/demonstration purposes.
[4] The EVAL-CED1Z is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the ED designator.

## AUTOMOTIVE PRODUCTS

The AD7357W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.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