

74ABT244

Octal Buffer/Line Driver with 3-STATE Outputs

Features

- Non-inverting buffers
- Output sink capability of 64mA, source capability of 32mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50pF and 250pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High-impedance, glitch-free bus loading during entire power up and power down cycle
- Nondestructive, hot-insertion capability
- Disable time less than enable time to avoid bus contention

General Description

The ABT244 is an octal buffer and line driver with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

Ordering Information

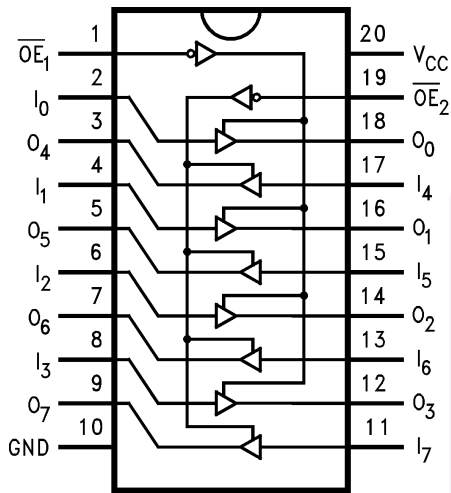
Order Number	Package Number	Package Description
74ABT244CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ABT244CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT244CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ABT244CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active LOW)
I_0-I_7	Inputs
O_0-O_7	Outputs

Truth Table

\overline{OE}_1	I_{0-3}	O_{0-3}	\overline{OE}_2	I_{4-7}	O_{4-7}
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	–65°C to +150°C
T_A	Ambient Temperature Under Bias	–55°C to +125°C
T_J	Junction Temperature Under Bias	–55°C to +150°C
V_{CC}	V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
V_{IN}	Input Voltage ⁽¹⁾	–0.5V to +7.0V
I_{IN}	Input Current ⁽¹⁾	–30mA to +5.0mA
V_O	Voltage Applied to Any Output Disabled or Power-Off State HIGH State	–0.5V to 5.5V –0.5V to V_{CC}
	Current Applied to Output in LOW State (Max.)	twice the rated I_{OL} (mA)
	DC Latchup Source Current	–500mA
	Over Voltage Latchup (I/O)	10V

Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	–40°C to +85°C
V_{CC}	Supply Voltage	+4.5V to +5.5V
$\Delta V / \Delta t$	Minimum Input Edge Rate	
	Data Input	50mV/ns
	Enable Input	20mV/ns

DC Electrical Characteristics

Symbol	Parameter		V _{CC}	Conditions	Min.	Typ.	Max.	Units
V _{IH}	Input HIGH Voltage			Recognized HIGH Signal	2.0			V
V _{IL}	Input LOW Voltage			Recognized LOW Signal			0.8	V
V _{CD}	Input Clamp Diode Voltage		Min.	I _{IN} = -18mA			-1.2	V
V _{OH}	Output HIGH Voltage		Min.	I _{OH} = -3mA	2.5			V
				I _{OH} = -32mA	2.0			
V _{OL}	Output LOW Voltage			I _{OL} = 64mA			0.55	V
I _{IH}	Input HIGH Current		Max.	V _{IN} = 2.7V ⁽³⁾			1	μA
				V _{IN} = V _{CC}			1	
I _{BVI}	Input HIGH Current Breakdown Test		Max.	V _{IN} = 7.0V			7	μA
I _{IL}	Input LOW Current		Max.	V _{IN} = 0.5V ⁽³⁾			-1	μA
				V _{IN} = 0.0V			-1	
V _{ID}	Input Leakage Test		0.0	I _{ID} = 1.9μA, All Other Pins Grounded	4.75			V
I _{OZH}	Output Leakage Current		0-5.5V	V _{OUT} = 2.7V, \overline{OE}_n = 2.0V			10	μA
I _{OZL}	Output Leakage Current		0-5.5V	V _{OUT} = 0.5V, \overline{OE}_n = 2.0V			-10	μA
I _{OS}	Output Short-Circuit Current		Max.	V _{OUT} = 0.0V	-100		-275	mA
I _{CEX}	Output High Leakage Current		Max.	V _{OUT} = V _{CC}			50	μA
I _{ZZ}	Bus Drainage Test		0.0	V _{OUT} = 5.5V, All Others GND			100	μA
I _{CCH}	Power Supply Current		Max.	All Outputs HIGH			50	μA
I _{CCL}	Power Supply Current		Max.	All Outputs LOW			30	mA
I _{CCZ}	Power Supply Current		Max.	\overline{OE}_n = V _{CC} , All Others at V _{CC} or Ground			50	μA
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled	Max.	V _I = V _{CC} - 2.1V			2.5	mA
		Outputs 3-STATE		Enable Input V _I = V _{CC} - 2.1V			2.5	mA
		Outputs 3-STATE		Data Input V _I = V _{CC} - 2.1V, All Others at V _{CC} or Ground			50	μA
I _{CCD}	Dynamic I _{CC} No Load ⁽³⁾		Max.	Outputs OPEN, \overline{OE}_n = GND ⁽²⁾ , One-Bit Toggling, 50% Duty Cycle			0.1	mA/MHz

Notes:

- For 8-bit toggling, I_{CCD} < 0.8mA/MHz.
- Guaranteed, but not tested.

DC Electrical Characteristics

SOIC package.

Symbol	Parameter	V _{CC}	Conditions C _L = 50pF, R _L = 500Ω	Min.	Typ.	Max.	Units
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	T _A = 25°C ⁽⁴⁾		0.5	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	T _A = 25°C ⁽⁴⁾	−1.3	−0.8		V
V _{OHV}	Minimum HIGH Level Dynamic Output Voltage	5.0	T _A = 25°C ⁽⁶⁾	2.7	3.1		V
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	T _A = 25°C ⁽⁵⁾	2.0	1.5		V
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	T _A = 25°C ⁽⁵⁾		1.1	0.8	V

Notes:

- Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.
- Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.
- Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

SOIC and SSOP package.

Symbol	Parameter	T _A = +25°C, V _{CC} = +5V, C _L = 50pF			T _A = −55°C to +125°C, V _{CC} = 4.5V–5.5V, C _L = 50pF		T _A = −40°C to +85°C, V _{CC} = 4.5V–5.5V, C _L = 50pF		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay Data to Outputs	1.0	2.5	3.6	1.0	5.3	1.0	3.6	ns
t _{PHL}		1.0	2.3	3.6	1.0	5.0	1.0	3.6	
t _{PZH}	Output Enable Time	1.5	3.5	6.0	0.8	6.5	1.5	6.0	ns
t _{PZL}		1.5	3.6	6.0	1.2	7.9	1.5	6.0	
t _{PHZ}	Output Disable Time	1.7	3.5	5.6	1.2	7.6	1.7	5.6	ns
t _{PLZ}		1.7	3.3	5.6	1.0	7.9	1.7	5.6	

Extended AC Electrical Characteristics

SOIC package.

Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$, $V_{CC} = 4.5\text{V} - 5.5\text{V}$, $C_L = 50\text{pF}$, 8 Outputs Switching ⁽⁷⁾			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$, $V_{CC} = 4.5\text{V} - 5.5\text{V}$, $C_L = 250\text{pF}$, 1 Output Switching ⁽⁸⁾		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$, $V_{CC} = 4.5\text{V} - 5.5\text{V}$, $C_L = 250\text{pF}$, 8 Outputs Switching ⁽⁹⁾		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f _{TOGGLE}	Max Toggle Frequency		100						MHz
t _{PLH}	Propagation Delay, Data to Outputs	1.5		5.0	1.5	6.0	2.5	8.5	ns
t _{PHL}		1.5		5.0	1.5	6.0	2.5	8.5	
t _{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	10.0	ns
t _{PZL}		1.5		6.5	2.5	7.5	2.5	12.0	
t _{PHZ}	Output Disable Time	1.0		5.6	(10)		(10)		ns
t _{PLZ}		1.0		5.6					

Notes:

- This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).
- This specification is guaranteed but not tested. The limits represent propagation delay with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load. This specification pertains to single output switching only.
- This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
- The 3-STATE delays are dominated by the RC network (500Ω, 250pF) on the output and have been excluded from the datasheet.

Skew

Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C},$ $V_{CC} = 4.5\text{V} - 5.5\text{V},$ $C_L = 50\text{pF},$ 8 Outputs Switching ⁽¹³⁾	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C},$ $V_{CC} = 4.5\text{V} - 5.5\text{V},$ $C_L = 250\text{pF},$ 8 Outputs Switching ⁽¹⁴⁾	Units
		Max.	Max.	
$t_{OSHL}^{(11)}$	Pin to Pin Skew, HL Transitions	0.8	1.8	ns
$t_{OSLH}^{(11)}$	Pin to Pin Skew, LH Transitions	0.8	1.8	ns
$t_{PS}^{(15)}$	Duty Cycle, LH–HL Skew	1.0	2.5	ns
$t_{OST}^{(11)}$	Pin to Pin Skew, LH/HL Transitions	1.0	2.5	ns
$t_{PV}^{(12)}$	Device to Device Skew, LH/HL Transitions	1.5	3.0	ns

Notes:

11. Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). The specification is guaranteed but not tested.
12. Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.
13. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)
14. These specifications guaranteed but not tested. The limits represent propagation delays with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
15. This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

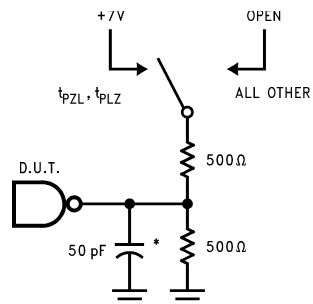
Capacitance

Symbol	Parameter	Conditions $T_A = 25^{\circ}\text{C}$	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = 0\text{V}$	5.0	pF
$C_{OUT}^{(16)}$	Output Capacitance	$V_{CC} = 5.0\text{V}$	9.0	pF

Note:

16. C_{OUT} is measured at frequency $f = 1\text{MHz}$, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

Figure 1. Standard AC Test Load

AC Waveforms

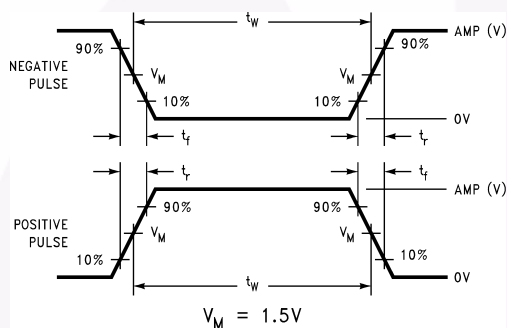


Figure 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500ns	2.5ns	2.5ns

Figure 3. Test Input Signal Requirements

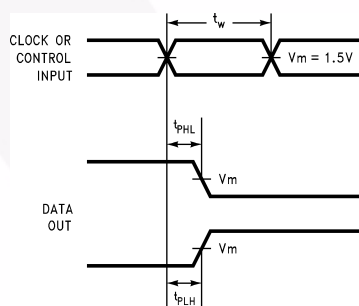


Figure 4. Propagation Delay, Pulse Width Waveforms

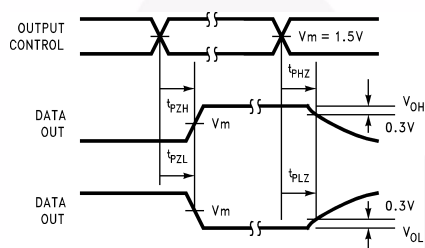


Figure 5. 3-STATE Output HIGH and LOW Enable and Disable Times

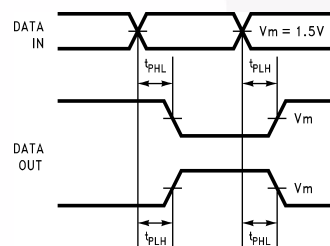


Figure 6. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

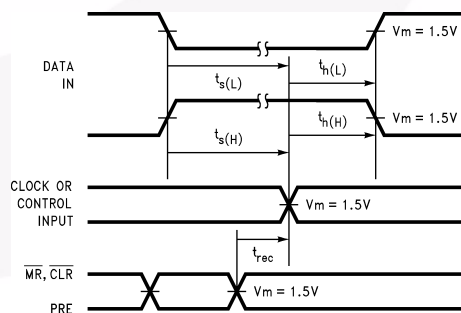


Figure 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions

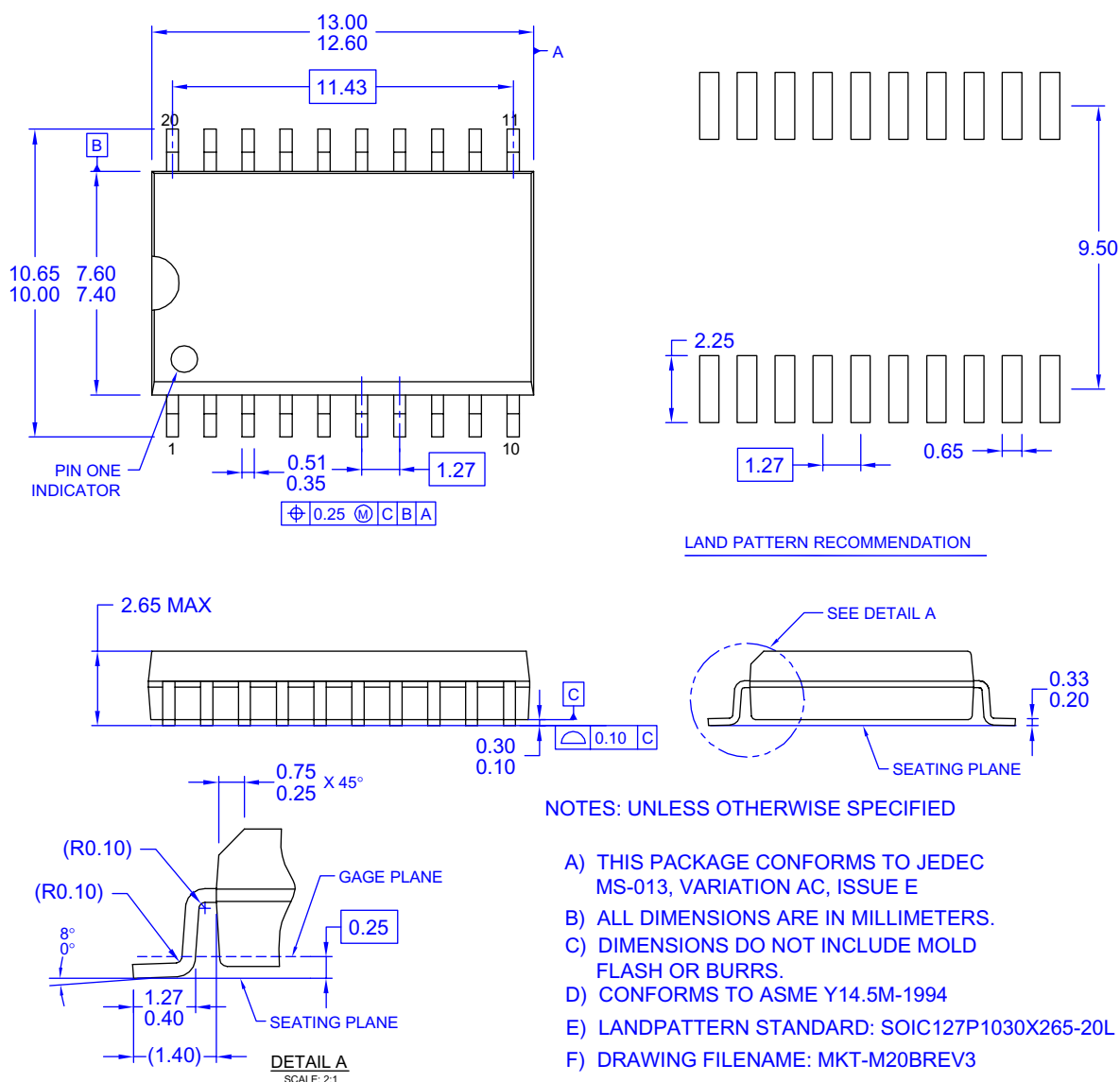


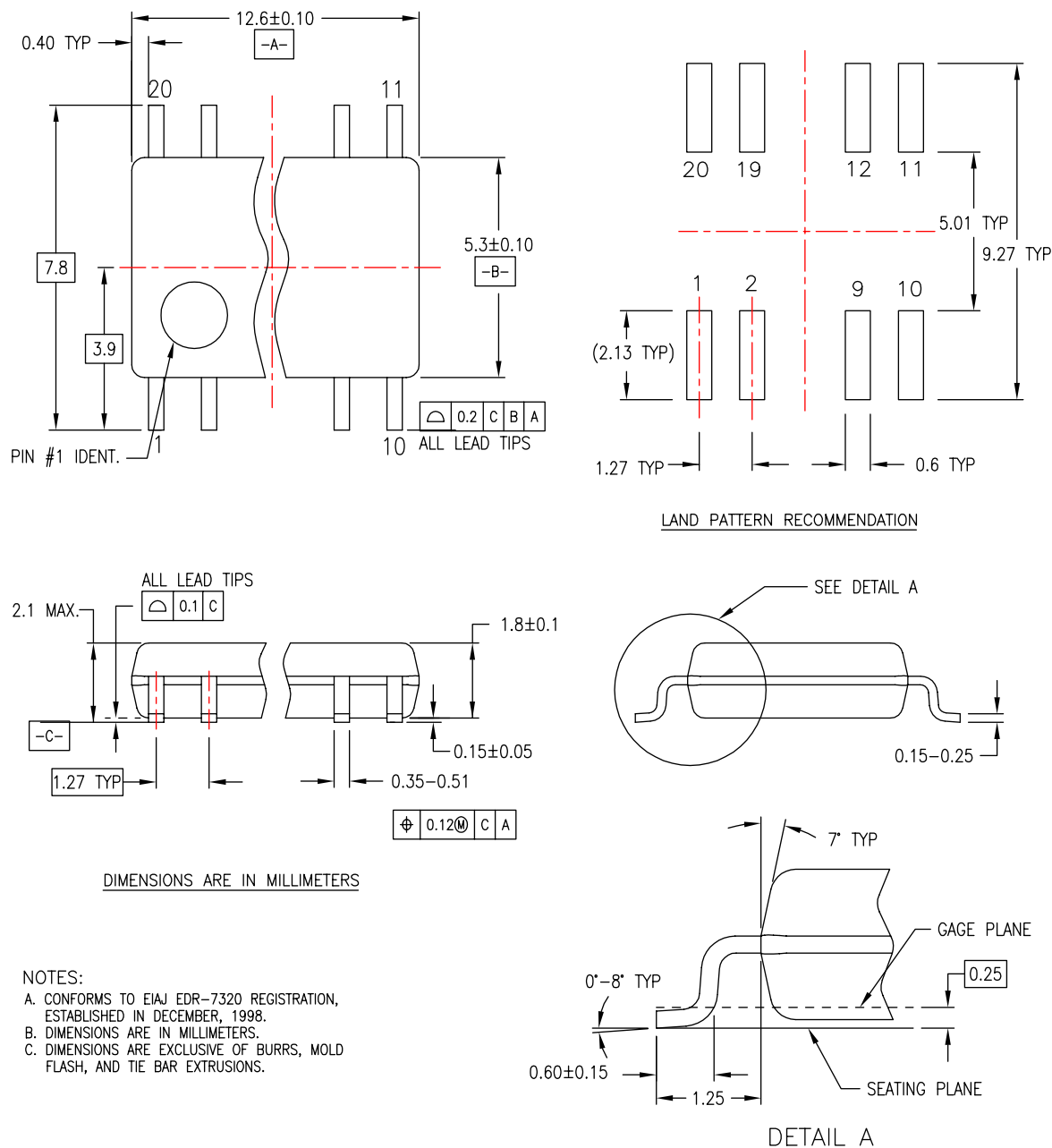
Figure 8. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



M20DREVC

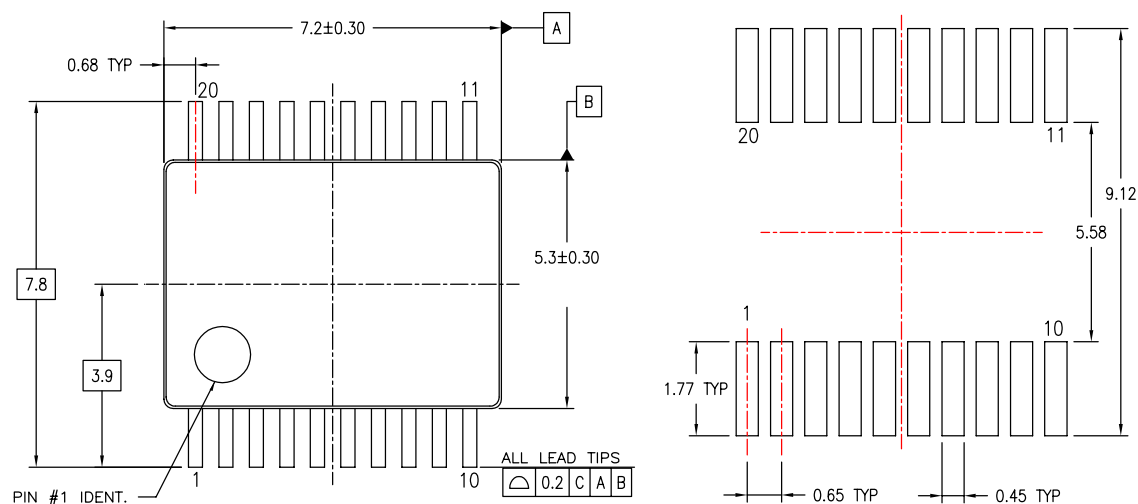
Figure 9. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

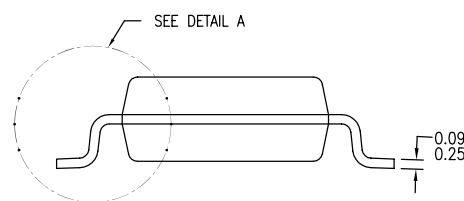
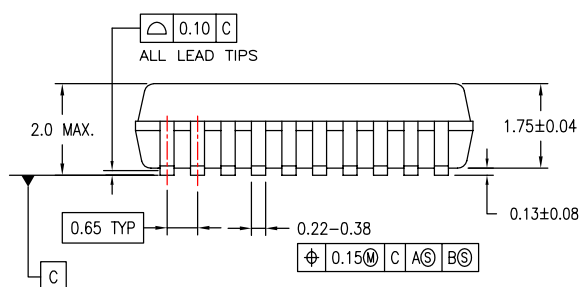
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



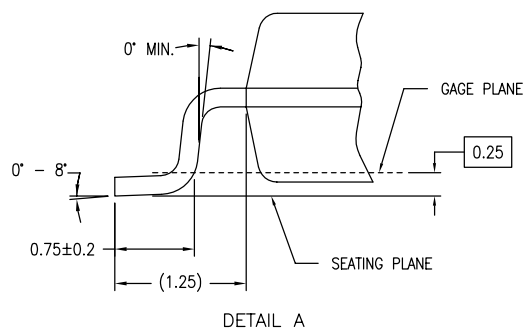
LAND PATTERN RECOMMENDATIONS



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-150, VARIATION AE, DATE 1/94.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M - 1994.



MSA20REVB

Figure 10. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.



Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx [®]	FPS [™]	PDP-SPM [™]	SyncFET [™]
Build it Now [™]	FRFET [®]	Power220 [®]	SYSTEM [®]
CorePLUS [™]	Global Power Resource SM	Power247 [®]	GENERAL
CROSSVOLT [™]	Green FPS [™]	POWEREDGE [™]	The Power Franchise [®]
CTL [™]	Green FPS [™] e-Series [™]	Power-SPM [™]	the power [™]
Current Transfer Logic [™]	GTO [™]	PowerTrench [®]	franchise
EcoSPARK [®]	i-Lo [™]	Programmable Active Droop [™]	TinyBoost [™]
EZSWITCH [™] *	IntelliMAX [™]	QFET [®]	TinyBuck [™]
 [™]	ISOPLANAR [™]	QS [™]	TinyLogic [®]
 [®]	MegaBuck [™]	QT Optoelectronics [™]	TINYOPTO [™]
Fairchild [®]	MICROCOUPLER [™]	Quiet Series [™]	TinyPower [™]
Fairchild Semiconductor [®]	MicroFET [™]	RapidConfigure [™]	TinyPWM [™]
FACT Quiet Series [™]	MicroPak [™]	SMART START [™]	TinyWire [™]
FACT [®]	MillerDrive [™]	SPM [®]	μSerDes [™]
FAST [®]	Motion-SPM [™]	STEALTH [™]	UHC [®]
FastvCore [™]	OPTOLOGIC [®]	SuperFET [™]	Ultra FRFET [™]
FlashWriter [®] *	OPTOPLANAR [®]	SuperSOT [™] -3	UniFET [™]
		SuperSOT [™] -6	VCX [™]
		SuperSOT [™] -8	

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I32

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative