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1 Maximum ratings

Symbol	Parameter		Unit	
Symbol	Farameter	SO20	PowerSO-10	Unit
V _{CC}	DC supply voltage		41	V
-V _{CC}	Reverse DC supply voltage		-0.3	V
-I _{GND}	DC reverse ground pin		-200	mA
I _{OUT}	DC output current	Internally limited		А
-I _{OUT}	Reverse DC output current	-2		А
I _{IN}	DC input current	± 10		mA
V _{IN}	Input voltage range	-3/+V _{CC}		V
V _{STAT}	DC status voltage	+ V _{CC}		V
V _{ESD}	Electrostatic discharge (R = $1.5 \text{ k}\Omega$; C = 100 pF)		2000	
P _{tot}	Power dissipation at $T_c \le 25 \degree C$	16	90	W
TJ	Junction operating temperature	Intern	Internally limited	
T _c	Case operating temperature	-40	-40 to 150	
T _{stg}	Storage temperature	-5	5 to 150	°C

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Table 2. Thermal data

Symbol	/mbol Parameter				alues	Unit
Farameter			SO20	PowerSO-10	Onit	
R _{th(JP)}	Thermal resistance junction-pins	Max.	8	-	°C/W	
R _{th(JA)}	Thermal resistance junction-ambient	Max.	58	52 ⁽¹⁾ 37 ⁽²⁾	°C/W	
R _{th(JC)}	Thermal resistance junction-case	Max.	-	1.4	°C/W	

1. When mounted on FR4 printed circuit board with 0.5 cm^2 of copper area (at least 35 μ thick) connected to all V_{CC} pins.

2. When mounted on FR4 printed circuit board with 6 cm² of copper area (at least 35 μ thick) connected to all V_{CC} pins.



2 Pin connection

Figure 2. Configuration diagram (top view)

Table 3. Pin connection

Connection / pin	Status	N.C.	Output	Input
Floating	Х	Х	Х	Х
To ground		Х		Through 10 k Ω resistor

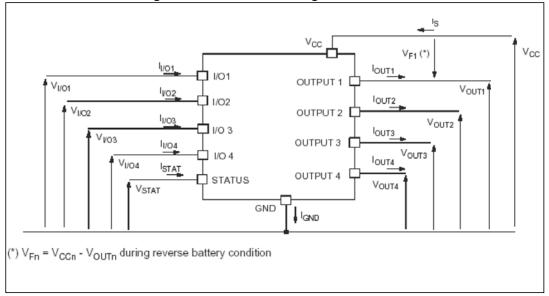


Figure 3. Current and voltage conventions



3 Electrical characteristics

8 V < V_{CC} < 36 V; -40 °C < T_J < 150 °C; unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit	
V _{CC}	Operating supply voltage		5.5		36	V	
V _{USD}	Undervoltage shutdown		3	4	5.5	V	
V _{OV}	Overvoltage shutdown		36	42	48	V	
R _{ON}	On state resistance (per channel)	I _{OUT} = 0.25 A; T _J = 25 °C; I _{OUT} = 0.25 A;			270 540	mΩ	
I _S	Supply current	OFF state; V _{CC} = 24 V;T _C = 25 °C ON state (all channels ON)		70 5	120 10	μA mA	
I _{LGND}	Output current	$V_{CC} - V_{STAT} = V_{IN} = V_{GND} = 24$ V; $V_{OUT} = 0$ V			1	mA	
I _{L(OFF)}	OFF state output current	V _{IN} = V _{OUT} = 0 V	0		10	μA	
I _{OUTleak}	OFF state output leakage current	V _{IN} = V _{GND} = 0 V; V _{CC} = V _{OUT} = 24 V; T _A = 25 °C			240	μA	
I _{OUTleak}	OFF state output leakage current	V _{IN} = V _{GND} = 0 V; V _{CC} = 24 V; V _{OUT} = 10 V; T _A = 25 °C			100	μA	

Table 4. Power section	on
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Table 5. Switching (V_{CC} = 24 V)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _(ON)	Turn-on delay time of output current	R _L = 96 Ω from V _{IN} rising edge to V _{OUT} = 2.4 V	-	10	-	μs
t _(OFF)	Turn-off delay time of output current	R_L = 96 Ω from V _{IN} rising edge to V _{OUT} = 21.6 V	-	40	-	μs
(dV _{OUT} /dt) _{on}	Turn-on voltage slope	R _L = 96 Ω from V _{OUT} = 2.4 V to 19.2 V	-	0.75	-	V/µs
(dV _{OUT} /dt) _{off}	Turn-off voltage slope	R _L = 96 Ω from V _{OUT} = 21.6 V to 2.4 V	-	0.25	-	V/µs

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit		
l _{lim}	Current limitation		0.35	0.7	1.1	А		
T _(hyst)	Thermal hysteresis		7	15		°C		
T _{TSD}	Thermal shutdown temperature		150	175	200	°C		
Τ _R	Reset temperature		135			°C		
V _{demag}	Turn-off output clamp voltage	I _{OUT} = 0.25 A, V _{CC} = 24 V	V _{CC} - 59	V _{CC} - 52	V _{CC} - 47	V		

Table 6. Protections (per channel)

Table 7. Logic input (per channel)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{IL}	Low level input voltage			-	1.25	V
۱ _{IL}	Low level input current	V _{IN} = 1.25 V	1	-		μA
V _{IH}	High level input voltage		3.25	-		V
IIH	High level input current	V _{IN} = 3.25 V		-	10	μA
V _{I(HYST)}	Input hysteresis voltage		0.5	-		V
I _{IN}	Input current	V _{IN} = V _{CC} = 36 V		-	200	μA
VOL	I/O output voltage	I _{IN} = 5 mA (fault condition)		-	1	V

Table 8. Status pin

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
VSTAT	Status low output voltage	I _{STAT} = 5 mA (fault condition)	-	-	1	V
ILSTAT	Status leakage current	Normal operation; $V_{STAT} = V_{CC} = 36 V$	-	-	20	μA
C _{STAT}	Status pin input capacitance	Normal operation; V _{STAT} = 5 V	-	-	100	pF

Table 9. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
VF	Forward on voltage	-I _{OUT} = 0.3 A; T _J = 150 °C	-	-	1	V



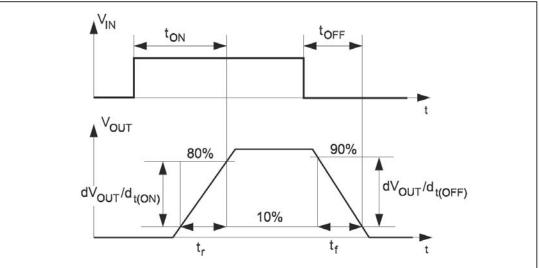
Truth table and switching characteristics

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Conditions	MCOUTn	l/On	OUTPUTn	STATUS
Normal an anation	L	L	L	Н
Normal operation	Н	Н	Н	н
Current limitation	L	L	L	Н
	Н	Н	Х	н
Overtemperature	L	L	L	L
	Н	Driven low	L	L
Undervoltage	L	L	L	Х
	Н	Н	L	Х
Overseltere	L	L	L	Н
Overvoltage	Н	Н	L	Н

Table 10. Truth table

Figure 4. Switching characteristics





5 Typical application schematic

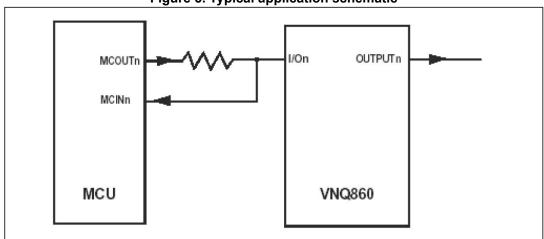
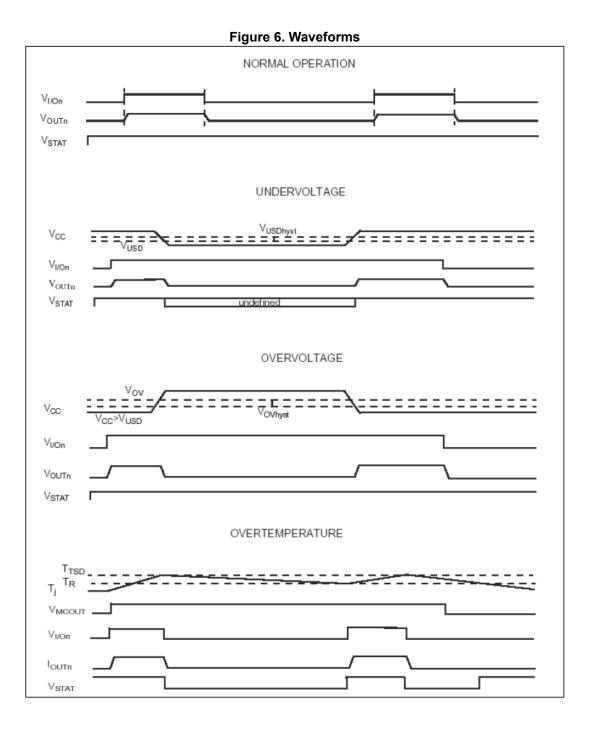


Figure 5. Typical application schematic



6 Waveforms



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7 PowerSO-10[™] thermal data

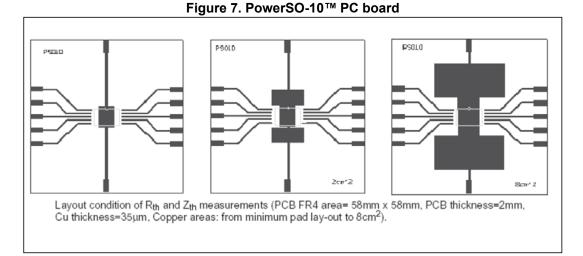
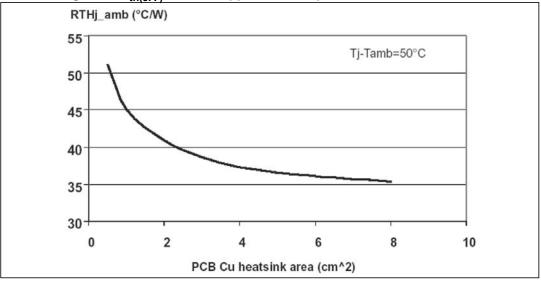


Figure 8. $R_{th(JA)}$ vs PBC copper area in open box free air condition





8 Reverse polarity protection

A solution to protect the IC against a reverse polarity condition is proposed in Figure 9.

This schematic is valid with any type of load connected to the outputs of the IC.

The R_{GND} resistor value can be selected according to the following conditions:

Equation 1

 $R_{GND} \leq~600~mV$ / (I_S in ON state max.).

Equation 2

 $R_{GND} \ge (-V_{CC}) / (-I_{GND})$

where -I_{GND} is the DC reverse ground pin current and can be found in *Table 1: Absolute maximum ratings*.

The power dissipation associated to R_{GND} during the reverse polarity condition is:

 $PD = (-V_{CC})^2 / R_{GND}$

This resistor can be shared by different ICs. In such case, I_S value, indicated in *Equation 1*, is the sum of the maximum ON-state currents of the different devices.

Please note that, if the microprocessor ground and the device ground are separated then the voltage drop across the R_{GND} (given by I_S in ON state max. * R_{GND}) produces a difference between the generated input level and the IC input signal level. This voltage drop varies depending on how many devices are ON in the case of several high-side switches sharing the same R_{GND} .

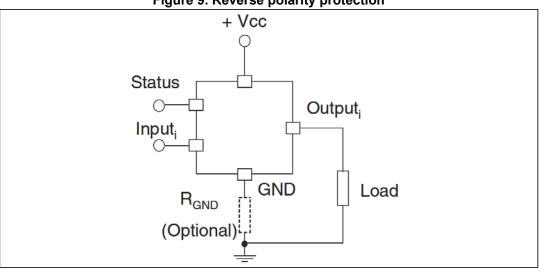


Figure 9. Reverse polarity protection



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

	mm			inch		
Dim.	Min	Тур	Мах	Min	Тур	Max
А	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
В	0.40		0.60	0.016		0.024
с	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
е		1.27			0.050	
F	1.25		1.35	0.049		0.053
Н	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
а	0°		8°			

Table 11	PowerSO-10™	mechanical	data
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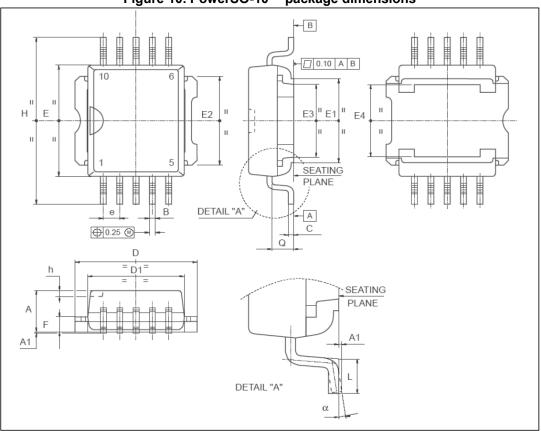
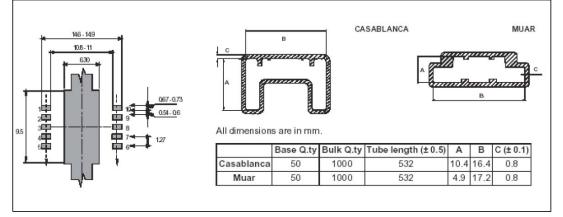


Figure 10. PowerSO-10[™] package dimensions

Figure 11. PowerSO-10[™] suggested pad and tube shipment (no suffix)





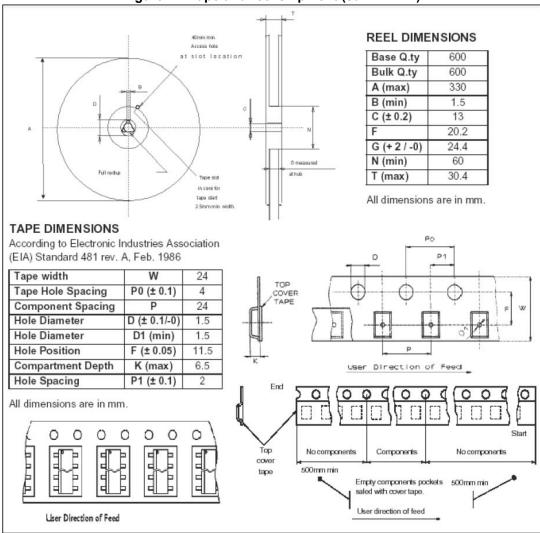


Figure 12. Tape and reel shipment (suffix "TR")



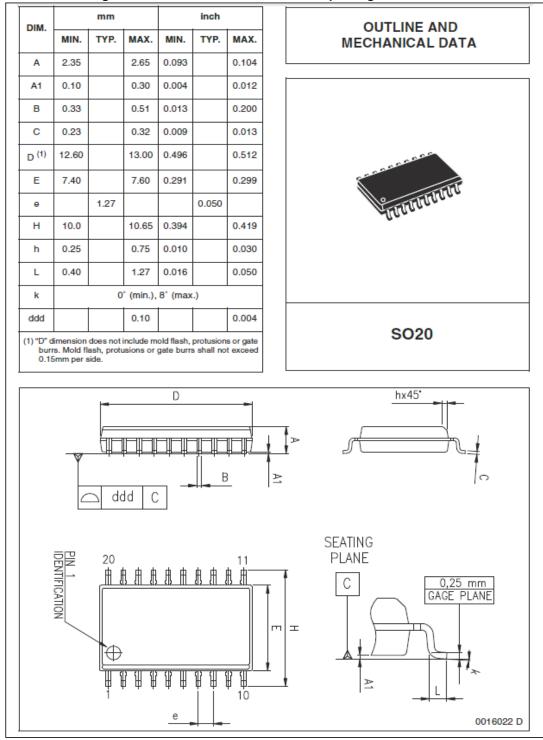


Figure 13. SO20 mechanical data and package dimensions



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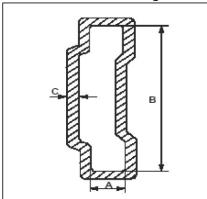


Figure 14. SO20 tube shipment (no suffix)

Base Q.ty	40
Bulk Q.ty	800
Tube length (± 0.5)	532
Α	3.5
В	13.8
C (± 0.1)	0.6
В	13.8

All dimensions are in mm.

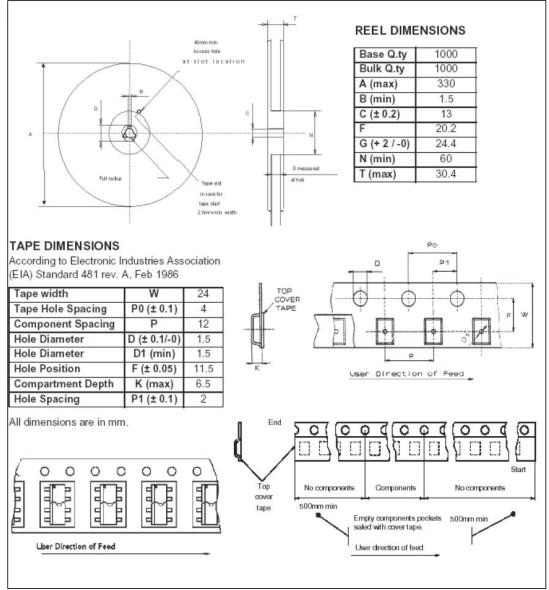


Figure 15. Tape and reel shipment (suffix "13TR")

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10 Ordering information

Order codes	Package	Packaging		
VNQ860-E	SO20	Tube		
VNQ860SP-E	PowerSO-10™			
VNQ860TR-E	SO20	Tapa and real		
VNQ860SPTR-E	PowerSO-10™	- Tape and reel		

Table 12. Ordering information



11 Revision history

Date	Revision Changes	
14-Jul-2005	1	Updates, new template
7-Nov-2005	2	Few updates
07-Jul-2008	3	Added Section 8 on page 11
28-Apr-2009	4	Updated Figure 13 on page 15
05-May-2010	5	Updated coverpage
31-Aug-2010	6	Updated Table 10 on page 7
15-Mar-2013	7	Updated <i>Table 1</i> and <i>Table 12</i> . Minor text changes.
15-Jan-2020	8	Change to <i>Table 8</i> value.

Table 13. Document revision history

