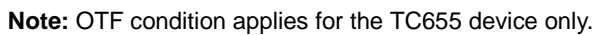


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## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings \*

$V_{DD}$  ..... 6.5V  
 Input Voltages ..... -0.3V to ( $V_{DD} + 0.3V$ )  
 Output Voltages ..... -0.3V to ( $V_{DD} + 0.3V$ )  
 Storage temperature ..... -65°C to +150°C  
 Ambient temp. with power applied ..... -40°C to +125°C  
 Maximum Junction Temperature,  $T_J$  ..... 150°C  
 ESD protection on all pins .....  $\geq 4$  kV

**\*Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## PIN FUNCTION TABLE

Name	Function
$V_{IN}$	Analog Input
$C_F$	Analog Output
SCLK	Serial Clock Input
SDA	Serial Data In/Out (Open Drain)
GND	Ground
$\overline{FAULT}$	Digital (Open Drain) Output
SENSE2	Analog Input
SENSE1	Analog Input
$V_{OUT}$	Digital Output
$V_{DD}$	Power Supply Input

## ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise noted, all limits are specified for  $V_{DD} = 3.0V$  to  $5.5V$ ,  $-40^\circ C < T_A < +85^\circ C$ .

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	$V_{DD}$	3.0	—	5.5	V	
Operating Supply Current	$I_{DD}$	—	150	300	$\mu A$	Pins 7, 8, 9 Open
Shutdown Mode Supply Current	$I_{DDSHDN}$	—	5	10	$\mu A$	Pins 7, 8, 9 Open
<b><math>V_{OUT}</math> PWM Output</b>						
$V_{OUT}$ Rise Time	$t_R$	—	—	50	$\mu sec$	$I_{OH} = 5$ mA, <a href="#">Note 1</a>
$V_{OUT}$ Fall Time	$t_F$	—	—	50	$\mu sec$	$I_{OL} = 1$ mA, <a href="#">Note 1</a>
Sink Current at $V_{OUT}$ Output	$I_{OL}$	1.0	—	—	mA	$V_{OL} = 10\%$ of $V_{DD}$
Source Current at $V_{OUT}$ Output	$I_{OH}$	5.0	—	—	mA	$V_{OH} = 80\%$ of $V_{DD}$
PWM Frequency	F	26	30	34	Hz	$C_F = 1$ $\mu F$
<b><math>V_{IN}</math> Input</b>						
$V_{IN}$ Input Voltage for 100% PWM duty-cycle	$V_{C(MAX)}$	2.45	2.6	2.75	V	
$V_{C(MAX)} - V_{C(MIN)}$	$V_{CRANGE}$	1.25	1.4	1.55	V	
$V_{IN}$ Input Resistance		—	10M	—	$\Omega$	$V_{DD} = 5.0V$
$V_{IN}$ Input Leakage Current	$I_{IN}$	-1.0	—	+1.0	$\mu A$	
<b>SENSE Input</b>						
SENSE Input Threshold Voltage with Respect to GND	$V_{THSENSE}$	80	100	120	mV	
<b>FAULT Output</b>						
$\overline{FAULT}$ Output LOW Voltage	$V_{OL}$	—	—	0.3	V	$I_{OL} = 2.5$ mA
$\overline{FAULT}$ Output Response Time	$t_{FAULT}$	—	2.4	—	sec	
<b>Fan RPM-to-Digital Output</b>						
Fan RPM ERROR		-15	—	+15	%	RPM > 1600

**Note 1:** Not production tested, ensured by design, tested during characterization.

**2:** For  $5.0V > V_{DD} \leq 5.5V$ , the limit for  $V_{IH} = 2.2V$ .

# TC654/TC655

## ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise noted, all limits are specified for  $V_{DD} = 3.0V$  to  $5.5V$ ,  $-40^{\circ}C < T_A < +85^{\circ}C$ .

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>2-Wire Serial Bus Interface</b>						
Logic Input High	$V_{IH}$	2.1	—	—	V	Note 2
Logic Input Low	$V_{IL}$	—	—	0.8	V	
Logic Output Low	$V_{OL}$	—	—	0.4	V	$I_{OL} = 3\text{ mA}$
Input Capacitance SDA, SCLK	$C_{IN}$	—	10	15	pF	Note 1
I/O Leakage Current	$I_{LEAK}$	-1.0	—	+1.0	$\mu A$	
SDA Output Low Current	$I_{OLSDA}$	6	—	—	mA	$V_{OL} = 0.6V$

**Note 1:** Not production tested, ensured by design, tested during characterization.

**2:** For  $5.0V > V_{DD} \leq 5.5V$ , the limit for  $V_{IH} = 2.2V$ .

## TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at  $V_{DD} = 3.0V$  to  $5.5V$

Parameters	Symbol	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+85	$^{\circ}C$	
Operating Temperature Range	$T_A$	-40	—	+125	$^{\circ}C$	
Storage Temperature Range	$T_A$	-65	—	+150	$^{\circ}C$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 10 Pin MSOP	$\theta_{JA}$	—	113	—	$^{\circ}C/W$	

## TIMING SPECIFICATIONS

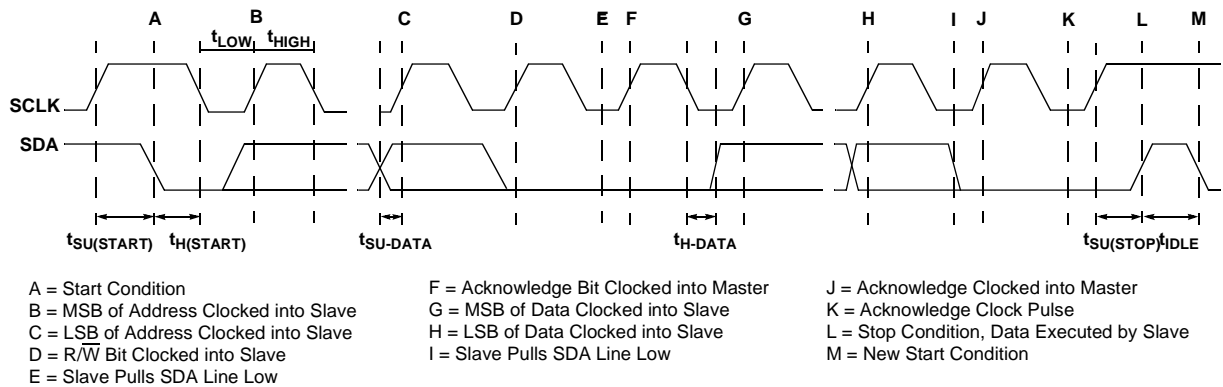
**Electrical Characteristics:** Unless otherwise noted, all limits are specified for  $V_{DD} = 3.0V$  to  $5.5V$ ,  $-40^{\circ}C < T_A < +85^{\circ}C$

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>SMBus Interface (See Figure 1-1)</b>						
Serial Port Frequency	$f_{SC}$	0	—	100	kHz	Note 1
Low Clock Period	$t_{LOW}$	4.7	—	—	$\mu sec$	Note 1
High Clock Period	$t_{HIGH}$	4.7	—	—	$\mu sec$	Note 1
SCLK and SDA Rise Time	$t_R$	—	—	1000	nsec	Note 1
SCLK and SDA Fall Time	$t_F$	—	—	300	nsec	Note 1
Start Condition Setup Time	$t_{SU(START)}$	4.7	—	—	$\mu sec$	Note 1
SCLK Clock Period Time	$t_{SC}$	10	—	—	$\mu sec$	Note 1
Start Condition Hold Time	$t_{H(START)}$	4.0	—	—	$\mu sec$	Note 1
Data in SetupTime to SCLK High	$t_{SU-DATA}$	250	—	—	nsec	Note 1
Data in Hold Time after SCLK Low	$t_{H-DATA}$	300	—	—	nsec	Note 1
Stop Condition Setup Time	$t_{SU(STOP)}$	4.0	—	—	$\mu sec$	Note 1
Bus Free Time Prior to New Transition	$t_{IDLE}$	4.7	—	—	$\mu sec$	Note 1 and Note 2

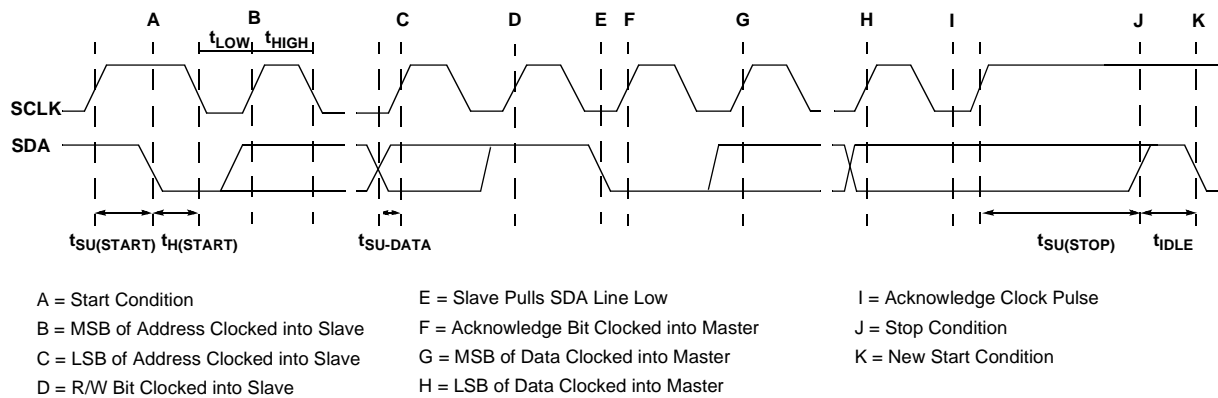
**Note 1:** Not production tested, ensured by design, tested during characterization.

**2:** Time the bus must be free before a new transmission can start.

## SMBus Write Timing Diagram



## SMBus Read Timing Diagram



**FIGURE 1-1:** Bus Timing Data.

# TC654/TC655

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

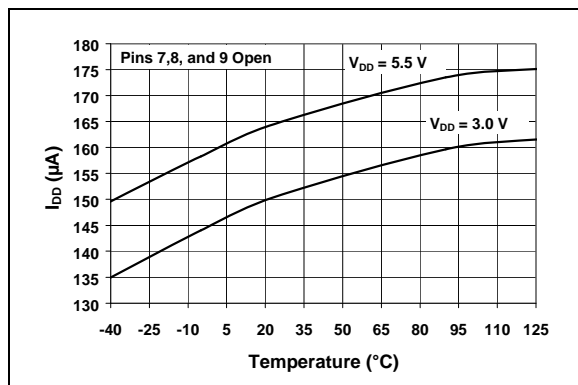


FIGURE 2-1:  $I_{DD}$  vs. Temperature.

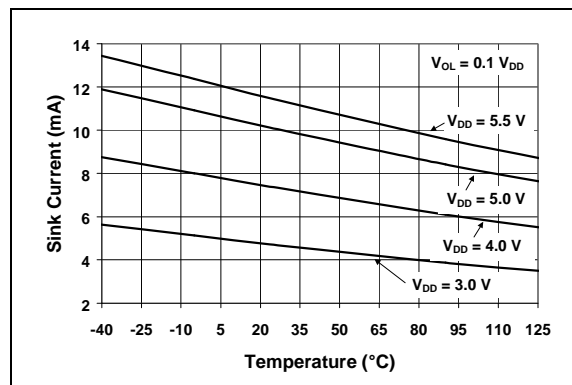


FIGURE 2-4: PWM, Sink Current vs. Temperature.

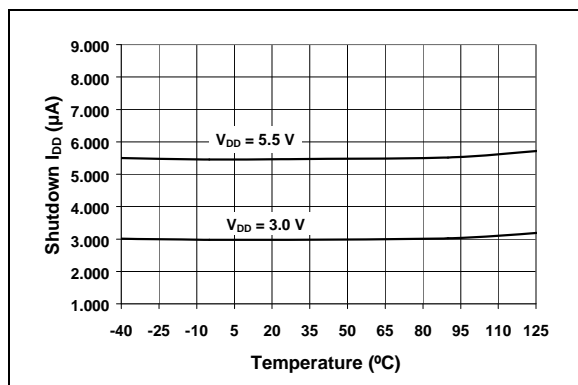


FIGURE 2-2:  $I_{DD}$  Shutdown vs. Temperature.

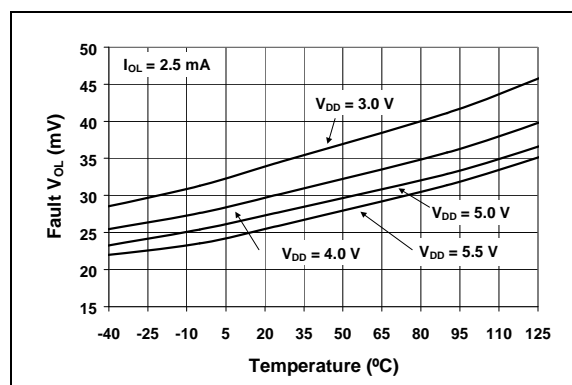


FIGURE 2-5: Fault  $V_{OL}$  vs. Temperature.

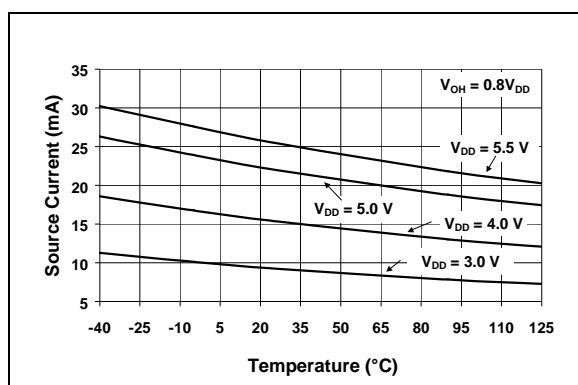


FIGURE 2-3: PWM, Source Current vs. Temperature.

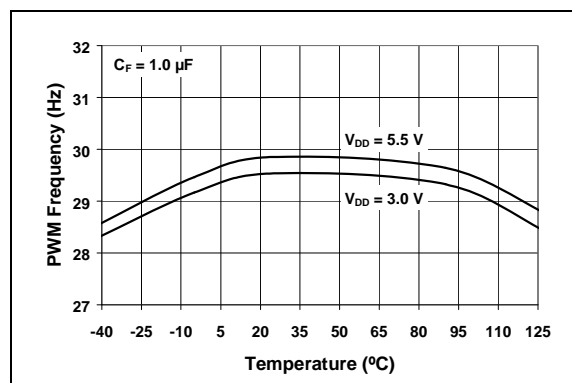
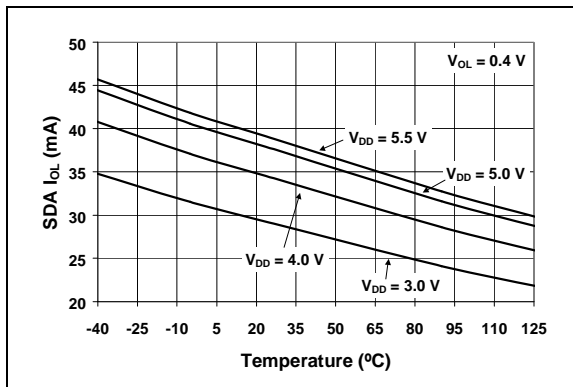
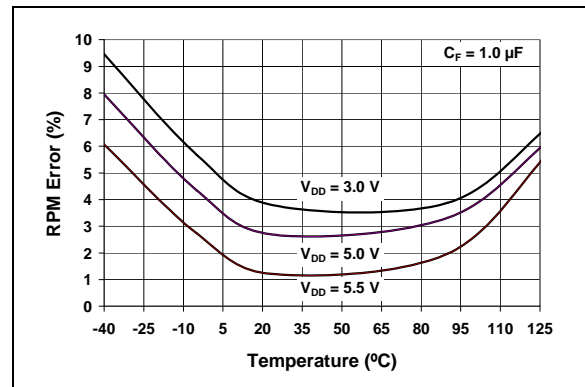


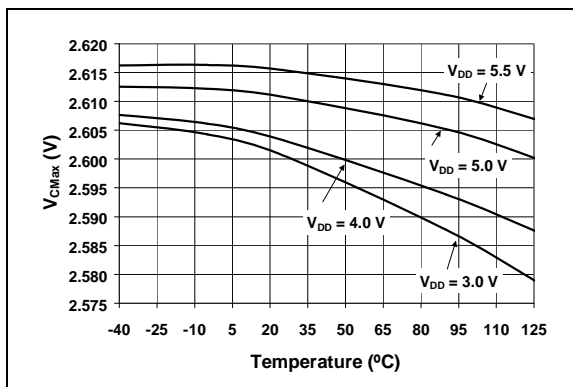
FIGURE 2-6: PWM Frequency vs. Temperature.



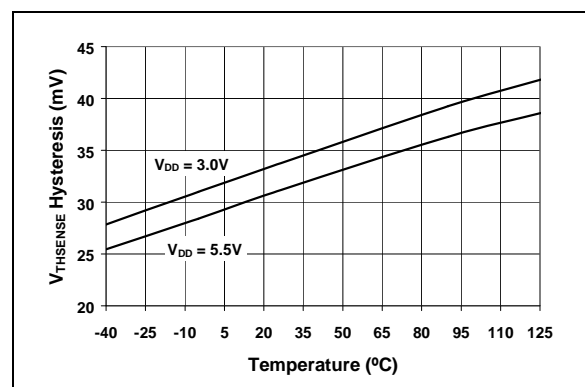
**FIGURE 2-7:** SDA  $I_{OL}$  vs. Temperature.



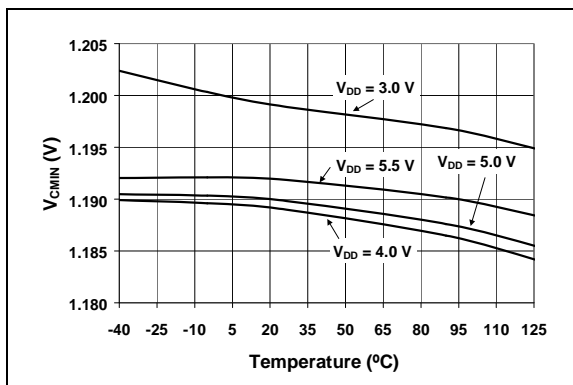
**FIGURE 2-10:** RPM %error vs. Temperature.



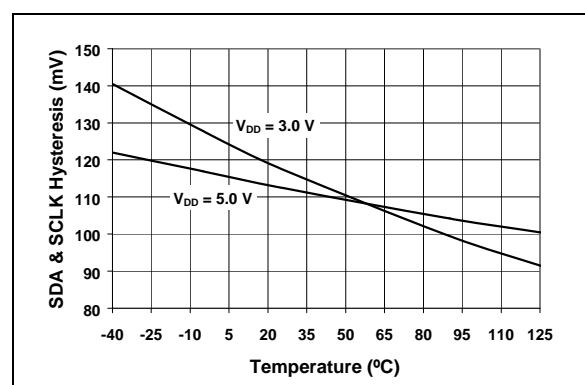
**FIGURE 2-8:**  $V_{CMAX}$  vs. Temperature.



**FIGURE 2-11:** Sense Threshold ( $V_{THSENSE}$ ) Hysteresis vs. Temperature.



**FIGURE 2-9:**  $V_{CMIN}$  vs. Temperature.



**FIGURE 2-12:** SDA, SCLK Hysteresis vs. Temperature.

# TC654/TC655

## 3.0 PIN FUNCTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

Name	Function
V <sub>IN</sub>	Analog Input
C <sub>F</sub>	Analog Output
SCLK	Serial Clock Input
SDA	Serial Data In/Out (Open Drain)
GND	Ground
FAULT	Digital (Open Drain) Output
SENSE2	Analog Input
SENSE1	Analog Input
V <sub>OUT</sub>	Digital Output
V <sub>DD</sub>	Power Supply Input

### 3.1 Analog Input (V<sub>IN</sub>)

A voltage range of 1.62V to 2.6V (typical) on this pin drives an active duty-cycle of 30% to 100% on the V<sub>OUT</sub> pin.

### 3.2 Analog Output (C<sub>F</sub>)

Positive terminal for the PWM ramp generator timing capacitor. The recommended C<sub>F</sub> is 1  $\mu$ F for 30 Hz PWM operation.

### 3.3 SMBus Serial Clock Input (SCLK)

Clocks data into and out of the TC654/TC655. See [Section 5.0 “Serial Communication”](#) for more information on the serial interface.

### 3.4 Serial Data (Bi-directional) (SDA)

Serial data is transferred on the SMBus in both directions using this pin. See [Section 5.0 “Serial Communication”](#) for more information on the serial interface.

### 3.5 Digital (Open Drain) Output (FAULT)

When the fan's RPM falls below the user-set RPM threshold (or OTF occurs with TC655), a logic low signal is asserted.

### 3.6 Analog Input (SENSE2)

Fan current pulses are detected at this pin. These pulses are counted and used in the calculation of the Fan 2 RPM.

### 3.7 Analog Input (SENSE1)

Fan current pulses are detected at this pin. These pulses are counted and used in the calculation of the Fan 1 RPM.

### 3.8 Digital Output (V<sub>OUT</sub>)

This active high complimentary output drives the base of an external transistor or the gate of a MOSFET.

### 3.9 Power Supply Input (V<sub>DD</sub>)

The V<sub>DD</sub> pin with respect to GND provides power to the device. This bias supply voltage may be independent of the fan power supply.

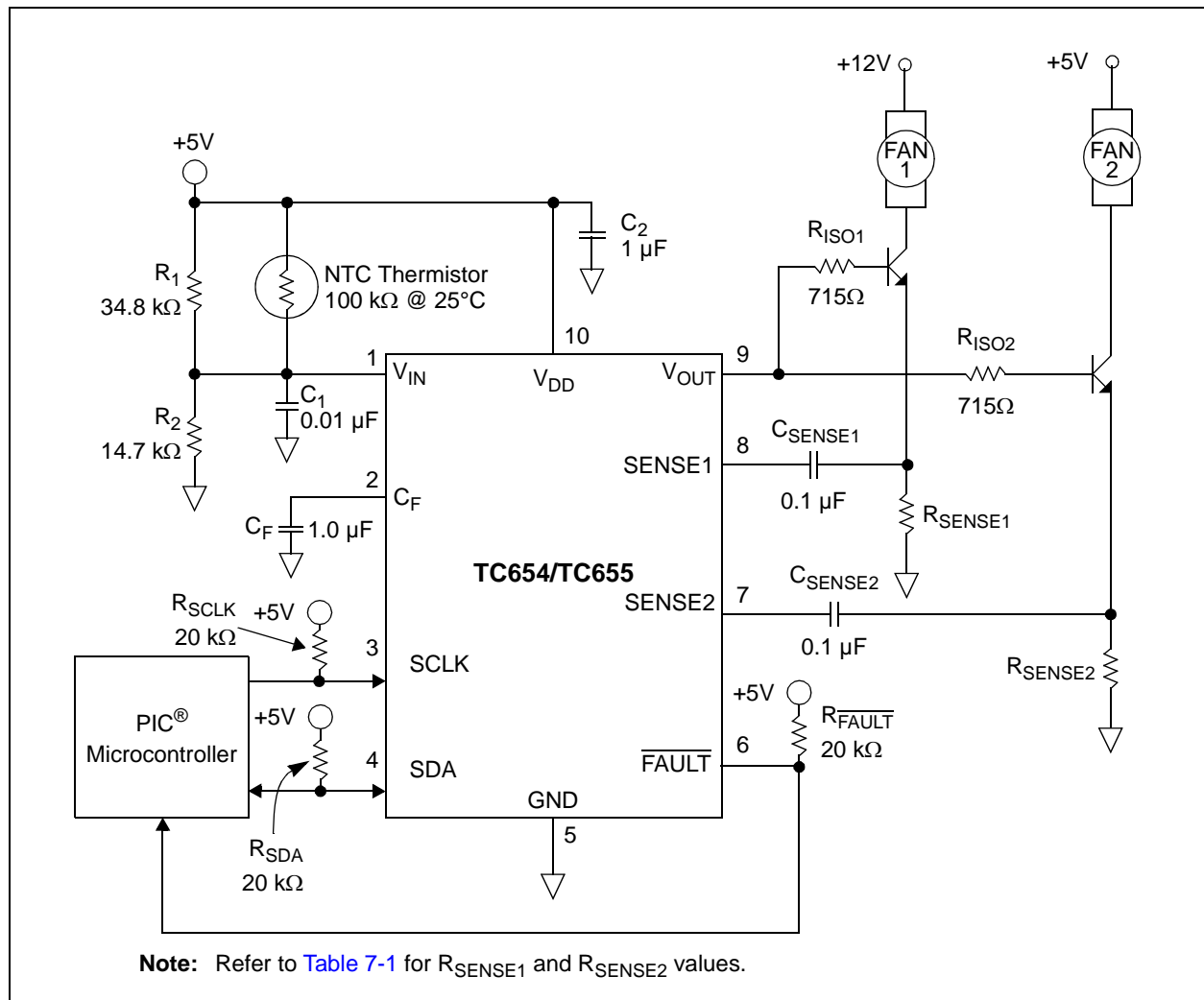
## 4.0 DEVICE OPERATION

The TC654 and TC655 devices allow you to control, monitor and communicate (via SMBus) fan speed for 2-wire and 3-wire DC brushless fans. By pulse-width modulating (PWM) the voltage across the fan, the TC654/TC655 controls fan speed according to the system temperature. The goal of temperature proportional fan speed control is to reduce fan power consumption, increase fan life and reduce system acoustic noise. With the TC654 and TC655 devices, fan speed can be controlled by the analog input  $V_{IN}$  or the SMBus interface, allowing for high system flexibility.

The TC654 and TC655 also measure and monitor fan revolutions per minute (RPM). A fan's speed (RPM) is a measure of its health. As a fan's bearings wear out, the fan slows down and eventually stops (locked rotor). By monitoring the fan's RPM level, the TC654/TC655 devices can detect open, shorted, unconnected and locked rotor fan conditions. The fan speed threshold

can be set to provide a predictive fan failure feature. This feature can be used to give a system warning and, in many cases, help to avoid a system thermal shut-down condition. The fan RPM data and threshold registers are available over the SMBus interface which allows for complete system control.

The TC654/TC655 devices are identical in every aspect except for how they indicate an over-temperature condition. When  $V_{IN}$  voltage exceeds 2.6V (typical), both devices will set OTF (bit 5<X>) in the Status Register to a '1'. The TC655 will additionally pull the  $\overline{\text{FAULT}}$  output low during an over-temperature condition.



**FIGURE 4-1:** Typical Application Circuit.

## 4.1 Fan Speed Control Methods

The speed of a DC brushless fan is proportional to the voltage across it. For example, if a fan's rating is 5000 RPM at 12V, its speed would be 2500 RPM at 6V. This, of course, will not be exact, but should be close.

There are two main methods for fan speed control. The first is pulse width modulation (PWM) and the second is linear. Using either method the total system power requirement to run the fan is equal. The difference between the two methods is where the power is consumed.

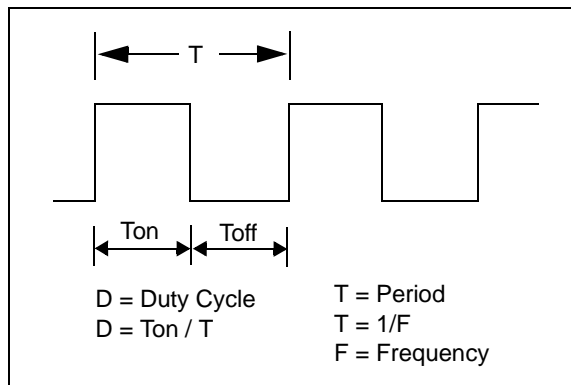
The following example compares the two methods for a 12V, 120 mA fan running at 50% speed. With 6V applied across the fan, the fan draws an average current of 68 mA. Using a linear control method, there are 6V across the fan and 6V across the drive element. With 6V and 68 mA, the drive element is dissipating 410 mW of power. Using the PWM approach, the fan is modulated at a 50% duty cycle, with most of the 12V being dropped across the fan. With 50% duty cycle, the fan draws an RMS current of 110 mA and an average current of 72 mA. Using a MOSFET with a  $1\ \Omega$   $R_{DS(on)}$  (a fairly typical value for this low current) the power dissipation in the drive element would be:  $12\text{ mW}$  ( $I_{rms}^2 * R_{DS(on)}$ ). Using a standard 2N2222A NPN transistor (assuming a  $V_{ce-sat}$  of 0.8V), the power dissipation would be 58 mW ( $I_{avg} * V_{ce-sat}$ ).

The PWM approach to fan speed control causes much less power dissipation in the drive element. This allows smaller devices to be used and will not require any special heatsinking to get rid of the power being dissipated in the package.

The other advantage to the PWM approach is that the voltage being applied to the fan is always near 12V. This eliminates any concern about not supplying a high enough voltage to run the internal fan components, which is very relevant in linear fan speed control.

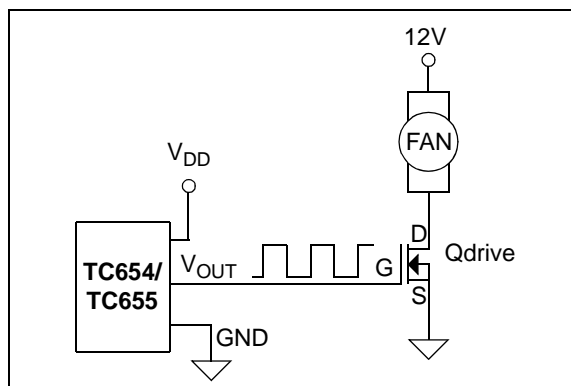
## 4.2 PWM Fan Speed Control

The TC654 and TC655 devices implement PWM fan speed control by varying the duty cycle of a fixed frequency pulse train. The duty cycle of a waveform is the on time divided by the total period of the pulse. For example, given a 100 Hz waveform (10 msec.) with an on time of 5.0 msec, the duty cycle of this waveform is 50% (5.0 msec/10.0 msec). An example of this is illustrated in Figure 4-2.



**FIGURE 4-2:** Duty Cycle Of A PWM Waveform.

The TC654 and TC655 generate a pulse train with a typical frequency of 30 Hz ( $C_F = 1\ \mu\text{F}$ ). The duty cycle can be varied from 30% to 100%. The pulse train generated by the TC654/TC655 devices drives the gate of an external N-channel MOSFET or the base of an NPN transistor (Figure 4-3). See Section 7.5 “Output Drive Device Selection” for more information on output drive device selection.



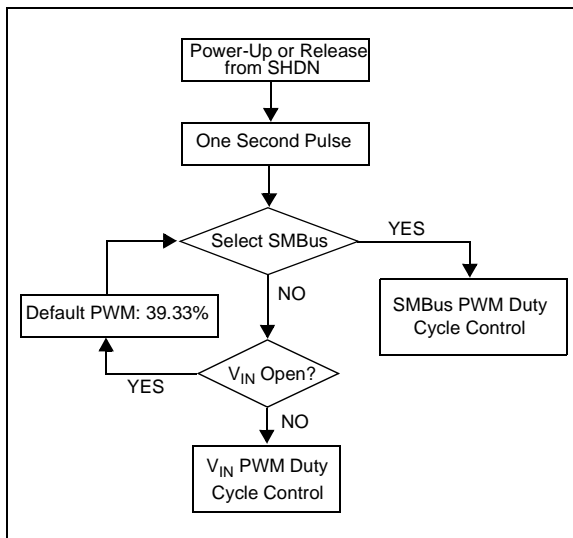
**FIGURE 4-3:** PWM Fan Drive.

By modulating the voltage applied to the gate of the MOSFET Qdrive, the voltage applied to the fan is also modulated. When the  $V_{OUT}$  pulse is high, the gate of the MOSFET is turned on, pulling the voltage at the drain of Qdrive to 0V. This places the full 12V across the fan for the  $T_{on}$  period of the pulse. When the duty cycle of the drive pulse is 100% (full on,  $T_{on} = T$ ), the fan will run at full speed. As the duty cycle is decreased (pulse on time “Ton” is lowered), the fan will slow down proportionally. With the TC654 and TC655 devices, the duty cycle can be controlled through the analog input pin ( $V_{IN}$ ) or through the SMBus interface by using the Duty-Cycle Register. See Section 4.5 “Duty Cycle Control ( $V_{IN}$  and Duty-Cycle Register)” for more details on duty cycle control.

## 4.3 Fan Start-up

Often overlooked in fan speed control is the actual start-up control period. When starting a fan from a non-operating condition (fan speed is zero RPM), the desired PWM duty cycle or average fan voltage can not be applied immediately. Since the fan is at a rest position, the fan's inertia must be overcome to get it started. The best way to accomplish this is to apply the full rated voltage to the fan for one second. This will ensure that in all operating environments, the fan will start and operate properly.

The TC654 and TC655 devices implement this fan control feature without any user programming. During a power-up or release from shutdown condition, the TC654 and TC655 devices force the  $V_{OUT}$  output to a 100% duty cycle, turning the fan full on for one second ( $C_F = 1 \mu F$ ). Once the one second period is over, the TC654/TC655 devices will look to see if SMBus or  $V_{IN}$  control has been selected in the Configuration Register (DUTYC bit 5<0>). Based on this register, the device will choose which input will control the  $V_{OUT}$  duty cycle. Duty cycle control based on  $V_{IN}$  is the default state. If  $V_{IN}$  control is selected and the  $V_{IN}$  pin is open (nothing is connected to the  $V_{IN}$  pin), then the TC654/TC655 will default to a duty cycle of 39.33%. This sequence is shown in Figure 4-4. This integrated one second start-up feature will ensure the fan starts-up every time.



**FIGURE 4-4:** Power-Up Flow Chart.

## 4.4 PWM Drive Frequency ( $C_F$ )

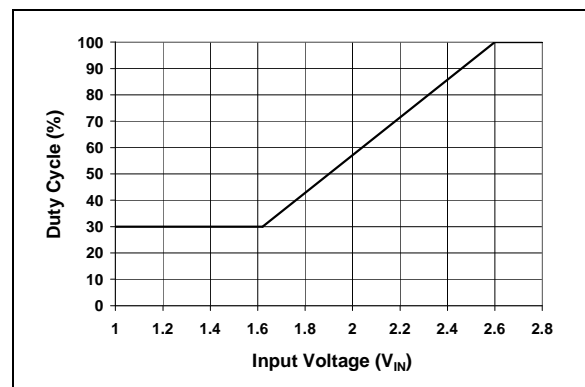
As previously discussed, the TC654 and TC655 devices operate with a fixed PWM frequency. The frequency of the PWM drive output ( $V_{OUT}$ ) is set by a capacitor at the  $C_F$  pin. With a  $1 \mu F$  capacitor at the  $C_F$  pin, the typical drive frequency is 30 Hz. This frequency can be raised, by decreasing the capacitor value, or lowered, by increasing the capacitor value. The relationship between the capacitor value and the PWM fre-

quency is linear. If a frequency of 15 Hz is desired, a capacitor value of  $2.0 \mu F$  should be used. The frequency should be kept in the range of 15 Hz to 35 Hz. See Section 7.2 "Setting the PWM Frequency" for more details.

## 4.5 Duty Cycle Control ( $V_{IN}$ and Duty-Cycle Register)

The duty cycle of the  $V_{OUT}$  PWM drive signal can be controlled by either the  $V_{IN}$  analog input pin or by the Duty-Cycle Register, which is accessible via the SMBus interface. The control method is selectable via DUTYC (bit 5<0>) of the Configuration Register. The default state is for  $V_{IN}$  control. If  $V_{IN}$  control is selected and the  $V_{IN}$  pin is open, the PWM duty cycle will default to 39.33%. The duty cycle control method can be changed at any time via the SMBus interface.

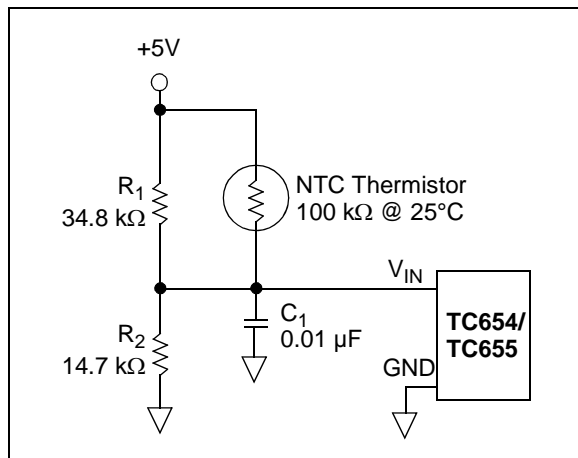
$V_{IN}$  is an analog input pin. A voltage in the range of 1.62V to 2.6V (typical) at this pin commands a 30% to 100% duty cycle on the  $V_{OUT}$  output, respectively. If the voltage at  $V_{IN}$  falls below the 1.62V level, the duty cycle will not go below 30%. The relationship between the voltage at  $V_{IN}$  and the PWM duty cycle is shown in Figure 4-5.



**FIGURE 4-5:** PWM Duty Cycle vs.  $V_{IN}$  Voltage (Typical).

For the TC655 device, if the voltage at  $V_{IN}$  exceeds the 2.6V (typical) level, an over-temperature fault indication will be given by asserting a low at the  $FAULT$  output and setting OTF (bit 5<X>) in the Status Register to a '1'.

A thermistor network or any other voltage output thermal sensor can be used to provide the voltage to the  $V_{IN}$  input. The voltage supplied to the  $V_{IN}$  pin can actually be thought of as a temperature. For example, the circuit shown in Figure 4-6 represents a typical solution for a thermistor based temperature sensing network. See Section 7.3 "Temperature Sensor Design" for more details.



**FIGURE 4-6:** NTC Thermistor Sensor Network.

The second method for controlling the duty cycle of the PWM output ( $V_{OUT}$ ) is via the SMBus interface. In order to control the PWM duty cycle via the SMBus, DUTYC (bit 5<0>) of the Configuration Register (Register 6.3) must be set to a '1'. This tells the TC654/TC655 device that the duty cycle should be controlled by the Duty Cycle Register. Next, the Duty Cycle Register must be programmed to the desired value. The Duty Cycle Register is a 4 Bit read/write register that allows duty cycles from 30% to 100% to be programmed. Table 4-1 shows the binary codes for each possible duty cycle.

**TABLE 4-1: DUTY-CYCLE REGISTER (DUTY-CYCLE) 4-BITS, READ/WRITE**

Duty-Cycle Register (Duty Cycle)				
D(3)	D(2)	D(1)	D(0)	Duty-Cycle
0	0	0	0	30%
0	0	0	1	34.67%
0	0	1	0	39.33% (default for $V_{IN}$ open and when SMBus is not selected)
0	0	1	1	44%
0	1	0	0	48.67%
0	1	0	1	53.33%
0	1	1	0	58%
0	1	1	1	62.67%
1	0	0	0	67.33%
1	0	0	1	72%
1	0	1	0	76.67%
1	0	1	1	81.33%
1	1	0	0	86%
1	1	0	1	90.67%
1	1	1	0	95.33%
1	1	1	1	100%

This method of control allows for more sophisticated algorithms to be implemented by utilizing microcontrollers or microprocessors in the system. In this way, multiple system temperatures can be taken into account for determining the necessary fan speed.

As shown in Table 4-1, the duty cycle has more of a step function look than did the  $V_{IN}$  control approach. Because the step changes in duty cycle are small, they are rarely audibly noticeable, especially when the fans are integrated into the system.

## 4.6 PWM Output ( $V_{OUT}$ )

The  $V_{OUT}$  pin is designed to drive two low-cost NPN transistors or N-channel MOSFETs as the low side power switching elements in the system as is shown in Figure 4-7. These switching elements are used to turn the fans on and off at the PWM duty cycle commanded by the  $V_{OUT}$  output.

This output has complementary drive (pull up and pull down) and is optimized for driving NPN transistors or N-channel MOSFETs (see Section 2.0 "Typical Performance CURVES" for sink and source current capability of the  $V_{OUT}$  drive stage).

The external device needs to be chosen to fit the voltage and current rating of the fan in a particular application (Refer to Section 7.5 "Output Drive Device Selection" Output Drive Device Selection). NPN transistors are often a good choice for low-current fans. If a NPN transistor is chosen, a base current-limiting resistor should be used. When using a MOSFET as the switching element, it is sometimes a good idea to have a gate resistor to help slow down the turn on and turn off of the MOSFET. As with any switching waveform, fast rising and falling edges can sometimes lead to noise problems.

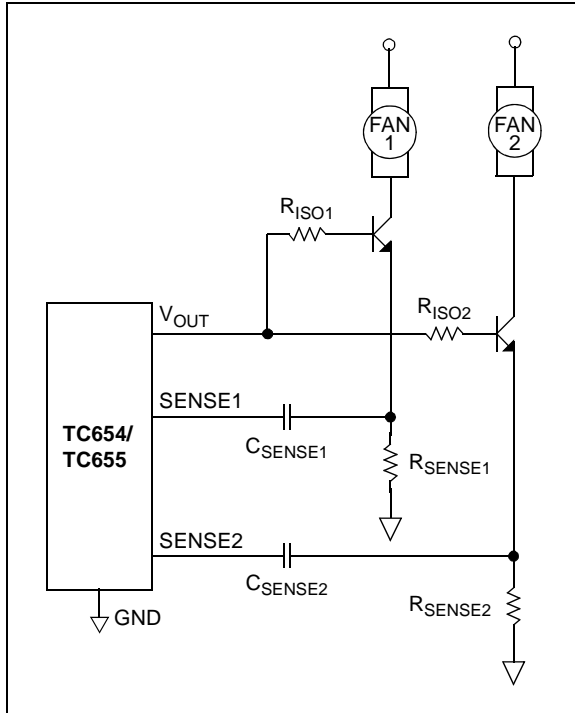
As previously stated, the  $V_{OUT}$  output will go to 100% duty cycle during power-up and release from shutdown conditions. The  $V_{OUT}$  output only shuts down when commanded to do so via the Configuration Register (SDM (bit 0<0>)). Even when a locked rotor condition is detected, the  $V_{OUT}$  output will continue to pulse at the programmed duty cycle.

## 4.7 Sensing Fan Operation (SENSE1 & SENSE2)

The TC654 and TC655 also feature Microchip's proprietary FanSense technology. During normal fan operation, commutation occurs as each pole of the fan is energized. The fan current pulses created by the fan commutation are sensed using low value current sense resistors in the ground return leg of the fan circuit. The voltage pulses across the sense resistor are then AC coupled through capacitors to the SENSE pins of the TC654/TC655 device. These pulses are utilized for calculating the RPM of the individual fans. The threshold voltage for the SENSE pins is 100 mV (typical). The

peak of the voltage pulse at the SENSE pins must exceed the 100 mV (typical) threshold in order for the pulse to be counted in the fan RPM measurement.

See [Section 7.4 “FanSense Network \( \$R\_{SENSE}\$  &  \$C\_{SENSE}\$ \)”](#) for more details on selecting the appropriate current sense resistor and coupling capacitor values.



**FIGURE 4-7:** Fan Current Sensing.

By selecting F1PPR (bits 2-1<01>) and F2PPR (bits 4-3<01>) in the Configuration Register, the TC654 and TC655 can be programmed to calculate RPM data for fans with 1, 2, 4 or 8 current pulses per rotation. The default state assumes a fan with 2 pulses per rotation.

The measured RPM data is then stored in the RPM-OUTPUT1 (RPM1, for SENSE1 input) and RPM-OUTPUT2 (RPM2, for SENSE2 input) Registers. These registers are 9-Bit Read-Only registers which store RPM data with 25 RPM resolution. By setting RES (bit 6<0>) of the Configuration Register to a '1', the RPM data can be read with 25 RPM resolution. If this Bit is left in the default state of '0', the RPM data will only be readable with resolution of 50 RPMs, which represents 8-Bit data.

The maximum fan RPM reading is 12775 RPM. If this value is exceeded, counter overflow bits in the Status Register are set. R1CO (bit 3<0>) and R2CO (bit 4<0>) in the Status Register represent the RPM1 and RPM2 counter overflow bits for the RPM1 and RPM2 registers, respectively. These bits will automatically be reset to zero if the fan RPM reading has been below the maximum value of 12775 RPM for 2.4 seconds.

See [Table 6-1](#) for RPM1, RPM2 and Status Register command byte assignments.

## 4.8 Fan Fault Threshold and Indication (FAULT)

For the TC654 and TC655 devices, a fault condition exists whenever a fan's sensed RPM level falls below the user programmable threshold. The RPM threshold values for fan fault detection are set in the FAN\_FAULT1 and FAN\_FAULT2 Registers (8-bit, read/write).

The RPM threshold represents the fan speed at which the TC654/TC655 devices will indicate a fan fault. This threshold can be set at lower levels to indicate fan locked rotor conditions or set to higher levels to give indications for predictive fan failure. It is recommended that the RPM threshold be at least 10% lower than the minimum fan speed which occurs at the lowest duty cycle set point. The default value for the fan RPM thresholds is 500 RPM. If the fan's sensed RPM is less than the fan fault threshold for 2.4 seconds (typical), a fan fault condition is indicated.

When a fault condition due to low fan RPM occurs, a logic low is asserted at the  $\overline{\text{FAULT}}$  output. F1F (bit 0<0>) and F2F (bit 1<0>) in the Status Register are set to '1' for respective low RPM levels on the SENSE1 and SENSE2 inputs. The  $\overline{\text{FAULT}}$  output and the fault bits in the Status Register can be reset by setting FFCLR (bit 7<0>) in the Configuration Register to a '1'.

For the TC655 device, a fault condition is also indicated when an Over-Temperature Fault condition occurs. This condition occurs when the  $V_{\text{OUT}}$  duty cycle exceeds the 100% value indicating that no additional cooling capability is available. For this condition, a logic low is asserted at the  $\overline{\text{FAULT}}$  output and OTF (bit 5<X>) of the Status Register, the over-temperature fault indicator, is set to a '1' (The TC654 also indicates an over-temperature condition via the OTF bit in the status register). If the duty cycle then decreases below 100%, the  $\overline{\text{FAULT}}$  output will be released and OTF (bit 5<X>) of the Status Register will be reset to '0'.

## 4.9 Low-Power Shutdown Mode

Some applications may have operating conditions where fan cooling is not required as a result of low ambient temperature or light system load. During these times it may be desirable to shut the fans down to save power and reduce system noise.

The TC654/TC655 devices can be put into a low-power Shutdown mode by setting SDM (bit 0<0>) in the Configuration register to a '1' (this bit is the shutdown bit). When the TC654/TC655 devices are in Shutdown mode, all functions except for the SMBus interface are suspended. During this mode of operation, the TC654 and TC655 devices will draw a typical supply current of only 5  $\mu\text{A}$ . Normal operation will resume as soon as Bit 0 in the Configuration Register is reset to '0'.

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When the TC654/TC655 devices are brought out of a Shutdown mode by resetting SDM (bit 0<0>) in the Configuration Register, all of the registers (except for the Configuration and FAN\_FAULT1 and 2 registers) assume their default power-up states. The Configuration Register and the FAN\_FAULT1 and 2 Registers maintain the states they were in prior to the device being put into the Shutdown mode. Since these are the registers which control the parts operation, the part does not have to be reprogrammed for operation when it comes out of Shutdown mode.

## 4.10 SMBus Interface (SCLK & SDA)

The TC654/TC655 feature an industry-standard, 2-wire serial interface with factory-set addresses. By communicating with the TC654/TC655 device registers, functions like PWM duty cycle, low-power Shutdown mode and fan RPM threshold can be controlled. Critical information, such as fan fault, over-temperature and fan RPM, can also be obtained via the device data registers. The available data and control registers make the TC654/TC655 devices very flexible and easy to use. All of the available registers are detailed in [Section 6.0 "Register Set"](#).

## 4.11 SMBus Slave Address

The slave address of the TC654/TC655 is 0011 011 and is fixed. This address is different from industry-standard digital temperature sensors (like TCN75) and, therefore, allows the TC654/TC655 to be utilized in systems in conjunction with these components. Please contact Microchip Technology Inc. if alternate addresses are required.

## 5.0 SERIAL COMMUNICATION

### 5.1 SMBus 2-Wire Interface

The Serial Clock Input (SCLK) and the bi-directional data port (SDA) form a 2-wire bi-directional serial port for communicating with the TC654/TC655. The following bus protocols have been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following Serial Bus conventions have been defined.

**TABLE 5-1: TC654/TC655 SERIAL BUS CONVENTIONS**

Term	Description
Transmitter	The device sending data to the bus.
Receiver	The device receiving data from the bus.
Master	The device which controls the bus: initiating transfers (Start), generating the clock and terminating transfers (Stop).
Slave	The device addressed by the master.
Start	A unique condition signaling the beginning of a transfer indicated by SDA falling (High to Low) while SCLK is high.
Stop	A unique condition signaling the end of a transfer indicated by SDA rising (Low to High) while SCLK is high.
ACK	A Receiver acknowledges the receipt of each byte with this unique condition. The Receiver pulls SDA low during SCLK high of the ACK clock-pulse. The Master provides the clock pulse for the ACK cycle.
Busy	Communication is not possible because the bus is in use.
NOT Busy	When the bus is idle, both SDA and SCLK will remain high.
Data Valid	The state of SDA must remain stable during the high period of SCLK in order for a data bit to be considered valid. SDA only changes state while SCLK is low during normal data transfers. (See Start and Stop conditions)

#### 5.1.1 DATA TRANSFER

The TC654/TC655 support a bi-directional 2-Wire bus and data transmission protocol. The serial protocol sequencing is illustrated in [Figure 1-1](#). Data transfers

are initiated by a Start condition (Start), followed by a device address byte and one or more data bytes. The device address byte includes a Read/Write selection bit. Each access must be terminated by a Stop Condition (Stop). A convention call Acknowledge (ACK) confirms the receipt of each byte. Note that SDA can only change during periods when SCLK is low (SDA changes while SCLK is high are reserved for Start and Stop conditions). All bytes are transferred MSB (most significant bit) first.

#### 5.1.2 MASTER/SLAVE

The device that sends data onto the bus is the transmitter and the device receiving data is the receiver. The bus is controlled by a master device which generates the serial clock (SCLK), controls the bus access and generates the Start and Stop conditions. The TC654/TC655 always work as a slave device. Both master and slave devices can operate as either transmitter or receiver, but the master device determines which mode is activated.

#### 5.1.3 START CONDITION (START)

A high-to-low transition of the SDA line while the clock (SCLK) is high determines a Start condition. All commands must be preceded by a Start condition.

#### 5.1.4 ADDRESS BYTE

Immediately following the Start Condition, the host must transmit the address byte to the TC654/TC655. The 7-bit SMBus address for the TC654/TC655 is 0011 011. The 7-bit address transmitted in the serial bit stream must match for the TC654/TC655 to respond with an Acknowledge (indicating the TC654/TC655 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read-Write Bit. This bit is a '1' for a read operation or '0' for a write operation. During the first phase of any transfer, this bit will be set = 0 to indicate that the command byte is being written.

#### 5.1.5 STOP CONDITION (STOP)

A low-to-high transition of the SDA line while the clock (SCLK) is high determines a Stop condition. All operations must be ended with a Stop condition.

#### 5.1.6 DATA VALID

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is unlimited.

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## 5.1.7 ACKNOWLEDGE (ACK)

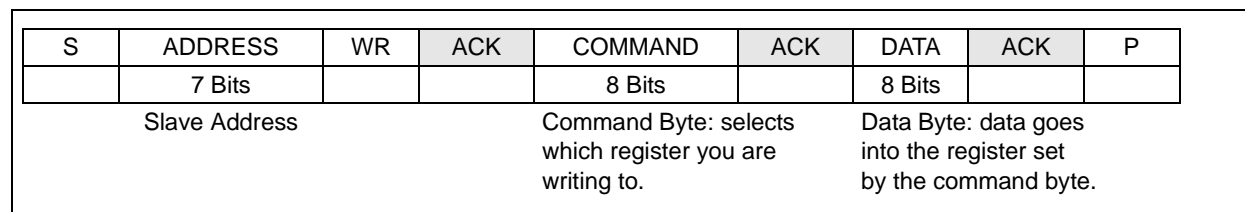
Each receiving device, when addressed, is obliged to generate an acknowledge bit after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Setup and hold times must be taken into account. During reads, a master device must signal an end of data to the slave by not generating an acknowledge bit on the

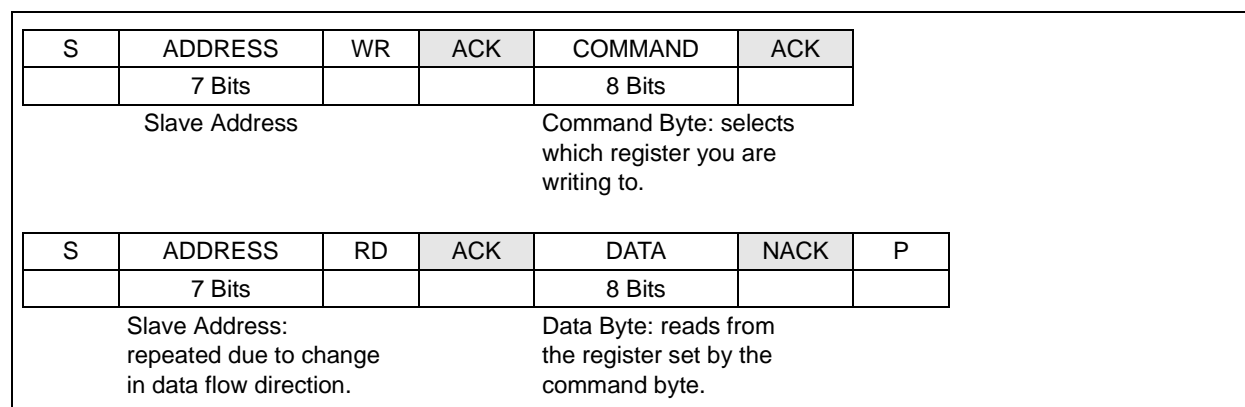
last byte that has been clocked out of the slave. In this case, the slave (TC654/TC655) will leave the data line high to enable the master device to generate the Stop condition.

## 5.2 SMBus Protocols

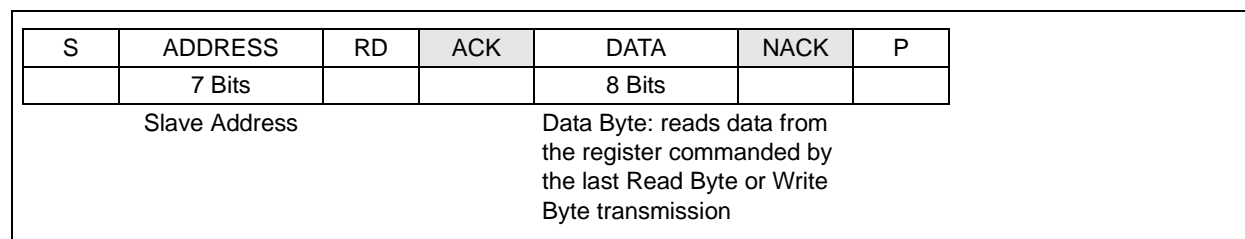
The TC654/TC655 devices communicate with three standard SMBus protocols. These are the write byte, read byte and receive byte. The receive byte is a shortened method for reading from, or writing to, a register which had been selected by the previous read or write command. These transmission protocols are shown in Figures 5-1, 5-2 and 5-3.



**FIGURE 5-1:** SMBus Protocol: Write Byte Format.



**FIGURE 5-2:** SMBus Protocol: Read Byte Format.



**FIGURE 5-3:** SMBus Protocol: Receive Byte Format.

S = Start Condition

P = Stop Condition

Shaded = Slave Transmission

ACK = Acknowledge = 0

NACK = Not Acknowledged = 1

WR = Write = 0

RD = Read = 1

## 6.0 REGISTER SET

The TC654/TC655 devices contain 9 registers that provide a variety of data and functionality control to the outside system. These registers are listed below in [Table 6-1](#). Of key importance is the command byte information, which is needed in the read and write protocols in order to select the individual registers.

**TABLE 6-1: COMMAND BYTE ASSIGNMENTS**

Register	Command	Read	Write	POR Default State	Function
RPM1	0000 0000	X	—	0 0000 0000	RPM Output 1
RPM2	0000 0001	X	—	0 0000 0000	RPM Output 2
FAN_FAULT1	0000 0010	X	X	0000 1010	Fan Fault 1 Threshold
FAN_FAULT2	0000 0011	X	X	0000 1010	Fan Fault 2 Threshold
CONFIG	0000 0100	X	X	0000 1010	Configuration
STATUS	0000 0101	X	—	00X0 0X00	Status. See <a href="#">Section 6.4 “Status Register (Status)”</a> , Status Register explanation of X
DUTY_CYCLE	0000 0110	X	X	0000 0010	Fan Speed Duty Cycle
MFR_ID	0000 0111	X	—	0101 0100	Manufacturer Identification
VER_ID	0000 1000	X	—	0000 000X	Version Identification: (X = ‘0’ TC654, X = ‘1’ TC655)

### 6.1 RPM-OUTPUT1 & RPM-OUTPUT2 Registers (RPM1 & RPM2)

As discussed in [Section 4.7 “Sensing Fan Operation \(SENSE1 & SENSE2\)”](#), fan current pulses are detected at the SENSE1 and SENSE2 inputs of the TC654/TC655 device. The current pulse information is used to calculate the fan RPM. The fan RPM data for fans 1 and 2 is then written to registers RPM1 and RPM2, respectively. RPM1 and RPM2 are 9-bit registers that provide

the RPM information in 50 RPM (8-bit) or 25 RPM (9-bit) increments. This is selected via RES (bit 6<0>) in the Configuration Register, with ‘0’ = 50 RPM and ‘1’ = 25 RPM. The default state is zero (50 RPM). The maximum fan RPM value that can be read is 12775 RPM. If this value is exceeded, R2CO (bit 4<0>) and R1CO (bit 3<0>) in the Status Register will be set to a ‘1’ to indicate that a counter overflow of the respective RPM register has occurred. [Register 6-1](#) shows the RPM output register 9-bit format.

**REGISTER 6-1: RPM OUTPUT REGISTERS (RPM1 & RPM2)**

D(8)	D(7)	D(6)	D(5)	D(4)	D(3)	D(2)	D(1)	D(0)	RPM
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	25
0	0	0	0	0	0	0	1	0	50
.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	
1	1	1	1	1	1	1	1	0	12750
1	1	1	1	1	1	1	1	1	12775

## 6.2 FAN\_FAULT1 & FAN\_FAULT2 Threshold Registers (FAN\_FAULT1 & FAN\_FAULT2)

The Fan Fault Threshold Registers (FAN\_FAULT1 and FAN\_FAULT2) are used to set the fan fault threshold levels for fan 1 and fan 2, respectively. The Fan Fault Registers are 8-bit, read/writable registers that allow the fan fault RPM threshold to be set in 50 RPM increments. The default setting for both Fan Fault registers is 500 RPM (0000 1010). The maximum set point value is 12750 RPM. If the measured fan RPM (stored

in RPM1 and RPM2 Registers) drops below the value that is set in the Fan Fault Registers for more than 2.4sec, a fan fault indication will be given. F1F (bit 0<0>) and F2F (bit 1<0>) in the Status Register indicate fan fault conditions for fan 1 and fan 2, respectively. The FAULT output will also be pulled low in a fan fault condition. Changing FFCLR (bit 7<0>) in the Configuration Register will reset the fan fault bits in the Status Register as well as the FAULT output. See [Register 6-2](#) for the Fan Fault Threshold Register 8-bit format.

**REGISTER 6-2: FAN FAULT THRESHOLD REGISTERS (FAN\_FAULT1 & FAN\_FAULT2)**

D(7)	D(6)	D(5)	D(4)	D(3)	D(2)	D(1)	D(0)	RPM
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	50
0	0	0	0	0	0	1	0	100
.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	
1	1	1	1	1	1	1	0	12700
1	1	1	1	1	1	1	1	12750

## 6.3 CONFIGURATION REGISTER (CONFIG)

The Configuration Register is an 8-bit read/writable multi-function control register. This register allows the user to clear fan faults, select RPM resolution, select

$V_{OUT}$  duty cycle (fan speed) control method, select the fan current pulses per rotation for fans 1 and 2 (for fan RPM calculation) and put the TC654/TC655 device into a Shutdown mode to save power consumption. See [Register 6-3](#) below for the Configuration Register bit descriptions.

### REGISTER 6-3: CONFIGURATION REGISTER (CONFIG)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
FFCLR	RES	DUTYC	F2PPR	F2PPR	F1PPR	F1PPR	SDM
bit 7							bit 0

bit 7 **FFCLR:** Fan Fault Clear

- 1 = Clear Fan Fault. This will reset the Fan Fault bits in the Status Register and the  $\overline{\text{FAULT}}$  output.
- 0 = Normal Operation (default)

bit 6 **RES:** Resolution Selection for RPM Output Registers

- 1 = RPM Output Registers (RPM1 and RPM2) will be set for 25 RPM (9-bit) resolution.
- 0 = RPM Output Registers (RPM1 and RPM2) will be set for 50 RPM (8-bit) resolution. (default)

bit 5 **DUTYC:** Duty Cycle Control Method

- 1 = The  $V_{OUT}$  duty cycle will be controlled via the SMBus interface. The value for the  $V_{OUT}$  duty cycle will be taken from the duty cycle register (DUTY\_CYCLE).
- 0 = The  $V_{OUT}$  duty cycle will be controlled via the  $V_{IN}$  analog input pin. The  $V_{OUT}$  duty cycle value will be between 30% and 100% for  $V_{IN}$  values between 1.62V and 2.6V typical. If the  $V_{IN}$  pin is open when this mode is selected, the  $V_{OUT}$  duty cycle will default to 39.33%. (default)

bit 4-3 **F2PPR:** Fan 2 Pulses Per Rotation

The TC654/TC655 device uses this setting to understand how many current pulses per revolution Fan 2 should have. It then uses this as part of the calculation for the fan 2 RPM value in the RPM2 Register. See [Section 7.7 "Determining Current Pulses Per Revolution of Fans"](#) for application information on determining your fan's number of current pulses per revolution.

- 00 = 1
- 01 = 2 (default)
- 10 = 4
- 11 = 8

bit 2-1 **F1PPR:** Fan 1 Pulses Per Rotation

The TC654/TC655 device uses this setting to understand how many current pulses per revolution Fan 1 should have. It then uses this as part of the calculation for the fan 1 RPM value for the RPM1 Register. See [Section 7.7 "Determining Current Pulses Per Revolution of Fans"](#) for application information on determining your fan's number of current pulses per revolution.

- 00 = 1
- 01 = 2 (default)
- 10 = 4
- 11 = 8

bit 0 **SDM:** Shutdown Mode

- 1 = Shutdown mode. See [Section 4.9 "Low-Power Shutdown Mode"](#) for more information on low-power Shutdown mode.
- 0 = Normal operation. (default)

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

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## 6.4 STATUS REGISTER (STATUS)

The Status register provides all the information about what is going on within the TC654/TC655 devices. Fan fault information,  $V_{IN}$  status, RPM counter overflow,

and over-temperature indication are all available in the Status register. The Status register is an 8-bit Read-Only register with bits 6 and 7 unused. See [Register 6-4](#) below for the bit descriptions.

**REGISTER 6-4: STATUS REGISTER (STATUS)**

U-0	U-0	R-X	R-0	R-0	R-X	R-0	R-0
—	—	OTF	R2CO	R1CO	VSTAT	F2F	F1F
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **OTF:** Over-Temperature Fault Condition

For the TC654/TC655 device, this bit is set to the proper state immediately at start-up and is therefore treated as an unknown (X). If  $V_{IN}$  is greater than the threshold required for 100% duty cycle on  $V_{OUT}$  (2.6V typical), then the bit will be set to a '1'. If it is less than the threshold, the bit will be set to '0'. This is determined at power-up.

1 = Over-Temperature condition has occurred.

0 = Normal operation.  $V_{IN}$  is less than 2.6V.

bit 4 **R2CO:** RPM2 Counter Overflow

1 = Fault condition. The maximum RPM reading of 12775 RPM in register RPM2 has been exceeded. This bit will automatically reset to zero when the RPM reading comes back into range.

0 = Normal operation. RPM reading is within limits (default).

bit 3 **R1CO:** RPM1 Counter Overflow

1 = Fault condition. The maximum RPM reading of 12775 RPM in register RPM1 has been exceeded. This bit will automatically reset to zero when the RPM reading comes back into range.

0 = Normal operation. RPM reading is within limits (default).

bit 2 **VSTAT:**  $V_{IN}$  Input Status

For the TC654/TC655 devices, the  $V_{IN}$  pin status is checked immediately at power-up. If no external thermistor or voltage output network is connected ( $V_{IN}$  is open), this bit is set to a '1'. If an external network is detected, this bit is set to '0'. If the  $V_{IN}$  pin is open and SMBus operation has not been selected in the Configuration Register, the  $V_{OUT}$  duty cycle will default to 39.33%.

1 =  $V_{IN}$  is open.

0 = Normal operation. voltage present at  $V_{IN}$ .

bit 1 **F2F:** Fan 2 Fault

1 = Fault Condition. The value for fan RPM in the RPM2 Register has fallen below the value set in the FAN\_FAULT2 Threshold Register. The speed of Fan 2 is too low and a fault condition is being indicated. The  $\overline{\text{FAULT}}$  output will be pulled low at the same time. This fault bit can be cleared using the Fan Fault Clear bit (FFCLR (bit 7<0>)) in the Configuration Register.

0 = Normal Operation (default).

bit 0 **F1F:** Fan 1 Fault

1 = Fault Condition. The value for fan RPM in the RPM1 Register has fallen below the value set in the FAN\_FAULT1 Threshold Register. The speed of Fan 1 is too low and a fault condition is being indicated. The  $\overline{\text{FAULT}}$  output will be pulled low at the same time. This fault bit can be cleared using the Fan Fault Clear bit (FFCLR (bit 7<0>)) in the Configuration Register.

0 = Normal Operation (default).

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

## 6.5 DUTY-CYCLE Register (DUTY\_CYCLE)

The DUTY\_CYCLE register is a 4-bit read/writable register used to control the duty cycle of the  $V_{OUT}$  output. The controllable duty cycle range via this register is 30% to 100%, with programming steps of 4.67%. This method of duty cycle control is mainly used with the SMBus interface. However, if the  $V_{IN}$  method of duty cycle control has been selected (or defaulted to), and the  $V_{IN}$  pin is open, the duty cycle will go to the default setting of this register, which is 0010 (39.33%). The duty cycle settings are shown in [Register 6-5](#).

**REGISTER 6-5: DUTY-CYCLE REGISTER (DUTY\_CYCLE)**

D(3)	D(2)	D(1)	D(0)	Duty-Cycle
0	0	0	0	30%
0	0	0	1	34.67%
0	0	1	0	39.33% (default for $V_{IN}$ open and when SMBus is not selected)
0	0	1	1	44%
0	1	0	0	48.67%
0	1	0	1	53.33%
0	1	1	0	58%
0	1	1	1	62.67%
1	0	0	0	67.33%
1	0	0	1	72%
1	0	1	0	76.67%
1	0	1	1	81.33%
1	1	0	0	86%
1	1	0	1	90.67%
1	1	1	0	95.33%
1	1	1	1	100%

## 6.6 Manufacturer's Identification Register (MFR\_ID)

This register allows the user to identify the manufacturer of the part. The MFR\_ID register is an 8-bit Read-Only register. See [Register 6-6](#) for the Microchip manufacturer ID.

**REGISTER 6-6: MANUFACTURER'S IDENTIFICATION REGISTER (MFR\_ID)**

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0	1	0	1	0	1	0	0

## 6.7 Version ID Register (VER\_ID)

This register is used to indicate which version of the device is being used, either the TC654 or the TC655. This register is a simple 2-bit Read-Only register.

**REGISTER 6-7: VERSION ID REGISTER (VER\_ID)**

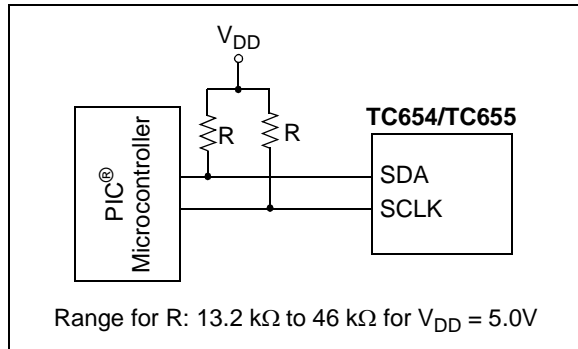
D[1]	D[0]	Version
0	0	TC654
0	1	TC655

# TC654/TC655

## 7.0 APPLICATIONS INFORMATION

### 7.1 Connecting to the SMBus

The SMBus is an open-collector bus, requiring pull-up resistors connected to the SDA and SCLK lines. This configuration is shown in Figure 7-1.

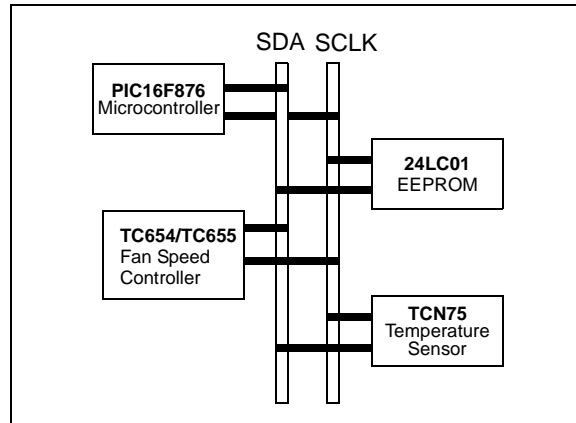


**FIGURE 7-1:** Pull-up Resistors On SMBus.

The number of devices connected to the bus is limited only by the maximum rise and fall times of the SDA and SCLK lines. Unlike I<sup>2</sup>C specifications, SMBus does not specify a maximum bus capacitance value. Rather, the SMBus specification calls out that the maximum current through the pull-up resistor be 350  $\mu A$  (minimum, 100  $\mu A$ , is also specified). Therefore, the value of the pull-up resistors will vary depending on the system's bias voltage,  $V_{DD}$ . Minimizing bus capacitance is still very important as it directly affects the rise and fall times of the SDA and SCLK lines. The range for pull-up resistor values for a 5V system are shown in Figure 7-1.

Although SMBus specifications only require the SDA and SCLK lines to pull down 350  $\mu A$ , with a maximum voltage drop of 0.4V, the TC654/TC655 has been designed to meet a maximum voltage drop of 0.4V, with 3 mA of current. This allows lower values of pull-up resistors to be used, which will allow higher bus capacitance. If this is to be done, though, all devices on the bus must be able to meet the same pull-down current requirements as well.

A possible configuration using multiple devices on the SMBus is shown in Figure 7-2.



**FIGURE 7-2:** Multiple Devices on SMBus.

### 7.2 Setting the PWM Frequency

The PWM frequency of the  $V_{OUT}$  output is set by the capacitor value attached to the  $C_F$  pin. The PWM frequency will be 30 Hz (typical) for a 1  $\mu F$  capacitor. The relationship between frequency and capacitor value is linear, making alternate frequency selections easy.

As stated in previous sections, the PWM frequency should be kept in the range of 15 Hz to 35 Hz. This will eliminate the possibility of having audible frequencies when varying the duty cycle of the fan drive.

A very important factor to consider when selecting the PWM frequency for the TC654/TC655 devices is the RPM rating of the selected fan and the minimum duty cycle for operation. For fans that have a full-speed rating of 3000 RPM or less, it is desirable to use a lower PWM frequency. A lower PWM frequency allows for a longer time period to monitor the fan current pulses. The goal is to be able to monitor at least two fan current pulses during the on time of the  $V_{OUT}$  output.

**Example:** Your system design requirement is to operate the fan at 50% duty cycle when ambient temperatures are below 20°C. The fan full-speed RPM rating is 3000 RPM and has four current pulses per rotation. At 50% duty cycle, the fan will be operating at approximately 1500 RPM.

#### EQUATION

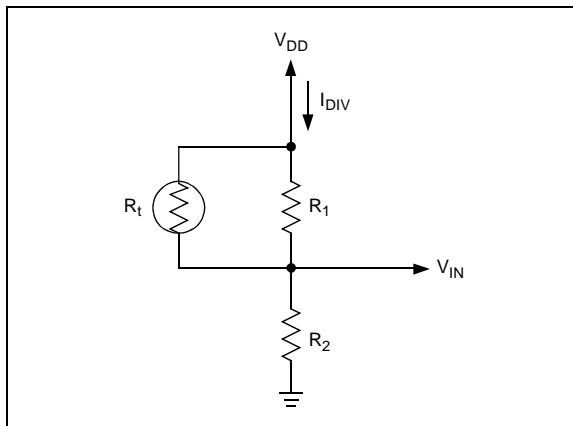
$$\text{Time for one revolution (msec.)} = \frac{60 \times 1000}{1500} = 40$$

If one fan revolution occurs in 40 msec, then each fan pulse occurs 10 msec apart. In order to detect two fan current pulses, the on time of the  $V_{OUT}$  pulse must be at least 20 msec. With the duty cycle at 50%, the total period of one cycle must be at least 40 msec, which makes the PWM frequency 25 Hz. For this example, a PWM frequency of 20 Hz is recommended. This would define a  $C_F$  capacitor value of 1.5  $\mu F$ .

## 7.3 Temperature Sensor Design

As discussed in previous sections, the  $V_{IN}$  analog input has a range of 1.62V to 2.6V (typical), which represents a duty cycle range on the  $V_{OUT}$  output of 30% to 100%, respectively. The  $V_{IN}$  voltages can be thought of as representing temperatures. The 1.62V level is the low temperature at which the system only requires 30% fan speed for proper cooling. The 2.6V level is the high temperature, for which the system needs maximum cooling capability. Therefore, the fan needs to be at 100% speed.

One of the simplest ways of sensing temperature over a given range is to use a thermistor. By using an NTC thermistor as shown in Figure 7-3, a temperature variant voltage can be created.



**FIGURE 7-3:** Temperature Sensing Circuit.

Figure 7-3 represents a temperature dependent voltage divider circuit.  $R_t$  is a conventional NTC thermistor,  $R_1$  and  $R_2$  are standard resistors.  $R_1$  and  $R_t$  form a parallel resistor combination that will be referred to as  $R_{TEMP}$  ( $R_{TEMP} = R_1 * R_t / (R_1 + R_t)$ ). As the temperature increases, the value of  $R_t$  decreases and the value of  $R_{TEMP}$  will decrease with it. Accordingly, the voltage at  $V_{IN}$  increases as temperature increases, giving the desired relationship for the  $V_{IN}$  input. The purpose of  $R_1$  is to help linearize the response of the sensing network. Figure 7-4 shows an example of this.

There are many values that can be chosen for the NTC thermistor. There are also thermistors which have a linear resistance instead of logarithmic, which can help to eliminate  $R_1$ . If less current draw from  $V_{DD}$  is desired, then a larger value thermistor should be chosen. The voltage at the  $V_{IN}$  pin can also be generated by a voltage output temperature sensor device. The key is to get the desired  $V_{IN}$  voltage to system (or component) temperature relationship.

The following equations apply to the circuit in Figure 7-3.

### EQUATION

$$V(t1) = \frac{V_{DD} \times R_2}{R_{TEMP}(t1) + R_2}$$

$$V(t2) = \frac{V_{DD} \times R_2}{R_{TEMP}(t2) + R_2}$$

In order to solve for the values of  $R_1$  and  $R_2$ , the values for  $V_{IN}$  and the temperatures at which they are to occur need to be selected. The variables,  $t1$  and  $t2$ , represent the selected temperatures. The value of the thermistor at these two temperatures can be found in the thermistor data sheet. With the values for the thermistor and the values for  $V_{IN}$ , you now have two equations from which the values for  $R_1$  and  $R_2$  can be found.

**Example:** The following design goals are desired:

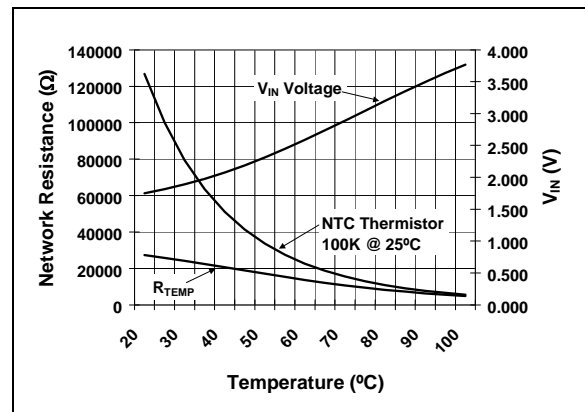
- Duty Cycle = 50% ( $V_{IN} = 1.9V$ ) with Temperature ( $t1$ ) = 30°C
- Duty Cycle = 100% ( $V_{IN} = 2.6V$ ) with Temperature ( $t2$ ) = 60°C

Using a 100 kΩ thermistor (25°C value), we look up the thermistor values at the desired temperatures:

- $R_t = 79428 \Omega$  @ 30°C
- $R_t = 22593 \Omega$  @ 60°C

Substituting these numbers into the given equations, we come up with the following numbers for  $R_1$  and  $R_2$ .

- $R_1 = 34.8 k\Omega$
- $R_2 = 14.7 k\Omega$



**FIGURE 7-4:** How Thermistor Resistance,  $V_{IN}$ , And  $R_{TEMP}$  Vary With Temperature.

Figure 7-4 graphs three parameters versus temperature. They are  $R_t$ ,  $R_1$  in parallel with  $R_t$ , and  $V_{IN}$ . As described earlier, you can see that the thermistor has a logarithmic resistance variation. When put in parallel with  $R_1$ , though, the combined resistance becomes more linear, which is the desired effect. This gives us the linear looking curve for  $V_{IN}$ .

7.4 FanSense Network (R<sub>SENSE</sub> & C<sub>SENSE</sub>)

The network comprised of R<sub>SENSE</sub> and C<sub>SENSE</sub> allows the TC654/TC655 devices to detect commutation of the fan motor. R<sub>SENSE</sub> converts the fan current into a voltage. C<sub>SENSE</sub> AC couples this voltage signal to the SENSE pins (SENSE1 and SENSE2). The goal of the SENSE network is to provide a voltage pulse to the SENSE pin that has a minimum amplitude of 120 mV. This will ensure that the current pulse caused by the fan commutation is recognized by the TC654/TC655 device.

A 0.1 µF ceramic capacitor is recommended for C<sub>SENSE</sub>. Smaller values will require larger sense resistors be used. Using a 0.1 µF capacitor results in reasonable values for R<sub>SENSE</sub>. Figure 7-5 illustrates a typical SENSE network.

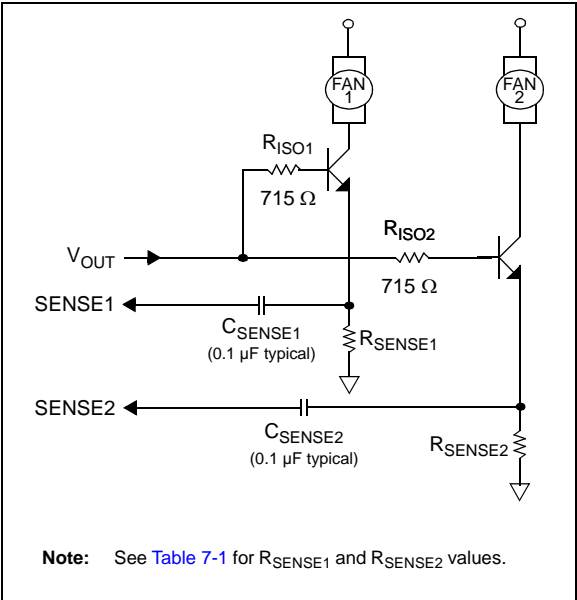


FIGURE 7-5: Typical Sense Network.

The value of R<sub>SENSE</sub> will change with the current rating of the fan. A key point is that the current rating of the fan specified by the manufacturer may be a worst case rating. The actual current drawn by the fan may be lower than this rating. For the purposes of setting the value for R<sub>SENSE</sub>, the operating fan current should be measured.

Table 7-1 shows values of R<sub>SENSE</sub> according to the nominal operating current of the fan. The fan currents are average values. If the fan current falls between two of the values listed, use the higher resistor value.

TABLE 7-1: R<sub>SENSE</sub> VS. FAN CURRENT

Nominal Fan Current (mA)	R <sub>SENSE</sub> (ohm)
50	9.1
100	4.7
150	3.0
200	2.4
250	2.0
300	1.8
350	1.5
400	1.3
450	1.2
500	1.0

Figure 7-6 shows some typical waveforms for the fan current and the voltage at the Sense pins.

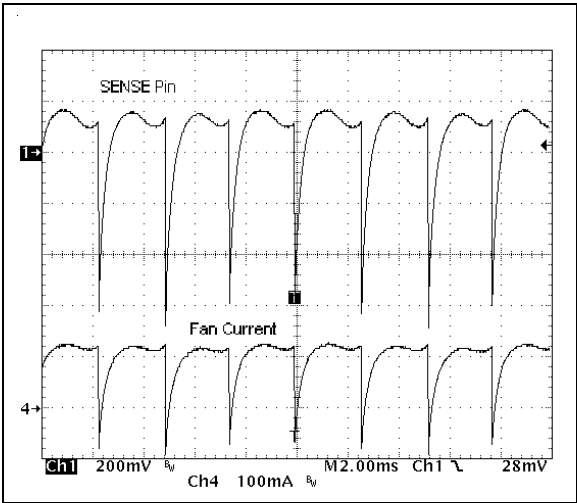


FIGURE 7-6: Typical Fan Current and Sense Pin Waveforms.

7.5 Output Drive Device Selection

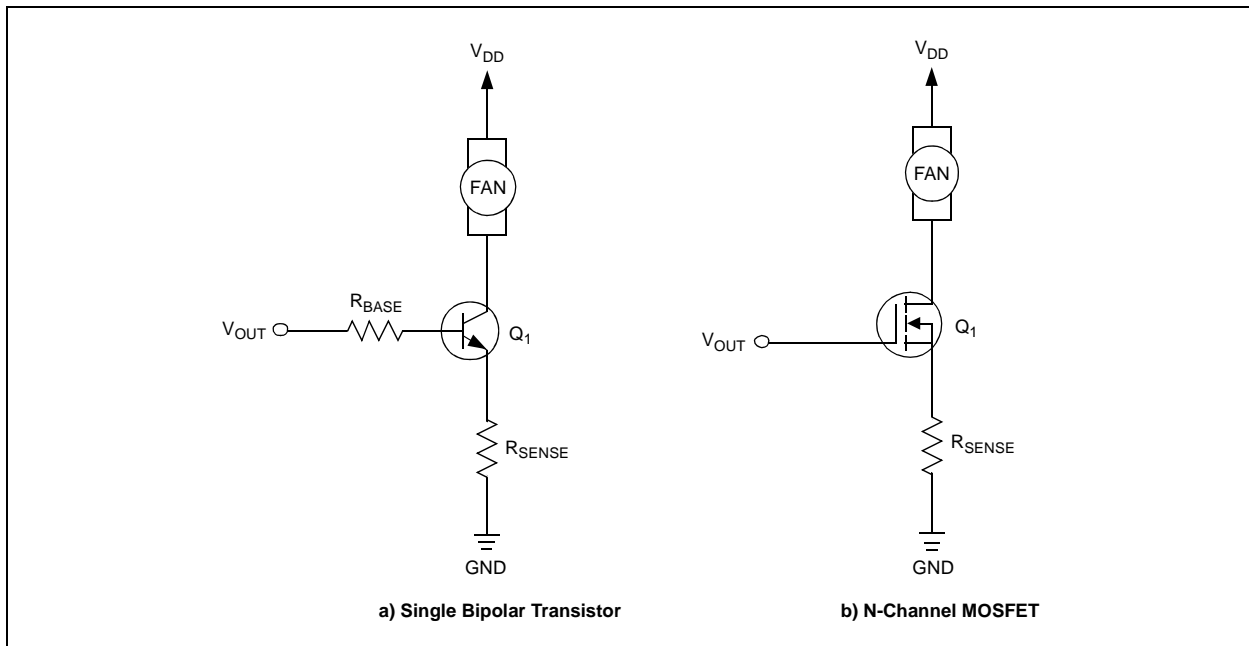
The TC654/TC655 is designed to drive two external NPN transistors or two external N-channel MOSFETs as the fan speed modulating elements. These two arrangements are shown in Figure 7-7. For lower current fans, NPN transistors are a very economical choice for the fan drive device. It is recommended that, for higher-current fans (500 mA and above), MOSFETs be used as the fan drive device. Table 7-2 provides some possible part numbers for use as the fan drive element.

When using an NPN transistor as the fan drive element, a base current limiting resistor must be used. This is shown in Figure 7-7.

When using MOSFETs as the fan drive element, it is very easy to turn the MOSFETs on and off at very high rates. Because the gate capacitances of these small

MOSFETs are very low, the TC654/TC655 can charge and discharge them very quickly, leading to very fast edges. Of key concern is the turn-off edge of the MOSFET. Since the fan motor winding is essentially an inductor, once the MOSFET is turned off, the current that was flowing through the motor wants to continue to flow. If the fan does not have internal clamp diodes around the windings of the motor, there is no path for this current to flow through, and the voltage at the drain of the MOSFET may rise until the drain to source rating of the MOSFET is exceeded. This will most likely cause the MOSFET to go into Avalanche mode. Since there is very little energy in this occurrence, it will probably not fail the device, but it would be a long term reliability issue. The following is recommended:

- Ask how the fan is designed. If the fan has clamp diodes internally, you will not experience this problem. If the fan does not have internal clamp diodes, it is a good idea to put one externally (Figure 7-8). You can also put a resistor between  $V_{OUT}$  and the gate of the MOSFET, which will help slow down the turn-off and limit this condition.



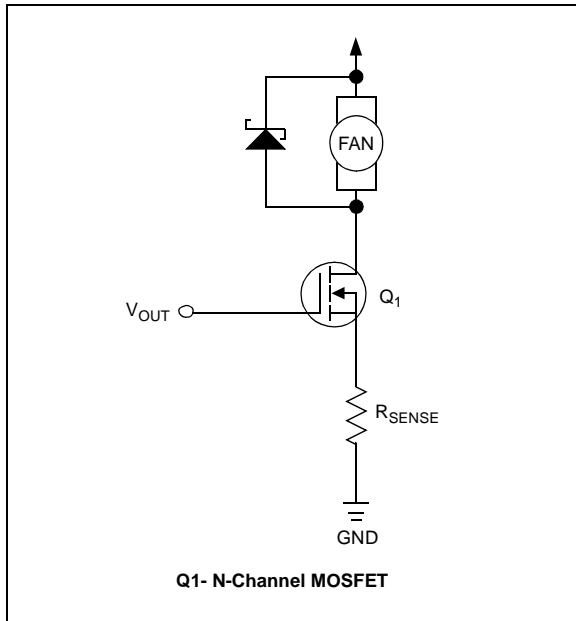
**FIGURE 7-7:** Output Drive Device Configurations.

**TABLE 7-2:** FAN DRIVE DEVICE SELECTION TABLE (Note 2)

Device	Package	Max Vbe sat / Vgs(V)	Min hfe	Vce/V <sub>DS</sub>	Fan Current (mA)	Suggested Rbase (ohms)
MMBT2222A	SOT-23	1.2	50	40	150	800
MPS2222A	TO-92	1.2	50	40	150	800
MPS6602	TO-92	1.2	50	40	500	301
SI2302	SOT-23	2.5	NA	20	500	Note 1
MGSF1N02E	SOT-23	2.5	NA	20	500	Note 1
SI4410	SO-8	4.5	NA	30	1000	Note 1
SI2308	SOT-23	4.5	NA	60	500	Note 1

**Note 1:** A series gate resistor may be used in order to control the MOSFET turn-on and turn-off times.

**2:** These drive devices are suggestions only. Fan currents listed are for individual fans.



**FIGURE 7-8:** Clamp Diode For Fan Turn-Off.

## 7.6 Bias Supply Bypassing and Noise Filtering

The bias supply ( $V_{DD}$ ) for the TC654/TC655 devices should be bypassed with a 1  $\mu$ F ceramic capacitor. This capacitor will help supply the peak currents that are required to drive the base/gate of the external fan drive devices.

As the  $V_{IN}$  pin controls the duty cycle in a linear fashion, any noise on this pin can cause duty cycle jittering. For this reason, the  $V_{IN}$  pin should be bypassed with a 0.01  $\mu$ F capacitor.

In order to keep fan noise off of the TC654/TC655 device ground, individual ground returns for the TC654/TC655 and the low side of the fan current sense resistor should be used.

## 7.7 Determining Current Pulses Per Revolution of Fans

There are many different fan designs available in the marketplace today. The motor designs can vary and, along with it, the number of current pulses in one fan revolution. In order to correctly measure and communicate the fan speed, the TC654/TC655 must be programmed for the proper number of fan current pulses per revolution. This is done by setting the F2PPR and F1PPR bits in the Configuration Register to the proper values (see [Section 6.3 "Configuration Register \(Config\)"](#) for settings). A fan's current pulses per revolution can be determined in the following manner.

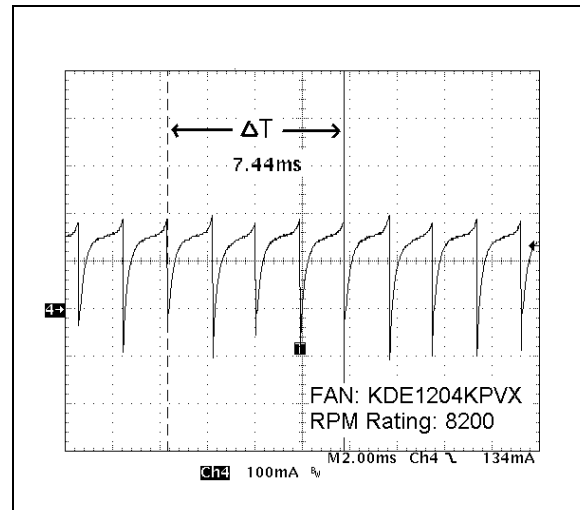
The first piece of information required is the fan's full-speed RPM rating. The fan RPM rating can then be converted to give the time for one revolution using the following equation:

### EQUATION

$$\text{Time for one revolution (msec.)} = \frac{60 \times 1000}{\text{Fan RPM}}$$

The fan current can now be monitored over this time period. The number of pulses occurring in this time period is the fan's "Current Pulses per Rotation" rating which is needed in order to accurately read fan RPM.

**Example:** The full-speed fan RPM rating is 8200 RPM. From this, the time for one fan revolution is calculated to be 7.3 msec, using the previously discussed equation. Using a current probe, the fan current can be monitored as the fan is operating at full speed. [Figure 7-9](#) shows the fan current pulses for this example. The 7.44 msec window, marked by the cursors, is very near the 7.3 msec calculated above, and is within the tolerance of the fan ratings. Four current pulses occur within this 7.44 msec time frame. Given this information, F2PPR (bits 4-3<01>) and F1PPR (bits 2-1<01>) in the Configuration Register, should be set to '10' to indicate 4 current pulses per revolution.

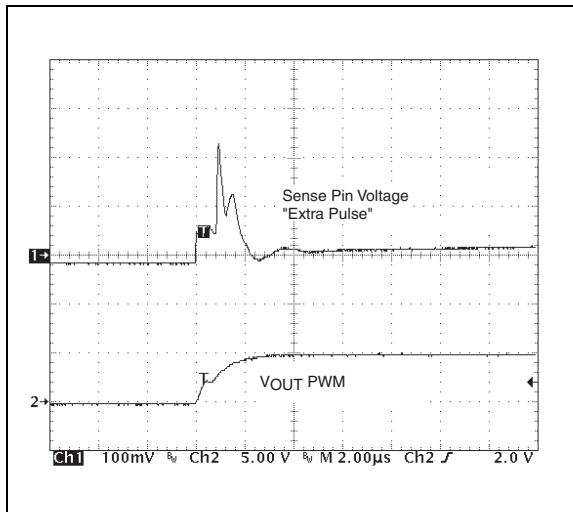


**FIGURE 7-9:** Four Current Pulses Per Revolution Fan.

## 7.8 How to Eliminate False Current Pulse Sensing

During the PWM mode of operation, some fans will generate an extra current pulse. This pulse occurs when the external drive device is turned on and is, in most cases, caused by the fan's electronics that control the fan motor. This pulse does not represent true fan current and needs to be blanked out. This is particularly important for detecting a fan in a locked rotor condition. [Figure 7-10](#) shows the voltage pulse at the Sense pin,

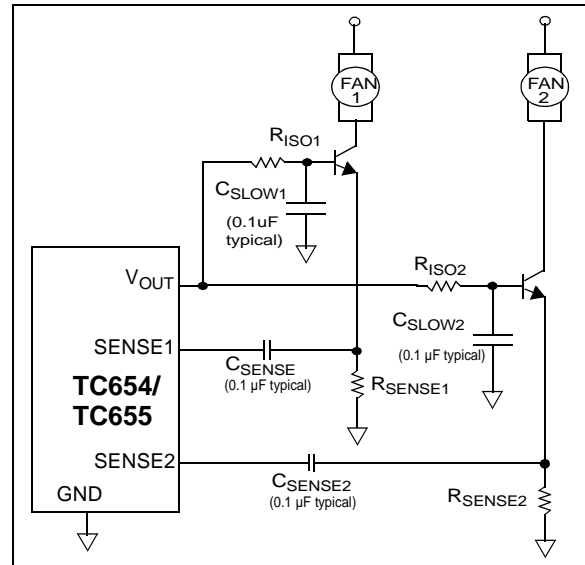
which is caused by the fan's "extra" current pulse during PWM output turn-on.



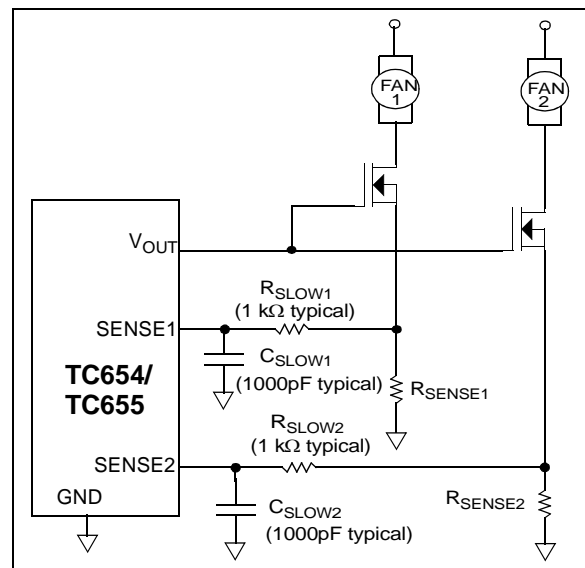
**FIGURE 7-10:** Extra Pulse at Sense Pin.

This problem occurs mainly with fans that have a current waveshape like the one shown in Figure 7-9. For configurations where an NPN transistor is being used as the external drive device, the typical  $R_{SENSE}$  and  $C_{SENSE}$  scheme can continue to be used to sense the fan current pulses. In order to eliminate the extra current pulse, a slow-down capacitor can be placed from the base of the transistor to ground. A 0.1  $\mu\text{F}$  capacitor is appropriate in most cases. This arrangement is shown in Figure 7-11. This capacitor will help to slow down the turn-on edge of the transistor and reduce the amplitude of the extra current pulse.

For configurations using an N-channel MOSFET as the drive device, the slow-down capacitor does not fix all conditions and the current sensing scheme must be changed. Since the current for this type of fan always returns to zero, the coupling capacitor ( $C_{SENSE}$ ) is not needed. Instead, it will be replaced by an R-C configuration to eliminate the voltage pulse generated by the extra current pulse. This new sensing configuration is shown in Figure 7-12. The values of the resistor/capacitor combination should be adjusted so that the voltage pulse generated by the extra current pulse is smoothed and is not registered by the TC654/TC655 as a true fan current pulse. Typical values for  $R_{SLOW}$  and  $C_{SLOW}$  are 1 K $\Omega$  and 1000 pF, respectively.



**FIGURE 7-11:** Transistor Drive with  $C_{SLOW}$  Capacitor.



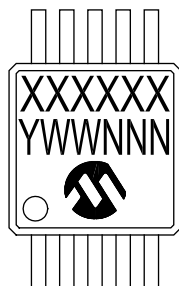
**FIGURE 7-12:** FET Drive with  $R_{SLOW}/C_{SLOW}$  Sense Scheme.

# TC654/TC655

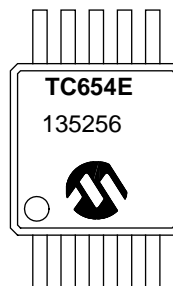
## 8.0 PACKAGING INFORMATION

### 8.1 Package Marking Information

10-Lead MSOP (3x3 mm)



Example

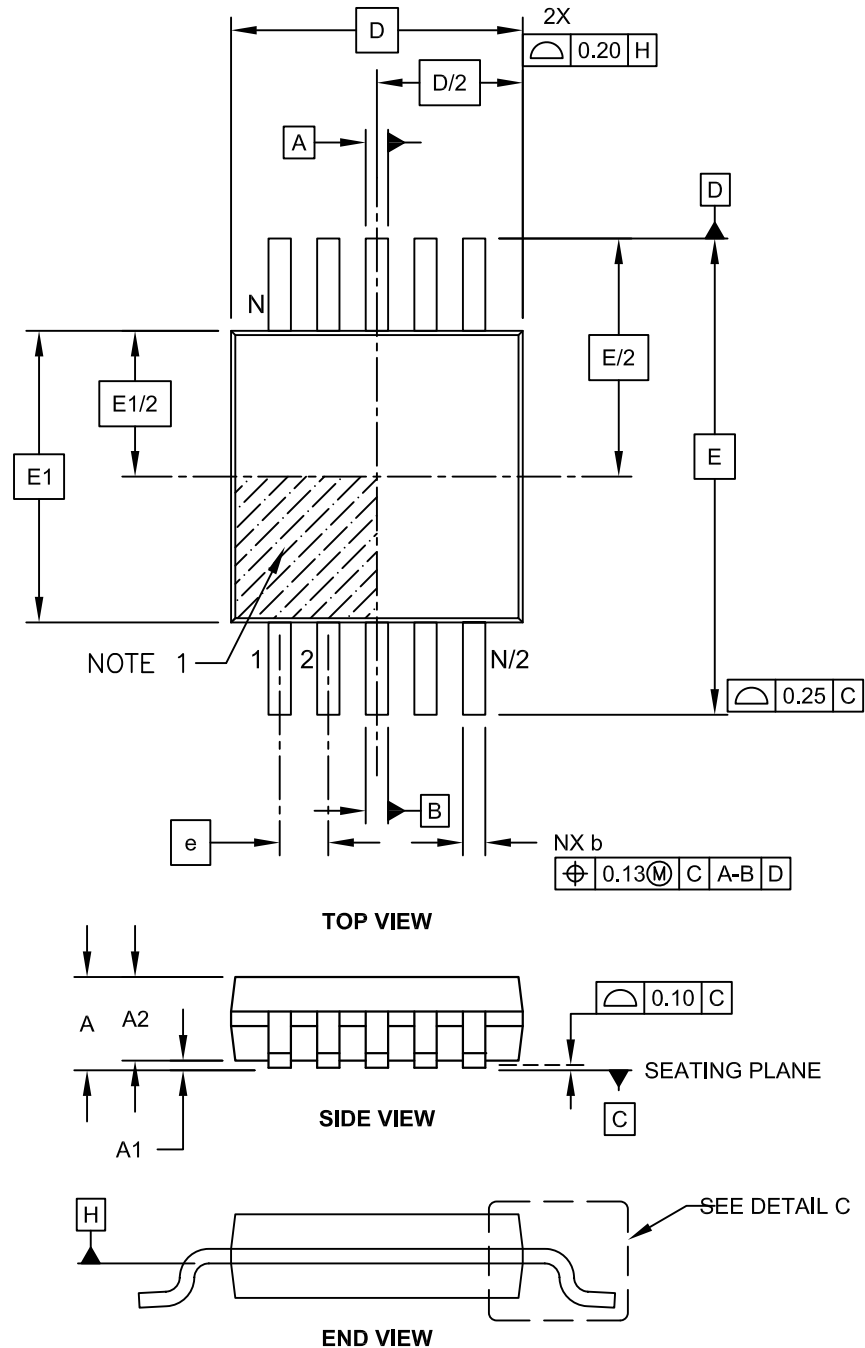


<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

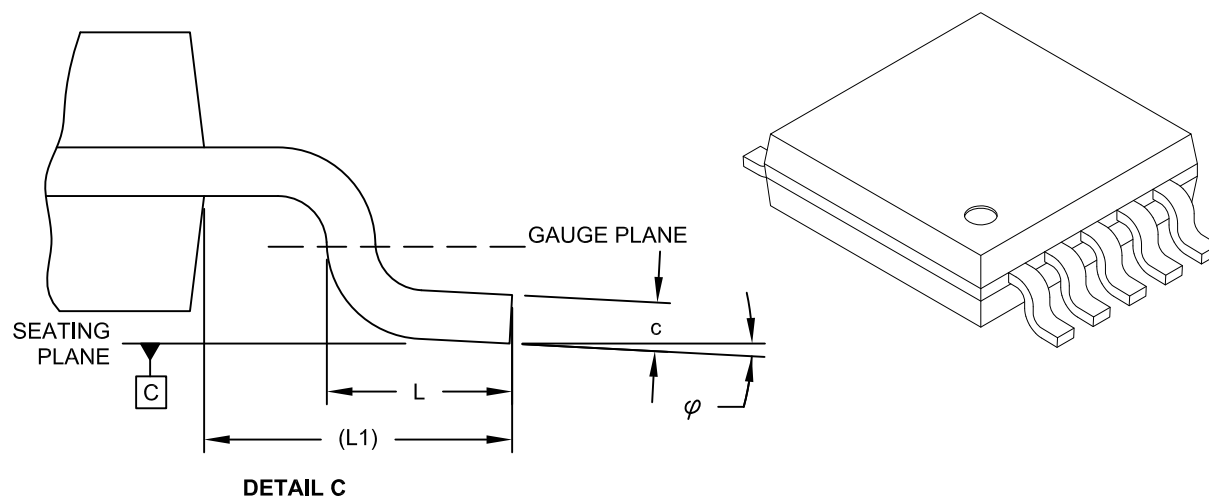


Microchip Technology Drawing C04-021C Sheet 1 of 2

# TC654/TC655

## 10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		10		
Pitch	e		0.50 BSC		
Overall Height	A		-	-	1.10
Molded Package Thickness	A2		0.75	0.85	0.95
Standoff	A1		0.00	-	0.15
Overall Width	E		4.90 BSC		
Molded Package Width	E1		3.00 BSC		
Overall Length	D		3.00 BSC		
Foot Length	L		0.40	0.60	0.80
Footprint	L1		0.95 REF		
Foot Angle	$\phi$		0°	-	8°
Lead Thickness	c		0.08	-	0.23
Lead Width	b		0.15	-	0.33

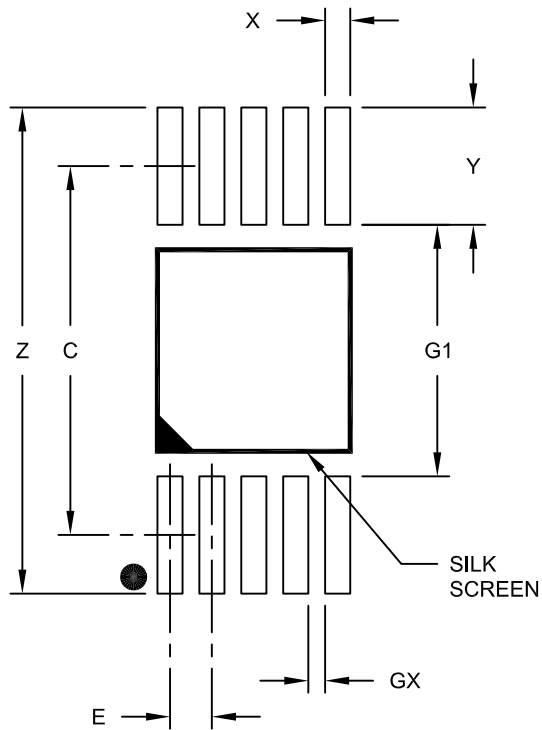
### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021C Sheet 2 of 2

## 10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads	G1	3.00		
Distance Between Pads	GX	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021A

# TC654/TC655

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NOTES:

## **APPENDIX A: REVISION HISTORY**

### **Revision C (July 2014)**

The following is the list of modifications.

1. Updated the package marking drawing.
2. Added Appendix A.

### **Revision B (January 2013)**

The following is the list of modifications.

1. Added a note to the package outline drawing.

### **Revision A (2002)**

- Original Release of this Document.

# TC654/TC655

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>		<u>X</u>	<u>/XX</u>
Device		Temperature Range	Package
<b>Device:</b>		TC654:	PWM Fan Speed Controller w/Fault Detection
		TC654T:	PWM Fan Speed Controller w/Fault Detection (Tape and Reel)
		TC655:	PWM Fan Speed Controller w/Fault Detection
		TC655T:	PWM Fan Speed Controller w/Fault Detection (Tape and Reel)
<b>Temperature Range:</b>		E	= -40°C to +85°C
<b>Package:</b>		UN	= Plastic Micro Small Outline (MSOP), 10-lead

### Examples:

- TC654EUN: PWM Fan Speed Controller w/ Fault Detection
- TC654EUNT: PWM Fan Speed Controller w/Fault Detection (Tape and Reel)
- TC655EUN: PWM Fan Speed Controller w/ Fault Detection
- TC655EUNT: PWM Fan Speed Controller w/Fault Detection (Tape and Reel)

# TC654/TC655

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

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*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

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