# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate- source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 58 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 36.5 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 232 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 330 | W |
| $I_{AR}$ | Max current during repetitive or single pulse avalanche (pulse width limited by $T_{JMAX}$) | 12 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 1410 | mJ |
| dv/dt (2) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 50 | V/ns |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | 150 | °C |

1. Pulse width limited by safe operating area
2. $I_{SD}$ ≤ 58 A, di/dt = 400 A/µs, peak $V_{DS} < V_{(BR)DSS}$, $V_{DD}$ = 400 V
3. $V_{DS} \leq$ 520 V

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.38 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 50 | °C/W |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 650 V<br>$V_{DS}$ = 650 V, $T_C$=125 °C | | | 1<br>100 | $\mu$A<br>$\mu$A |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 25 V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 $\mu$A | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 29 A | | 0.037 | 0.045 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 6420 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 170 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 11 | - | pF |
| $C_{o(tr)}$(1) | Equivalent capacitance time related | $V_{GS}$ = 0, $V_{DS}$ = 0 to 520 V | - | 536 | - | pF |
| $C_{o(er)}$(2) | Equivalent capacitance energy related | $V_{GS}$ = 0, $V_{DS}$ = 0 to 520 V | - | 146 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 1.3 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 29 A, $V_{GS}$ = 10 V (see *Figure 16*) | - | 143 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 38 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 64 | - | nC |

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.
2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(V)}$ | Voltage delay time | $V_{DD}$ = 400 V, $I_D$ = 38 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 17*) (see *Figure 20*) | - | 102 | - | ns |
| $t_{r(V)}$ | Voltage rise time | | - | 10 | - | ns |
| $t_{f(i)}$ | Current fall time | | - | 11.5 | - | ns |
| $t_{c(off)}$ | Crossing time | | - | 14.5 | - | ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 58 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 232 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 58 A, $V_{GS}$ = 0 | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 58 A, di/dt = 100 A/µs $V_{DD}$ = 100 V (see *Figure 17*) | - | 480 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 11 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 46 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 58 A, di/dt = 100 A/µs $V_{DD}$ = 100 V, $T_j$ = 150 °C (see *Figure 17*) | - | 592 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 16 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 53 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

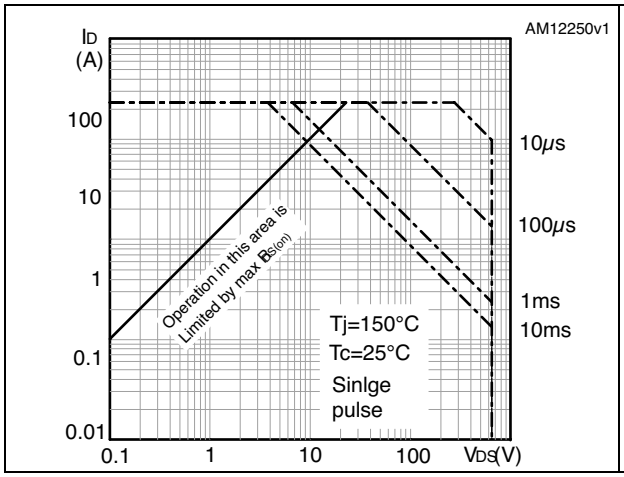



**Figure 3. Thermal impedance**

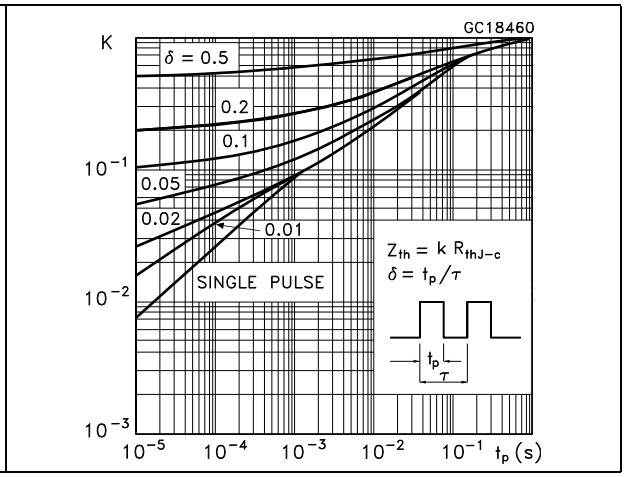



**Figure 4. Output characteristics**

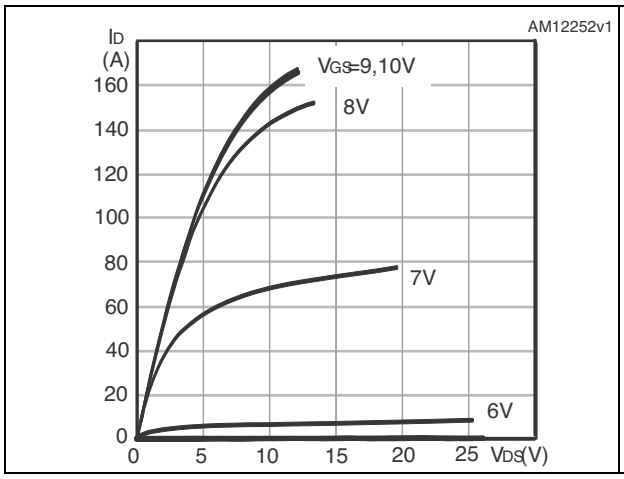



**Figure 5. Transfer characteristics**

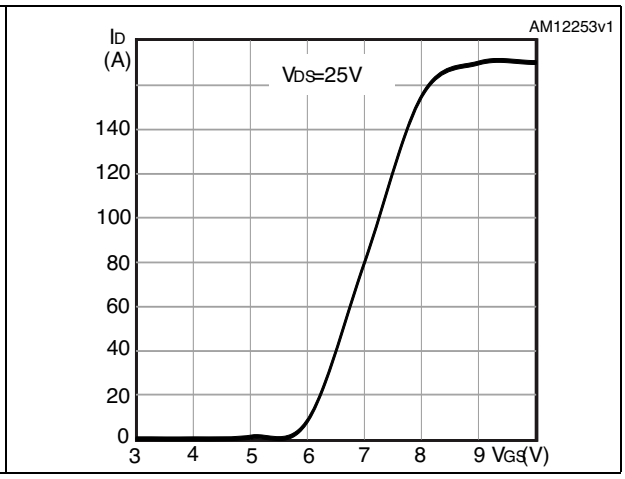



**Figure 6. Gate charge vs gate-source voltage**

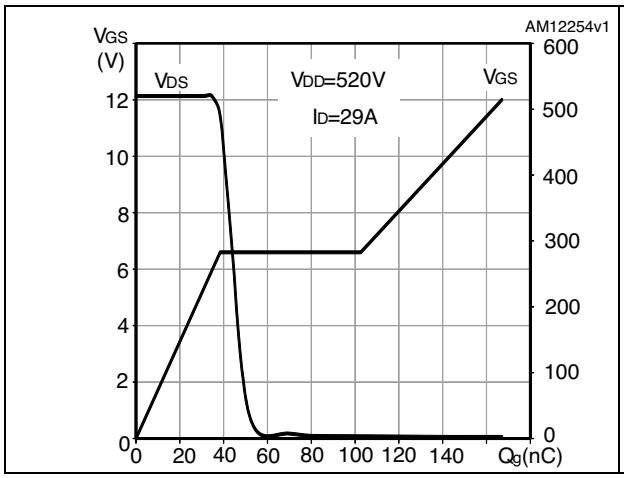



**Figure 7. Static drain-source on-resistance**

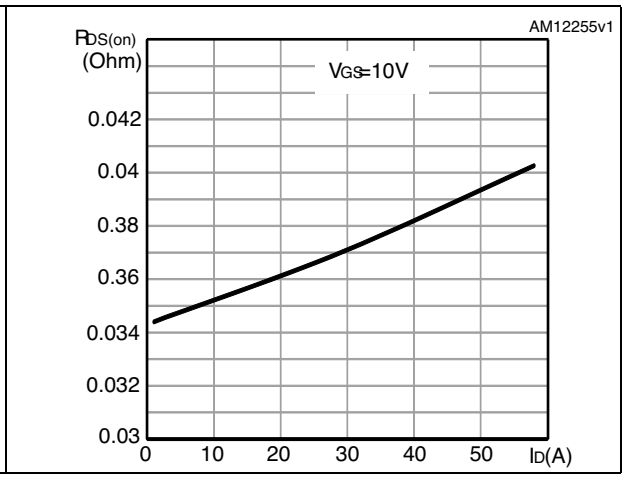


**Figure 8. Capacitance variations**

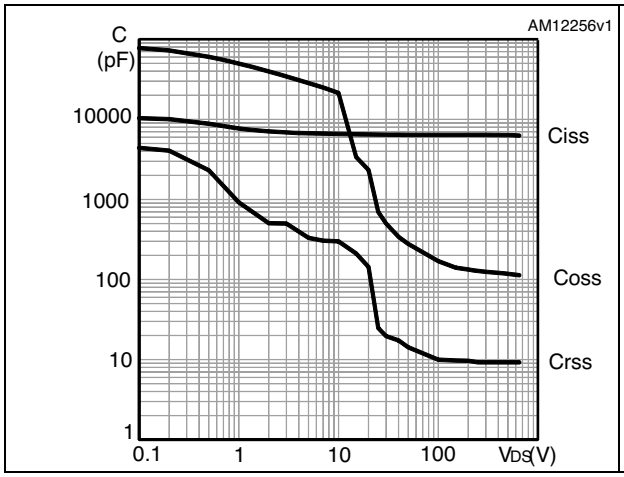



**Figure 9. Output capacitance stored energy**

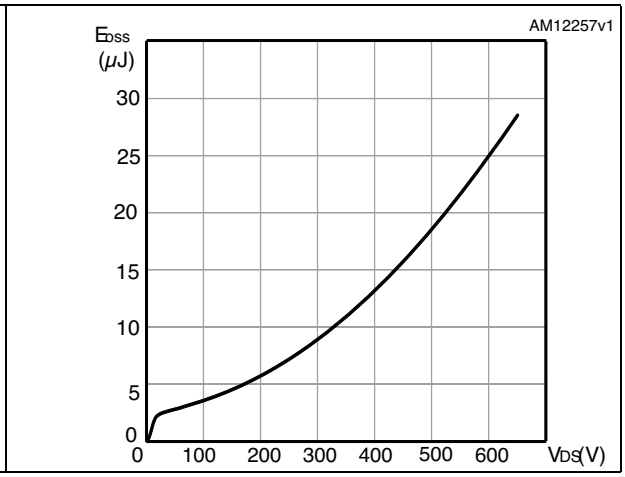



**Figure 10. Normalized gate threshold voltage vs temperature**

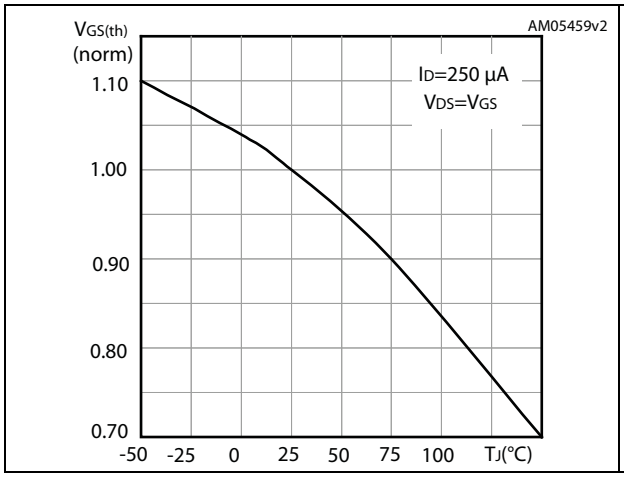



**Figure 11. Normalized on-resistance vs temperature**

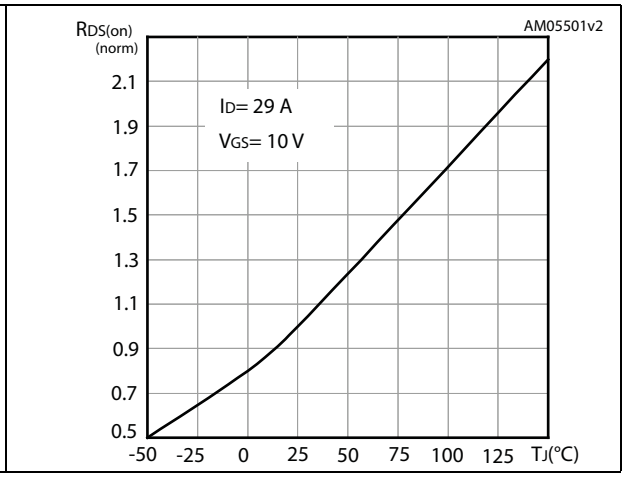



**Figure 12. Source-drain diode forward characteristics**

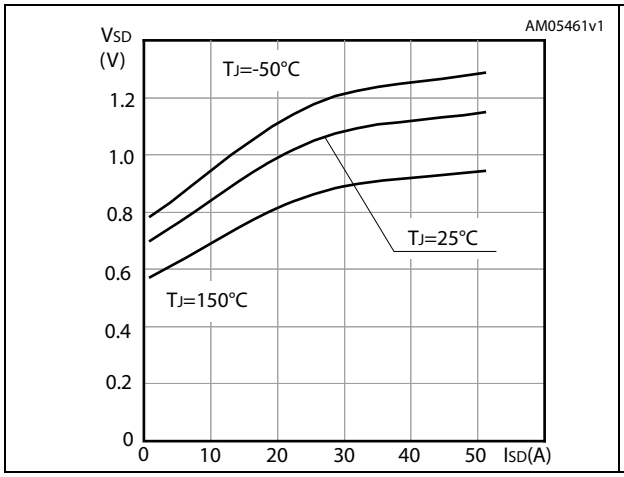



**Figure 13. Normalized $V_{DS}$ vs temperature**

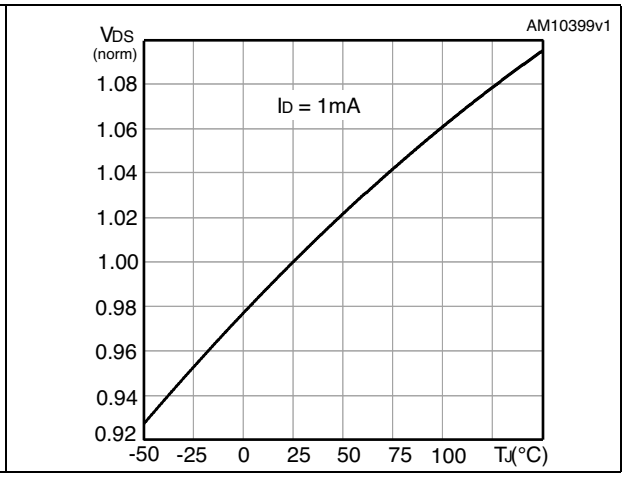
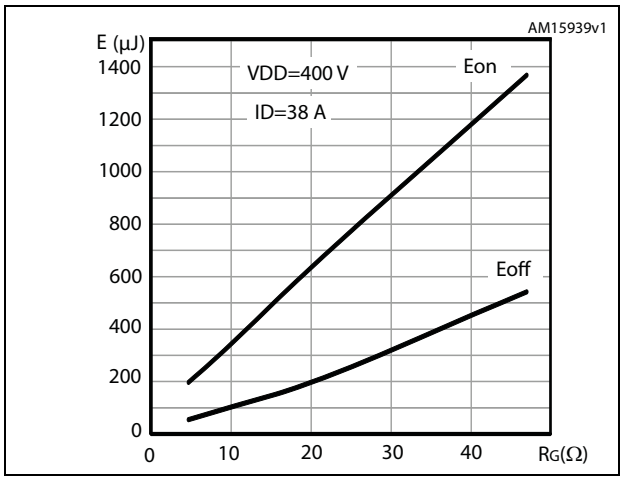


**Figure 14. Switching losses vs gate resistance (1)**




1. Eon including reverse recovery of a SiC diode.

# 3 Test circuits

**Figure 15. Switching times test circuit for resistive load**

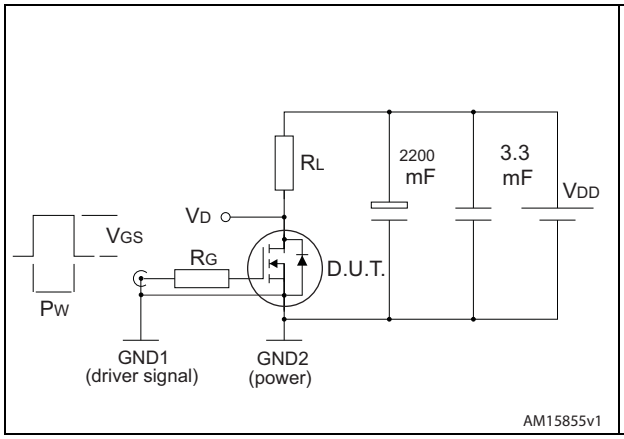



**Figure 16. Gate charge test circuit**

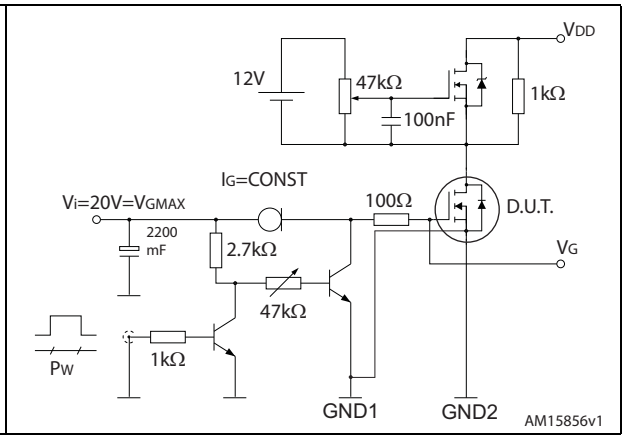



**Figure 17. Test circuit for inductive load switching and diode recovery times**

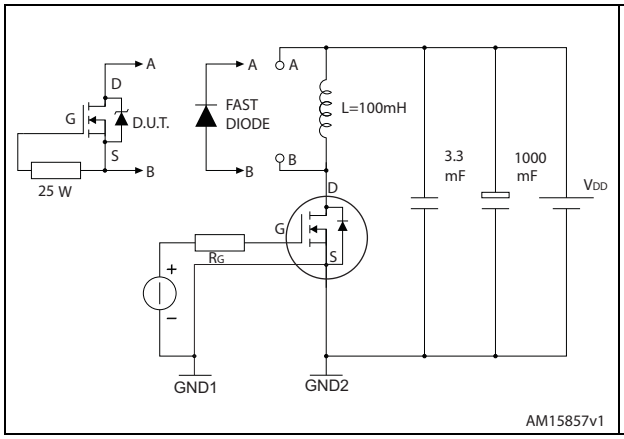



**Figure 18. Unclamped inductive load test circuit**

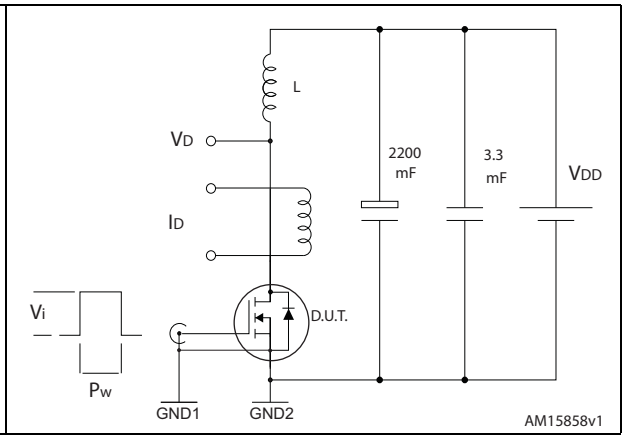



**Figure 19. Unclamped inductive waveform**

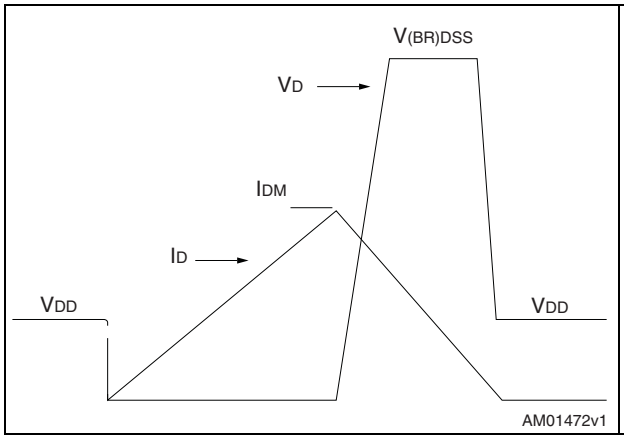
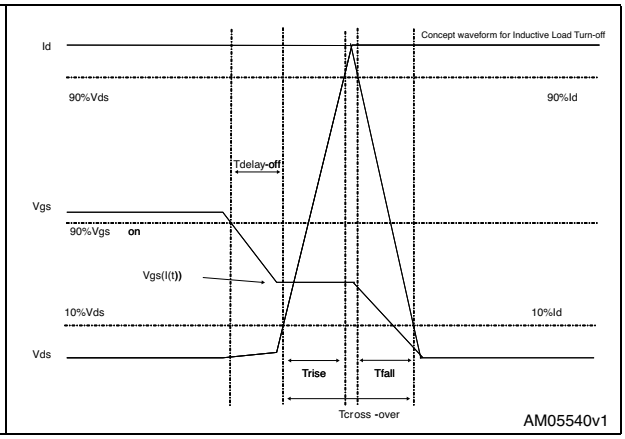



**Figure 20. Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 21. TO247-4 drawing**

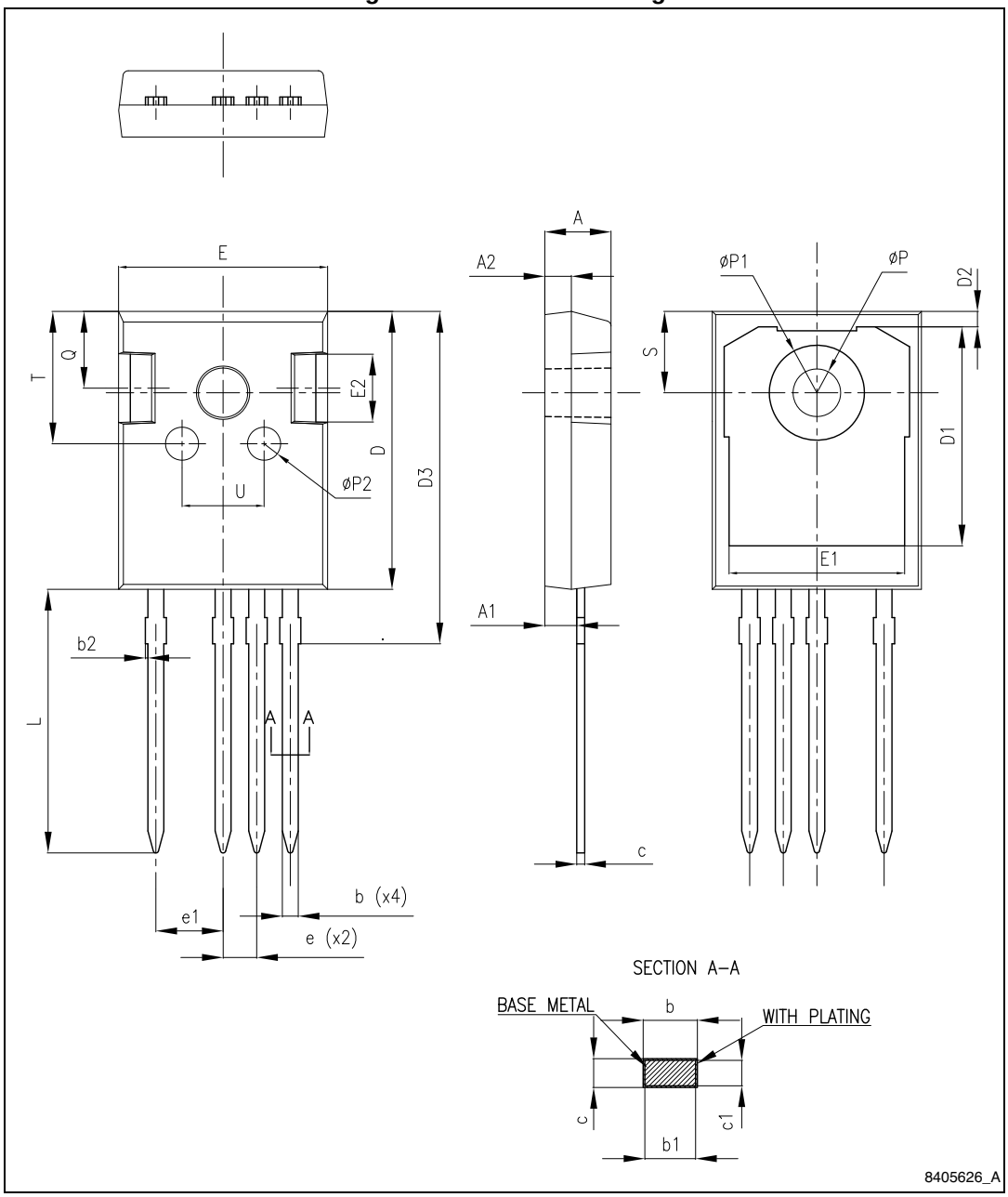


Table 8. TO247-4 mechanical data

| Dim. | mm. | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.90 | 5.00 | 5.10 |
| A1 | 2.31 | 2.41 | 2.51 |
| A2 | 1.90 | 2.00 | 2.10 |
| b | 1.16 | | 1.29 |
| b1 | 1.15 | 1.20 | 1.25 |
| b2 | 0 | | 0.20 |
| c | 0.59 | | 0.66 |
| c1 | 0.58 | 0.60 | 0.62 |
| D | 20.90 | 21.00 | 21.10 |
| D1 | 16.25 | 16.55 | 16.85 |
| D2 | 1.05 | 1.20 | 1.35 |
| D3 | 24.97 | 25.12 | 25.27 |
| E | 15.70 | 15.80 | 15.90 |
| E1 | 13.10 | 13.30 | 13.50 |
| E2 | 4.90 | 5.00 | 5.10 |
| E3 | 2.40 | 2.50 | 2.60 |
| e | 2.44 | 2.54 | 2.64 |
| e1 | 4.98 | 5.08 | 5.18 |
| L | 19.80 | 19.92 | 20.10 |
| P | 3.50 | 3.60 | 3.70 |
| P1 | | | 7.40 |
| P2 | 2.40 | 2.50 | 2.60 |
| Q | 5.60 | | 6.00 |
| S | | 6.15 | |
| T | 9.80 | | 10.20 |
| U | 6.00 | | 6.40 |

# 5 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 28-Jun-2013 | 1 | Initial release. |
| 17-Jan-2014 | 2 | Document status promoted from preliminary to production data. |

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