Contents

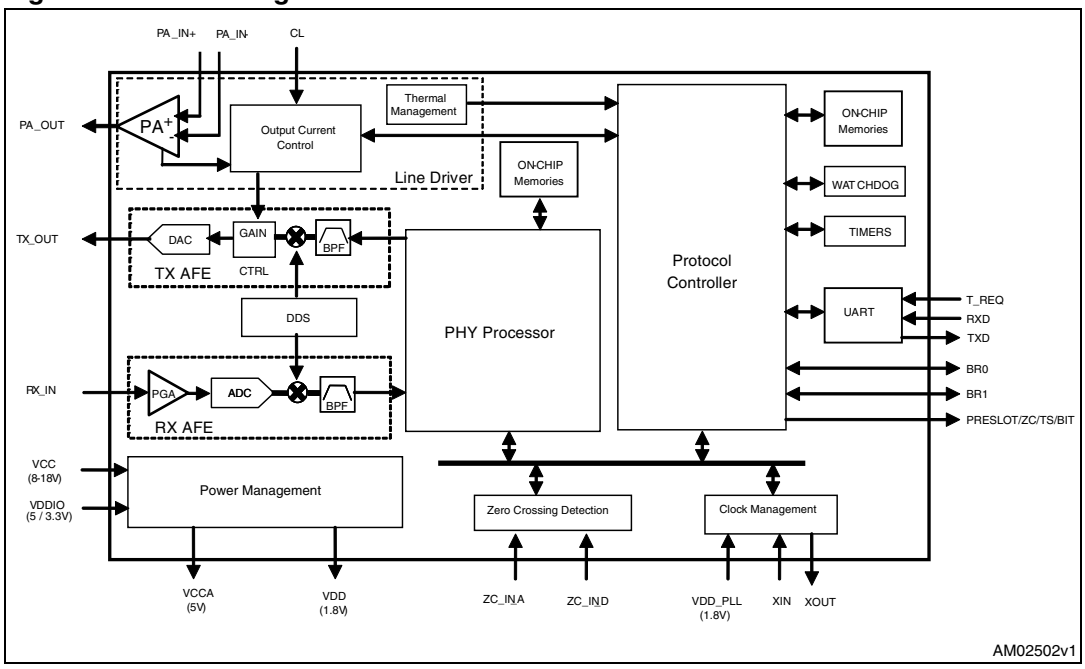
1 Device overview

Realized using a multi-power technology with state-of-the-art VLSI CMOS lithography, the ST7570 is based on dual digital core architecture (a PHY processor engine and a protocol controller core) to guarantee outstanding communication performance with a high level of flexibility and programmability.

The on-chip analog front end, featuring analog to digital and digital to analog conversion and automatic receiver gain control, plus the integrated Power Amplifier delivering up to 1Arms output current, makes the ST7570 the first complete system-on-chip for power line communication.

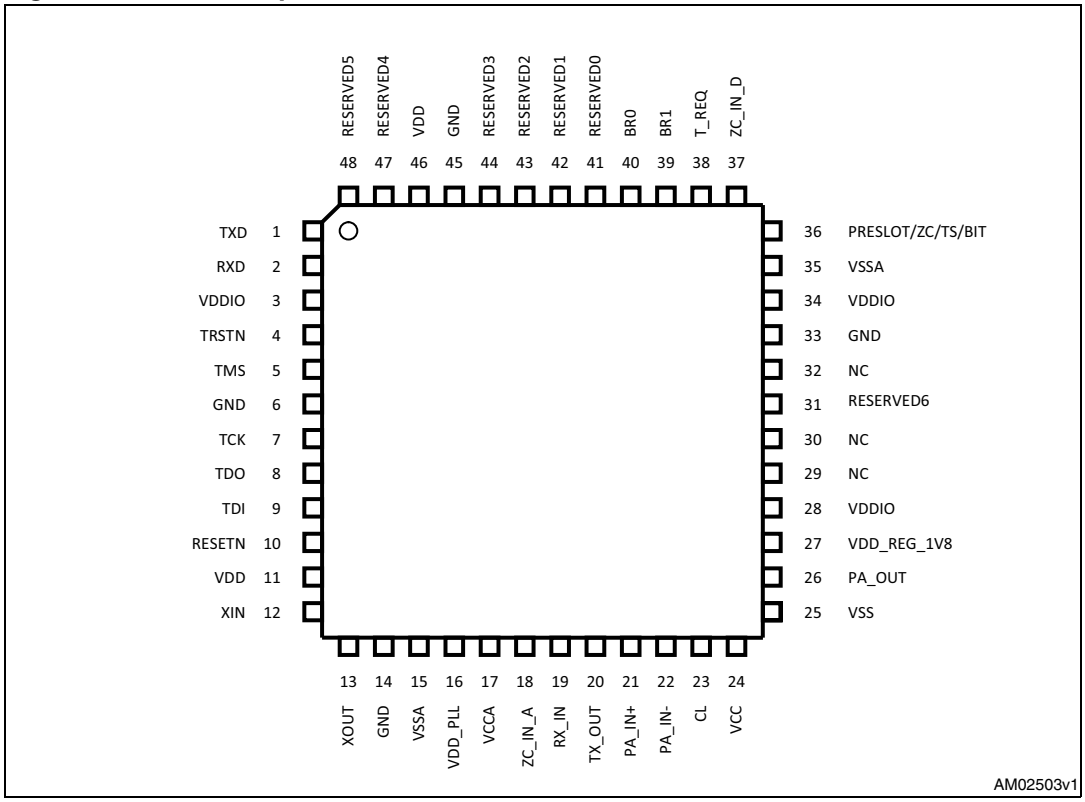
Line coupling network design is also simplified, leading to a very low cost BOM. Safe and performing operations are guaranteed while keeping power consumption and distortion levels very low, thus making ST7570 an ideal platform for the most stringent application requirements and regulatory standards compliance.

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin out top view



2.1 Pin description

Table 2. Pin description

Pin	Name	Type	Reset state	Pull-up	Description
1	TXD	Digital output	High Z	Disabled	UART data out External pull-up to VDDIO required
2	RXD	Digital input	High Z	Disabled	UART data in
3	VDDIO	Power	-	-	3.3 V – 5 V I/O external supply
4	TRSTN	Digital input	Input	Enabled	System JTAG interface reset (active low)
5	TMS	Digital input	Input	Enabled	System JTAG interface mode select
6	GND	Power	-	-	Digital ground
7	TCK	Digital input	High Z	Disabled	System JTAG interface clock. External pull-up to VDDIO required
8	TDO	Digital output	High Z	Disabled	System JTAG interface data out
9	TDI	Digital input	Input	Enabled	System JTAG interface data in
10	RESETN	Digital input	Input	Disabled	System reset (active low)
11	VDD	Power	-	-	1.8 V digital supply. Internally connected to VDD_REG_1V8 Externally accessible for filtering purposes only
12	XIN	Analog	-	-	Crystal oscillator input / external clock input
13	XOUT	Analog	-	-	Crystal oscillator output (if external clock supplied on XIN, XOUT must be left floating)
14	GND	Power	-	-	Digital ground
15	VSSA	Power	-	-	Analog ground
16	VDD_PLL	Power	-	-	1.8 V PLL supply voltage. Connect externally to VDD
17	VCCA	Power	-	-	5 V analog supply / internal regulator output Externally accessible for filtering purposes only
18	ZC_IN_A	Analog input	-	-	Analog zero-crossing input
19	RX_IN	Analog input	-	-	Reception analog input
20	TX_OUT	Analog output	-	-	Transmission analog output
21	PA_IN+	Analog input	-	-	Power amplifier Non-inverting input
22	PA_IN-	Analog input	-	-	Power amplifier Inverting input
23	CL	Analog input	-	-	Current limit sense input
24	VCC	Power	-	-	Power supply
25	VSS	Power	-	-	Power ground

Table 2. Pin description (continued)

Pin	Name	Type	Reset state	Pull-up	Description
26	PA_OUT	Analog output	-	-	Power amplifier output
27	VDD_REG_1V8	Power	-	-	1.8 V digital supply / internal regulator output Externally accessible for filtering purposes only
28	VDDIO	Power	-	-	3.3 V – 5 V I/O external supply
29	NC	-	-	-	Not used, leave floating
30	NC	-	-	-	Not used, leave floating
31	RESERVED6	-	-	-	Pull up to VDDIO
32	NC	-	-	-	Not used, leave floating
33	GND	Power	-	-	Digital ground
34	VDDIO	Power	-	-	3.3 V – 5 V I/O supply
35	VSSA	Power	-	-	Analog ground
36	PRESLOT /ZC/TS/BIT	Digital output	High Z	Disabled	Configurable digital output: - Slot synchronization (PRESLOT), - Zero Crossing (ZC), - Timeslot (TS), - Bit synchronization (BIT), - Transmission in progress (TXP), - Reception in progress (RXP), - Transmission or Reception in progress (TXRXP). If not used, this pin can be left floating.
37	ZC_IN_D	Digital input	High Z	Disabled	Digital zero-crossing input. Pull up to VDDIO if not used
38	T_REQ	Digital input	High Z	Disabled	UART communication control line
39	BR1	Digital input	High Z	Disabled	UART baud rate selection (sampled after each reset event) see *Table 3*
40	BR0	Digital input	High Z	Disabled	
41	RESERVED0	-	-	-	Connect to GND
42	RESERVED1	-	-	-	Pull up to VDDIO
43	RESERVED2	-	-	-	Pull up to VDDIO
44	RESERVED3	-	-	-	Pull up to VDDIO
45	GND	Power	-	-	Digital ground
46	VDD	Power	-	-	1.8 V digital supply. Internally connected to VDD_REG_1V8 Externally accessible for filtering purposes only
47	RESERVED4	-	-	-	Connect to VDDIO
48	RESERVED5	-	-	-	Pull up to VDDIO

Table 3. UART baud rate selection

BR1	BR0	Baud rate
0	0	9600
0	1	19200
1	0	38400
1	1	57600

3 Maximum ratings

3.1 Absolute maximum ratings

Figure 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
VCC	Power supply voltage	-0.3	20	V
VSSA-GND	Voltage between VSSA and GND	-0.3	0.3	V
VDDIO	I/O supply voltage	-0.3	5.5	V
VI	Digital input voltage	GND-0.3	VDDIO+0.3	V
VO	Digital output voltage	GND-0.3	VDDIO+0.3	V
V(PA_IN)	PA inputs voltage range	VSS-0.3	VCC+0.3	V
V(PA_OUT)	PA_OUT voltage range	VSS-0.3	VCC+0.3	V
V(RX_IN)	RX_IN voltage range	-(VCCA+0.3)	VCC+0.3	V
V(ZC_IN_A)	ZC_IN_A voltage range	-(VCCA+0.3)	VCCA+0.3	V
V(TX_OUT, CL)	TX_OUT, CL voltage range	VSSA-0.3	VCCA+0.3	V
V(XIN)	XIN voltage range	GND-0.3	VDDIO+0.3	V
I(PA_OUT)	Power amplifier output non-repetitive peak current		5	A peak
I(PA_OUT)	Power amplifier output non-repetitive rms current		1.4	A rms
T_{amb}	Operating ambient temperature	-40	85	°C
T_{stg}	Storage temperature	-50	150	°C
V(ESD)	Maximum withstanding voltage range Test condition: CDF-AEC-Q100-002 “Human Body Model” Acceptance criteria: “Normal Performance”	-2	+2	kV

3.2 Thermal data

Table 4. Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thJA1}	Maximum thermal resistance junction-ambient steady state (1)	50	°C/W
R_{thJA2}	Maximum thermal resistance junction-ambient steady state (2)	42	°C/W

1. Mounted on a 2-side + vias PCB with a ground dissipating area on the bottom side.
2. Same conditions as in Note 1, with maximum transmission duration limited to 100 s.

4 Electrical characteristics

T_A = -40 to +85°C, T_J < 125°C, V_{CC} = 18 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
Power supply						
VCC	Power supply voltage		8	13	18	V
I(VCC) RX	Power supply current - Rx mode	VCCA externally supplied		0.35	0.5	mA
I(VCC) TX	Power supply current - Tx mode, no load	VCCA externally supplied		22	30	mA
VCC UVLO_TL	VCC under voltage lock out low threshold		6.1	6.5	6.95	V
VCC UVLO_TH	VCC under voltage lock out high threshold		6.8	7.2	7.5	V
VCC UVLO_HYST	VCC under voltage lock out hysteresis		250 (1)	700		mV
I(VCCA) RX	Analog supply current - Rx mode			5	6	mA
I(VCCA) TX	Analog supply current - Tx mode	V(TX_OUT) =5 V p-p, No load		8	10	mA
I(VDD)	Digital core supply current			35	41	mA
I(VDD) RESET	Digital core supply current in RESET state			8		mA
VDD_PLL	PLL supply voltage			VDD		V
I(VDD_PLL)	PLL supply current			0.4	0.45	mA
VDDIO	Digital I/O supply voltage	Externally supplied	-10%	3.3 or 5	+10%	V
VDDIO UVLO_TL	VDDIO under voltage lock out low threshold		2.2	2.4	2.6	V
VDDIO UVLO_TH	VDDIO under voltage lock out high threshold		2.45	2.65	2.85	V
VDDIO UVLO_HYST	VDDIO under voltage lock out hysteresis		180	240		mV
Analog front end						
Power amplifier						
V(PA_OUT) BIAS	Power amplifier output bias voltage - Rx mode			VCC/2		V
GBWP	Power amplifier gain-bandwidth product		100			MHz
I(PA_OUT) MAX	Power amplifier maximum output current				1000	mA rms

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
V(PA_OUT) TOL	Power amplifier output tolerance (2)	VCC=18 V, V(PA_OUT) = 14 V p-p (typ), V(PA_OUT) BIAS = VCC/2, R_{LOAD}=50Ω, T = 25°C See *Figure 3*	-3%		+3%	
V(PA_OUT) HD2	Power amplifier output 2nd harmonic distortion			-70	-63	dBc
V(PA_OUT) HD3	Power amplifier output 3rd harmonic distortion			-66	-63	dBc
V(PA_OUT) THD	Power amplifier output total harmonic distortion			0.1	0.15	%
C(PA_IN)	Power amplifier input capacitance	PA_IN+ vs. VSS (3)		10		pF
		PA_IN- vs. VSS (3)		10		pF
PSRR	Power supply rejection ratio	50 Hz		100		dB
		1 kHz		93		dB
		100 kHz		70		dB
CL_TH	Current sense high threshold on CL pin		2.25	2.35	2.4	V
CL_RATIO	Ratio between PA_OUT and CL output current.			80		
Transmitter						
V(TX_OUT) BIAS	Transmitter output bias voltage - Rx mode			VCCA/2		V
V(TX_OUT) MAX	Transmitter output maximum voltage swing	TX_GAIN = 31, No load	4.8	4.95	VCCA	V p-p
TX_GAIN	Transmitter output digital gain range		0		31	
TX_GAIN TOL	Transmitter output digital gain tolerance		-0.35		0.35	dB
R(TX_OUT)	Transmitter output resistance			1		kΩ
V(TX_OUT) HD2	Transmitter output 2nd harmonic distortion	V(TX_OUT) = 4.5 Vpkpk (typ.), no load, T = 25°C		-72	-55	dBc
V(TX_OUT) HD3	Transmitter output 3rd harmonic distortion			-70	-67	dBc
V(TX_OUT) THD	Transmitter output Total harmonic distortion			0.1	0.2	%
Receiver						
V(RX_IN) MAX	Receiver input maximum voltage	VCC = 18 V		16		V p-p
V(RX_IN) BIAS	Receiver input bias voltage			VCCA/2		V
Z(RX_IN)	Receiver input Impedance			10		kΩ
V(RX_IN) MIN	Receiver input sensitivity	Bit rate = 1200 bps @ 50 Hz, BER = 10-3, SNR = 20 dB		45		dBµV rms

Table 5. Electrical characteristics (continued)

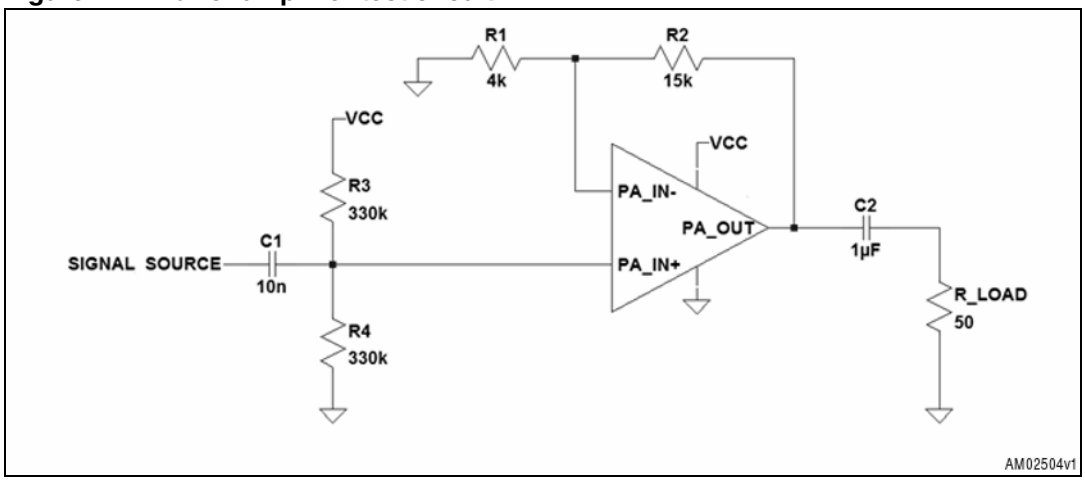
Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
PGA_MIN	PGA minimum gain			-18		dB
PGA_MAX	PGA maximum gain			30		dB
Oscillator						
V(XIN)	Oscillator input voltage swing	Clock frequency supplied externally		1.8	VDDIO	V p-p
V(XIN) TH	Oscillator input voltage threshold		0.8	0.9	1	V
f(XIN)	Crystal oscillator frequency			8		MHz
f(XIN) TOL	External quartz crystal frequency tolerance		-150		+150	ppm
ESR	External quartz crystal ESR value				100	Ω
C_L	External quartz crystal load capacitance			16	20	pF
f_{CLK}_AFE	Internal frequency of the analog front end			8		MHz
f_{CLK}_PROT_ctrl	Internal frequency of the protocol Ctrl core			28		MHz
f_{CLK}_PHY_processor	Internal frequency of the PHY processor core			56		MHz
Temperature sensor						
T_TH_1	Temperature threshold 1		63	70	77	°C
T_TH_2	Temperature threshold 2		90	100	110	°C
T_TH_3	Temperature threshold 3		112	125	138	°C
T_TH_4	Temperature threshold 4		153	170	187	°C
Zero crossing comparator						
V(ZC_IN_A) MAX	Zero crossing analog input voltage range				10	V p-p
V(ZC_IN_A) TL	Zero crossing analog input low threshold		-40	-30	-20	mV
V(ZC_IN_A) TH	Zero crossing analog input high threshold		30	40	50	mV
V(ZC_IN_A) HYST	Zero crossing analog input hysteresis		62	70	78	mV
ZC_IN_D d.c.	Zero crossing digital input duty cycle			50		%
Digital section						
Digital I/O						

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
$R_{PULL-UP}$	Internal pull-up resistors	VDDIO = 3.3 V		66		kΩ
		VDDIO = 5 V		41		kΩ
VIH	High logic level input voltage		0.65*V DDIO		VDDIO +0.3	V
VIL	Low logic level input voltage		-0.3		0.35*V DDIO	V
VOH	High logic level output voltage	IOH= -4 mA	VDDIO -0.4			V
VOL	Low logic level output voltage	IOL= 4 mA			0.4	V
UART interface						
Baud rate			-1.5%	57600	+1.5%	BAUD
			-1.5%	38400	+1.5%	BAUD
			-1.5%	19200	+1.5%	BAUD
			-1.5%	9600	+1.5%	BAUD
Reset and power on						
t_{RESETN}	Minimum valid reset pulse duration			1		µs
$t_{STARTUP}$	Start-up time at power on or after a reset event			60		ms

1. Referred to T_A = -40 °C
2. This parameter does not include the tolerance of external components
3. Guaranteed by design

Figure 4. Power amplifier test circuit

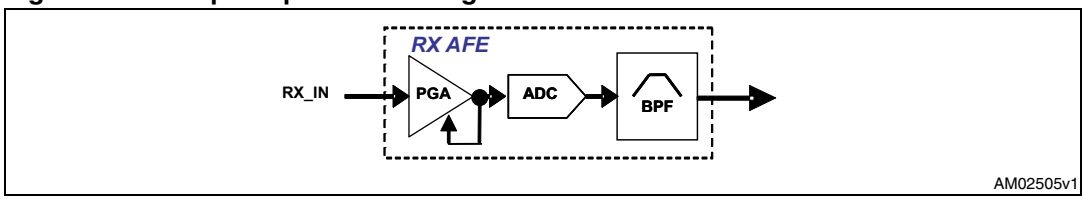


5 Analog front end (AFE)

5.1 Reception path

Figure 4 shows the block diagram of the ST7570 input receiving path. The main blocks are a wide input range analog programmable gain amplifier (PGA) and the analog to digital converter (ADC).

Figure 5. reception path block diagram



The PGA is controlled by an embedded loop algorithm, adapting the PGA gain to amplify or attenuate the input signal according to the input voltage range for the ADC.

The PGA gain ranges from -18 dB up to 30 dB, with steps of 6 dB (typ.), as described in *Table 5*.

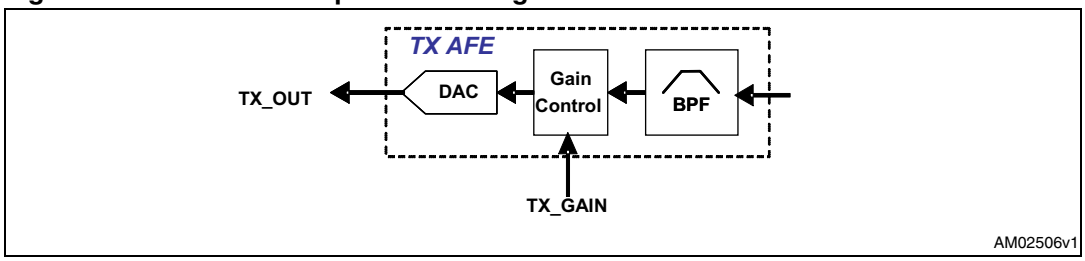
Table 6. PGA gain table

PGA code	PGA gain (typ) [dB]	RX_IN max range [V p-p]
0	-18	16
1	-12	8
2	-6	4
3	0	2
4	6	1
5	12	0.500
6	18	0.250
7	24	0.125
8	30	0.0625

5.2 Transmission path

Figure 5 shows the transmission path block diagram. it is mainly based on a digital to analog converter (DAC), capable to generate a linear signal up to its full scale output. A gain control block before the DAC gives the possibility to scale down the output signal to match the desired transmission level.

Figure 6. Transmission path block diagram



The amplitude of the transmitted signal can be set on a 32-step logarithmic scale through the TX_GAIN parameter, introducing an attenuation ranging from 0 dB (typ.), corresponding to the TX_OUT full range, down to -31 dB (typ.).

The attenuation set by the TX_GAIN parameter can be calculated using the formula of Equation 1:

Equation 1 Output attenuation A [dB] vs. TX GAIN

$$A[dB] = (TX\_GAIN - 31) + TX\_GAIN_{TOL}$$

5.3 Power amplifier

The integrated power amplifier is characterized by very high linearity, required to be compliant with the different international regulations (CENELEC, FCC etc.) limiting the spurious conducted emissions on the mains, and a current capability of 1 A rms that allows the amplifier driving even very low impedance points of the network.

All the pins of the power amplifier are accessible, making it possible to build an active filter network to increase the linearity of the output signal.

5.4 Current and voltage control

The power amplifier output current sensing is performed by mirroring a fraction of the output current and making it flow through a resistor R_{CL} connected between the C_L pin and VSS. The following relationship can be established between V(CL) and I(PA_OUT):

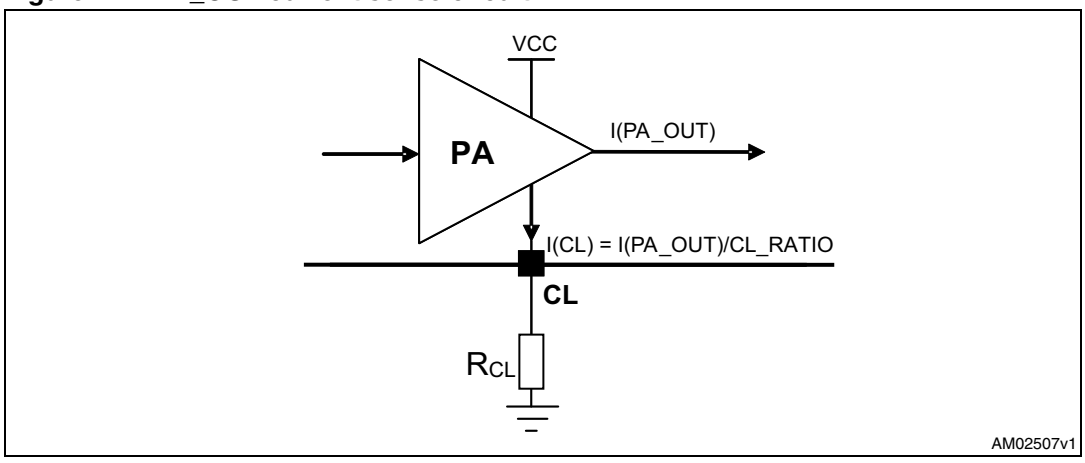
Equation 2 V(CL) vs. I(PA_OUT)

$$V(CL) = \frac{R_{CL} \cdot I(PA\_OUT)}{CL\_RATIO}$$

The voltage level V(CL) is compared with the internal threshold CL_TH. When the V(CL) exceeds the CL_TH level, the V(TX_OUT) voltage is decreased by one TX_GAIN step at a time until V(CL) goes below the CL_TH threshold.

The current sense circuit is depicted in *Figure 6*.

Figure 7. PA_OUT current sense circuit



The R_{CL} value to get the desired output current limit I(PA_OUT)LIM can be calculated according to Equation 3:

Equation 3 R_{CL} calculation

$$R_{CL} = \frac{CL\_TH}{I(PA\_OUT)_{LIM} / CL\_RATIO}$$

Note that $I(PA\_OUT)_{LIM}$ is expressed as peak current, so the corresponding rms current value shall be calculated according to the transmitted signal waveform.

The R_{CL} value to get 1 A rms output current limit, calculated with typical values for CL_TH and CL_RATIO parameters, is indicated in *Table 7*.

Table 7. CL resistor typical values

Parameter	Description	Value	Unit
R_{CL}	Resistor value for I(PA_OUT) MAX = 1 A rms (1.41 A peak)	133	Ω

5.5 Thermal shutdown and temperature control

The ST7570 performs an automatic shutdown of the power amplifier circuitry when the internal temperature exceeds T_TH_4. After a thermal shutdown event, the temperature must get below T_TH_3 before the ST7570 power amplifier comes back to operation.

Moreover, a digital thermometer is embedded to identify the internal temperature among four zones, as indicated in *Table 8*.

Table 8. Temperature zones

Temperature zone	Temperature value
1	$T < T\_TH_1$
2	$T\_TH_1 < T < T\_TH_2$
3	$T\_TH_2 < T < T\_TH_3$
4	$T > T\_TH_3$

5.6 Zero-crossing PLL and delay compensation

In operating mode, ST7570 needs to be synchronized with an external signal period through zero crossing detection.

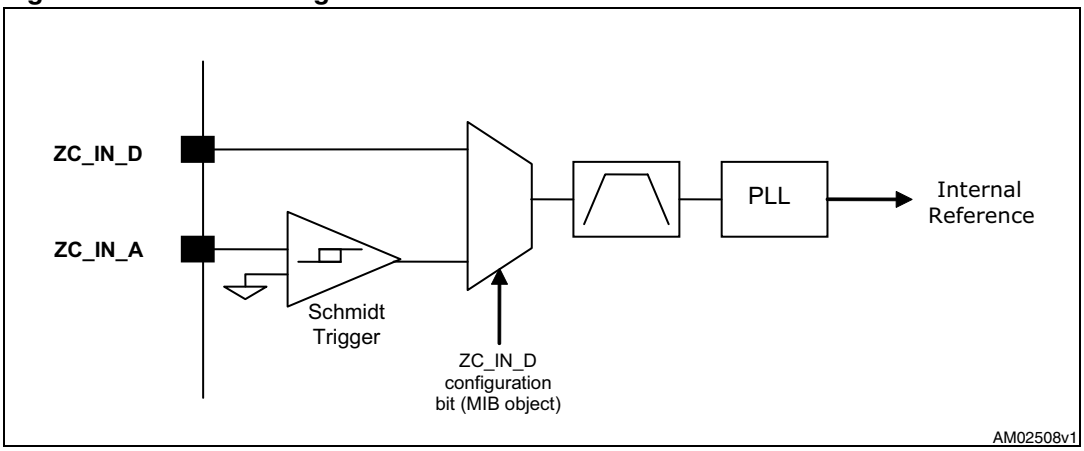
The user can select among two input pins for the external zero-crossing reference:

- Analog input (ZC_IN_A): it requires a bipolar analog input signal which is internally squared through a Schmidt Trigger comparator with symmetrical thresholds;
- Digital input (ZC_IN_D): it requires a 50% duty-cycle square-wave digital signal (with two levels).

The desired input can be selected by accessing a dedicated management information base (MIB) object.

The ST7570 embeds a phase-locked loop (PLL) to generate the internal reference based on the external zero-crossing. In case of delay due to external zero crossing coupling circuits (i.e. based on optocouplers) or to improve interoperability, it is possible to introduce delay compensation through a dedicated MIB object.

Figure 8. Zero crossing detection



6 Power management

Figure 9 shows the power supply structure for the ST7570 device. The ST7570 operates from two external supply voltages:

- VCC (8 to 18 V) for the power amplifier and the analog section;
- VDDIO (3.3 or 5 V) for interface lines and digital blocks.

Two internal linear regulators provide the remaining required voltages:

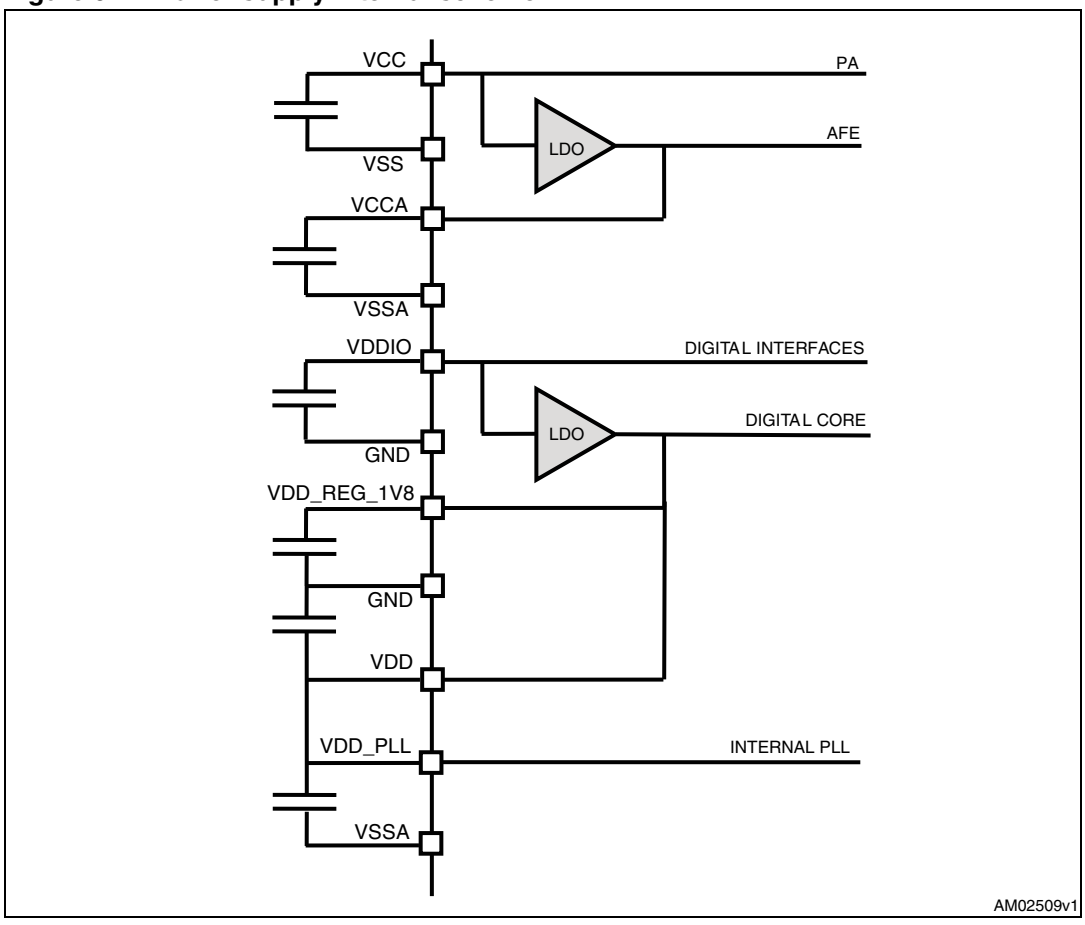
- 5 V analog front end supply: generated from the VCC voltage and connected to the VCCA pin;
- 1.8 V digital core supply: generated from the VDDIO voltage and connected to VDD_REG_1V8 (direct regulator output) and VDD pins.

The VDD_PLL pin, supplying the internal clock PLL, must be externally connected to VDD.

All supply voltages must be properly filtered to their respective ground, using external capacitors close to each supply pin, in accordance to the supply scheme depicted in *Figure 9*.

Note that the internal regulators connected to VDD_REG_1V8 and to VCCA are not designed to supply external circuitry; their outputs are externally accessible for filtering purpose only.

Figure 9. Power supply internal scheme



7 Clock management

The main clock source is an 8 MHz crystal connected to the internal oscillator through XIN and XOUT pins. Both XIN and XOUT pins have a 32 pF integrated capacitor, in order to drive a crystal having a load capacitance of 16 pF with no additional components.

Alternatively, an 8 MHz external clock can be directly supplied to XIN pin, leaving XOUT floating.

A PLL internally connected to the output of the oscillator generates the f_{CLK_PHY}, required by the PHY processor block. f_{CLK_PHY} is then scaled down by two to obtain f_{CLK_PC}, required by the protocol controller.

8 Functional overview

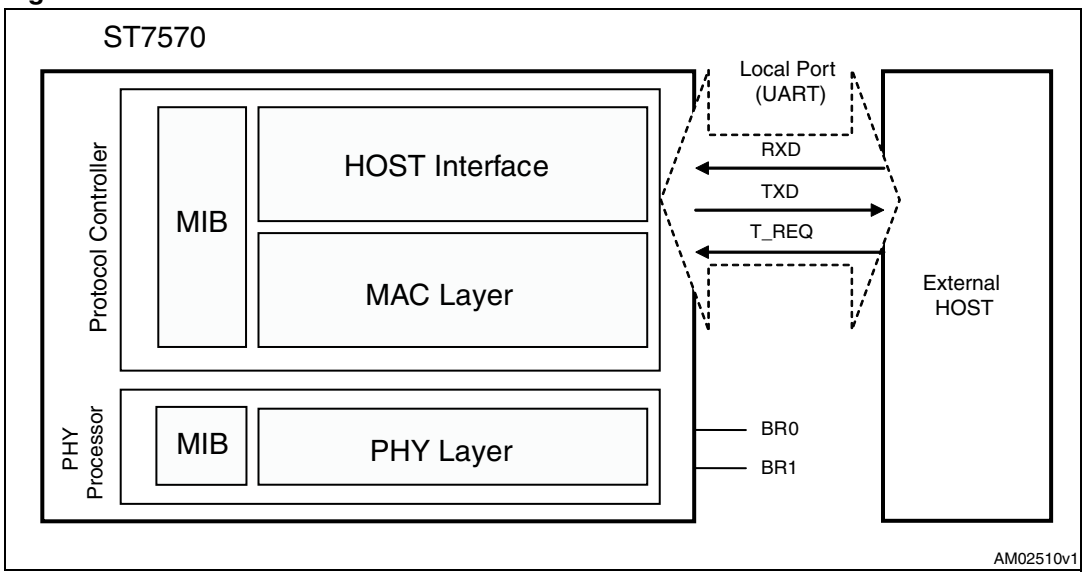
The ST7570 embeds complete physical (PHY) and a medium access control (MAC) protocol layers and services compliant with the open standard IEC61334-5-1, mainly developed for smart metering applications, but suitable also for other command and control applications and remote load management in CENELEC B and D bands.

A local port (UART) is available for communication with an external host, exporting all the functions and services required to configure and control the device and its protocol stack.

Below a list of the protocol layers and functions embedded in the ST7570 (*Figure 10*):

- Physical layer: implemented in the PHY processor and exporting all the primitive functions listed in the international standard document IEC61334-5-1, plus additional services for configuration, alarm management, signal and noise amplitude estimation, phase detection, statistical information;
- MAC layer: implemented on the protocol controller and exporting all the primitive functions listed in the international standard document IEC61334-5-1, Repeater Call and Intelligent search initiator process together with additional services.
- Management information base (MIB): an information database with all the data required for proper configuration of the system (at both PHY and MAC layer);
- Host interface: all the services of the PHY, MAC and MIB are exported to an external host through the local UART port.

Figure 10. Functional overview



8.1 References

Additional information regarding the PHY and MAC layers, the MIB and the HOST interface, including a detailed description of all services, extended functionalities and commands can be found in the following documents:

1. ST7570 user manual, www.st.com/powerline
2. International standard CEI-IEC-61334-5-1

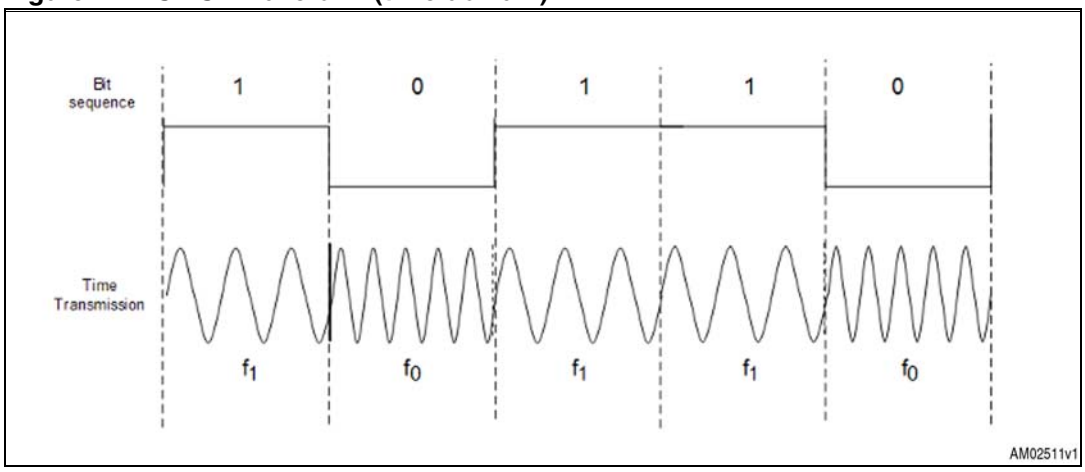
9 Physical layer

The ST7570 embeds a IEC-61334-5-1 PHY layer, which is based on the S-FSK (spread FSK) modulation technique.

9.1 S-FSK principles

The S-FSK modulation technique is aimed at strengthening the classical FSK by adding higher robustness against narrow-band interferers typical of a spread-spectrum approach. Non-return-to-zero (NRZ) coding is used to map the binary data “0” or “1” to sinusoidal carriers at frequencies f_0 and f_1 (*Figure 11*).

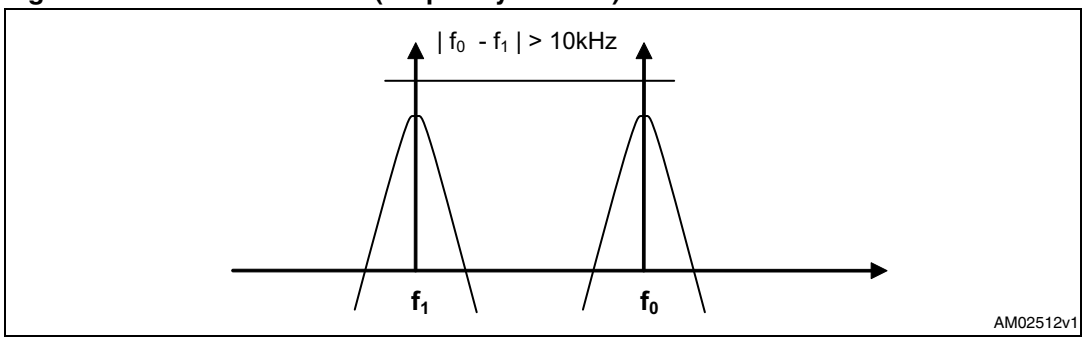
Figure 11. S-FSK waveform (time domain)



The absolute frequency deviation $|f_0 - f_1|$ is at least 10 kHz, in order to reduce the probability that a narrow-band interferer could corrupt both carriers at the same time.

f_0 and f_1 can be set at any value in CENELEC bands A, B, D.

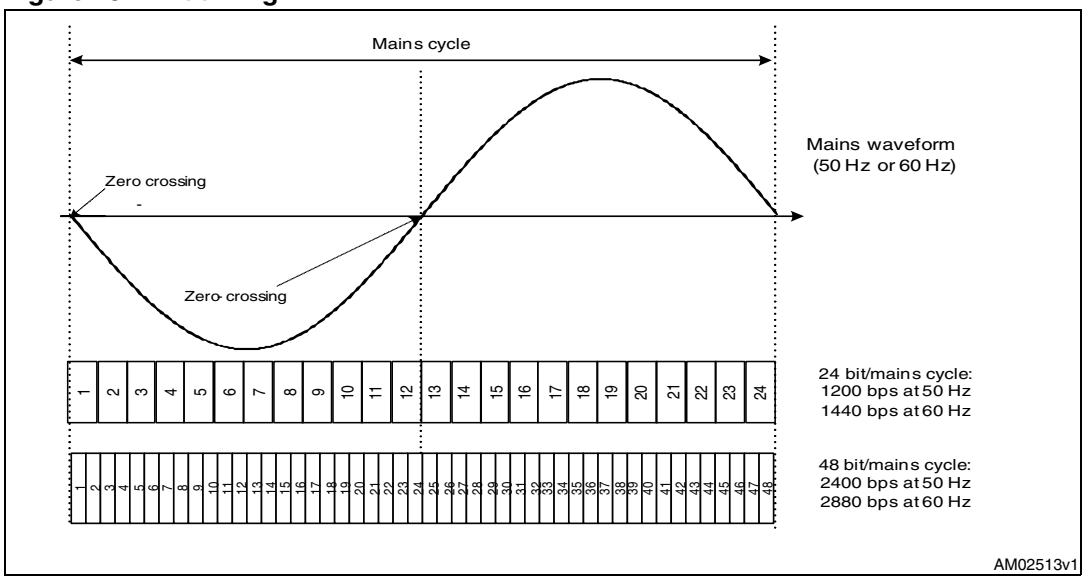
Figure 12. S-FSK waveform (frequency domain)



9.2 Bit timing

The data communication is synchronized to the mains zero-crossing through an internal PLL. The bit time is dynamically adapted in order to have always 24 or 48 bits in each mains cycle, according to the desired configuration (*Figure 13*). The resulting bit-rate is thus dependent on the instantaneous mains frequency. With a nominal frequency of 50 Hz, the resulting bit-rate is 1200 bps in the case of 24 bit/mains cycle, while 2400 bps in the case of 48 bit/mains cycle.

Figure 13. Bit timing



9.3 Frame structure at physical level

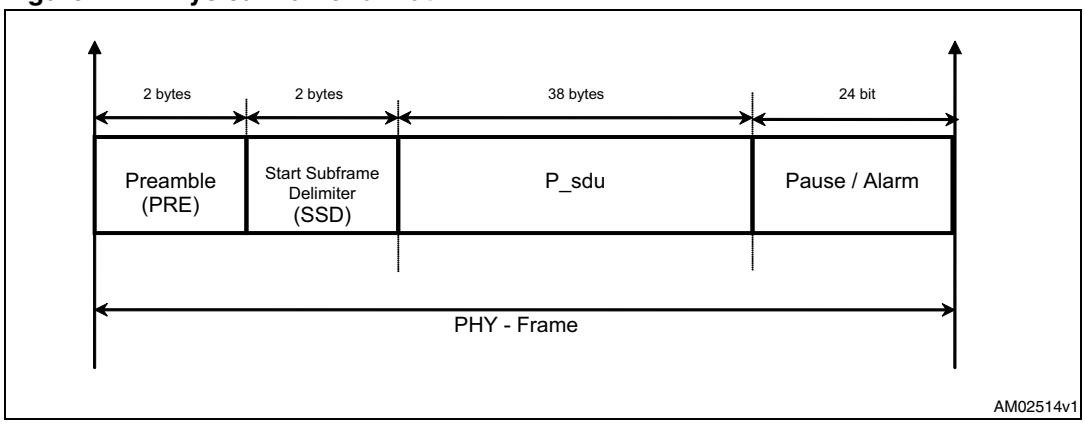
The frame at physical level is compliant with the IEC61334-5-1 and is composed of 45 bytes (360 bits) as follows:

- 2 byte preamble (PRE) (AAAAh);
- 2 byte start subframe delimiter (SSD) (54C7h);
- 38 byte physical service data unit (P_sdu);
- 3 byte for pause or alarm;

The bytes are sent from the most significant byte (MSB) to the least significant byte (LSB).

Bits within the byte are packed with the same order (msb to lsb).

Figure 14. Physical frame format



9.4 Frame timing and time-slot synchronization

The IEC61334-5-1 protocol specifies a master-slave network with time-division medium access: in order to properly communicate, all the nodes belonging to a network must share the same “slot synchronization”.

The time division is fixed through the use of time-slots, corresponding to a physical frame length of 45 bytes (i.e. 360 bits) with a total duration equal to:

- 15 mains cycles, at the 1200 bps operating speed (at 50 Hz);
- 7.5 mains cycles, at the 2400 bps operating speed (at 50 Hz).

The slot synchronization is first achieved by the master (i.e. ST7570 modem in 'Client' mode) setting the time-slot starting at the mains zero-crossing instant. The frames transmitted by the master will enable the slot synchronization of all other slave nodes (i.e. ST7570 working in 'Server' mode): the reception of the sequence composed by PRE and SSD will allow all the 'Server' nodes aligning their time-slots to the Client's time-slot.

10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

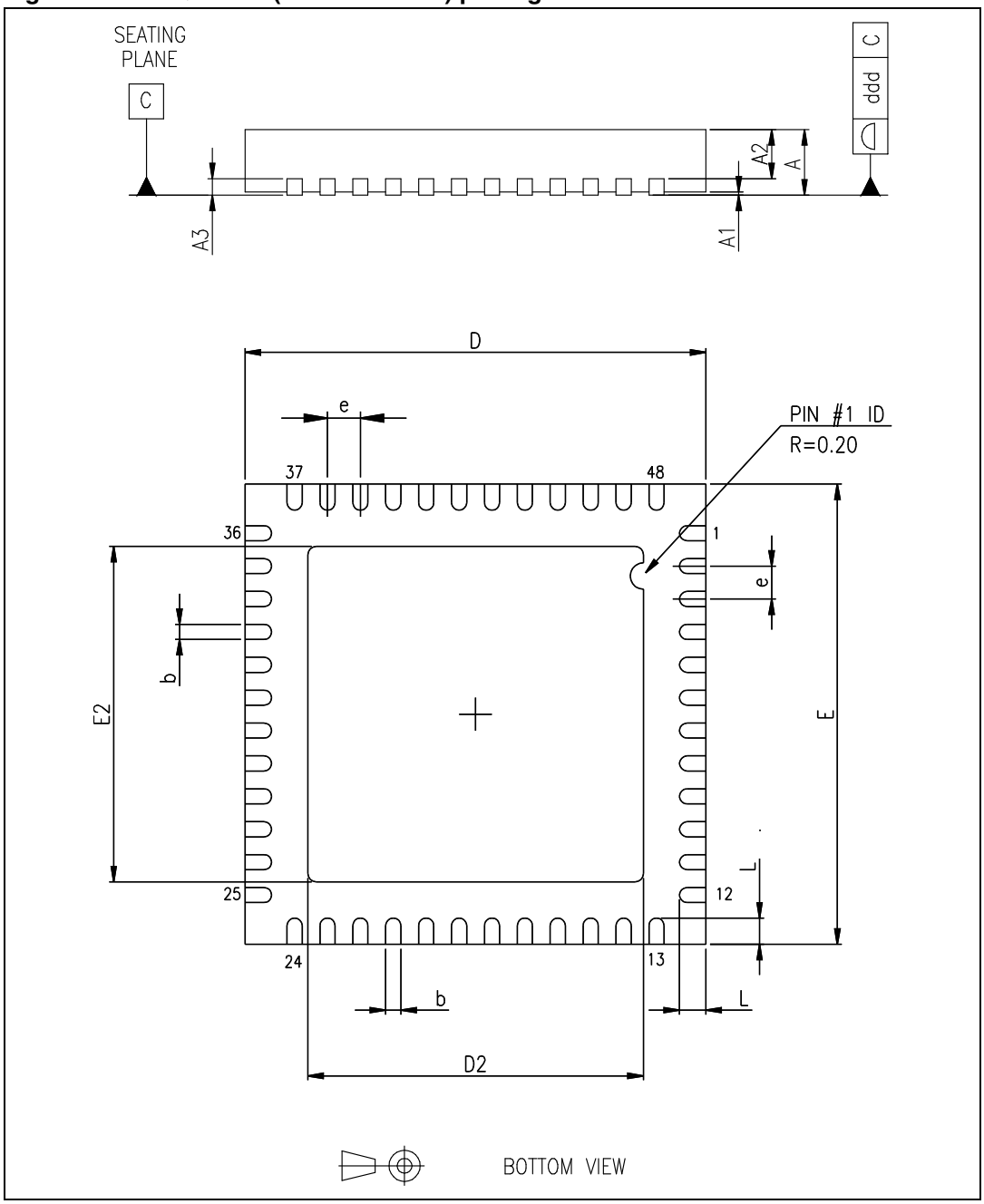
The ST7570 is hosted in a 48 pin thermally enhanced very thin fine pitch quad flat package no lead (VFQFPN) with exposed pad, which allows the device dissipating the heat that is generated by the operation of the two linear regulators and the power amplifier.

A mechanical drawing of the VFQFPN48 package is included in *Figure 15*.

Table 9. VFQFPN48 (7 x 7 x 1.0 mm) package mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	4.95	5.10	5.25
E	6.85	7.00	7.15
E2	4.95	5.10	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd		0.08	

Figure 15. VFQFPN48 (7 x 7 x 1.0 mm) package outline



11 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-May-2010	1	Initial release.
24-Sep-2012	2	Added specifications about ErDF Linky requirements in features introduction in the coverpage and functional specifications in *Chapter 8* . Updated pinout in *Table 2*, Electrical values in *Table 5*.

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