

ABSOLUTE MAXIMUM RATINGS (all voltages referenced to GND = 0 V)

Parameter	Limit	Unit
Input Voltage, V_{IN}	- 0.3 to 6	V
LX Voltage	- 0.3 to $V_{OUT} + 0.5$	
Output Voltage, V_{OUT}	- 0.3 to 6	
XSHD Voltage	- 0.3 to $V_{IN} + 0.5$	
FB Voltage	- 0.3 to 6	
Maximum Junction Temperature	150	°C
Storage Temperature	- 55 to 150	
Operating Junction Temperature	125	
Power Dissipation ^a	PowerPAK MLP33-6 ($T_A = 70\text{ °C}$) ^a	mW
Thermal Resistance ^b	PowerPAK MLP33-6	°C/W

Notes:

a. Derate 20 mW/°C above 70 °C.

b. Device mounted with all leads soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (all voltages referenced to GND = 0 V)

Parameter	Limit	Unit
Input Voltage, V_{IN}	0.85 to 5.0	V
Output Voltage, V_{OUT}	2.0 to 5	
XSHD Voltage	0 to V_{IN}	
LX Voltage	0 to $V_{OUT} + 0.5$	
FB Voltage	0 to 5 V_{OUT}	
Operating Temperature Range	- 40 to 85	°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified $V_{IN} = 1.2\text{ V}$, $V_{OUT} = V_{nom}$ ^e , $T_A = 25\text{ °C}$	Temp. ^a	Limits			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Minimum Start-Up Voltage	V_{START}	$I_{LOAD} = 1\text{ mA}$	Full		0.65	0.85	V
Minimum Operating Voltage ^d	V_{HOLD}	XSHD = V_{IN}			0.55		
UVLO	V_{UVLO}	Rising V_{OUT}	Full		1.8	2	
UVLO Hysteresis	$V_{UVLOHYST}$		Full		0.100		
FB Voltage Accuracy	V_{FB}			- 1.5		+ 1.5	%
			- 25 to 85 °C	- 3.0		+ 3.0	
			Full	- 3.5		+ 3.5	
Feedback Input Current	I_{FB}	$V_{FB} = 0.6\text{ V}$			1		nA
Maximum PWM Duty Cycle	MAXDTY		Full	80	87		%
PWM Switching Frequency	f_{OSC}		Full	225	300	375	kHz



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Parameter	Symbol	Test Conditions Unless Specified $V_{IN} = 1.2\text{ V}$, $V_{OUT} = V_{nom}^e$, $T_A = 25\text{ }^\circ\text{C}$	Temp. ^a	Limits			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Supply Current 1	OUT	$V_{OUT} = V_{nom} \times 0.95$			330	450	μA
Supply Current 2		$V_{OUT} = V_{nom} + 0.5\text{ V}$, $V_{LX} > V_{IN}$			134		
Supply Current 3		$V_{OUT} = V_{nom} + 0.5\text{ V}$, $V_{LX} < V_{IN}$			44		
Stand-By Current	I_{STB}	XSHD = 0 V, not including switch leakage	Full			1	
NMOS Switch Leakage	I_{LEAK}	$LX = 5\text{ V}$	Full		1	2	Ω
NMOS Switch On Resistance	$R_{DS(on)}$	$V_{OUT} = 3.3\text{ V}$			0.2		
PWM to PFM Current Threshold	I_{WTOF}				3		mA
PFM to PWM Current Threshold	I_{FTOF}				22		
XSHD Input High Level	V_{XSHDH}	$0.8\text{ V} \leq V_{IN} \leq 0.9\text{ V}$	Full	0.55			V
		$0.9\text{ V} < V_{IN} \leq 2\text{ V}$	Full	0.8			
		$2\text{ V} < V_{IN} \leq 5\text{ V}$	Full	1.2			
XSHD Input Low Level	V_{XSHDL}		Full			0.2	
Softstart Time	t_{START}	$V_{IN} = 1.8\text{ V}$			1.6		ms
Over Voltage Threshold	V_{OV}				110		%
Over Voltage Hysteresis	V_{OVHYST}				10		
Thermal Shutdown	T_{SHD}				160		$^\circ\text{C}$
Thermal Shutdown Hysteresis	T_{HYST}				20		

Notes:

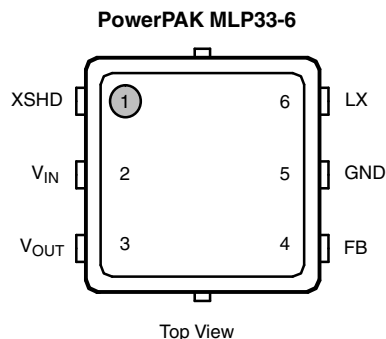
a. Full = - 40 °C to 85 °C.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (- 40 °C to 85 °C).

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. Minimum operating voltage is determined by the battery's capability to provide energy as it is deeply discharged.

e. V_{nom} equals programmed output voltage.

PIN CONFIGURATION AND TRUTH TABLE**ORDERING INFORMATION**

Part Number	Temperature Range	Marking
SiP12503DMP-T1-E3	- 40 °C to 85 °C	2503

PIN DESCRIPTION

Pin Number	Name	Function
1	XSDH	Logic controlled shutdown Input, XSHD = high: normal operation, XSHD = low: shutdown
2	V _{IN}	Input voltage
3	V _{OUT}	Output of the boost converter and power source for the IC-battery
4	FB	Output voltage feedback pin
5	GND	Signal and power ground
6	LX	Switch pin

PIN FUNCTIONS**XSHD (Pin 1)**

XSHD is a logic-level shutdown control pin. When XSHD is low, the IC's switching is disabled, and an antiringing switch is connected between LX and V_{IN}. When XSHD is high, the IC is working in normal operation.

V_{IN} (Pin 2)

V_{IN} is the pin connected to battery input voltage. At start-up, SiP12503 is powered from the voltage at the V_{IN} pin. Once V_{OUT} exceeds V_{IN}, the SiP12503 is powered from V_{OUT}. This increases the drive to the gate of the internal power switch, to allow higher maximum output currents and higher converter efficiency.

V_{OUT} (Pin 3)

V_{OUT} is the output of the boost converter and also the power source for the IC.

FB (Pin 4)

FB is the output voltage feedback pin via an external resistor divider. The feedback voltage is nominally 0.6 V.

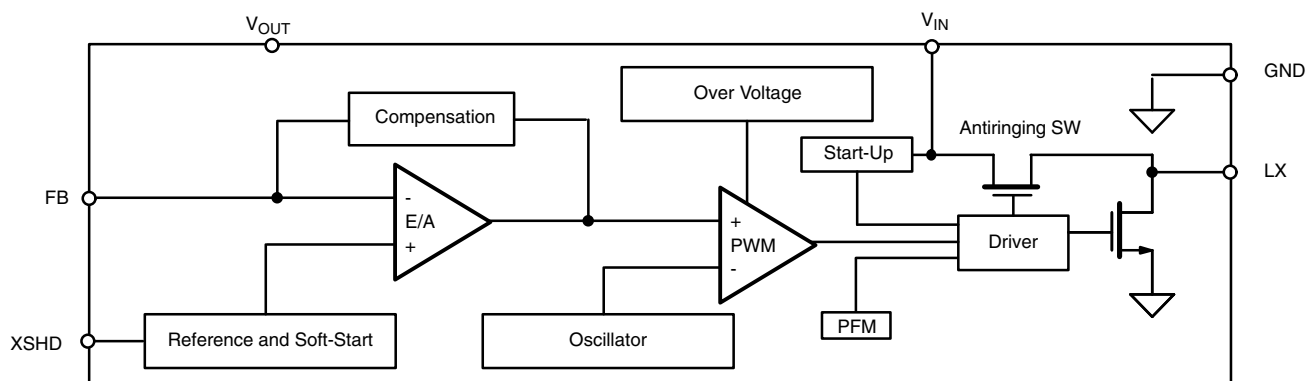
GND (Pin 5)

GND is the ground pin for signal and power ground.

LX (Pin 6)

LX connects to the drain of the internal power MOSFET (boost switch). Externally, the LX pin should be connected to the boost inductor and Schottky diode. If the inductor current falls to zero, or XSHD is low, an internal antiringing switch is short from LX to V_{IN} to minimize EMI.

FUNCTIONAL BLOCK DIAGRAM



DETAILED OPERATION

SiP12503 is a 300 kHz boost converter IC, packaged in 6 pin MLP33 PowerPAK™ package. With start-up from input voltages as low as 0.65 V, this device features fixed frequency voltage mode PWM control with internal frequency compensation. With its low $R_{DS(on)}$ internal power MOSFET, this device maintains high efficiency over a wide range of load current. Under light load conditions, it switches to in PFM mode to maintain high efficiency. A FB pin is available to adjust the output voltage.

Low Voltage Start-Up

SiP12503 is designed to start-up at input voltage of typically 0.65 V. At start-up, V_{OUT} is lower than V_{IN} due to the voltage drop of the Schottky diode. Therefore, the device uses V_{IN} as the power source for its control logic and internal gate drive, until V_{OUT} exceeds V_{IN} . During the start-up interval, the boost switch's conduction interval during each cycle is determined by the time taken for the inductor current to reach internal current limit, followed by a fixed off time before the switch is allowed to turn on again. Once V_{OUT} exceeds V_{IN} , the device uses V_{OUT} as the IC's power source. When V_{OUT} exceeds 1.89 V, the device engages its built-in soft-start circuitry.

Soft-Start

During soft-start, the loop compensation guarantees the slow increase of output voltage, so that no large voltage overshoot or inrush current transients occur when the soft-start period ends.

PWM operation

After the soft-start interval is over, the device works in PWM operation with a fixed frequency of 300 kHz, with automatic switch-over to PFM operation during light load conditions.

PFM Operation

When operating into light loads, the SiP12502 automatically switches to PFM operation. This reduces gate charge losses in the boost switch, hence raising converter efficiency.

Over Voltage Protection

If the output voltage is above 10 % of the regulation voltage, the device will turn off the internal power MOSFET and wait until the output voltage falls below the regulation voltage, then the PWM operation is enabled again.

Thermal Shutdown Protection

If the internal device temperature rises above 160 °C, the device will turn off the internal power MOSFET. Once the die temperature falls below 140 °C, then the device performs a new soft-start cycle, and the converter resumes normal operation.

Antiringing Control

The antiringing control circuitry prevents high frequency ringing at the LX pin as the inductor current goes to zero by damping the resonant circuit formed by L and C_{LX} (capacitance on LX pin). When the IC is shutdown, this antiringing switch is also turned on.

APPLICATION INFORMATION

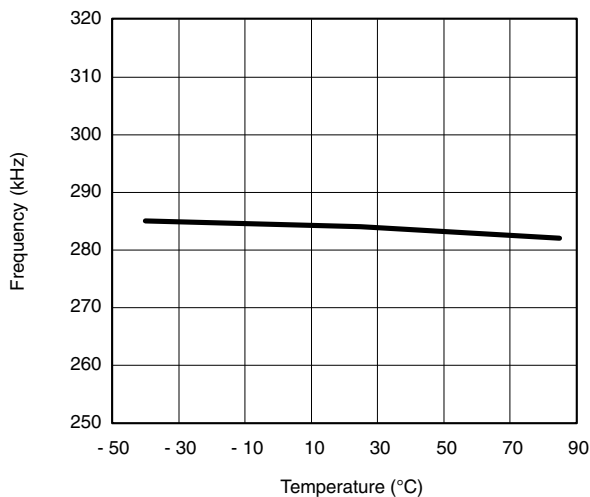
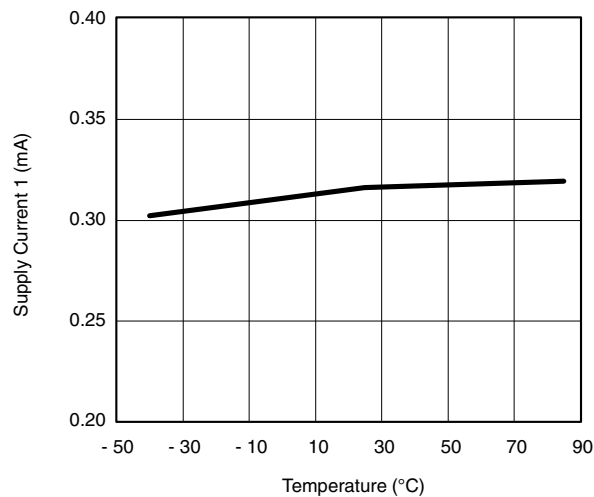
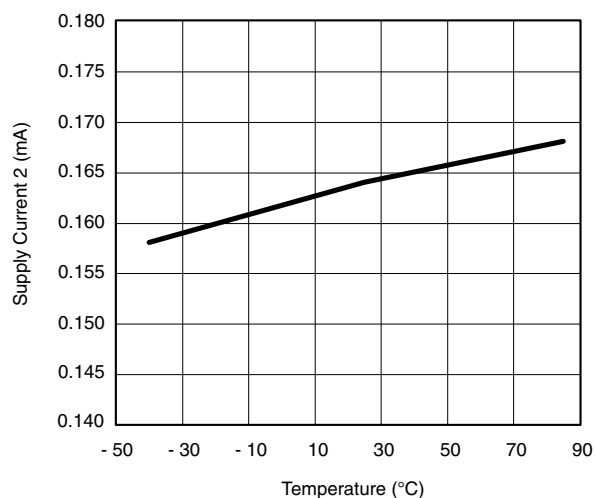
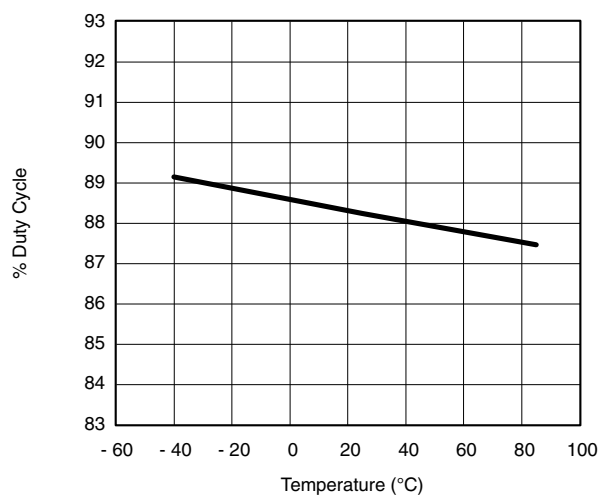
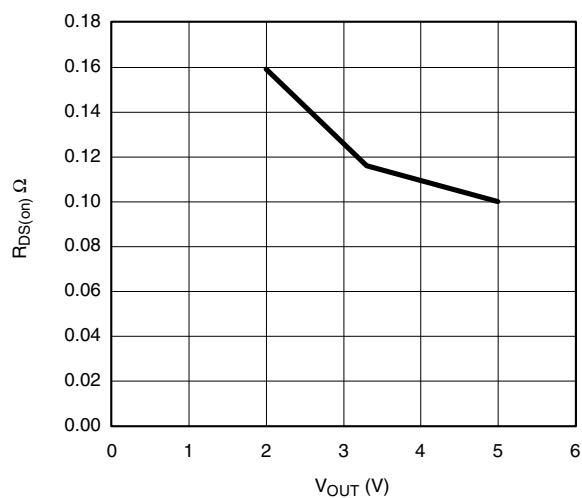
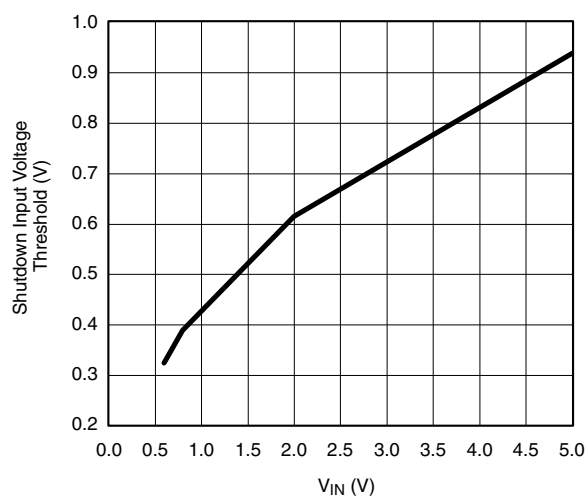
Setting the Adjustable Output Voltage

The SiP12503 regulated output can be adjusted from 1.8 V to 5.0 V via a resistor divider network from V_{OUT} to GND . $R1$ and $R2$ should be kept in the 50 k Ω to 100 k Ω range for low power consumption while maintaining adequate noise immunity. The value of $R1$ is calculated using the following formula:

$$R1 = R2 * [(V_{OUT}/V_{FB}) - 1]$$

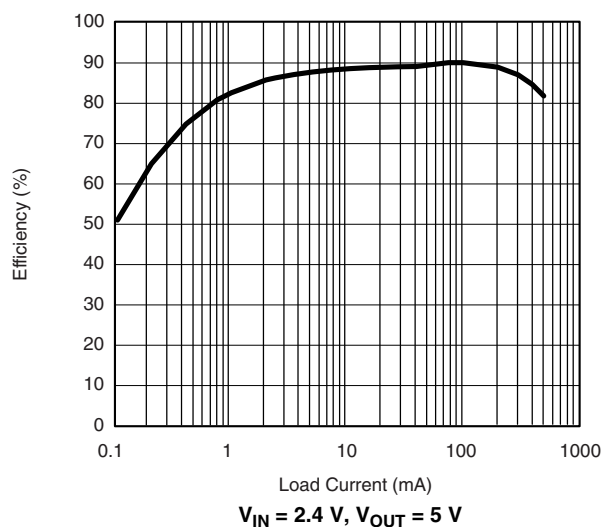
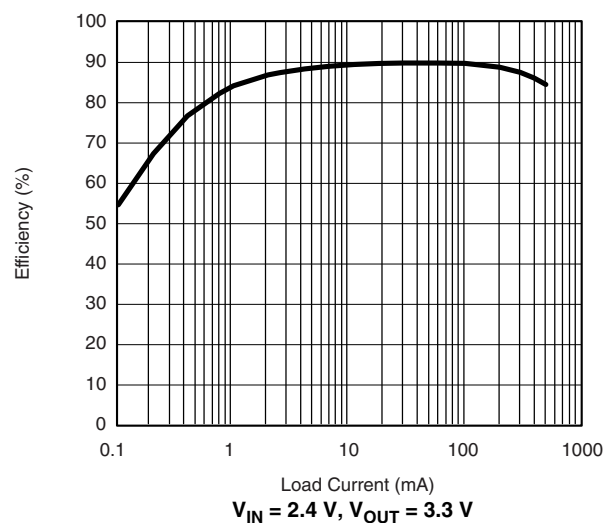
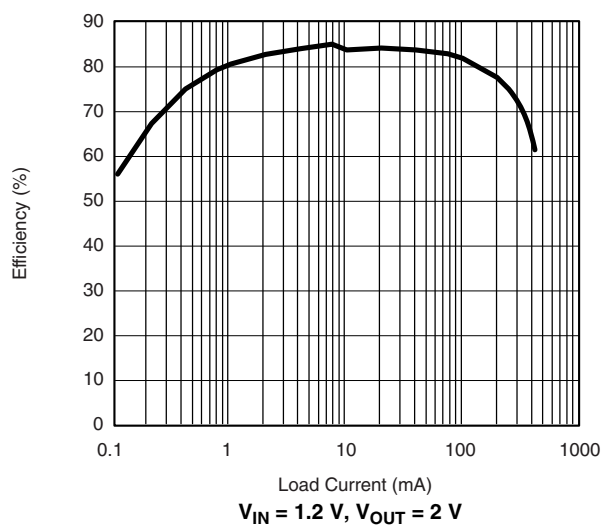
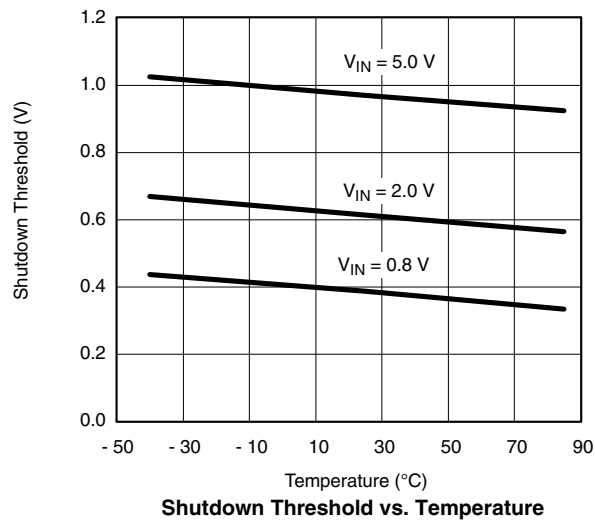
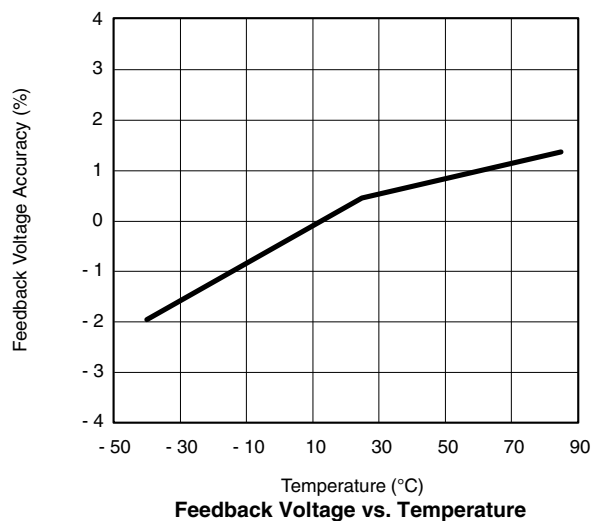
$$V_{FB} = 0.6 \text{ V}$$

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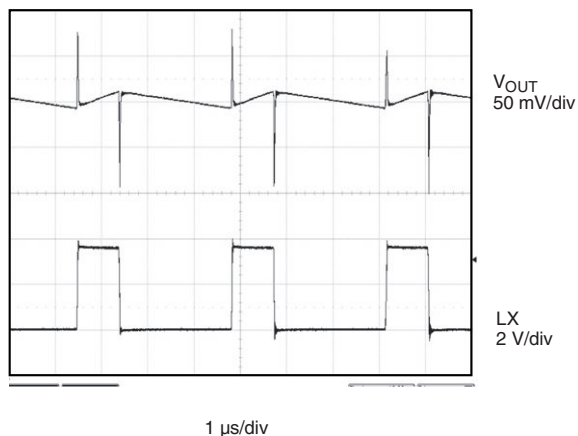
TYPICAL CHARACTERISTICS**Frequency vs. Temperature****Supply Current 1 vs Temperature****Supply Current 2 vs. Temperature****Maximum PWM Duty Cycle vs. Temperature** **$R_{DS(on)}$ vs. Output Voltage****Shutdown Input Voltage Threshold vs. V_{IN}**



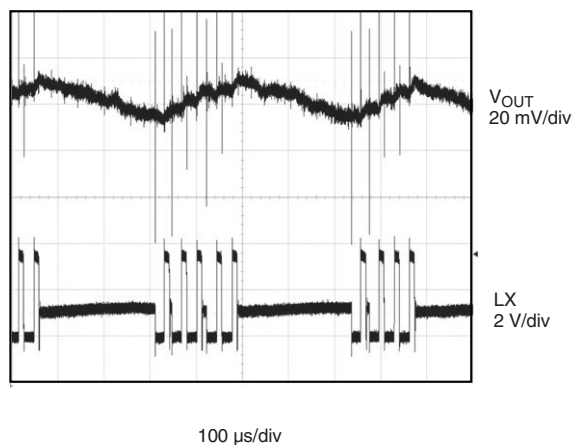
TYPICAL CHARACTERISTICS



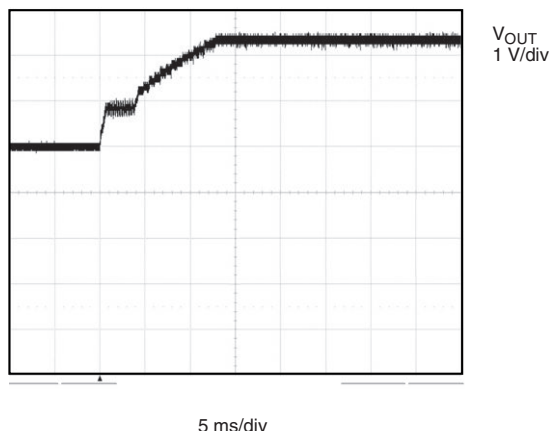
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TYPICAL WAVEFORMS**Typical Switching Waveform PWM Mode**

$V_{IN} = 1.2$ V, $V_{OUT} = 3.3$ V, Load Current = 150 mA,
 $L = 10$ μ H; $C_{OUT} = 47$ μ F

**Typical Switching Waveform PFM Mode**

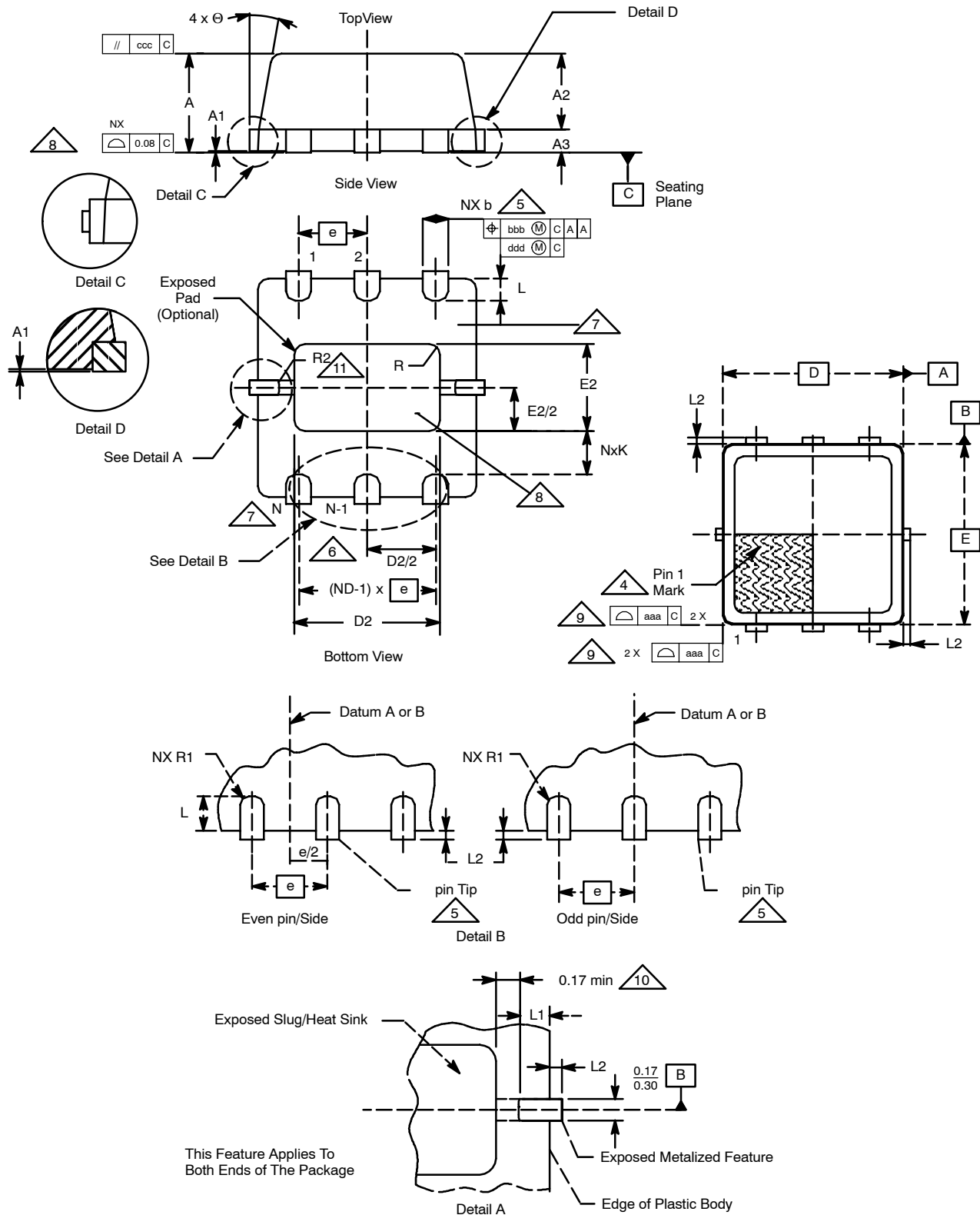
$V_{IN} = 1.2$ V, $V_{OUT} = 3.3$ V, Load Current = 10 mA,
 $L = 10$ μ H; $C_{OUT} = 47$ μ F

**Soft Start**

$V_{IN} = 1.2$ V, $V_{OUT} = 3.3$ V, Load Current = 50 mA,
 $L = 10$ μ H; $C_{OUT} = 47$ μ F

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73579.

PowerPAK® MLP33-6, 8 and 10 (POWER IC ONLY)





PowerPAK® MLP33-6, 8, 10

N = 6 PITCH: 0.95 mm
N = 8 PITCH: 0.65 mm
N = 10 PITCH: 0.50 mm

Dim	MILLIMETERS*				INCHES				Notes
	Basic	Min	Nom	Max	Basic	Min	Nom	Max	
A	–	0.80	0.90	1.00	–	0.031	0.035	0.039	1, 2
A1	–	0.00	0.025	0.05	–	0.000	0.001	0.002	1, 2
A2	–	0.65	0.70	0.75	–	0.026	0.028	0.030	1, 2
A3	–	0.15	0.20	0.25	–	0.006	0.008	0.010	1, 2
aaa	–	–	0.10	–	–	–	0.004	–	1, 2
b-6	–	0.33	0.35	0.43	–	0.013	0.014	0.017	1, 2, 8
b-8	–	0.285	0.305	0.385	–	0.011	0.012	0.015	1, 2, 8
b-10	–	0.18	0.20	0.28	–	0.007	0.008	0.011	1, 2, 8
bbb	–	–	0.10	–	–	–	0.004	–	1, 2
ccc	–	–	0.10	–	–	–	0.004	–	1, 2
D	3.00	–	–	–	0.118	–	–	–	1, 2, 8
D2	–	1.92	2.02	2.12	–	0.076	0.080	0.083	1, 2, 8
ddd	–	–	0.05	–	–	–	0.002	–	1, 2
E	3.00	–	–	–	0.118	–	–	–	1, 2, 8
E2	–	1.10	1.20	1.30	–	0.043	0.047	0.051	1, 2, 8
e-6	–	–	0.95	–	–	–	0.037	–	1, 2
e-8	–	–	0.65	–	–	–	0.026	–	1, 2
e-10	–	–	0.50	–	–	–	0.020	–	1, 2
K	–	0.20	–	–	–	0.008	–	–	5, 11
L	–	0.20	0.29	0.45	–	0.008	0.011	0.018	1, 2, 8
L1-6	–	0.16	0.24	0.40	–	0.006	0.009	0.016	1, 2, 8
L1-8	–	0.16	0.24	0.40	–	0.006	0.009	0.016	1, 2, 8
L1-10	–	–	–	–	–	–	–	–	1, 2, 8
L2	–	–	–	0.125	–	–	–	0.005	5, 11
R Ref	–	–	0.15	–	–	–	0.006	–	1, 2, 8
R1 Ref-6	–	–	0.127	–	–	–	0.005	–	1, 2, 8
R1 Ref-8	–	–	0.15	–	–	–	0.006	–	1, 2, 8
R1 Ref-10	–	–	0.075	–	–	–	0.003	–	1, 2, 8
Θ	–	0°	10°	12°	–	0°	10°	12°	1, 2

* Use millimeters as the primary measurement.

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 DWG: 5925

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angles are in degrees.
3. N is the total number of pins.

4. The pin #1 identifier and pin numbering convention shall conform to JESD 95-1 SPP-012. Details of pin #1 identifier is located within the zone indicated. The pin #1 identifier is marked.
5. Dimension b applies to metallized pin and is measured between 0.15 mm and 0.20 mm from the pin tip.
6. ND refers to the maximum number of pins on the D side.
7. Depopulation of pins is allowed and will be called out on the individual variation.
8. Coplanarity applies to the exposed heat sink slug as well as the pins.
9. Profile tolerance (aaa) will be applicable only to the plastic body and not to the metallized features (such as the pin tips and tie bars.) Metallized features may protrude a maximum of L2 from the plastic body profile.
10. L1 max is not called out, the metallized feature will extend to the exposed pad. Thus, the 0.17-mm gap does not apply.
11. The corner will be sharp unless otherwise specified with radius dimensions.



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