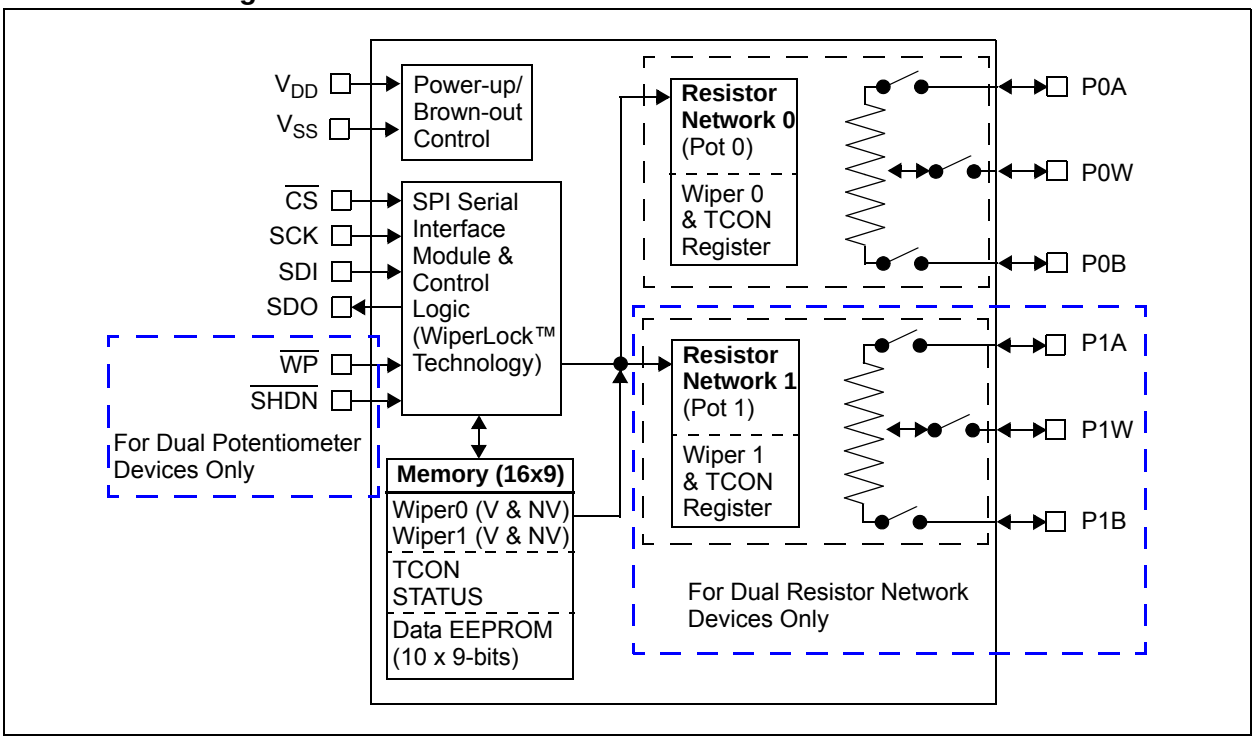
## Device Block Diagram




## Device Features

| Device | # of POTs | Wiper Configuration | Control Interface | Memory Type | WiperLock Technology | POR Wiper Setting | Resistance (typical) | | # of Steps | $V_{DD}$ Operating Range (2) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | $R_{AB}$ Options (kΩ) | Wiper - $R_W$ (Ω) | | |
| MCP4131 (3) | 1 | Potentiometer (1) | SPI | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 1.8V to 5.5V |
| MCP4132 (3) | 1 | Rheostat | SPI | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 1.8V to 5.5V |
| MCP4141 | 1 | Potentiometer (1) | SPI | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 2.7V to 5.5V |
| MCP4142 | 1 | Rheostat | SPI | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 2.7V to 5.5V |
| MCP4151 (3) | 1 | Potentiometer (1) | SPI | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 1.8V to 5.5V |
| MCP4152 (3) | 1 | Rheostat | SPI | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 1.8V to 5.5V |
| MCP4161 | 1 | Potentiometer (1) | SPI | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 2.7V to 5.5V |
| MCP4162 | 1 | Rheostat | SPI | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 2.7V to 5.5V |
| MCP4231 (3) | 2 | Potentiometer (1) | SPI | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 1.8V to 5.5V |
| MCP4232 (3) | 2 | Rheostat | SPI | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 1.8V to 5.5V |
| MCP4241 | 2 | Potentiometer (1) | SPI | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 2.7V to 5.5V |
| MCP4242 | 2 | Rheostat | SPI | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 129 | 2.7V to 5.5V |
| MCP4251 (3) | 2 | Potentiometer (1) | SPI | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 1.8V to 5.5V |
| MCP4252 (3) | 2 | Rheostat | SPI | RAM | No | Mid-Scale | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 1.8V to 5.5V |
| MCP4261 | 2 | Potentiometer (1) | SPI | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 2.7V to 5.5V |
| MCP4262 | 2 | Rheostat | SPI | EE | Yes | NV Wiper | 5.0, 10.0, 50.0, 100.0 | 75 | 257 | 2.7V to 5.5V |

**Note 1:** Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).

**2:** Analog characteristics only tested from 2.7V to 5.5V unless otherwise noted.

**3:** Please check Microchip web site for device release and availability

# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.6V to +7.0V
Voltage on $\overline{CS}$, SCK, SDI, SDI/SDO, $\overline{WP}$, and $\overline{SHDN}$ with respect to $V_{SS}$ ..... -0.6V to 12.5V
Voltage on all other pins (PxA, PxW, PxB, and SDO) with respect to $V_{SS}$ ..... -0.3V to $V_{DD}$ + 0.3V
Input clamp current, $I_{IK}$
($V_I$ < 0, $V_I$ > $V_{DD}$, $V_I$ > $V_{PP}$ ON HV pins) .....±20 mA
Output clamp current, $I_{OK}$
($V_O$ < 0 or $V_O$ > $V_{DD}$) .....±20 mA
Maximum output current sunk by any Output pin .....25 mA
Maximum output current sourced by any Output pin .....25 mA
Maximum current out of $V_{SS}$ pin .....100 mA
Maximum current into $V_{DD}$ pin .....100 mA
Maximum current into PxA, PxW & PxB pins .....±2.5 mA
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied .....-40°C to +125°C
Total power dissipation (**Note 1**) .....400 mW
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins .....≥ 4 kV (HBM), ..... ≥ 300V (MM)
Maximum Junction Temperature ($T_J$) ..... +150°C

**Note 1:** Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD}-V_{OH}) \times I_{OH}\} + \Sigma(V_{OI} \times I_{OL})$$

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## AC/DC CHARACTERISTICS

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| Supply Voltage | $V_{DD}$ | 2.7 | — | 5.5 | V | | |
| | | 1.8 | — | 2.7 | V | Serial Interface only. | |
| $\overline{CS}$, SDI, SDO, SCK, WP, SHDN pin Voltage Range | $V_{HV}$ | $V_{SS}$ | — | 12.5V | V | $V_{DD} \geq$ 4.5V | The $\overline{CS}$ pin will be at one of three input levels ($V_{IL}$, $V_{IH}$ or $V_{IHH}$). (**Note 6**) |
| | | $V_{SS}$ | — | $V_{DD}$ + 8.0V | V | $V_{DD}$ < 4.5V | |
| VDD Start Voltage to ensure Wiper Reset | $V_{BOR}$ | — | — | 1.65 | V | RAM retention voltage ($V_{RAM}$) < $V_{BOR}$ | |
| VDD Rise Rate to ensure Power-on Reset | $V_{DDRR}$ | (**Note 9**) | | | V/ms | | |
| Delay after device exits the reset state ($V_{DD}$ > $V_{BOR}$) | $T_{BORD}$ | — | 10 | 20 | µs | | |
| Supply Current **(Note 10)** | $I_{DD}$ | — | — | 450 | µA | Serial Interface Active, $V_{DD}$ = 5.5V, $\overline{CS}$ = $V_{IL}$, SCK @ 5 MHz, write all 0's to volatile Wiper 0 (address 0h) | |
| | | — | — | 1 | mA | EE Write Current, $V_{DD}$ = 5.5V, $\overline{CS}$ = $V_{IL}$, SCK @ 5 MHz, write all 0's to non-volatile Wiper 0 (address 2h) | |
| | | — | 2.5 | 5 | µA | Serial Interface Inactive, $\overline{CS}$ = $V_{IH}$, $V_{DD}$ = 5.5V | |
| | | — | 0.55 | 1 | mA | Serial Interface Active, $V_{DD}$ = 5.5V, $\overline{CS}$ = $V_{IHH}$, SCK @ 5 MHz, decrement non-volatile Wiper 0 (address 2h) | |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP4XX1** only.

**4:** **MCP4XX2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| Resistance (± 20%) | $R_{AB}$ | 4.0 | 5 | 6.0 | kΩ | -502 devices **(Note 1)** | |
| | | 8.0 | 10 | 12.0 | kΩ | -103 devices **(Note 1)** | |
| | | 40.0 | 50 | 60.0 | kΩ | -503 devices **(Note 1)** | |
| | | 80.0 | 100 | 120.0 | kΩ | -104 devices **(Note 1)** | |
| Resolution | N | 257 | | | Taps | 8-bit | No Missing Codes |
| | | 129 | | | Taps | 7-bit | No Missing Codes |
| Step Resistance | $R_S$ | — | $R_{AB}$ / (256) | — | Ω | 8-bit | **Note 6** |
| | | — | $R_{AB}$ / (128) | — | Ω | 7-bit | **Note 6** |
| Nominal Resistance Match | $\lvert R_{AB0} - R_{AB1} \rvert / R_{AB}$ | — | 0.2 | 1.25 | % | **MCP42X1** devices only | |
| | $\lvert R_{BW0} - R_{BW1} \rvert / R_{BW}$ | — | 0.25 | 1.5 | % | **MCP42X2** devices only, Code = Full-Scale | |
| Wiper Resistance (**Note 3, Note 4**) | $R_W$ | — | 75 | 160 | Ω | $V_{DD}$ = 5.5 V, $I_W$ = 2.0 mA, code = 00h | |
| | | — | 75 | 300 | Ω | $V_{DD}$ = 2.7 V, $I_W$ = 2.0 mA, code = 00h | |
| Nominal Resistance Tempco | $\Delta R_{AB}/\Delta T$ | — | 50 | — | ppm/°C | $T_A$ = -20°C to +70°C | |
| | | — | 100 | — | ppm/°C | $T_A$ = -40°C to +85°C | |
| | | — | 150 | — | ppm/°C | $T_A$ = -40°C to +125°C | |
| Ratiometeric Tempco | $\Delta V_{WB}/\Delta T$ | — | 15 | — | ppm/°C | Code = Midscale (80h or 40h) | |
| Resistor Terminal Input Voltage Range (Terminals A, B and W) | $V_A, V_W, V_B$ | Vss | — | $V_{DD}$ | V | **Note 5, Note 6** | |
| Maximum current through A, W or B | $I_W$ | — | — | 2.5 | mA | **Note 6**, Worst case current through wiper when wiper is either Full-Scale or Zero Scale. | |
| Leakage current into A, W or B | $I_{WL}$ | — | 100 | — | nA | **MCP4XX1** PxA = PxW = PxB = $V_{SS}$ | |
| | | — | 100 | — | nA | **MCP4XX2** PxB = PxW = $V_{SS}$ | |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP4XX1** only.

**4:** **MCP4XX2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | | |
| Full-Scale Error (**MCP4XX1** only) (8-bit code = 100h, 7-bit code = 80h) | $V_{WFSE}$ | -6.0 | -0.1 | — | LSb | 5 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -4.0 | -0.1 | — | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -3.5 | -0.1 | — | LSb | 10 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -2.0 | -0.1 | — | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -0.8 | -0.1 | — | LSb | 50 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -0.5 | -0.1 | — | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -0.5 | -0.1 | — | LSb | 100 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | -0.5 | -0.1 | — | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| Zero-Scale Error (**MCP4XX1** only) (8-bit code = 00h, 7-bit code = 00h) | $V_{WZSE}$ | — | +0.1 | +6.0 | LSb | 5 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +3.0 | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +3.5 | LSb | 10 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +2.0 | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +0.8 | LSb | 50 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +0.5 | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +0.5 | LSb | 100 kΩ | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| | | — | +0.1 | +0.5 | LSb | | 7-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V |
| Potentiometer Integral Non-linearity | INL | -1 | ±0.5 | +1 | LSb | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V **MCP4XX1** devices only **(Note 2)** | |
| | | -0.5 | ±0.25 | +0.5 | LSb | 7-bit | | |
| Potentiometer Differential Non-linearity | DNL | -0.5 | ±0.25 | +0.5 | LSb | 8-bit | 3.0V ≤ $V_{DD}$ ≤ 5.5V **MCP4XX1** devices only **(Note 2)** | |
| | | -0.25 | ±0.125 | +0.25 | LSb | 7-bit | | |
| Bandwidth -3 dB (See Figure 2-58, load = 30 pF) | BW | — | 2 | — | MHz | 5 kΩ | 8-bit | Code = 80h |
| | | — | 2 | — | MHz | | 7-bit | Code = 40h |
| | | — | 1 | — | MHz | 10 kΩ | 8-bit | Code = 80h |
| | | — | 1 | — | MHz | | 7-bit | Code = 40h |
| | | — | 200 | — | kHz | 50 kΩ | 8-bit | Code = 80h |
| | | — | 200 | — | kHz | | 7-bit | Code = 40h |
| | | — | 100 | — | kHz | 100 kΩ | 8-bit | Code = 80h |
| | | — | 100 | — | kHz | | 7-bit | Code = 40h |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP4XX1** only.

**4:** **MCP4XX2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | | |
| Rheostat Integral Non-linearity **MCP41X1** (**Note 4, Note 8**) **MCP4XX2** devices only **(Note 4)** | R-INL | -1.5 | ±0.5 | +1.5 | LSb | 5 kΩ | 8-bit | 5.5V, $I_W$ = 900 µA |
| | | -8.25 | +4.5 | +8.25 | LSb | | | 3.0V, $I_W$ = 480 µA (**Note 7**) |
| | | -1.125 | ±0.5 | +1.125 | LSb | | 7-bit | 5.5V, $I_W$ = 900 µA |
| | | -6.0 | +4.5 | +6.0 | LSb | | | 3.0V, $I_W$ = 480 µA (**Note 7**) |
| | | -1.5 | ±0.5 | +1.5 | LSb | 10 kΩ | 8-bit | 5.5V, $I_W$ = 450 µA |
| | | -5.5 | +2.5 | +5.5 | LSb | | | 3.0V, $I_W$ = 240 µA (**Note 7**) |
| | | -1.125 | ±0.5 | +1.125 | LSb | | 7-bit | 5.5V, $I_W$ = 450 µA |
| | | -4.0 | +2.5 | +4.0 | LSb | | | 3.0V, $I_W$ = 240 µA (**Note 7**) |
| | | -1.5 | ±0.5 | +1.5 | LSb | 50 kΩ | 8-bit | 5.5V, $I_W$ = 90 µA |
| | | -2.0 | +1 | +2.0 | LSb | | | 3.0V, $I_W$ = 48 µA (**Note 7**) |
| | | -1.125 | ±0.5 | +1.125 | LSb | | 7-bit | 5.5V, $I_W$ = 90 µA |
| | | -1.5 | +1 | +1.5 | LSb | | | 3.0V, $I_W$ = 48 µA (**Note 7**) |
| | | -1.0 | ±0.5 | +1.0 | LSb | 100 kΩ | 8-bit | 5.5V, $I_W$ = 45 µA |
| | | -1.5 | +0.25 | +1.5 | LSb | | | 3.0V, $I_W$ = 24 µA (**Note 7**) |
| | | -0.8 | ±0.5 | +0.8 | LSb | | 7-bit | 5.5V, $I_W$ = 45 µA |
| | | -1.125 | +0.25 | +1.125 | LSb | | | 3.0V, $I_W$ = 24 µA (**Note 7**) |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP4XX1** only.

**4:** **MCP4XX2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | | |
| Rheostat Differential Non-linearity **MCP41X1** (**Note 4, Note 8**) **MCP4XX2** devices only **(Note 4)** | R-DNL | -0.5 | ±0.25 | +0.5 | LSb | 5 kΩ | 8-bit | 5.5V, $I_W$ = 900 µA |
| | | -1.0 | +0.5 | +1.0 | LSb | | | 3.0V (**Note 7**) |
| | | -0.375 | ±0.25 | +0.375 | LSb | | 7-bit | 5.5V, $I_W$ = 900 µA |
| | | -0.75 | +0.5 | +0.75 | LSb | | | 3.0V (**Note 7**) |
| | | -0.5 | ±0.25 | +0.5 | LSb | 10 kΩ | 8-bit | 5.5V, $I_W$ = 450 µA |
| | | -1.0 | +0.25 | +1.0 | LSb | | | 3.0V (**Note 7**) |
| | | -0.375 | ±0.25 | +0.375 | LSb | | 7-bit | 5.5V, $I_W$ = 450 µA |
| | | -0.75 | +0.5 | +0.75 | LSb | | | 3.0V (**Note 7**) |
| | | -0.5 | ±0.25 | +0.5 | LSb | 50 kΩ | 8-bit | 5.5V, $I_W$ = 90 µA |
| | | -0.5 | ±0.25 | +0.5 | LSb | | | 3.0V (**Note 7**) |
| | | -0.375 | ±0.25 | +0.375 | LSb | | 7-bit | 5.5V, $I_W$ = 90 µA |
| | | -0.375 | ±0.25 | +0.375 | LSb | | | 3.0V (**Note 7**) |
| | | -0.5 | ±0.25 | +0.5 | LSb | 100 kΩ | 8-bit | 5.5V, $I_W$ = 45 µA |
| | | -0.5 | ±0.25 | +0.5 | LSb | | | 3.0V (**Note 7**) |
| | | -0.375 | ±0.25 | +0.375 | LSb | | 7-bit | 5.5V, $I_W$ = 45 µA |
| | | -0.375 | ±0.25 | +0.375 | LSb | | | 3.0V (**Note 7**) |
| Capacitance ($P_A$) | $C_{AW}$ | — | 75 | — | pF | f =1 MHz, Code = Full-Scale | | |
| Capacitance ($P_w$) | $C_W$ | — | 120 | — | pF | f =1 MHz, Code = Full-Scale | | |
| Capacitance ($P_B$) | $C_{BW}$ | — | 75 | — | pF | f =1 MHz, Code = Full-Scale | | |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP4XX1** only.

**4:** **MCP4XX2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Digital Inputs/Outputs (CS, SDI, SDO, SCK, WP, SHDN)** | | | | | | |
| Schmitt Trigger High Input Threshold | $V_{IH}$ | 0.45 $V_{DD}$ | — | — | V | 2.7V ≤ $V_{DD}$ ≤ 5.5V (Allows 2.7V Digital $V_{DD}$ with 5V Analog $V_{DD}$) |
| | | 0.5 $V_{DD}$ | — | — | V | 1.8V ≤ $V_{DD}$ ≤ 2.7V |
| Schmitt Trigger Low Input Threshold | $V_{IL}$ | — | — | 0.2$V_{DD}$ | V | |
| Hysteresis of Schmitt Trigger Inputs | $V_{HYS}$ | — | 0.1$V_{DD}$ | — | V | |
| High Voltage Input Entry Voltage | $V_{IHH}$ | 8.5 | — | 12.5 (6) | V | Threshold for WiperLock™ Technology |
| High Voltage Input Exit Voltage | $V_{IHH}$ | — | — | $V_{DD}$ + 0.8V (6) | V | |
| High Voltage Limit | $V_{MAX}$ | — | — | 12.5 (6) | V | Pin can tolerate $V_{MAX}$ or less. |
| Output Low Voltage (SDO) | $V_{OL}$ | $V_{SS}$ | — | 0.3$V_{DD}$ | V | $I_{OL}$ = 5 mA, $V_{DD}$ = 5.5V |
| | | $V_{SS}$ | — | 0.3$V_{DD}$ | V | $I_{OL}$ = 1 mA, $V_{DD}$ = 1.8V |
| Output High Voltage (SDO) | $V_{OH}$ | 0.7$V_{DD}$ | — | $V_{DD}$ | V | $I_{OH}$ = -2.5 mA, $V_{DD}$ = 5.5V |
| | | 0.7$V_{DD}$ | — | $V_{DD}$ | V | $I_{OL}$ = -1 mA, $V_{DD}$ = 1.8V |
| Weak Pull-up / Pull-down Current | $I_{PU}$ | — | — | 1.75 | mA | Internal $V_{DD}$ pull-up, $V_{IHH}$ pull-down, $V_{DD}$ = 5.5V, $V_{\overline{CS}}$ = 12.5V |
| | | — | 170 | — | µA | $\overline{CS}$ pin, $V_{DD}$ = 5.5V, $V_{\overline{CS}}$ = 3V |
| $\overline{CS}$ Pull-up / Pull-down Resistance | $R_{CS}$ | — | 16 | — | kΩ | $V_{DD}$ = 5.5V, $V_{\overline{CS}}$ = 3V |
| Input Leakage Current | $I_{IL}$ | -1 | — | 1 | µA | $V_{IN}$ = $V_{DD}$ and $V_{IN}$ = $V_{SS}$ |
| Pin Capacitance | $C_{IN}$, $C_{OUT}$ | — | 10 | — | pF | $f_C$ = 20 MHz |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP4XX1** only.

**4:** **MCP4XX2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network

## AC/DC CHARACTERISTICS (CONTINUED)

| DC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ $T_A$ ≤ +125°C (extended)<br>All parameters apply across the specified operating ranges unless noted.<br>$V_{DD}$ = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.<br>Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| **RAM (Wiper) Value** | | | | | | | |
| Value Range | N | 0h | — | 1FFh | hex | 8-bit device | |
| | | 0h | — | 1FFh | hex | 7-bit device | |
| **EEPROM** | | | | | | | |
| Endurance | $E_{ndurance}$ | — | 1M | — | Cycles | | |
| EEPROM Range | N | 0h | — | 1FFh | hex | | |
| Initial Factory Setting | N | 80h | | | hex | 8-bit | WiperLock Technology = Off |
| | | 40h | | | hex | 7-bit | WiperLock Technology = Off |
| EEPROM Programming Write Cycle Time | $t_{WC}$ | — | 5 | 10 | ms | | |
| **Power Requirements** | | | | | | | |
| Power Supply Sensitivity (**MCP41X2** and **MCP42X2** only) | PSS | — | 0.0015 | 0.0035 | %/% | 8-bit | $V_{DD}$ = 2.7V to 5.5V, $V_A$ = 2.7V, Code = 80h |
| | | — | 0.0015 | 0.0035 | %/% | 7-bit | $V_{DD}$ = 2.7V to 5.5V, $V_A$ = 2.7V, Code = 40h |

**Note 1:** Resistance is defined as the resistance between terminal A to terminal B.

**2:** INL and DNL are measured at $V_W$ with $V_A$ = $V_{DD}$ and $V_B$ = $V_{SS}$.

**3:** **MCP4XX1** only.

**4:** **MCP4XX2** only, includes $V_{WZSE}$ and $V_{WFSE}$.

**5:** Resistor terminals A, W and B's polarity with respect to each other is not restricted.

**6:** This specification by design.

**7:** Non-linearity is affected by wiper resistance ($R_W$), which changes significantly over voltage and temperature.

**8:** The **MCP4XX1** is externally connected to match the configurations of the **MCP41X2** and **MCP42X2**, and then tested.

**9:** POR/BOR is not rate dependent.

**10:** Supply current is independent of current through the resistor network

## 1.1 SPI Mode Timing Waveforms and Requirements

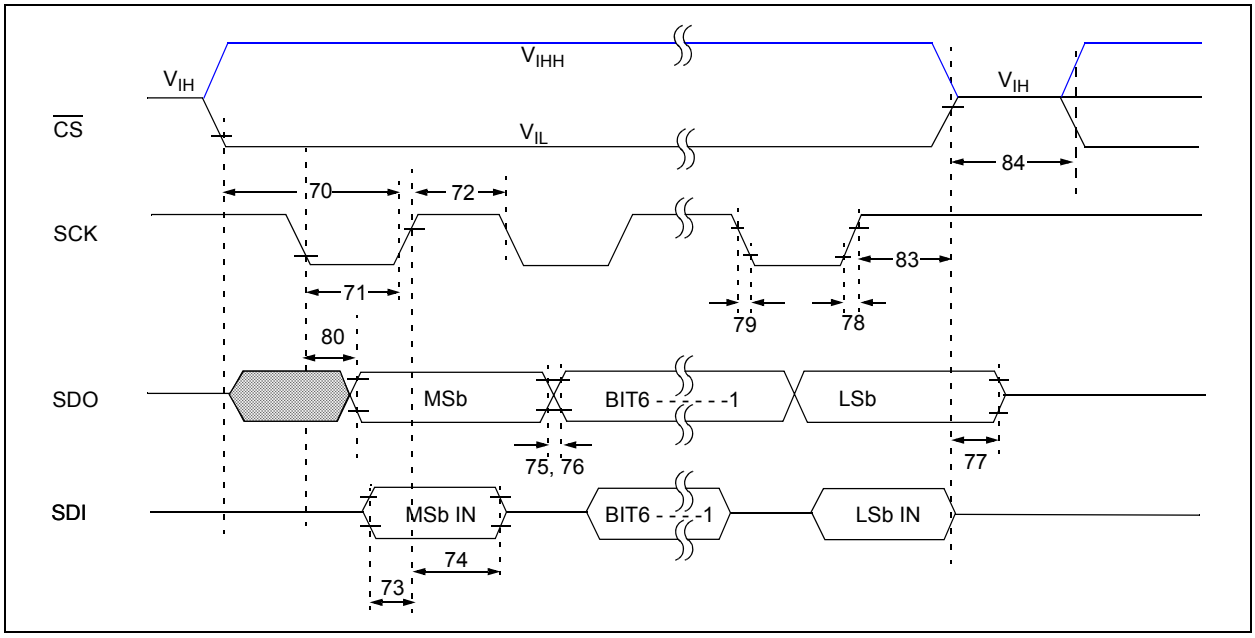



***FIGURE 1-1:*** *SPI Timing Waveform (Mode = 11).*

**TABLE 1-1: SPI REQUIREMENTS (MODE = 11)**

| # | Characteristic | Symbol | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| | SCK Input Frequency | $F_{SCK}$ | — | 10 | MHz | $V_{DD}$ = 2.7V to 5.5V |
| | | | — | 1 | MHz | $V_{DD}$ = 1.8V to 2.7V |
| 70 | $\overline{CS}$ Active ($V_{IL}$ or $V_{IHH}$) to SCK↑ input | TcsA2scH | 60 | — | ns | |
| 71 | SCK input high time | TscH | 45 | — | ns | $V_{DD}$ = 2.7V to 5.5V |
| | | | 500 | — | ns | $V_{DD}$ = 1.8V to 2.7V |
| 72 | SCK input low time | TscL | 45 | — | ns | $V_{DD}$ = 2.7V to 5.5V |
| | | | 500 | — | ns | $V_{DD}$ = 1.8V to 2.7V |
| 73 | Setup time of SDI input to SCK↑ edge | TDIV2scH | 10 | — | ns | |
| 74 | Hold time of SDI input from SCK↑ edge | TscH2DIL | 20 | — | ns | |
| 77 | $\overline{CS}$ Inactive ($V_{IH}$) to SDO output hi-impedance | TcsH2DOZ | — | 50 | ns | **Note 1** |
| 80 | SDO data output valid after SCK↓ edge | TscL2DOV | — | 70 | ns | $V_{DD}$ = 2.7V to 5.5V |
| | | | | 170 | ns | $V_{DD}$ = 1.8V to 2.7V |
| 83 | $\overline{CS}$ Inactive ($V_{IH}$) after SCK↑ edge | TscH2csI | 100 | — | ns | $V_{DD}$ = 2.7V to 5.5V |
| | | | 1 | | ms | $V_{DD}$ = 1.8V to 2.7V |
| 84 | Hold time of $\overline{CS}$ Inactive ($V_{IH}$) to $\overline{CS}$ Active ($V_{IL}$ or $V_{IHH}$) | TcsA2csI | 50 | — | ns | |

**Note 1:** This specification by design.

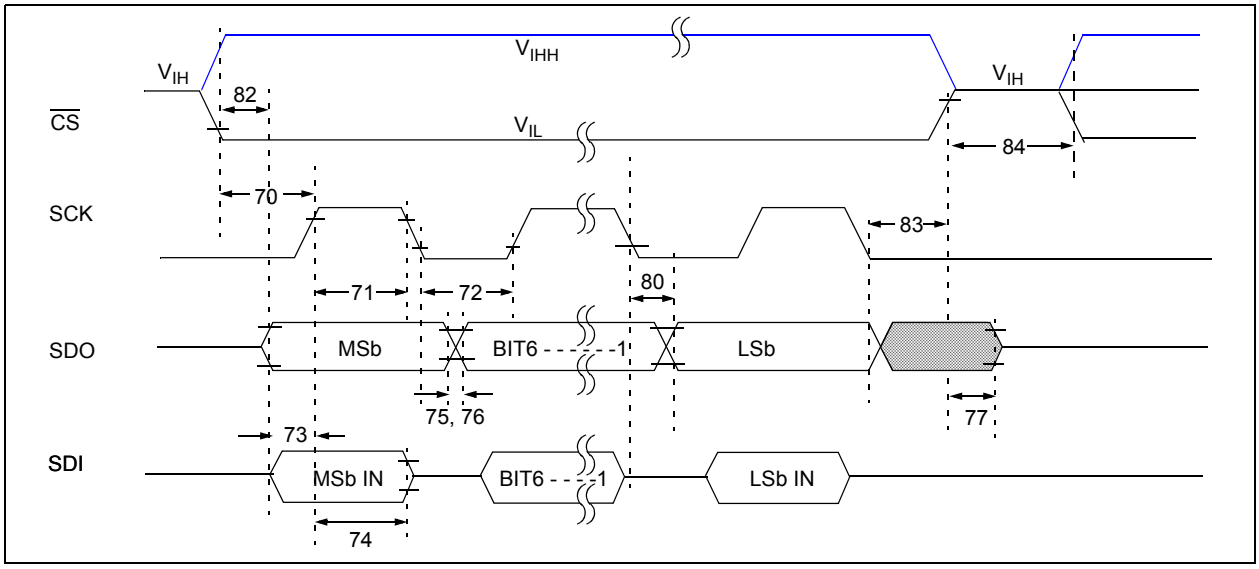



***FIGURE 1-2:*** *SPI Timing Waveform (Mode = 00).*

**TABLE 1-2: SPI REQUIREMENTS (MODE = 00)**

| # | Characteristic | Symbol | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| | SCK Input Frequency | $F_{SCK}$ | — | 10 | MHz | $V_{DD}$ = 2.7V to 5.5V |
| | | | — | 1 | MHz | $V_{DD}$ = 1.8V to 2.7V |
| 70 | $\overline{CS}$ Active ($V_{IL}$ or $V_{IHH}$) to SCK↑ input | TcsA2scH | 60 | — | ns | |
| 71 | SCK input high time | TscH | 45 | — | ns | $V_{DD}$ = 2.7V to 5.5V |
| | | | 500 | — | ns | $V_{DD}$ = 1.8V to 2.7V |
| 72 | SCK input low time | TscL | 45 | — | ns | $V_{DD}$ = 2.7V to 5.5V |
| | | | 500 | — | ns | $V_{DD}$ = 1.8V to 2.7V |
| 73 | Setup time of SDI input to SCK↑ edge | TDIV2scH | 10 | — | ns | |
| 74 | Hold time of SDI input from SCK↑ edge | TscH2DIL | 20 | — | ns | |
| 77 | $\overline{CS}$ Inactive ($V_{IH}$) to SDO output hi-impedance | TcsH2DOZ | — | 50 | ns | **Note 1** |
| 80 | SDO data output valid after SCK↓ edge | TscL2DOV | — | 70 | ns | $V_{DD}$ = 2.7V to 5.5V |
| | | | | 170 | ns | $V_{DD}$ = 1.8V to 2.7V |
| 82 | SDO data output valid after $\overline{CS}$ Active ($V_{IL}$ or $V_{IHH}$) | TssL2doV | — | 70 | ns | |
| 83 | $\overline{CS}$ Inactive ($V_{IH}$) after SCK↓ edge | TscH2csI | 100 | — | ns | $V_{DD}$ = 2.7V to 5.5V |
| | | | 1 | | ms | $V_{DD}$ = 1.8V to 2.7V |
| 84 | Hold time of $\overline{CS}$ Inactive ($V_{IH}$) to $\overline{CS}$ Active ($V_{IL}$ or $V_{IHH}$) | TcsA2csI | 50 | — | ns | |

**Note 1:** This specification by design.

**TABLE 1-3: SPI REQUIREMENTS FOR SDI/SDO MULTIPLEXED (READ OPERATION ONLY) (2)**

| Characteristic | Symbol | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| SCK Input Frequency | $F_{SCK}$ | — | 250 | kHz | $V_{DD}$= 2.7V to 5.5V |
| $\overline{CS}$ Active ($V_{IL}$ or $V_{IHH}$) to SCK↑ input | TcsA2scH | 60 | — | ns | |
| SCK input high time | TscH | 1.8 | — | us | |
| SCK input low time | TscL | 1.8 | — | ns | |
| Setup time of SDI input to SCK↑ edge | TDIV2scH | 40 | — | ns | |
| Hold time of SDI input from SCK↑ edge | TscH2DIL | 40 | — | ns | |
| $\overline{CS}$ Inactive ($V_{IH}$) to SDO output hi-impedance | TcsH2DOZ | — | 50 | ns | **Note 1** |
| SDO data output valid after SCK↓ edge | TscL2DOV | — | 1.6 | us | |
| SDO data output valid after $\overline{CS}$ Active ($V_{IL}$ or $V_{IHH}$) | TssL2doV | — | 50 | ns | |
| $\overline{CS}$ Inactive ($V_{IH}$) after SCK↓ edge | TscH2csI | 100 | — | ns | |
| Hold time of $\overline{CS}$ Inactive ($V_{IH}$) to $\overline{CS}$ Active ($V_{II}$ or $V_{IHH}$) | TcsA2csI | 50 | — | ns | |

**Note 1:** This specification by design

**2:** This table is for the devices where the SPI's SDI and SDO pins are multiplexed (SDI/SDO) and a Read command is issued. This is NOT required for SDI/SDO operation with the Increment, Decrement, or Write commands. This data rate can be increased by having external pull-up resistors to increase the rising edges of each bit.

## TEMPERATURE CHARACTERISTICS

| **Electrical Specifications:** Unless otherwise indicated, $V_{DD}$ = +2.7V to +5.5V, $V_{SS}$ = GND. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 8L-MSOP | $\theta_{JA}$ | — | 211 | — | °C/W | |
| Thermal Resistance, 8L-PDIP | $\theta_{JA}$ | — | 89.3 | — | °C/W | |
| Thermal Resistance, 8L-SOIC | $\theta_{JA}$ | — | 149.5 | — | °C/W | |
| Thermal Resistance, 8L-DFN (3x3) | $\theta_{JA}$ | — | 60 | — | °C/W | |
| Thermal Resistance, 10L-DFN (3x3) | $\theta_{JA}$ | — | 57 | — | °C/W | |
| Thermal Resistance, 10L-MSOP | $\theta_{JA}$ | — | 202 | — | °C/W | |
| Thermal Resistance, 14L-PDIP | $\theta_{JA}$ | — | 70 | — | °C/W | |
| Thermal Resistance, 14L-SOIC | $\theta_{JA}$ | — | 95.3 | — | °C/W | |
| Thermal Resistance, 14L-TSSOP | $\theta_{JA}$ | — | 100 | — | °C/W | |
| Thermal Resistance, 16L-QFN | $\theta_{JA}$ | — | 43 | — | °C/W | |

## 2.0 TYPICAL PERFORMANCE CURVES

| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range. |
|---|---|

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

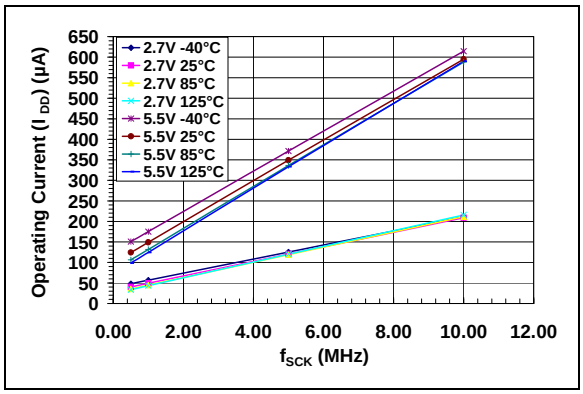



***FIGURE 2-1:*** *Device Current ($I_{DD}$) vs. SPI Frequency ($f_{SCK}$) and Ambient Temperature ($V_{DD}$ = 2.7V and 5.5V).*

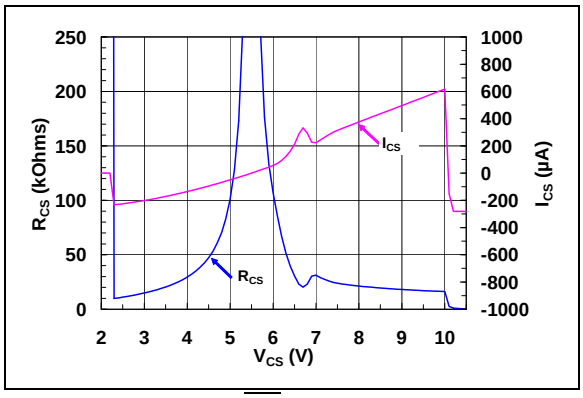



***FIGURE 2-4:*** *$\overline{CS}$ Pull-up/Pull-down Resistance ($R_{\overline{CS}}$) and Current ($I_{\overline{CS}}$) vs. $\overline{CS}$ Input Voltage ($V_{\overline{CS}}$) ($V_{DD}$ = 5.5V).*

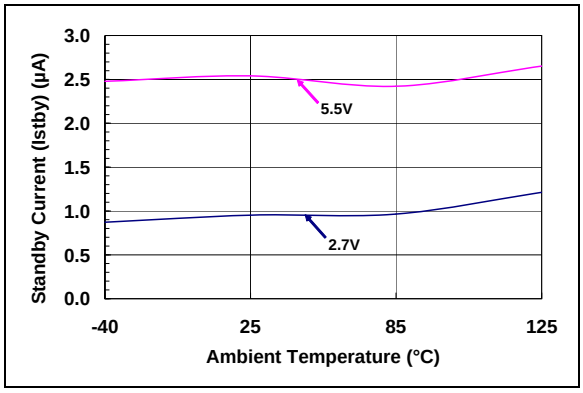



***FIGURE 2-2:*** *Device Current ($I_{SHDN}$) and $V_{DD}$. ($\overline{CS}$ = $V_{DD}$) vs. Ambient Temperature.*

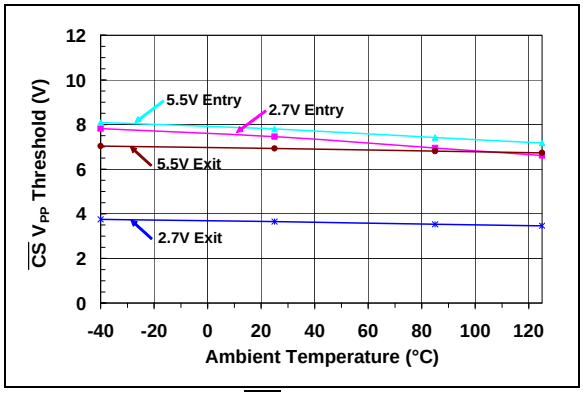



***FIGURE 2-5:*** *$\overline{CS}$ High Input Entry/Exit Threshold vs. Ambient Temperature and $V_{DD}$.*

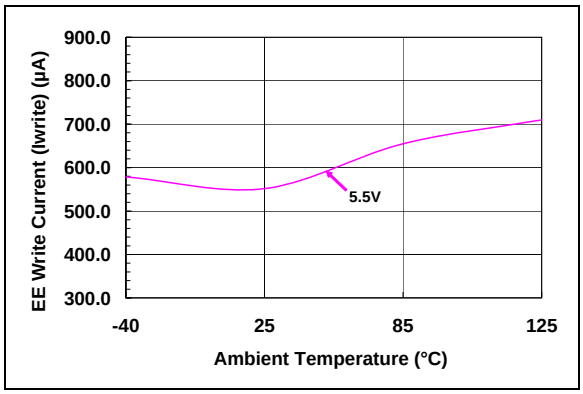



***FIGURE 2-3:*** *Write Current ($I_{WRITE}$) vs. Ambient Temperature and $V_{DD}$.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

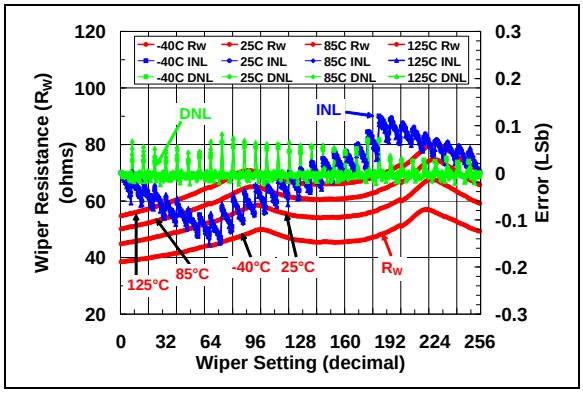



***FIGURE 2-6:*** *5 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

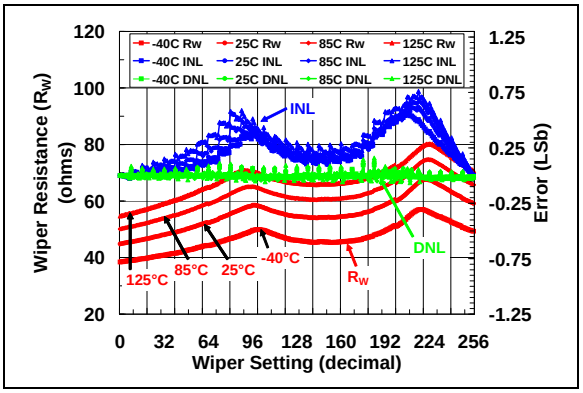



***FIGURE 2-9:*** *5 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

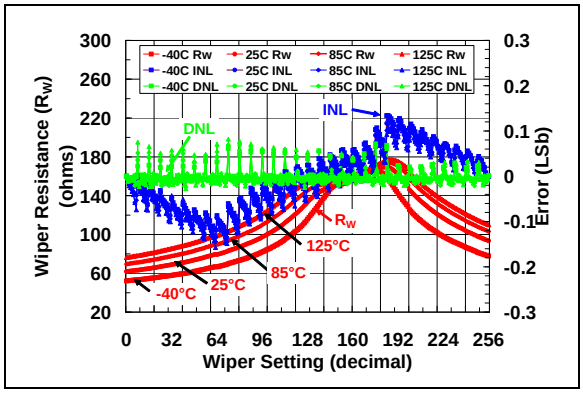



***FIGURE 2-7:*** *5 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

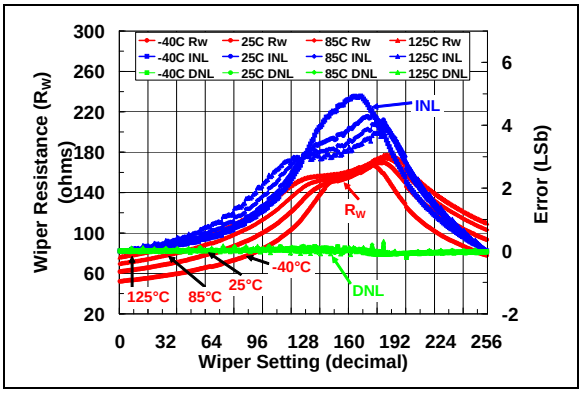



***FIGURE 2-10:*** *5 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

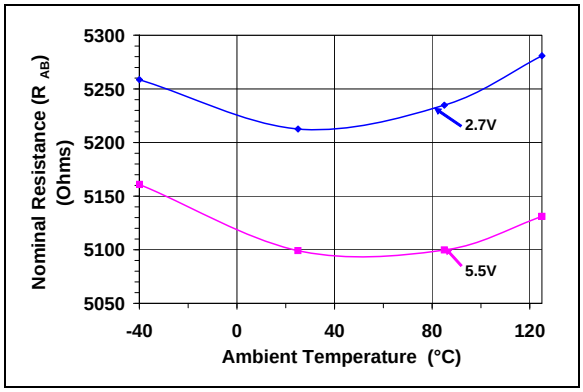



***FIGURE 2-8:*** *5 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and $V_{DD}$.*

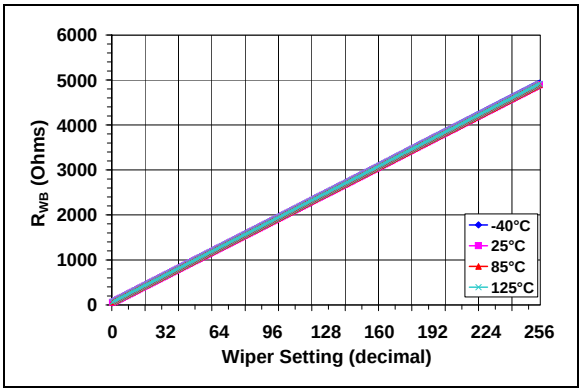



***FIGURE 2-11:*** *5 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

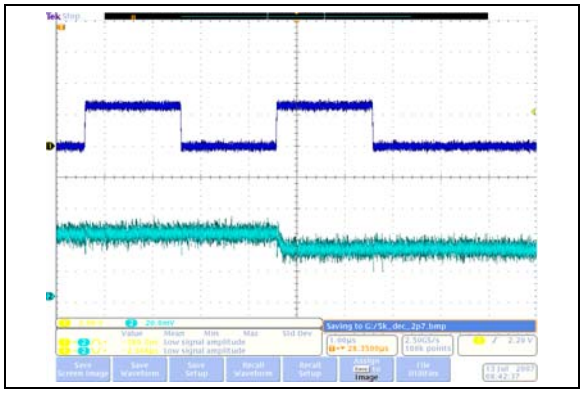


***FIGURE 2-12:*** *5 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

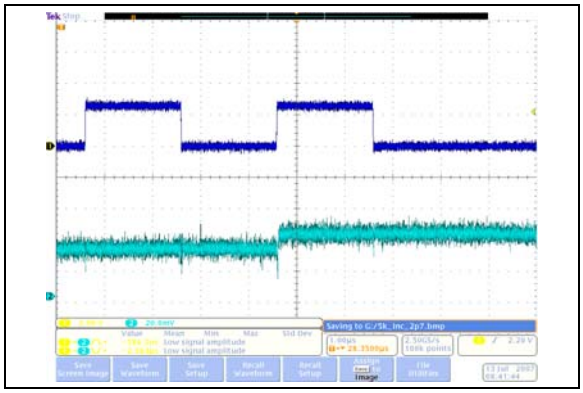


***FIGURE 2-15:*** *5 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

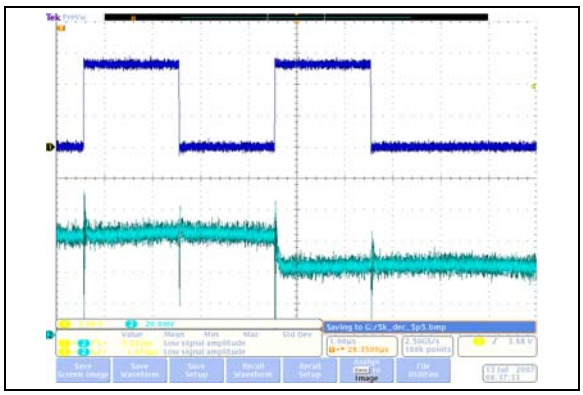


***FIGURE 2-13:*** *5 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

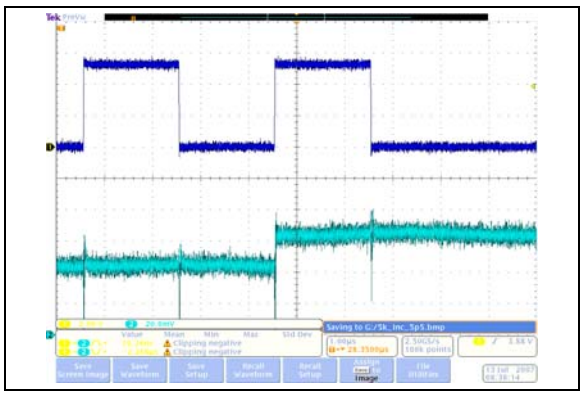


***FIGURE 2-16:*** *5 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

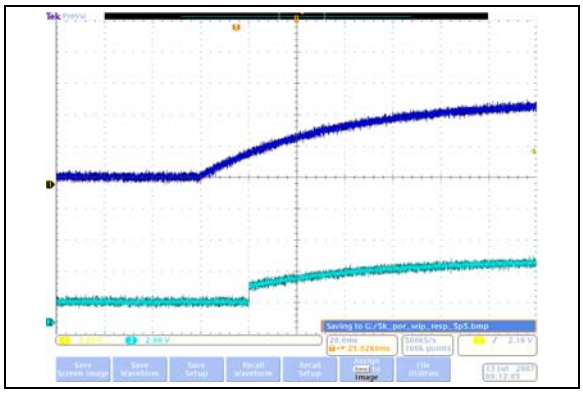


***FIGURE 2-14:*** *5 kΩ – Power-Up Wiper Response Time (20 ms/Div).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

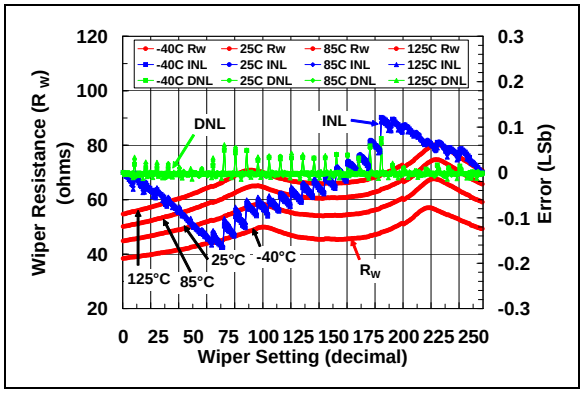



***FIGURE 2-17:*** *10 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

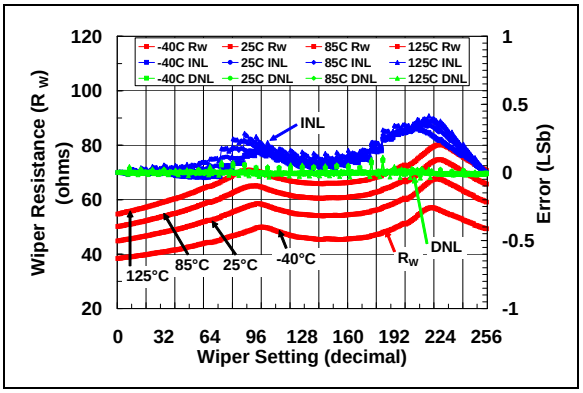



***FIGURE 2-20:*** *10 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

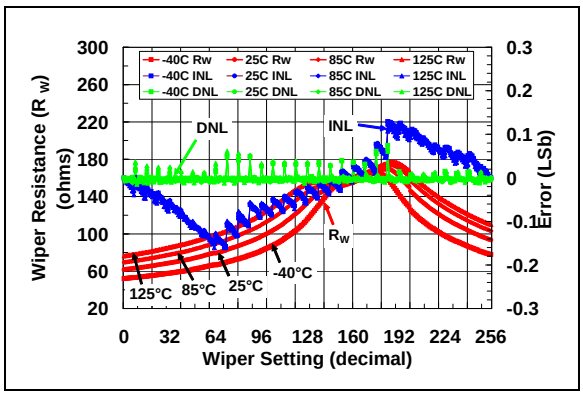



***FIGURE 2-18:*** *10 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

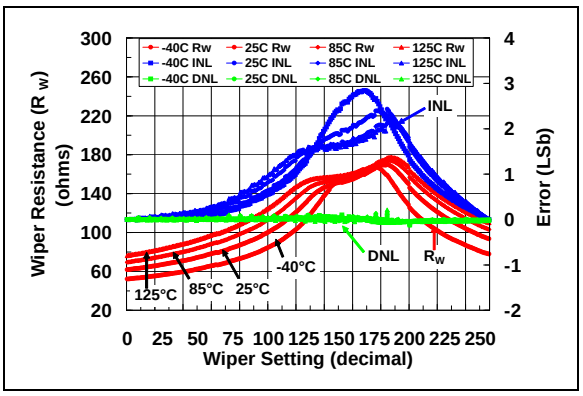



***FIGURE 2-21:*** *10 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

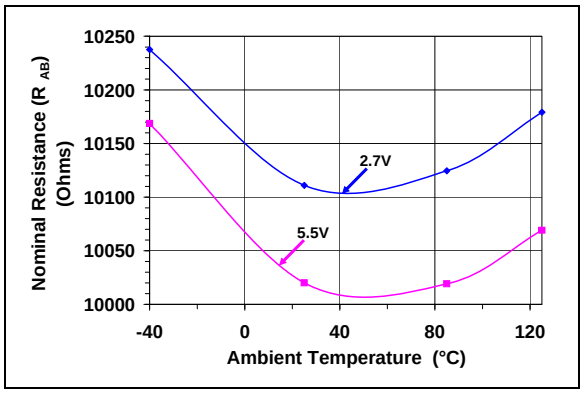



***FIGURE 2-19:*** *10 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and $V_{DD}$.*

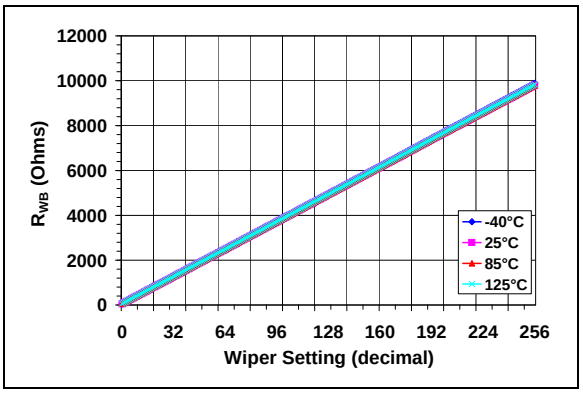



***FIGURE 2-22:*** *10 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

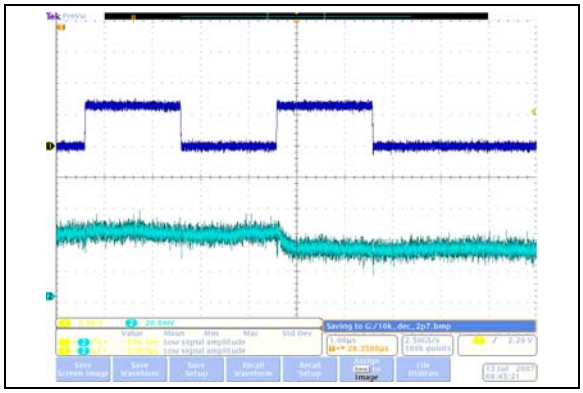


***FIGURE 2-23:*** *10 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

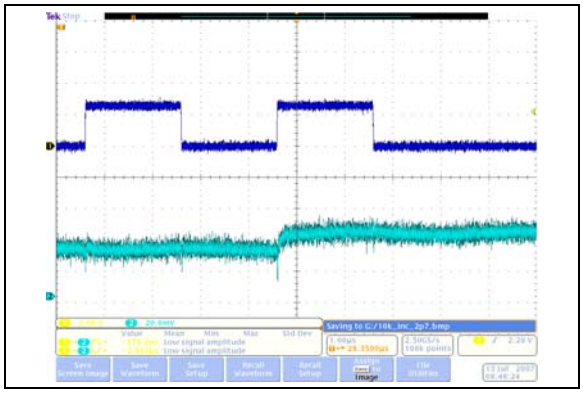


***FIGURE 2-25:*** *10 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

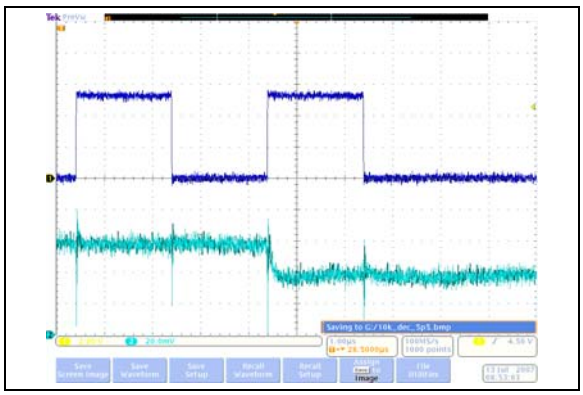


***FIGURE 2-24:*** *10 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

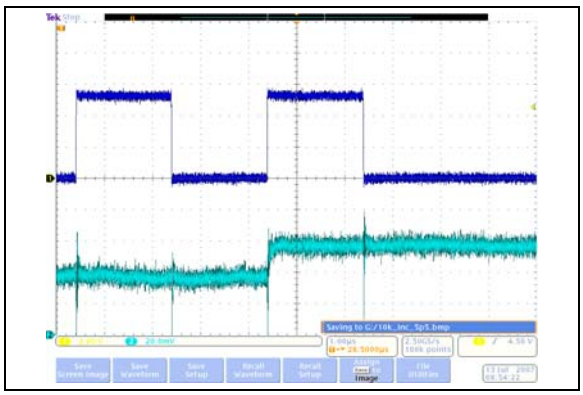


***FIGURE 2-26:*** *10 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

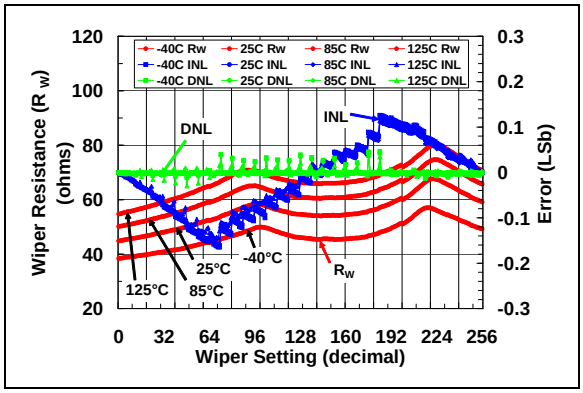



***FIGURE 2-27:*** *50 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

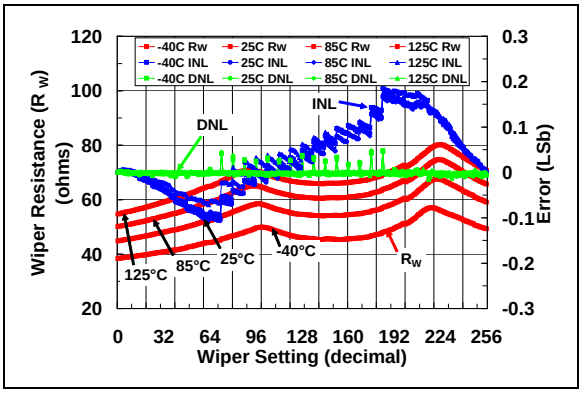



***FIGURE 2-30:*** *50 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

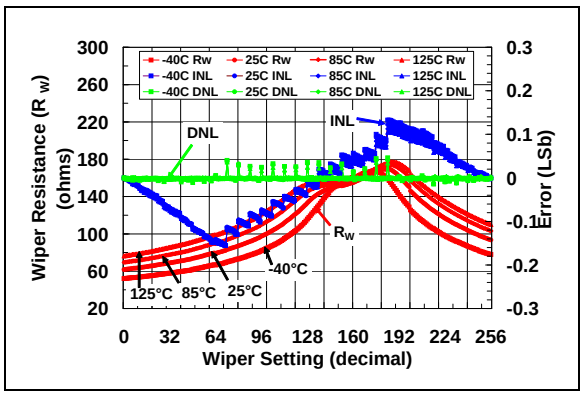



***FIGURE 2-28:*** *50 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

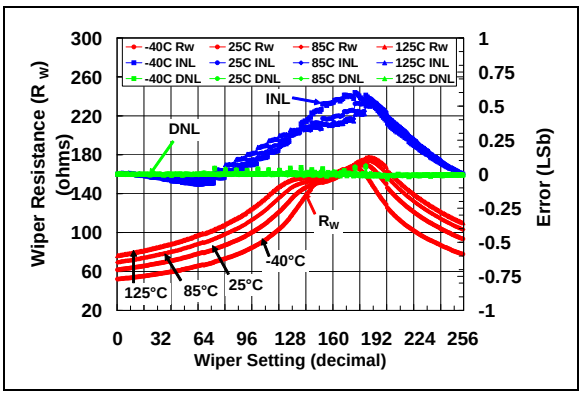



***FIGURE 2-31:*** *50 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

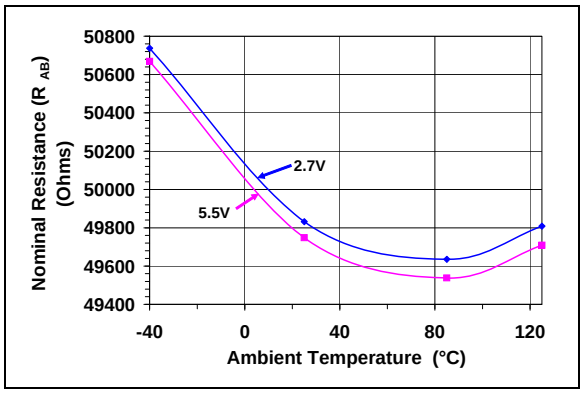



***FIGURE 2-29:*** *50 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and $V_{DD}$.*

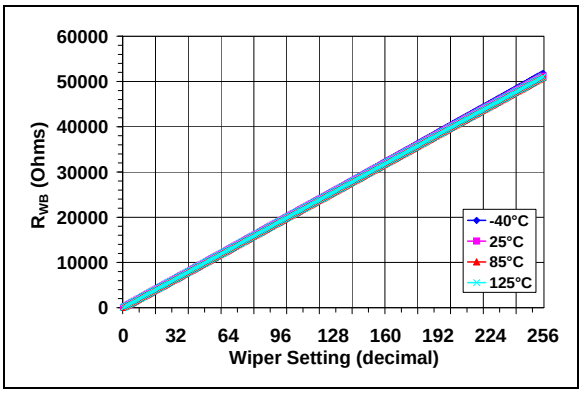



***FIGURE 2-32:*** *50 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

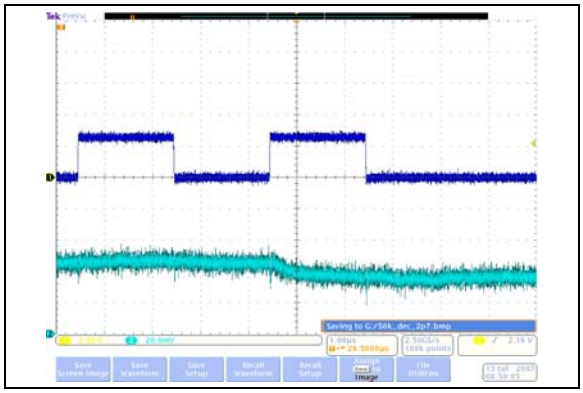


***FIGURE 2-33:*** *50 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

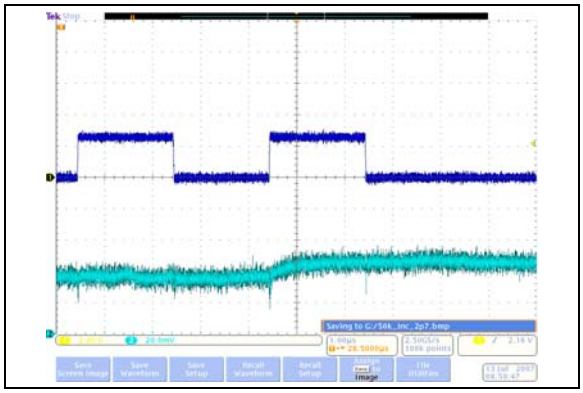


***FIGURE 2-35:*** *50 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

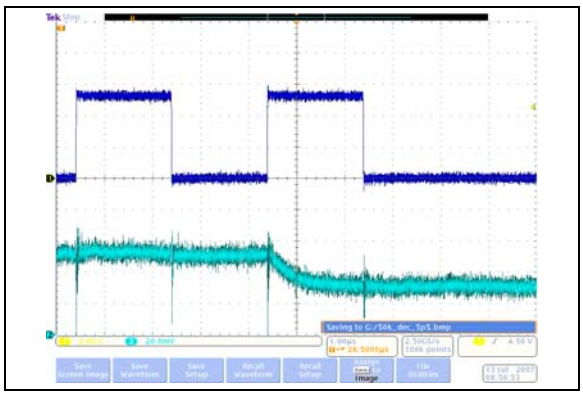


***FIGURE 2-34:*** *50 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

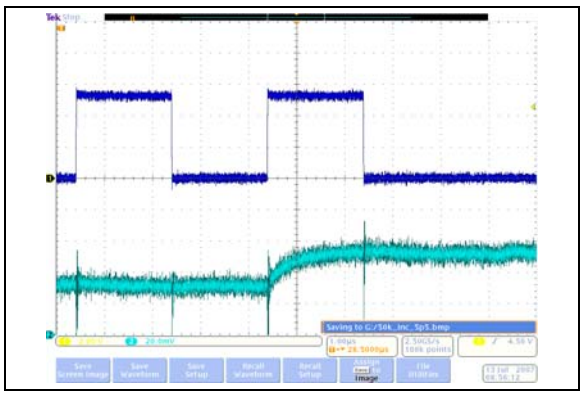


***FIGURE 2-36:*** *50 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

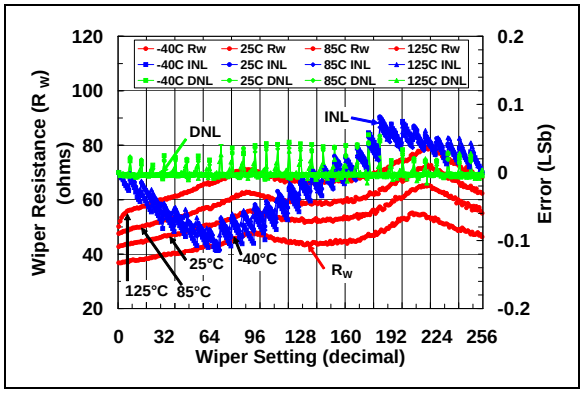



***FIGURE 2-37:*** *100 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

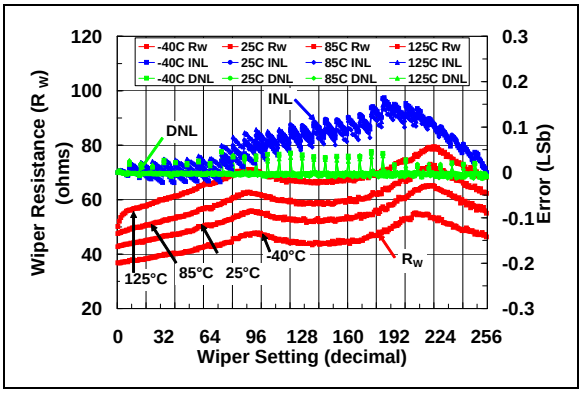



***FIGURE 2-40:*** *100 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 5.5V).*

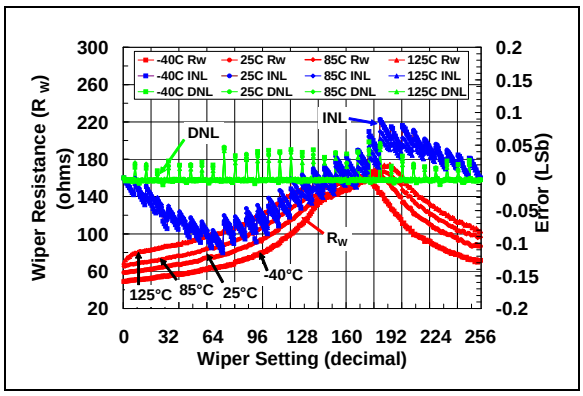



***FIGURE 2-38:*** *100 kΩ Pot Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

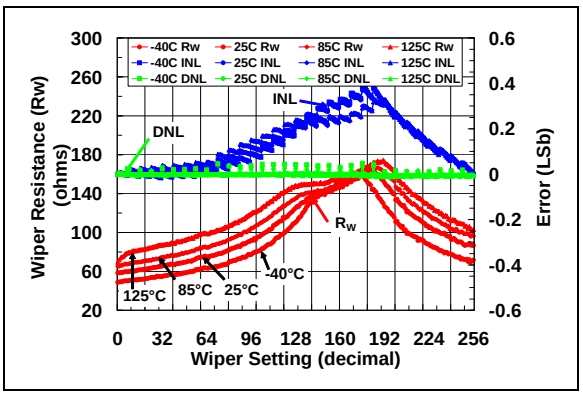



***FIGURE 2-41:*** *100 kΩ Rheo Mode – $R_W$ (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature ($V_{DD}$ = 3.0V).*

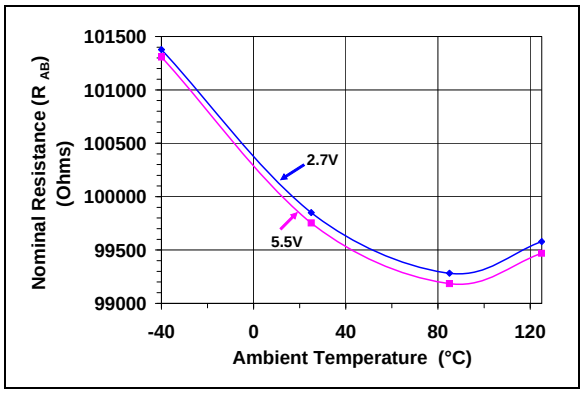



***FIGURE 2-39:*** *100 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and $V_{DD}$.*

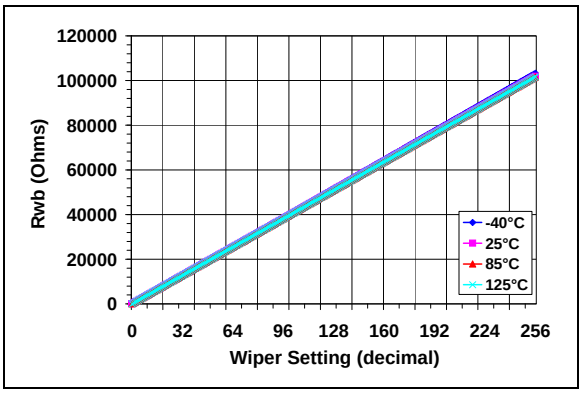



***FIGURE 2-42:*** *100 kΩ – $R_{WB}$ (Ω) vs. Wiper Setting and Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

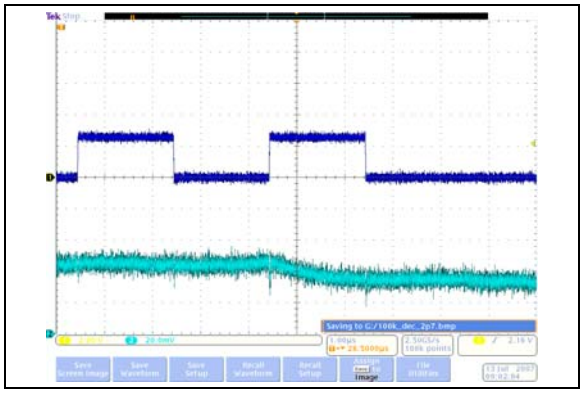


***FIGURE 2-43:*** *100 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

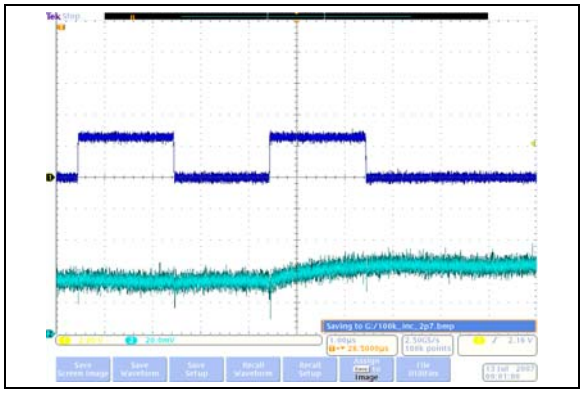


***FIGURE 2-45:*** *100 kΩ – Power-Up Wiper Response Time (1 µs/Div).*

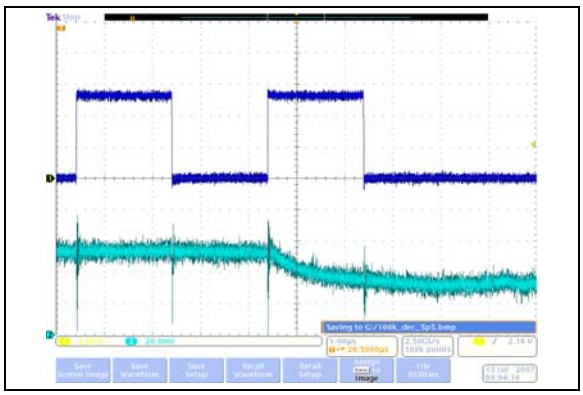


***FIGURE 2-44:*** *100 kΩ – Low-Voltage Decrement Wiper Settling Time ($V_{DD}$ = 5.5V) (1 µs/Div).*

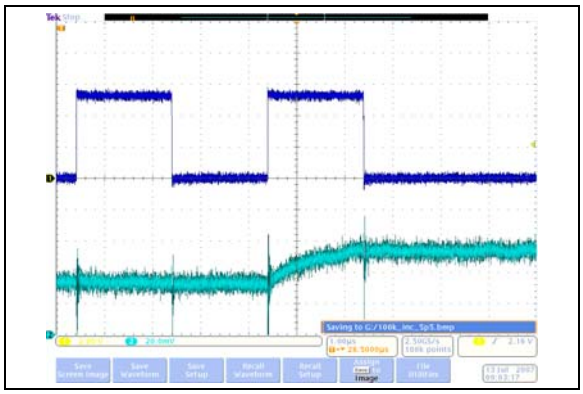


***FIGURE 2-46:*** *100 kΩ – Low-Voltage Increment Wiper Settling Time ($V_{DD}$ = 2.7V) (1 µs/Div).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

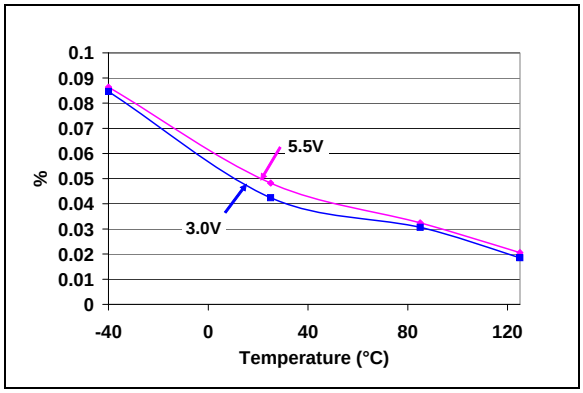



***FIGURE 2-47:*** *Resistor Network 0 to Resistor Network 1 $R_{AB}$ (5 kΩ) Mismatch vs. $V_{DD}$ and Temperature.*

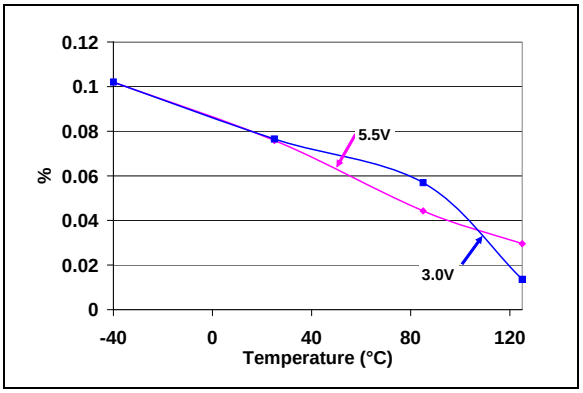



***FIGURE 2-49:*** *Resistor Network 0 to Resistor Network 1 $R_{AB}$ (50 kΩ) Mismatch vs. $V_{DD}$ and Temperature.*

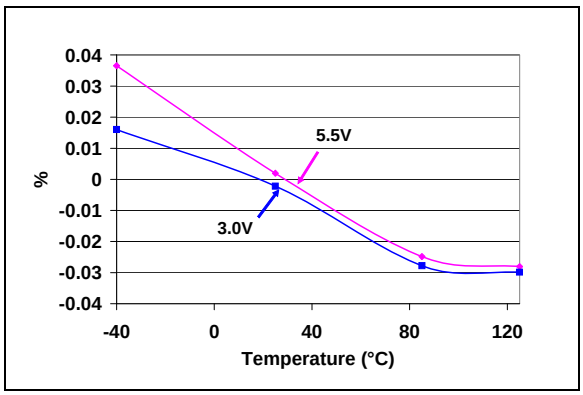



***FIGURE 2-48:*** *Resistor Network 0 to Resistor Network 1 $R_{AB}$ (10 kΩ) Mismatch vs. $V_{DD}$ and Temperature.*

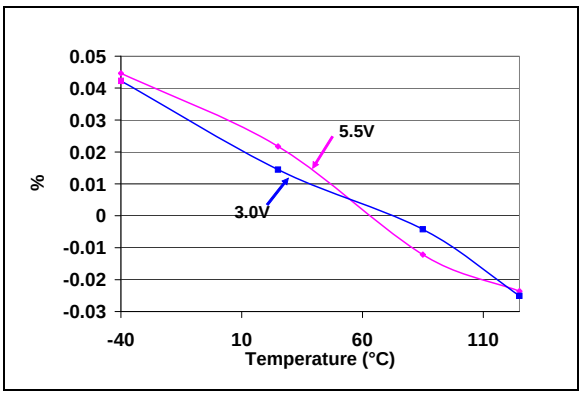



***FIGURE 2-50:*** *Resistor Network 0 to Resistor Network 1 $R_{AB}$ (100 kΩ) Mismatch vs. $V_{DD}$ and Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

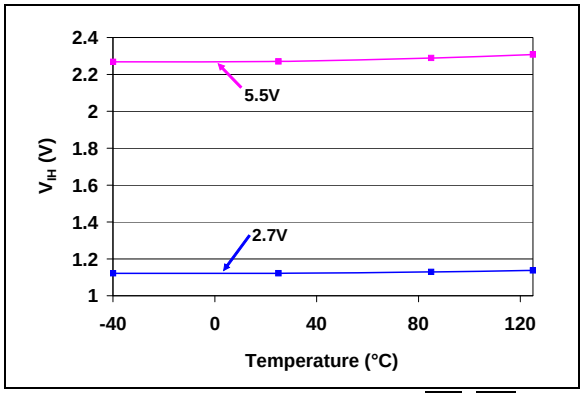



***FIGURE 2-51:*** *$V_{IH}$ (SDI, SCK, $\overline{CS}$, $\overline{WP}$, and $\overline{SHDN}$) vs. $V_{DD}$ and Temperature.*

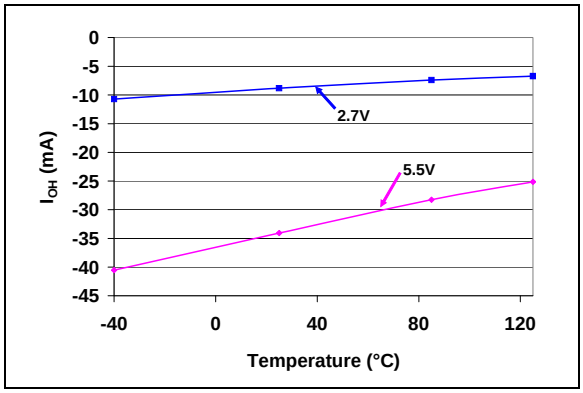



***FIGURE 2-53:*** *$I_{OH}$ (SDO) vs. $V_{DD}$ and Temperature.*

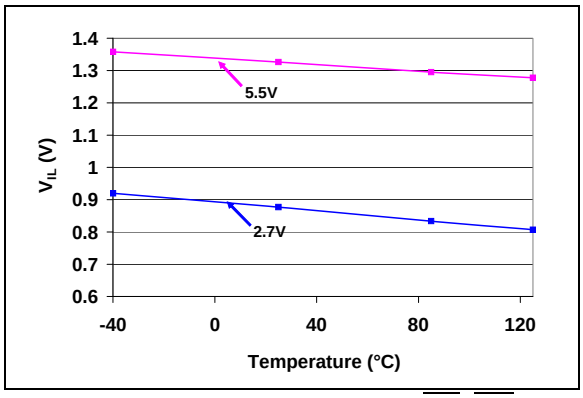



***FIGURE 2-52:*** *$V_{IL}$ (SDI, SCK, $\overline{CS}$, $\overline{WP}$, and $\overline{SHDN}$) vs. $V_{DD}$ and Temperature.*

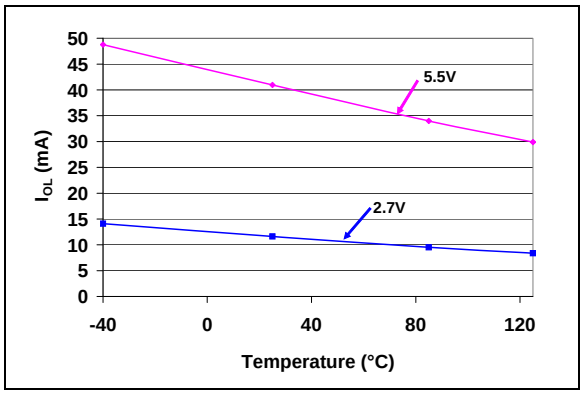



***FIGURE 2-54:*** *$I_{OL}$ (SDO) vs. $V_{DD}$ and Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{SS}$ = 0V.

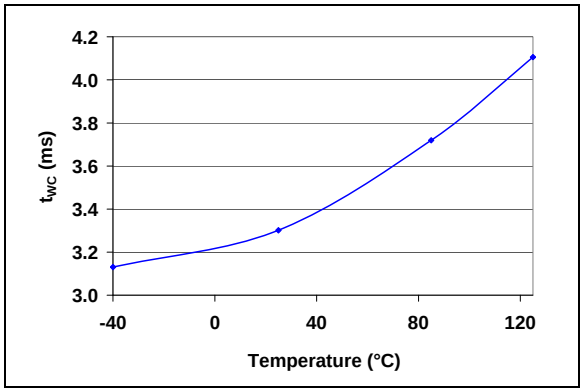



***FIGURE 2-55:*** *Nominal EEPROM Write Cycle Time vs. $V_{DD}$ and Temperature.*

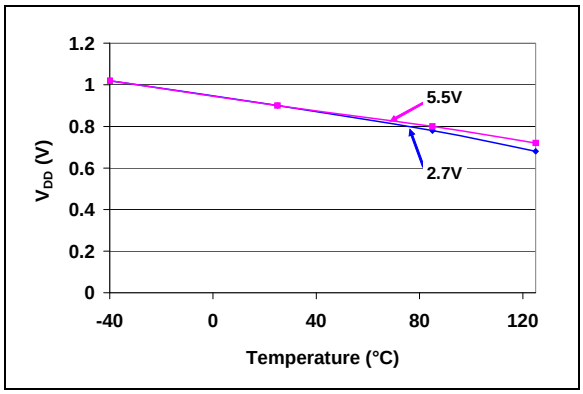



***FIGURE 2-56:*** *POR/BOR Trip point vs. $V_{DD}$ and Temperature.*

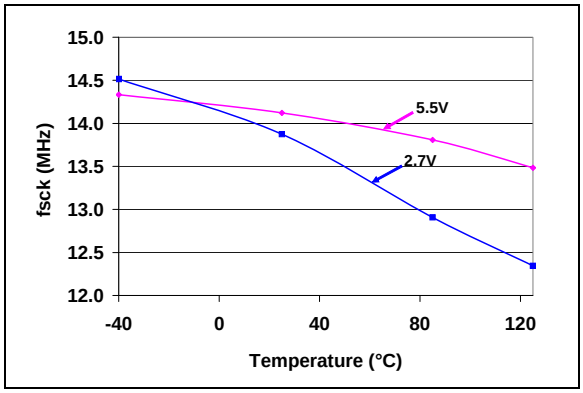



***FIGURE 2-57:*** *SCK Input Frequency vs. Voltage and Temperature.*

## 2.1 Test Circuits

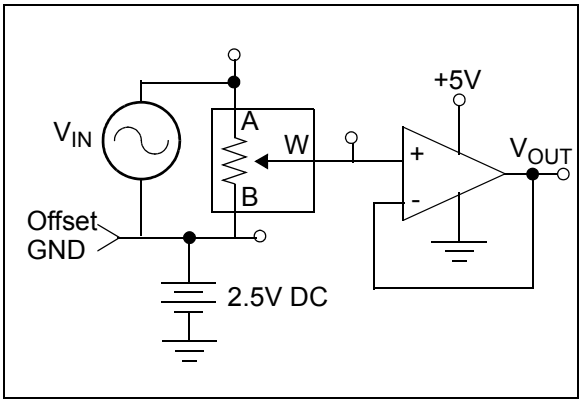



***FIGURE 2-58:*** *-3 db Gain vs. Frequency Test.*

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.
Additional descriptions of the device pins follows.

**TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP414X/416X/424X/426X**

| Pin | | | | | Symbol | I/O | Buffer Type | Weak Pull-up/ down (Note 2) | Standard Function |
|---|---|---|---|---|---|---|---|---|---|
| Single | | Dual | | | | | | | |
| Rheo | Pot (1) | Rheo | Pot | | | | | | |
| 8L | 8L | 10L | 14L | 16L | | | | | |
| 1 | 1 | 1 | 1 | 16 | $\overline{CS}$ | I | HV w/ST | “smart” | SPI Chip Select Input |
| 2 | 2 | 2 | 2 | 1 | SCK | I | HV w/ST | “smart” | SPI Clock Input |
| 3 | — | 3 | 3 | 2 | SDI | I | HV w/ST | “smart” | SPI Serial Data Input |
| — | 3 | — | — | — | SDI/SDO | I/O | HV w/ST | “smart” | SPI Serial Data Input/Output **(Note 1, Note 3)** |
| 4 | 4 | 4 | 4 | 3, 4 | $V_{SS}$ | — | P | — | Ground |
| — | — | 5 | 5 | 5 | P1B | A | Analog | No | Potentiometer 1 Terminal B |
| — | — | 6 | 6 | 6 | P1W | A | Analog | No | Potentiometer 1 Wiper Terminal |
| — | — | — | 7 | 7 | P1A | A | Analog | No | Potentiometer 1 Terminal A |
| — | 5 | — | 8 | 8 | P0A | A | Analog | No | Potentiometer 0 Terminal A |
| 5 | 6 | 7 | 9 | 9 | P0W | A | Analog | No | Potentiometer 0 Wiper Terminal |
| 6 | 7 | 8 | 10 | 10 | P0B | A | Analog | No | Potentiometer 0 Terminal B |
| — | — | — | 11 | 12 | $\overline{WP}$ | I | I | “smart” | Hardware EEPROM Write Protect |
| — | — | — | 12 | 13 | $\overline{SHDN}$ | I | HV w/ST | “smart” | Hardware Shutdown |
| 7 | — | 9 | 13 | 14 | SDO | O | O | No | SPI Serial Data Out |
| 8 | 8 | 10 | 14 | 15 | $V_{DD}$ | — | P | — | Positive Power Supply Input |
| — | — | — | — | 11 | NC | — | — | — | No Connection |
| 9 | 9 | 11 | — | 17 | EP | — | — | — | Exposed Pad. **(Note 4)** |

**Legend:** HV w/ST = High Voltage tolerant input (with Schmidtt trigger input)
A = Analog pins (Potentiometer terminals) I = digital input (high Z)
O = digital output I/O = Input / Output
P = Power

**Note 1:** The 8-lead Single Potentiometer devices are pin limited so the SDO pin is multiplexed with the SDI pin (SDI/SDO pin). After the Address/Command (first 6-bits) are received, If a valid Read command has been requested, the SDO pin starts driving the requested read data onto the SDI/SDO pin.

**2:** The pin’s “smart” pull-up shuts off while the pin is forced low. This is done to reduce the standby and shut-down current.

**3:** The SDO is an open drain output, which uses the internal “smart” pull-up. The SDI input data rate can be at the maximum SPI frequency. the SDO output data rate will be limited by the “speed” of the pull-up, customers can increase the rate with external pull-up resistors.

**4:** The DFN and QFN packages have a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device’s $V_{SS}$ pin.

### 3.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is the serial interface's chip select input. Forcing the $\overline{CS}$ pin to $V_{IL}$ enables the serial commands. Forcing the $\overline{CS}$ pin to $V_{IHH}$ enables the high-voltage serial commands.

### 3.2 Serial Data In (SDI)

The SDI pin is the serial interfaces Serial Data In pin. This pin is connected to the Host Controllers SDO pin.

### 3.3 Serial Data In / Serial Data Out (SDI/SDO)

On the MCP41X1 devices, pin-out limitations do not allow for individual SDI and SDO pins. On these devices, the SDI and SDO pins are multiplexed.

The MCP41X1 serial interface knows when the pin needs to change from being an input (SDI) to being an output (SDO). The Host Controller's SDO pin must be properly protected from a drive conflict.

### 3.4 Ground ($V_{SS}$)

The $V_{SS}$ pin is the device ground reference.

### 3.5 Potentiometer Terminal B

The terminal B pin is connected to the internal potentiometer's terminal B.

The potentiometer's terminal B is the fixed connection to the Zero Scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x00 for both 7-bit and 8-bit devices.

The terminal B pin does not have a polarity relative to the terminal W or A pins. The terminal B pin can support both positive and negative current. The voltage on terminal B must be between $V_{SS}$ and $V_{DD}$.

MCP42XX devices have two terminal B pins, one for each resistor network.

### 3.6 Potentiometer Wiper (W) Terminal

The terminal W pin is connected to the internal potentiometer's terminal W (the wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The terminal W pin does not have a polarity relative to terminals A or B pins. The terminal W pin can support both positive and negative current. The voltage on terminal W must be between $V_{SS}$ and $V_{DD}$.

MCP42XX devices have two terminal W pins, one for each resistor network.

### 3.7 Potentiometer Terminal A

The terminal A pin is available on the MCP4XX1 devices, and is connected to the internal potentiometer's terminal A.

The potentiometer's terminal A is the fixed connection to the Full Scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x100 for 8-bit devices or 0x80 for 7-bit devices.

The terminal A pin does not have a polarity relative to the terminal W or B pins. The terminal A pin can support both positive and negative current. The voltage on terminal A must be between $V_{SS}$ and $V_{DD}$.

The terminal A pin is not available on the MCP4XX2 devices, and the internally terminal A signal is floating.

MCP42X1 devices have two terminal A pins, one for each resistor network.

### 3.8 Write Protect ($\overline{WP}$)

The $\overline{WP}$ pin is used to force the non-volatile memory to be write protected.

### 3.9 Shutdown ($\overline{SHDN}$)

The $\overline{SHDN}$ pin is used to force the resistor network terminals into the hardware shutdown state.

### 3.10 Serial Data Out (SDO)

The SDO pin is the serial interfaces Serial Data Out pin. This pin is connected to the Host Controllers SDI pin.

This pin allows the Host Controller to read the digital potentiometers registers, or monitor the state of the command error bit.

### 3.11 Positive Power Supply Input ($V_{DD}$)

The $V_{DD}$ pin is the device's positive power supply input. The input power supply is relative to $V_{SS}$.

While the device $V_{DD} < V_{min}$ (2.7V), the electrical performance of the device may not meet the data sheet specifications.

### 3.12 No Connection (NC)

Those pins should be either connected to $V_{DD}$ or $V_{SS}$.

### 3.13 Exposed Pad (EP)

This pad is conductively connected to the device's substrate. This pad should be tied to the same potential as the $V_{SS}$ pin (or left unconnected). This pad could be used to assist as a heat sink for the device when connected to a PCB heat sink.

## 4.0 FUNCTIONAL OVERVIEW

This Data Sheet covers a family of thirty-two Digital Potentiometer and Rheostat devices that will be referred to as MCP4XXX. The MCP4XX1 devices are the Potentiometer configuration, while the MCP4XX2 devices are the Rheostat configuration.

As the **Device Block Diagram** shows, there are four main functional blocks. These are:

- **POR/BOR Operation**
- **Memory Map**
- **Resistor Network**
- **Serial Interface (SPI)**

The POR/BOR operation and the Memory Map are discussed in this section and the Resistor Network and SPI operation are described in their own sections. The **Device Commands** commands are discussed in **Section 7.0**.

## 4.1 POR/BOR Operation

The Power-on Reset is the case where the device is having power applied to it from $V_{SS}$. The Brown-out Reset occurs when a device had power applied to it, and that power (voltage) drops below the specified range.

The devices RAM retention voltage ($V_{RAM}$) is lower than the POR/BOR voltage trip point ($V_{POR}/V_{BOR}$). The maximum $V_{POR}/V_{BOR}$ voltage is less then 1.8V.

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its EEPROM and incrementing, decrementing, reading and writing to its volatile memory if the proper serial command is executed.

### 4.1.1 POWER-ON RESET

When the device powers up, the device $V_{DD}$ will cross the $V_{POR}/V_{BOR}$ voltage. Once the $V_{DD}$ voltage crosses the $V_{POR}/V_{BOR}$ voltage the following happens:

- Volatile wiper register is loaded with value in the corresponding non-volatile wiper register
- The TCON register is loaded it's default value
- The device is capable of digital operation

### 4.1.2 BROWN-OUT RESET

When the device powers down, the device $V_{DD}$ will cross the $V_{POR}/V_{BOR}$ voltage.

Once the $V_{DD}$ voltage decreases below the $V_{POR}/V_{BOR}$ voltage the following happens:

- Serial Interface is disabled
- EEPROM Writes are disabled

If the $V_{DD}$ voltage decreases below the $V_{RAM}$ voltage the following happens:

- Volatile wiper registers may become corrupted
- TCON register may become corrupted

As the voltage recovers above the $V_{POR}/V_{BOR}$ voltage see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a brown-out condition may cause the memory location (volatile and non-volatile) to become corrupted.

## 4.2 Memory Map

The device memory is 16 locations that are 9-bits wide (16x9 bits). This memory space contains both volatile and non-volatile locations (see Table 4-1).

**TABLE 4-1: MEMORY MAP**

| Address | Function | Memory Type |
|---|---|---|
| 00h | Volatile Wiper 0 | RAM |
| 01h | Volatile Wiper 1 | RAM |
| 02h | Non-Volatile Wiper 0 | EEPROM |
| 03h | Non-Volatile Wiper 1 | EEPROM |
| 04h | Volatile TCON Register | RAM |
| 05h | Status Register | RAM |
| 06h | Data EEPROM | EEPROM |
| 07h | Data EEPROM | EEPROM |
| 08h | Data EEPROM | EEPROM |
| 09h | Data EEPROM | EEPROM |
| 0Ah | Data EEPROM | EEPROM |
| 0Bh | Data EEPROM | EEPROM |
| 0Ch | Data EEPROM | EEPROM |
| 0Dh | Data EEPROM | EEPROM |
| 0Eh | Data EEPROM | EEPROM |
| 0Fh | Data EEPROM | EEPROM |

### 4.2.1 NON-VOLATILE MEMORY (EEPROM)

This memory can be grouped into two uses of non-volatile memory. These are:

- **General Purpose Registers**
- **Non-Volatile Wiper Registers**

The non-volatile wipers starts functioning below the devices $V_{POR}/V_{BOR}$ trip point.

#### 4.2.1.1 General Purpose Registers

These locations allow the user to store up to 10 (9-bit) locations worth of information.

#### 4.2.1.2 Non-Volatile Wiper Registers

These locations contain the wiper values that are loaded into the corresponding volatile wiper register whenever the device has a POR/BOR event. There are up to two registers, one for each resistor network.

The non-volatile wiper register enables stand-alone operation of the device (without Microcontroller control) after being programmed to the desired value.

#### 4.2.1.3 Factory Initialization of Non-Volatile Memory (EEPROM)

The Non-Volatile Wiper values will be initialized to mid-scale value. This is shown in Table 4-2.

The General purpose EEPROM memory will be programmed to a default value of 0xFF.

It is good practice in the manufacturing flow to configure the device to your desired settings.

**TABLE 4-2: DEFAULT FACTORY SETTINGS SELECTION**

| Resistance Code | Typical $R_{AB}$ Value | Default POR Wiper Setting | Wiper Code | | WiperLock™ Technology and Write Protect Setting |
|---|---|---|---|---|---|
| | | | 8-bit | 7-bit | |
| -502 | 5.0 kΩ | Mid-scale | 80h | 40h | Disabled |
| -103 | 10.0 kΩ | Mid-scale | 80h | 40h | Disabled |
| -503 | 50.0 kΩ | Mid-scale | 80h | 40h | Disabled |
| -104 | 100.0 kΩ | Mid-scale | 80h | 40h | Disabled |

#### 4.2.1.4 Special Features

There are 3 non-volatile bits that are not directly mapped into the address space. These bits control the following functions:

- EEPROM Write Protect
- WiperLock Technology for Non-Volatile Wiper 0
- WiperLock Technology for Non-Volatile Wiper 1

The operation of WiperLock Technology is discussed in **Section 5.3**. The state of the WL0, WL1, and WP bits is reflected in the STATUS register (see Register 4-1).

### EEPROM Write Protect

All internal EEPROM memory can be Write Protected. When EEPROM memory is Write Protected, Write commands to the internal EEPROM are prevented.

Write Protect ($\overline{WP}$) can be enabled/disabled by two methods. These are:

- External $\overline{WP}$ Hardware pin (MCP42X1 devices only)
- Non-Volatile configuration bit

High Voltage commands are required to enable and disable the nonvolatile WP bit. These commands are shown in **Section 7.9 "Modify Write Protect or WiperLock Technology (High Voltage)"**.

To write to EEPROM, both the external $\overline{WP}$ pin and the internal WP EEPROM bit must be disabled. Write Protect does not block commands to the volatile registers.

### 4.2.2 VOLATILE MEMORY (RAM)

There are four Volatile Memory locations. These are:

- Volatile Wiper 0
- Volatile Wiper 1
  (Dual Resistor Network devices only)
- Status Register
- Terminal Control (TCON) Register

The volatile memory starts functioning at the RAM retention voltage ($V_{RAM}$).

#### 4.2.2.1 Status (STATUS) Register

This register contains 5 status bits. These bits show the state of the WiperLock bits, the Shutdown bit the Write Protect bit, and if an EEPROM write cycle is active. The STATUS register can be accessed via the READ commands. Register 4-1 describes each STATUS register bit.

The STATUS register is placed at Address 05h.

**REGISTER 4-1: STATUS REGISTER**

| R-1 | R-1 | R-1 | R-1 | R-0 | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|---|
| D8:D5 | | | | EEWA | WL1 (1) | WL0 (1) | SHDN | WP (1) |
| bit 7 | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 8-5 **D8:D5:** Reserved. Forced to "1"

bit 4 **EEWA:** EEPROM Write Active Status bit

This bit indicates if the EEPROM Write Cycle is occurring.

1 = An EEPROM Write cycle is currently occurring. Only serial commands to the Volatile memory locations are allowed (addresses 00h, 01h, 04h, and 05h)

0 = An EEPROM Write cycle is NOT currently occurring

bit 3 **WL1:** WiperLock Status bit for Resistor Network 1 (Refer to **Section 5.3 "WiperLock™ Technology"** for further information)

WiperLock (WL) prevents the Volatile and Non-Volatile Wiper 1 addresses and the TCON register bits R1HW, R1A, R1W, and R1B from being written to. High Voltage commands are required to enable and disable WiperLock Technology.

1 = Wiper and TCON register bits R1HW, R1A, R1W, and R1B of Resistor Network 1 (Pot 1) are "Locked" (Write Protected)

0 = Wiper and TCON of Resistor Network 1 (Pot 1) can be modified

**Note:** The WL1 bit always reflects the result of the last programming cycle to the non-volatile WL1 bit. After a POR or BOR event, the WL1 bit is loaded with the non-volatile WL1 bit value.

bit 2 **WL0:** WiperLock Status bit for Resistor Network 0 (Refer to **Section 5.3 "WiperLock™ Technology"** for further information)

The WiperLock Technology bits (WLx) prevents the Volatile and Non-Volatile Wiper 0 addresses and the TCON register bits R0HW, R0A, R0W, and R0B from being written to. High Voltage commands are required to enable and disable WiperLock Technology.

1 = Wiper and TCON register bits R0HW, R0A, R0W, and R0B of Resistor Network 0 (Pot 0) are "Locked" (Write Protected)

0 = Wiper and TCON of Resistor Network 0 (Pot 0) can be modified

**Note:** The WL0 bit always reflects the result of the last programming cycle to the non-volatile WL0 bit. After a POR or BOR event, the WL0 bit is loaded with the non-volatile WL0 bit value.

bit 1 **SHDN:** Hardware Shutdown pin Status bit (Refer to **Section 5.4 "Shutdown"** for further information)

This bit indicates if the Hardware shutdown pin ($\overline{SHDN}$) is low. A hardware shutdown disconnects the Terminal A and forces the wiper (Terminal W) to Terminal B (see Figure 5-2). While the device is in Hardware Shutdown (the $\overline{SHDN}$ pin is low) the serial interface is operational so the STATUS register may be read.

1 = MCP4XXX is in the Hardware Shutdown state

0 = MCP4XXX is NOT in the Hardware Shutdown state

**Note 1:** Requires a High Voltage command to modify the state of this bit (for Non-Volatile devices only). This bit is Not directly written, but reflects the system state (for this feature).

**REGISTER 4-1: STATUS REGISTER (CONTINUED)**

bit 0 **WP:** EEPROM Write Protect Status bit (Refer to **Section "EEPROM Write Protect"** for further information)

This bit indicates the status of the write protection on the EEPROM memory. When Write Protect is enabled, writes to all non-volatile memory are prevented. This includes the General Purpose EEPROM memory, and the non-volatile Wiper registers. Write Protect does not block modification of the volatile wiper register values or the volatile TCON register value (via Increment, Decrement, or Write commands).

This status bit is an OR of the devices Write Protect pin ($\overline{WP}$) and the internal non-volatile WP bit. High Voltage commands are required to enable and disable the internal WP EEPROM bit.

1 = EEPROM memory is Write Protected

0 = EEPROM memory can be written

**Note 1:** Requires a High Voltage command to modify the state of this bit (for Non-Volatile devices only). This bit is Not directly written, but reflects the system state (for this feature).

#### 4.2.2.2 Terminal Control (TCON) Register

This register contains 8 control bits. Four bits are for Wiper 0, and four bits are for Wiper 1. Register 4-2 describes each bit of the TCON register.

The state of each resistor network terminal connection is individually controlled. That is, each terminal connection (A, B and W) can be individually connected/ disconnected from the resistor network. This allows the system to minimize the currents through the digital potentiometer.

The value that is written to this register will appear on the resistor network terminals when the serial command has completed.

When the WL1 bit is enabled, writes to the TCON register bits R1HW, R1A, R1W, and R1B are inhibited.

When the WL0 bit is enabled, writes to the TCON register bits R0HW, R0A, R0W, and R0B are inhibited.

On a POR/BOR this register is loaded with 1FFh (9-bits), for all terminals connected. The HostController needs to detect the POR/BOR event and then update the Volatile TCON register value.

**REGISTER 4-2: TCON BITS (1, 2)**

| R-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|---|
| D8 | R1HW | R1A | R1W | R1B | R0HW | R0A | R0W | R0B |
| bit 8 | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 8 **D8:** Reserved. Forced to "1"

bit 7 **R1HW:** Resistor 1 Hardware Configuration Control bit

This bit forces Resistor 1 into the "shutdown" configuration of the Hardware pin
1 = Resistor 1 is NOT forced to the hardware pin "shutdown" configuration
0 = Resistor 1 is forced to the hardware pin "shutdown" configuration

bit 6 **R1A:** Resistor 1 Terminal A (P1A pin) Connect Control bit

This bit connects/disconnects the Resistor 1 Terminal A to the Resistor 1 Network
1 = P1A pin is connected to the Resistor 1 Network
0 = P1A pin is disconnected from the Resistor 1 Network

bit 5 **R1W:** Resistor 1 Wiper (P1W pin) Connect Control bit

This bit connects/disconnects the Resistor 1 Wiper to the Resistor 1 Network
1 = P1W pin is connected to the Resistor 1 Network
0 = P1W pin is disconnected from the Resistor 1 Network

bit 4 **R1B:** Resistor 1 Terminal B (P1B pin) Connect Control bit

This bit connects/disconnects the Resistor 1 Terminal B to the Resistor 1 Network
1 = P1B pin is connected to the Resistor 1 Network
0 = P1B pin is disconnected from the Resistor 1 Network

bit 3 **R0HW:** Resistor 0 Hardware Configuration Control bit

This bit forces Resistor 0 into the "shutdown" configuration of the Hardware pin
1 = Resistor 0 is NOT forced to the hardware pin "shutdown" configuration
0 = Resistor 0 is forced to the hardware pin "shutdown" configuration

bit 2 **R0A:** Resistor 0 Terminal A (P0A pin) Connect Control bit

This bit connects/disconnects the Resistor 0 Terminal A to the Resistor 0 Network
1 = P0A pin is connected to the Resistor 0 Network
0 = P0A pin is disconnected from the Resistor 0 Network

bit 1 **R0W:** Resistor 0 Wiper (P0W pin) Connect Control bit

This bit connects/disconnects the Resistor 0 Wiper to the Resistor 0 Network
1 = P0W pin is connected to the Resistor 0 Network
0 = P0W pin is disconnected from the Resistor 0 Network

bit 0 **R0B:** Resistor 0 Terminal B (P0B pin) Connect Control bit

This bit connects/disconnects the Resistor 0 Terminal B to the Resistor 0 Network
1 = P0B pin is connected to the Resistor 0 Network
0 = P0B pin is disconnected from the Resistor 0 Network

**Note 1:** The hardware $\overline{\text{SHDN}}$ pin (when active) overrides the state of these bits. When the $\overline{\text{SHDN}}$ pin returns to the inactive state, the TCON register will control the state of the terminals. The $\overline{\text{SHDN}}$ pin does not modify the state of the TCON bits.

**2:** These bits do not affect the wiper register values.

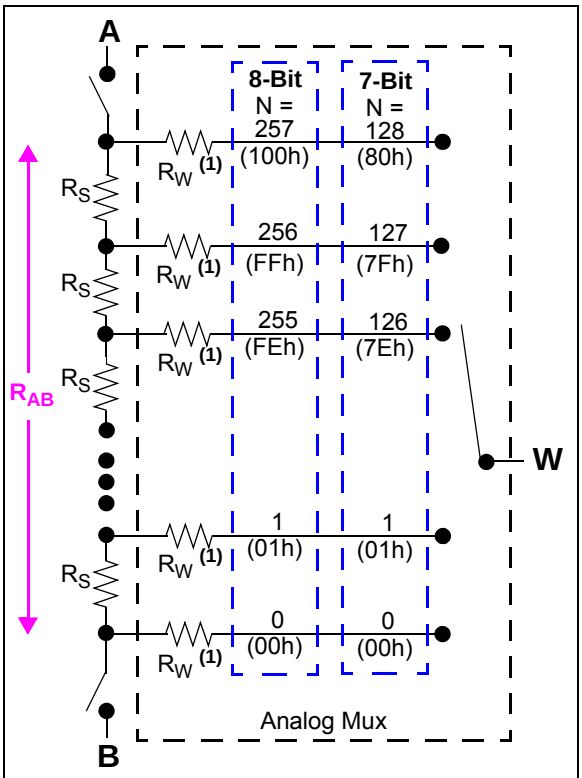
## 5.0 RESISTOR NETWORK

The Resistor Network has either 7-bit or 8-bit resolution. Each Resistor Network allows zero scale to full scale connections. Figure 5-1 shows a block diagram for the resistive network of a device.

The Resistor Network is made up of several parts. These include:

- Resistor Ladder
- Wiper
- Shutdown (Terminal Connections)

Devices have either one or two resistor networks, These are referred to as Pot 0 and Pot 1.




**Note 1:** The wiper resistance is dependent on several factors including, wiper code, device $V_{DD}$, Terminal voltages (on A, B, and W), and temperature.
Also for the same conditions, each tap selection resistance has a small variation. This $R_W$ variation has greater effects on some specifications (such as INL) for the smaller resistance devices (5.0 kΩ) compared to larger resistance devices (100.0 kΩ).

***FIGURE 5-1:*** *Resistor Block Diagram.*

### 5.1 Resistor Ladder Module

The resistor ladder is a series of equal value resistors ($R_S$) with a connection point (tap) between the two resistors. The total number of resistors in the series (ladder) determines the $R_{AB}$ resistance (see Figure 5-1). The end points of the resistor ladder are connected to analog switches which are connected to the device Terminal A and Terminal B pins. The $R_{AB}$ (and $R_S$) resistance has small variations over voltage and temperature.

For an 8-bit device, there are 256 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 256 resistors thus providing 257 possible settings (including terminal A and terminal B).

For a 7-bit device, there are 128 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 128 resistors thus providing 129 possible settings (including terminal A and terminal B).

Equation 5-1 shows the calculation for the step resistance.

**EQUATION 5-1: $R_S$ CALCULATION**

$$R_S = \frac{R_{AB}}{(256)} \quad \text{8-bit Device}$$

$$R_S = \frac{R_{AB}}{(128)} \quad \text{7-bit Device}$$

## 5.2 Wiper

Each tap point (between the $R_S$ resistors) is a connection point for an analog switch. The opposite side of the analog switch is connected to a common signal which is connected to the Terminal W (Wiper) pin.

A value in the volatile wiper register selects which analog switch to close, connecting the W terminal to the selected node of the resistor ladder.

The wiper can connect directly to Terminal B or to Terminal A. A zero-scale connections, connects the Terminal W (wiper) to Terminal B (wiper setting of 000h). A full-scale connections, connects the Terminal W (wiper) to Terminal A (wiper setting of 100h or 80h). In these configurations the only resistance between the Terminal W and the other Terminal (A or B) is that of the analog switches.

A wiper setting value greater than full scale (wiper setting of 100h for 8-bit device or 80h for 7-bit devices) will also be a Full Scale setting (Terminal W (wiper) connected to Terminal A). Table 5-1 illustrates the full wiper setting map.

Equation 5-2 illustrates the calculation used to determine the resistance between the wiper and terminal B.

**EQUATION 5-2: $R_{WB}$ CALCULATION**

$$R_{WB} = \frac{R_{AB}N}{(256)} + R_W \quad \text{8-bit Device}$$

N = 0 to 256 (decimal)

$$R_{WB} = \frac{R_{AB}N}{(128)} + R_W \quad \text{7-bit Device}$$

N = 0 to 128 (decimal)

**TABLE 5-1: VOLATILE WIPER VALUE VS. WIPER POSITION MAP**

| Wiper Setting | | Properties |
|---|---|---|
| 7-bit Pot | 8-bit Pot | |
| 3FFh<br>081h | 3FFh<br>101h | Reserved (Full Scale (W = A)), Increment and Decrement commands ignored |
| 080h | 100h | Full Scale (W = A), Increment commands ignored |
| 07Fh<br>041h | 0FFh<br>081 | W = N |
| 040h | 080h | W = N (Mid-Scale) |
| 03Fh<br>001h | 07Fh<br>001 | W = N |
| 000h | 000h | Zero Scale (W = B) Decrement command ignored |

## 5.3 WiperLock™ Technology

The MCP4XXX device's WiperLock technology allows application-specific calibration settings to be secured in the EEPROM without requiring the use of an additional write-protect pin. There are two WiperLock Technology configuration bits (WL0 and WL1). These bits prevent the Non-Volatile and Volatile addresses and bits for the specified resistor network from being written.

The WiperLock technology prevents the serial commands from doing the following:

- Changing a volatile wiper value
- Writing to a non-volatile wiper memory location
- Changing the volatile TCON register value

For either Resistor Network 0 or Resistor Network 1 (Potx), the WLx bit controls the following:

- Non-Volatile Wiper Register
- Volatile Wiper Register
- Volatile TCON register bits RxHW, RxA, RxW, and RxB

High Voltage commands are required to enable and disable WiperLock. Please refer to the **Modify Write Protect or WiperLock Technology (High Voltage)** command for operation.

### 5.3.1 POR/BOR OPERATION WHEN WIPERLOCK TECHNOLOGY ENABLED

The WiperLock Technology state is not affected by a POR/BOR event. A POR/BOR event will load the Volatile Wiper register value with the Non-Volatile Wiper register value, refer to **Section 4.1**.

## 5.4 Shutdown

Shutdown is used to minimize the device's current consumption. The MCP4XXX has two methods to achieve this. These are:

- **Hardware Shutdown Pin (SHDN)**
- **Terminal Control Register (TCON)**

The Hardware Shutdown pin is backwards compatible with the MCP42XXX devices.

### 5.4.1 HARDWARE SHUTDOWN PIN ($\overline{SHDN}$)

The $\overline{SHDN}$ pin is available on the dual potentiometer devices. When the $\overline{SHDN}$ pin is forced active ($V_{IL}$):

- The P0A and P1A terminals are disconnected
- The P0W and P1W terminals are simultaneously connect to the P0B and P1B terminals, respectively (see Figure 5-2)
- The Serial Interface is NOT disabled, and all Serial Interface activity is executed
- Any EEPROM write cycles are completed

The Hardware Shutdown pin mode does NOT corrupt the values in the Volatile Wiper Registers nor the TCON register. When the Shutdown mode is exited ($\overline{SHDN}$ pin is inactive ($V_{IH}$)):

- The device returns to the Wiper setting specified by the Volatile Wiper value
- The TCON register bits return to controlling the terminal connection state

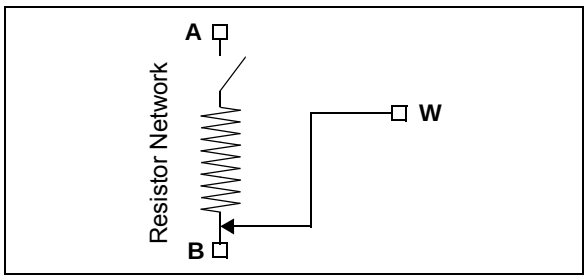



***FIGURE 5-2:*** *Hardware Shutdown Resistor Network Configuration.*

### 5.4.2 TERMINAL CONTROL REGISTER (TCON)

The Terminal Control (TCON) register is a volatile register used to configure the connection of each resistor network terminal pin (A, B, and W) to the Resistor Network. This register is shown in Register 4-2.

The RxHW bits forces the selected resistor network into the same state as the $\overline{SHDN}$ pin. Alternate low power configurations may be achieved with the RxA, RxW, and RxB bits.

| | |
|---|---|
| **Note:** | When the RxHW bit forces the resistor network into the hardware $\overline{SHDN}$ state, the state of the TCON register RxA, RxW, and RxB bits is overridden (ignored). When the state of the RxHW bit no longer forces the resistor network into the hardware $\overline{SHDN}$ state, the TCON register RxA, RxW, and RxB bits return to controlling the terminal connection state. In other words, the RxHW bit does not corrupt the state of the RxA, RxW, and RxB bits. |

### 5.4.3 INTERACTION OF $\overline{SHDN}$ PIN AND TCON REGISTER

Figure 5-3 shows how the $\overline{SHDN}$ pin signal and the RxHW bit signal interact to control the hardware shutdown of each resistor network (independently). Using the TCON bits allows each resistor network (Pot 0 and Pot 1) to be individually "shutdown" while the hardware pin forces both resistor networks to be "shutdown" at the same time.

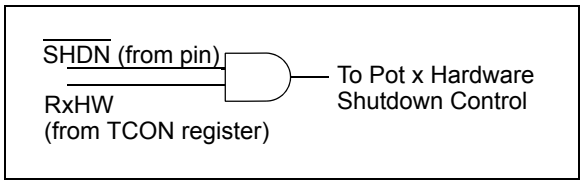



***FIGURE 5-3:*** *RxHW bit and $\overline{SHDN}$ pin Interaction.*

**NOTES:**

## 6.0 SERIAL INTERFACE (SPI)

The MCP4XXX devices support the SPI serial protocol. This SPI operates in the slave mode (does not generate the serial clock).

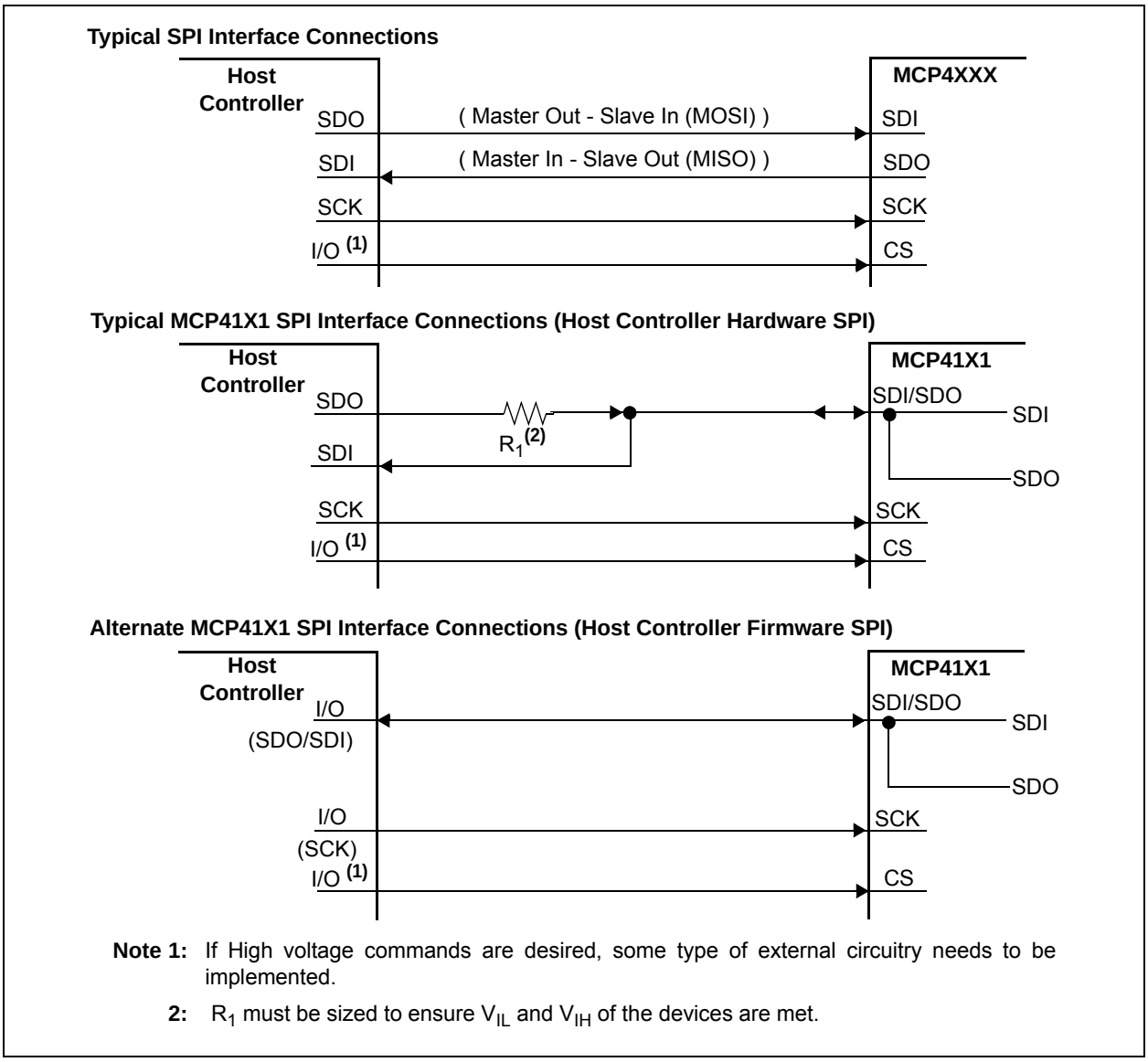
The SPI interface uses up to four pins. These are:

- $\overline{CS}$ - Chip Select
- SCK - Serial Clock
- SDI - Serial Data In
- SDO - Serial Data Out

Typical SPI Interfaces are shown in Figure 6-1. In the SPI interface, The Master's Output pin is connected to the Slave's Input pin and the Master's Input pin is connected to the Slave's Output pin.

The MCP4XXX SPI's module supports two (of the four) standard SPI modes. These are Mode `0,0` and `1,1`. The SPI mode is determined by the state of the SCK pin ($V_{IH}$ or $V_{IL}$) on the when the $\overline{CS}$ pin transitions from inactive ($V_{IH}$) to active ($V_{IL}$ or $V_{IHH}$).

All SPI interface signals are high-voltage tolerant.




**Note 1:** If High voltage commands are desired, some type of external circuitry needs to be implemented.

**2:** $R_1$ must be sized to ensure $V_{IL}$ and $V_{IH}$ of the devices are met.

***FIGURE 6-1:*** *Typical SPI Interface Block Diagram.*

## 6.1 SDI, SDO, SCK, and $\overline{CS}$ Operation

The operation of the four SPI interface pins are discussed in this section. These pins are:

- SDI (Serial Data In)
- SDO (Serial Data Out)
- SCK (Serial Clock)
- $\overline{CS}$ (Chip Select)

The serial interface works on either 8-bit or 16-bit boundaries depending on the selected command. The Chip Select ($\overline{CS}$) pin frames the SPI commands.

### 6.1.1 SERIAL DATA IN (SDI)

The Serial Data In (SDI) signal is the data signal into the device. The value on this pin is latched on the rising edge of the SCK signal.

### 6.1.2 SERIAL DATA OUT (SDO)

The Serial Data Out (SDO) signal is the data signal out of the device. The value on this pin is driven on the falling edge of the SCK signal.

Once the $\overline{CS}$ pin is forced to the active level ($V_{IL}$ or $V_{IHH}$), the SDO pin will be driven. The state of the SDO pin is determined by the serial bit's position in the command, the command selected, and if there is a command error state (CMDERR).

### 6.1.3 SDI/SDO

| **Note:** | MCP41X1 Devices Only . |
|---|---|

For device packages that do not have enough pins for both an SDI and SDO pin, the SDI and SDO functionality is multiplexed onto a single I/O pin called SDI/SDO.

The SDO will only be driven for the command error bit (CMDERR) and during the data bits of a read command (after the memory address and command has been received).

#### 6.1.3.1 SDI/SDO Operation

Figure 6-2 shows a block diagram of the SDI/SDO pin. The SDI signal has an internal "smart" pull-up. The value of this pull-up determines the frequency that data can be read from the device. An external pull-up can be added to the SDI/SDO pin to improve the rise time and therefore improve the frequency that data can be read.

| **Note:** | To support the High voltage requirement of the SDI function, the SDO function is an open-drain output. |
|---|---|

Data written on the SDI/SDO pin can be at the maximum SPI frequency.

| **Note:** | Care must be take to ensure that a Drive conflict does not exist between the Host Controllers SDO pin (or software SDI/SDO pin) and the MCP41x1 SDI/SDO pin (see Figure 6-1). |
|---|---|

On the falling edge of the SCK pin during the C0 bit (see Figure 7-1), the SDI/SDO pin will start outputting the SDO value. The SDO signal overrides the control of the smart pull-up, such that whenever the SDI/SDO pin is outputting data, the smart pull-up is enabled.

The SDI/SDO pin will change from an input (SDI) to an output (SDO) after the state machine has received the Address and Command bits of the Command Byte. If the command is a Read command, then the SDI/SDO pin will remain an output for the remainder of the command. For any other command, the SDI/SDO pin returns to an input.

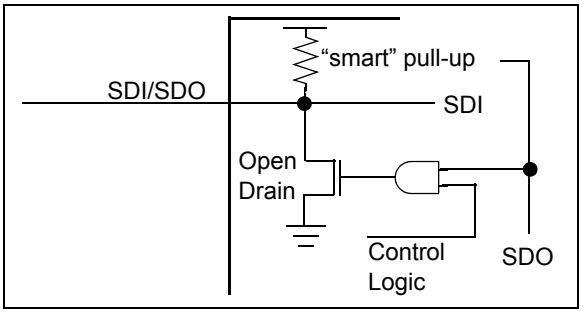



***FIGURE 6-2:*** *Serial I/O Mux Block Diagram.*

### 6.1.4 SERIAL CLOCK (SCK) (SPI FREQUENCY OF OPERATION)

The SPI interface is specified to operate up to 10 MHz. The actual clock rate depends on the configuration of the system and the serial command used. Table 6-1 shows the SCK frequency for different configurations.

**TABLE 6-1: SCK FREQUENCY**

| Memory Type Access | | Command | |
|---|---|---|---|
| | | Read | Write, Increment, Decrement |
| Non-Volatile Memory | SDI, SDO | 10 MHz | 10 MHz (2, 3) |
| | SDI/SDO (1) | 250 kHz (4) | 10 MHz (2, 3) |
| Volatile Memory | SDI, SDO | 10 MHz | 10 MHz |
| | SDI/SDO (1) | 250 kHz (4) | 10 MHz |

**Note 1:** MCP41X1 devices only

**2:** Non-Volatile memory does not support the Increment or Decrement command.

**3:** After a Write command, the internal write cycle must complete before the next SPI command is received.

**4:** This is the maximum clock frequency without an external pull-up resistor.

### 6.1.5 THE $\overline{CS}$ SIGNAL

The Chip Select ($\overline{CS}$) signal is used to select the device and frame a command sequence. To start a command, or sequence of commands, the $\overline{CS}$ signal must transition from the inactive state ($V_{IH}$) to an active state ($V_{IL}$ or $V_{IHH}$).

After the $\overline{CS}$ signal has gone active, the SDO pin is driven and the clock bit counter is reset.

| **Note:** | There is a required delay after the $\overline{CS}$ pin goes active to the 1st edge of the SCK pin. |
|---|---|

If an error condition occurs for an SPI command, then the Command byte's Command Error (CMDERR) bit (on the SDO pin) will be driven low ($V_{IL}$). To exit the error condition, the user must take the $\overline{CS}$ pin to the $V_{IH}$ level.

When the $\overline{CS}$ pin returns to the inactive state ($V_{IH}$) the SPI module resets (including the address pointer). While the $\overline{CS}$ pin is in the inactive state ($V_{IH}$), the serial interface is ignored. This allows the Host Controller to interface to other SPI devices using the same SDI, SDO, and SCK signals.

The $\overline{CS}$ pin has an internal pull-up resistor. The resistor is disabled when the voltage on the $\overline{CS}$ pin is at the $V_{IL}$ level. This means that when the $\overline{CS}$ pin is not driven, the internal pull-up resistor will pull this signal to the $V_{IH}$ level. When the $\overline{CS}$ pin is driven low ($V_{IL}$), the resistance becomes very large to reduce the device current consumption.

The high voltage capability of the $\overline{CS}$ pin allows High Voltage commands. High Voltage commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

## 6.2 The SPI Modes

The SPI module supports two (of the four) standard SPI modes. These are Mode 0,0 and 1,1. The mode is determined by the state of the SDI pin on the rising edge of the 1st clock bit (of the 8-bit byte).

### 6.2.1 MODE 0,0

In **Mode 0,0**: SCK idle state = low ($V_{IL}$), data is clocked in on the SDI pin on the rising edge of SCK and clocked out on the SDO pin on the falling edge of SCK.

### 6.2.2 MODE 1,1

In **Mode 1,1**: SCK idle state = high ($V_{IH}$), data is clocked in on the SDI pin on the rising edge of SCK and clocked out on the SDO pin on the falling edge of SCK.

## 6.3 SPI Waveforms

Figure 6-3 through Figure 6-8 show the different SPI command waveforms. Figure 6-3 and Figure 6-4 are read and write commands. Figure 6-5 and Figure 6-6 are read commands when the SDI and SDO pins are multiplexed on the same pin (SDI/SDO). Figure 6-7 and Figure 6-8 are increment and decrement commands. The high voltage increment and decrement commands are used to enable and disable WiperLock Technology and Write Protect.

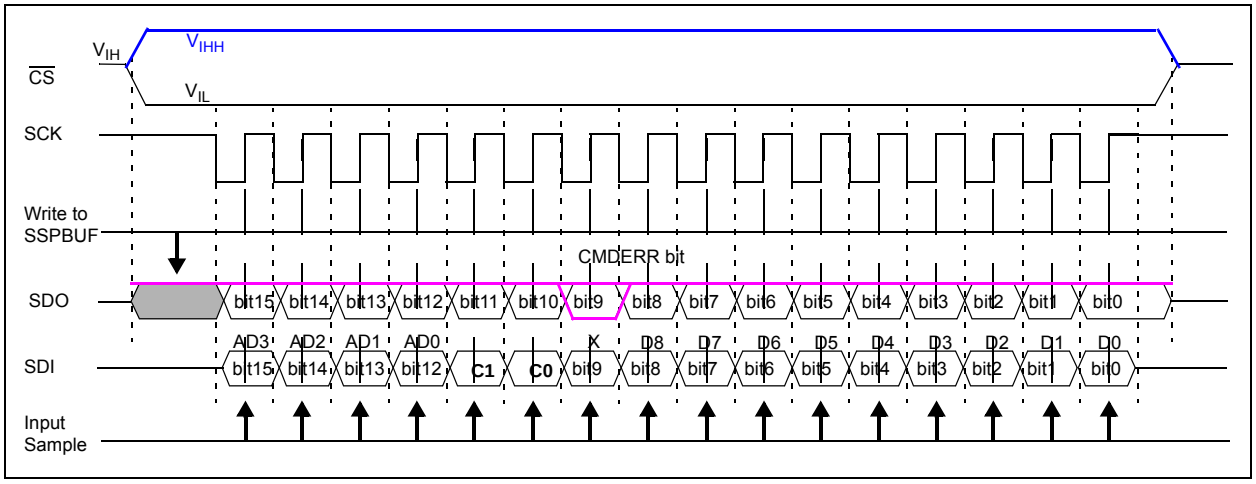



***FIGURE 6-3:*** *16-Bit Commands (Write, Read) - SPI Waveform (Mode 1,1).*

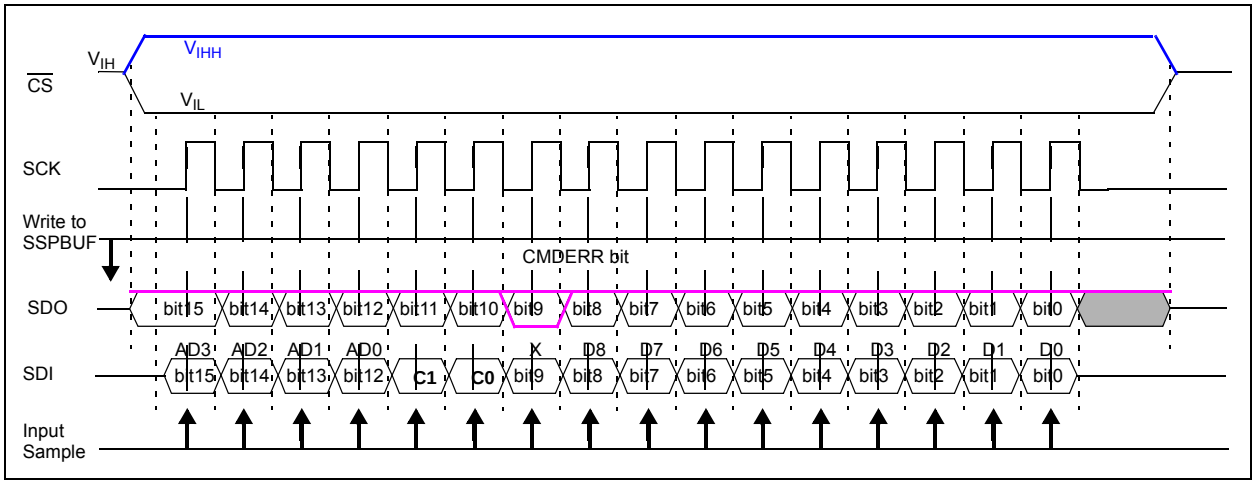
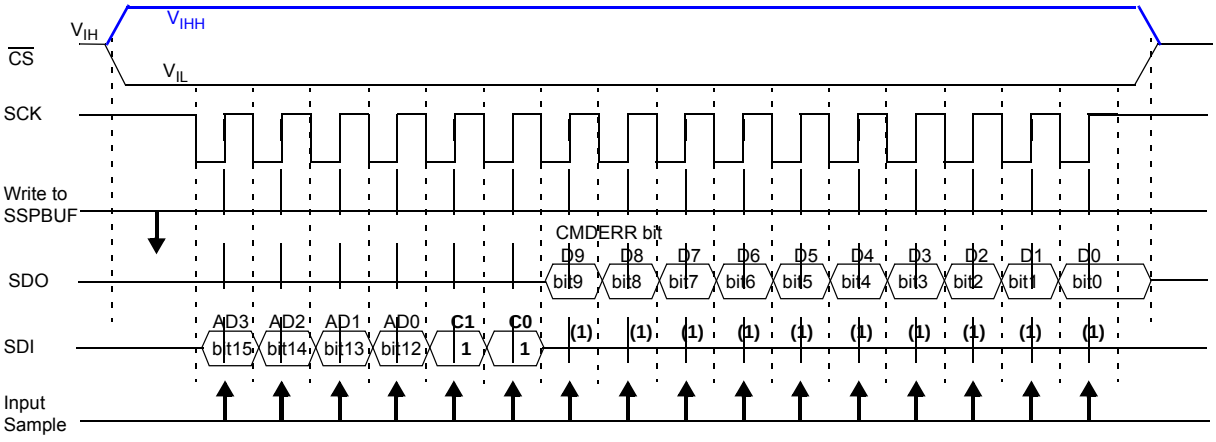
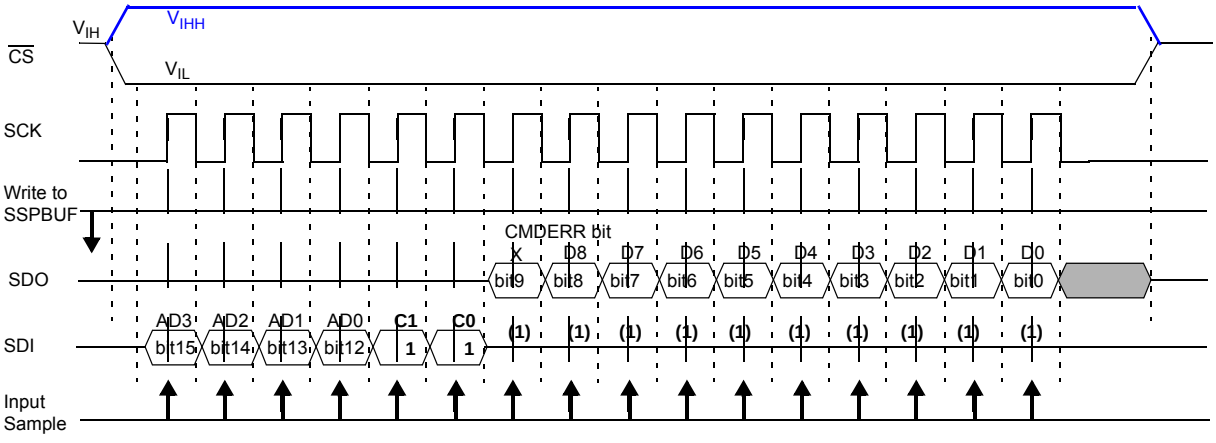



***FIGURE 6-4:*** *16-Bit Commands (Write, Read) - SPI Waveform (Mode 0,0).*




**Note 1:** The SDI pin will read the state of the SDI pin which will be the SDO signal, unless overdriven

***FIGURE 6-5:*** *16-Bit Read Command for Devices with SDI/SDO multiplexed - SPI Waveform (Mode 1,1).*




**Note 1:** The SDI pin will read the state of the SDI pin which will be the SDO signal, unless overdriven

***FIGURE 6-6:*** *16-Bit Read Command for Devices with SDI/SDO multiplexed - SPI Waveform (Mode 0,0).*

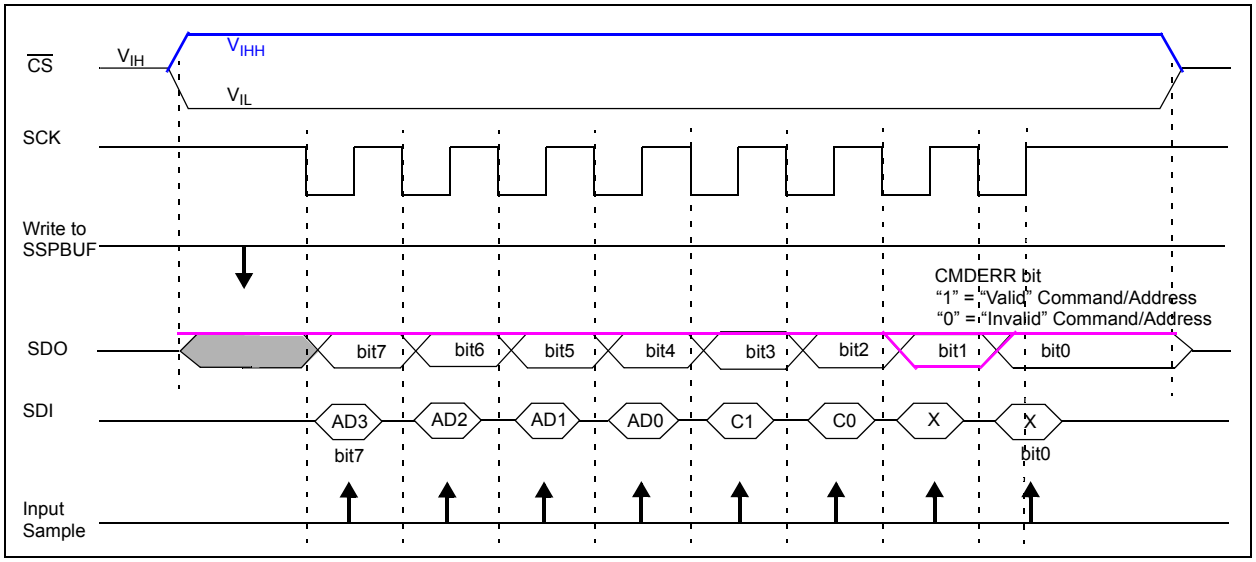



***FIGURE 6-7:*** *8-Bit Commands (Increment, Decrement, Modify Write Protect or WiperLock Technology) - SPI Waveform with PIC MCU (Mode 1,1).*

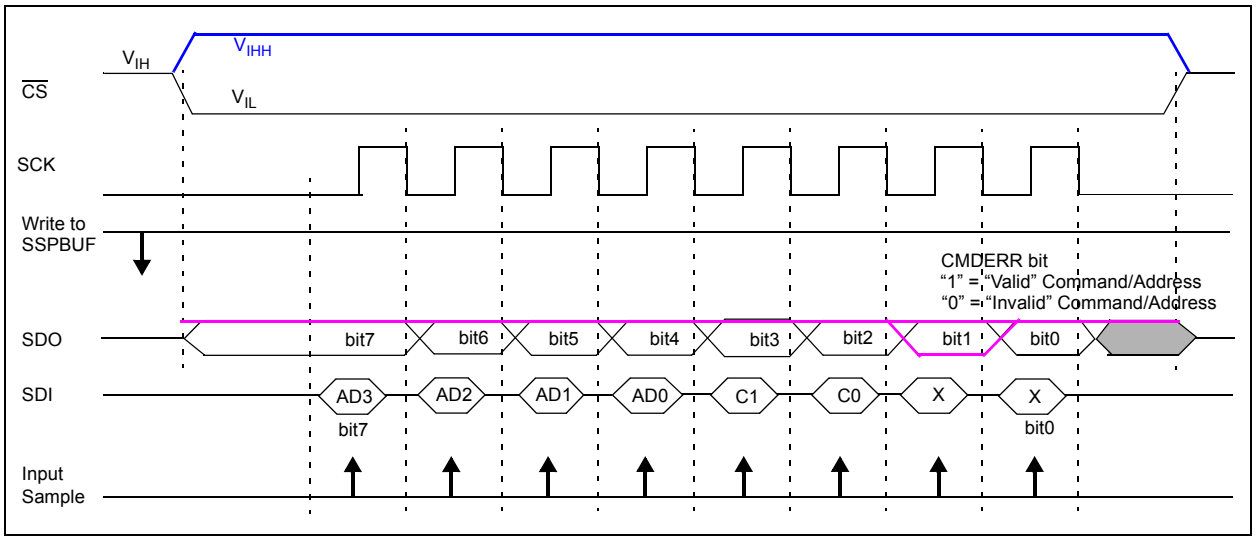



***FIGURE 6-8:*** *8-Bit Commands (Increment, Decrement, Modify Write Protect or WiperLock Technology) - SPI Waveform with PIC MCU (Mode 0,0).*

## 7.0 DEVICE COMMANDS

The MCP4XXX's SPI command format supports 16 memory address locations and four commands. Each command has two modes. These are:

- Normal Serial Commands
- High-Voltage Serial Commands

Normal serial commands are those where the $\overline{CS}$ pin is driven to $V_{IL}$. With High-Voltage Serial Commands, the $\overline{CS}$ pin is driven to $V_{IHH}$. In each mode, there are four possible commands. These commands are shown in Table 7-1.

The 8-bit commands (**Increment Wiper** and **Decrement Wiper** commands) contain a Command Byte, see Figure 7-1, while 16-bit commands (**Read Data** and **Write Data** commands) contain a Command Byte and a Data Byte. The Command Byte contains two data bits, see Figure 7-1.

Table 7-2 shows the supported commands for each memory location and the corresponding values on the SDI and SDO pins.

Table 7-3 shows an overview of all the SPI commands and their interaction with other device features.

### 7.1 Command Byte

The Command Byte has three fields, the Address, the Command, and 2 Data bits, see Figure 7-1. Currently only one of the data bits is defined (D8). This is for the Write command.

The device memory is accessed when the master sends a proper Command Byte to select the desired operation. The memory location getting accessed is contained in the Command Byte's AD3:AD0 bits. The action desired is contained in the Command Byte's C1:C0 bits, see Table 7-1. C1:C0 determines if the desired memory location will be read, written, Incremented (wiper setting +1) or Decremented (wiper setting -1). The Increment and Decrement commands are only valid on the volatile wiper registers, and in High Voltage commands to enable/disable WiperLock Technology and Software Write Protect.

As the Command Byte is being loaded into the device (on the SDI pin), the device's SDO pin is driving. The SDO pin will output high bits for the first six bits of that command. On the 7th bit, the SDO pin will output the CMDERR bit state (see **Section 7.3 "Error Condition"**). The 8th bit state depends on the the command selected.

**TABLE 7-1: COMMAND BIT OVERVIEW**

| C1:C0 Bit States | Command | # of Bits | Operates on Volatile/ Non-Volatile memory |
|---|---|---|---|
| 11 | Read Data | 16-Bits | Both |
| 00 | Write Data | 16-Bits | Both |
| 01 | Increment (1) | 8-Bits | Volatile Only |
| 10 | Decrement (1) | 8-Bits | Volatile Only |

**Note 1:** High Voltage Increment and Decrement commands on select non-volatile memory locations enable/disable WiperLock Technology and the software Write Protect feature.

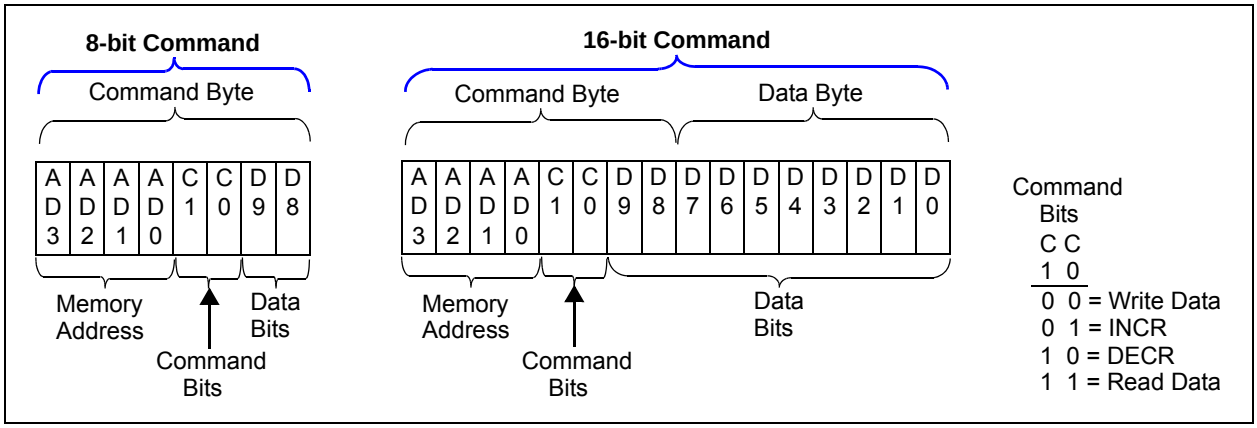



***FIGURE 7-1:*** *General SPI Command Formats.*

**TABLE 7-2: MEMORY MAP AND THE SUPPORTED COMMANDS**

| Address | | Command | Data (10-bits) (1) | SPI String (Binary) | |
|---|---|---|---|---|---|
| Value | Function | | | MOSI (SDI pin) | MISO (SDO pin) (2) |
| 00h | Volatile Wiper 0 | Write Data | nn nnnn nnnn | 0000 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 0000 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| | | Increment Wiper | — | 0000 0100 | 1111 1111 |
| | | Decrement Wiper | — | 0000 1000 | 1111 1111 |
| 01h | Volatile Wiper 1 | Write Data | nn nnnn nnnn | 0001 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 0001 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| | | Increment Wiper | — | 0001 0100 | 1111 1111 |
| | | Decrement Wiper | — | 0001 1000 | 1111 1111 |
| 02h | NV Wiper 0 | Write Data | nn nnnn nnnn | 0010 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 0010 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| | | HV Inc. (WL0 DIS) (3) | — | 0010 0100 | 1111 1111 |
| | | HV Dec. (WL0 EN) (4) | — | 0010 1000 | 1111 1111 |
| 03h | NV Wiper 1 | Write Data | nn nnnn nnnn | 0011 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 0011 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| | | HV Inc. (WL1 DIS) (3) | — | 0011 0100 | 1111 1111 |
| | | HV Dec. (WL1 EN) (4) | — | 0011 1000 | 1111 1111 |
| 04h (5) | Volatile TCON Register | Write Data | nn nnnn nnnn | 0100 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 0100 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 05h (5) | Status Register | Read Data | nn nnnn nnnn | 0101 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 06h (5) | Data EEPROM | Write Data | nn nnnn nnnn | 0110 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 0110 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 07h (5) | Data EEPROM | Write Data | nn nnnn nnnn | 0111 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 0111 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 08h (5) | Data EEPROM | Write Data | nn nnnn nnnn | 1000 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 1000 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 09h (5) | Data EEPROM | Write Data | nn nnnn nnnn | 1001 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 1001 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 0Ah (5) | Data EEPROM | Write Data | nn nnnn nnnn | 1010 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 1010 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 0Bh (5) | Data EEPROM | Write Data | nn nnnn nnnn | 1011 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 1011 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 0Ch (5) | Data EEPROM | Write Data | nn nnnn nnnn | 1100 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 1100 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 0Dh (5) | Data EEPROM | Write Data | nn nnnn nnnn | 1101 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 1101 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 0Eh (5) | Data EEPROM | Write Data | nn nnnn nnnn | 1110 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 1110 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| 0Fh | Data EEPROM | Write Data | nn nnnn nnnn | 1111 00nn nnnn nnnn | 1111 1111 1111 1111 |
| | | Read Data | nn nnnn nnnn | 1111 11nn nnnn nnnn | 1111 111n nnnn nnnn |
| | | HV Inc. (WP DIS) (3) | — | 1111 0100 | 1111 1111 |
| | | HV Dec. (WP EN) (4) | — | 1111 1000 | 1111 1111 |

**Note 1:** The Data Memory is only 9-bits wide, so the MSb is ignored by the device.

**2:** All these Address/Command combinations are valid, so the CMDERR bit is set. Any other Address/Command combination is a command error state and the CMDERR bit will be clear.

**3:** Disables WiperLock Technology for wiper 0 or wiper 1, or disables Write Protect.

**4:** Enables WiperLock Technology for wiper 0 or wiper 1, or enables Write Protect.

**5:** **Reserved addresses**: Increment or Decrement commands are invalid for these addresses.

## 7.2 Data Byte

Only the Read Command and the Write Command use the Data Byte, see Figure 7-1. These commands concatenate the 8-bits of the Data Byte with the one data bit (D8) contained in the Command Byte to form 9-bits of data (D8:D0). The Command Byte format supports up to 9-bits of data so that the 8-bit resistor network can be set to Full Scale (100h or greater). This allows wiper connections to Terminal A and to Terminal B.

The D9 bit is currently unused, and corresponds to the position on the SDO data of the CMDERR bit.

## 7.3 Error Condition

The CMDERR bit indicates if the four address bits received (AD3:AD0) and the two command bits received (C1:C0) are a valid combination (see Table 4-1). The CMDERR bit is high if the combination is valid and low if the combination is invalid.

The command error bit will also be low if a write to a Non-Volatile Address has been specified and another SPI command occurs before the $\overline{CS}$ pin is driven inactive ($V_{IH}$).

SPI commands that do not have a multiple of 8 clocks are ignored.

Once an error condition has occurred, any following commands are ignored. All following SDO bits will be low until the CMDERR condition is cleared by forcing the $\overline{CS}$ pin to the inactive state ($V_{IH}$).

### 7.3.1 ABORTING A TRANSMISSION

All SPI transmissions must have the correct number of SCK pulses to be executed. The command is not executed until the complete number of clocks have been received. Some commands also require the $\overline{CS}$ pin to be forced inactive ($V_{IH}$). If the $\overline{CS}$ pin is forced to the inactive state ($V_{IH}$) the serial interface is reset. Partial commands are not executed.

SPI is more susceptible to noise than other bus protocols. The most likely case is that this noise corrupts the value of the data being clocked into the MCP4XXX or the SCK pin is injected with extra clock pulses. This may cause data to be corrupted in the device, or a command error to occur, since the address and command bits were not a valid combination. The extra SCK pulse will also cause the SPI data (SDI) and clock (SCK) to be out of sync. Forcing the $\overline{CS}$ pin to the inactive state ($V_{IH}$) resets the serial interface. The SPI interface will ignore activity on the SDI and SCK pins until the $\overline{CS}$ pin transition to the active state is detected ($V_{IH}$ to $V_{IL}$ or $V_{IH}$ to $V_{IHH}$).

**Note 1:** When data is not being received by the MCP4XXX, It is recommended that the $\overline{CS}$ pin be forced to the inactive level ($V_{IL}$)

**2:** It is also recommended that long continuous command strings should be broken down into single commands or shorter continuous command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI commands.

## 7.4 Continuous Commands

The device supports the ability to execute commands continuously. While the $\overline{CS}$ pin is in the active state ($V_{IL}$ or $V_{IHH}$). Any sequence of valid commands may be received.

The following example is a valid sequence of events:

1. $\overline{CS}$ pin driven active ($V_{IL}$ or $V_{IHH}$).
2. Read Command.
3. Increment Command (Wiper 0).
4. Increment Command (Wiper 0).
5. Decrement Command (Wiper 1).
6. Write Command (Volatile memory).
7. Write Command (Non-Volatile memory).
8. $\overline{CS}$ pin driven inactive ($V_{IH}$).

**Note 1:** It is recommended that while the $\overline{CS}$ pin is active, only one type of command should be issued. When changing commands, it is recommended to take the $\overline{CS}$ pin inactive then force it back to the active state.

**2:** It is also recommended that long command strings should be broken down into shorter command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI command string.

**TABLE 7-3: COMMANDS**

| Command Name | # of Bits | Writes Value in EEPROM | Operates on Volatile/ Non-Volatile memory | High Voltage ($V_{IHH}$) on CS pin? | Impact on WiperLock or Write Protect | Works when Wiper is "locked"? |
|---|---|---|---|---|---|---|
| **Write Data** | 16-Bits | Yes (1) | Both | — | unlocked (1) | No |
| **Read Data** | 16-Bits | — | Both | — | unlocked (1) | No |
| **Increment Wiper** | 8-Bits | — | Volatile Only | — | unlocked (1) | No |
| **Decrement Wiper** | 8-Bits | — | Volatile Only | — | unlocked (1) | No |
| High Voltage **Write Data** | 16-Bits | Yes | Both | Yes | unchanged | No |
| High Voltage **Read Data** | 16-Bits | — | Both | Yes | unchanged | Yes |
| High Voltage **Increment Wiper** | 8-Bits | — | Volatile Only | Yes | unchanged | No |
| High Voltage **Decrement Wiper** | 8-Bits | — | Volatile Only | Yes | unchanged | No |
| **Modify Write Protect or Wiper-Lock Technology (High Voltage)** - Enable | 8-Bits | — (2) | Non-Volatile Only (2) | Yes | locked/ protected (2) | Yes |
| **Modify Write Protect or Wiper-Lock Technology (High Voltage)** - Disable | 8-Bits | — (3) | Non-Volatile Only (3) | Yes | unlocked/ unprotected (3) | Yes |

**Note 1:** This command will only complete if wiper is "unlocked" (WiperLock Technology is Disabled).

**2:** If the command is executed using address 02h or 03h, then that corresponding wiper is locked or if with address 0Fh, then Write Protect is enabled.

**3:** If the command is executed using with address 02h or 03h, then that corresponding wiper is unlocked or if with address 0Fh, then Write Protect is disabled.

## 7.5 Write Data Normal and High Voltage

The Write command is a 16-bit command. The Write Command can be issued to both the Volatile and Non-Volatile memory locations. The format of the command is shown in Figure 7-2.

A Write command to a Volatile memory location changes that location after a properly formatted Write Command (16-clock) have been received.

A Write command to a Non-Volatile memory location will only start a write cycle after a properly formatted Write Command (16-clock) have been received and the $\overline{CS}$ pin transitions to the inactive state ($V_{IH}$).

| **Note:** | Writes to certain memory locations will be dependant on the state of the WiperLock Technology bits and the Write Protect bit. |
|---|---|

### 7.5.1 SINGLE WRITE TO VOLATILE MEMORY

The write operation requires that the $\overline{CS}$ pin be in the active state ($V_{IL}$ or $V_{IHH}$). Typically, the $\overline{CS}$ pin will be in the inactive state ($V_{IH}$) and is driven to the active state ($V_{IL}$). The 16-bit Write Command (Command Byte and Data Byte) is then clocked in on the SCK and SDI pins. Once all 16 bits have been received, the specified volatile address is updated. A write will not occur if the write command isn't exactly 16 clocks pulses. This protects against system issues from corrupting the Non-Volatile memory locations.

Figure 6-3 and Figure 6-4 show possible waveforms for a single write.

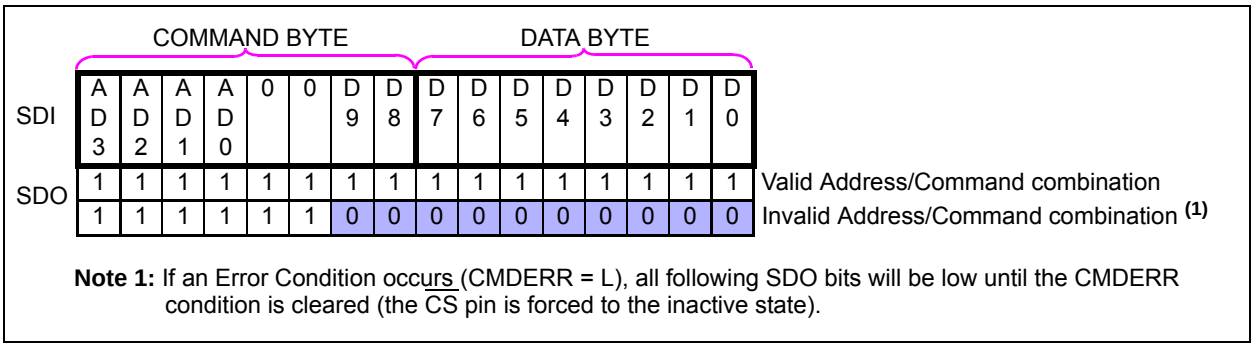
### 7.5.2 SINGLE WRITE TO NON-VOLATILE MEMORY

The sequence to write to to a single non-volatile memory location is the same as a single write to volatile memory with the exception that after the $\overline{CS}$ pin is driven inactive ($V_{IH}$), the EEPROM write cycle ($t_{WC}$) is started. A write cycle will not start if the write command isn't exactly 16 clocks pulses. This protects against system issues from corrupting the Non-Volatile memory locations.

After the $\overline{CS}$ pin is driven inactive ($V_{IH}$), the serial interface may immediately be re-enabled by driving the $\overline{CS}$ pin to the active state ($V_{IL}$ or $V_{IHH}$).

During an EEPROM write cycle, only serial commands to Volatile memory (addresses 00h, 01h, 04h, and 05h) are accepted. All other serial commands are ignored until the EEPROM write cycle ($t_{wc}$) completes. This allows the Host Controller to operate on the Volatile Wiper registers and the TCON register, and to Read the Status Register. The EEWA bit in the Status register indicates the status of an EEPROM Write Cycle.

Once a write command to a Non-Volatile memory location has been received, NO other SPI commands should be received before the $\overline{CS}$ pin transitions to the inactive state ($V_{IH}$) or the current SPI command will have a Command Error (CMDERR) occur.




**Note 1:** If an Error Condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

***FIGURE 7-2:*** *Write Command - SDI and SDO States.*

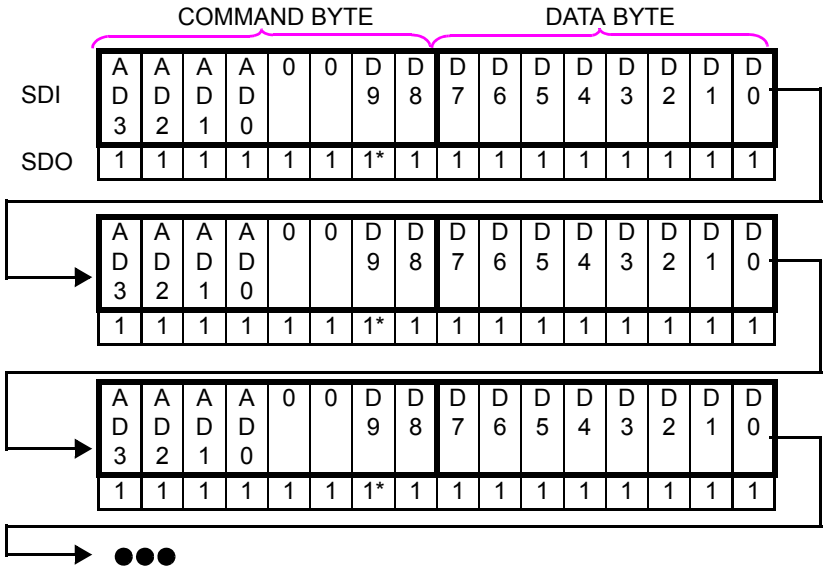
### 7.5.3 CONTINUOUS WRITES TO VOLATILE MEMORY

Continuous writes are possible only when writing to the volatile memory registers (address 00h, 01h, and 04h).

Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

### 7.5.4 CONTINUOUS WRITES TO NON-VOLATILE MEMORY

Continuous writes to non-volatile memory are not allowed, and attempts to do so will result in a command error (CMDERR) condition.




**Note 1:** If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the CS pin is driven inactive ($V_{IH}$).

***FIGURE 7-3:*** *Continuous Write Sequence (Volatile Memory only).*

## 7.6 Read Data Normal and High Voltage

The Read command is a 16-bit command. The Read Command can be issued to both the Volatile and Non-Volatile memory locations. The format of the command is shown in Figure 7-4.

The first 6-bits of the Read command determine the address and the command. The 7th clock will output the CMDERR bit on the SDO pin. The remaining 9-clocks the device will transmit the 9 data bits (D8:D0) of the specified address (AD3:AD0).

Figure 7-4 shows the SDI and SDO information for a Read command.

During a write cycle (Write or High Voltage Write to a Non-Volatile memory location) the Read command can only read the Volatile memory locations. By reading the Status Register (04h), the Host Controller can determine when the write cycle has completed (via the state of the EEWA bit).

### 7.6.1 SINGLE READ

The read operation requires that the $\overline{CS}$ pin be in the active state ($V_{IL}$ or $V_{IHH}$). Typically, the $\overline{CS}$ pin will be in the inactive state ($V_{IH}$) and is driven to the active state ($V_{IL}$ or $V_{IHH}$). The 16-bit Read Command (Command Byte and Data Byte) is then clocked in on the SCK and SDI pins. The SDO pin starts driving data on the 7th bit (CMDERR bit) and the addressed data comes out on the 8th through 16th clocks. Figure 6-3 through Figure 6-6 show possible waveforms for a single read.

Figure 6-5 and Figure 6-6 show the single read waveforms when the SDI and SDO signals are multiplexed on the same pin. For additional information on the multiplexing of these signals, refer to **Section 6.1.3 “SDI/SDO”**.

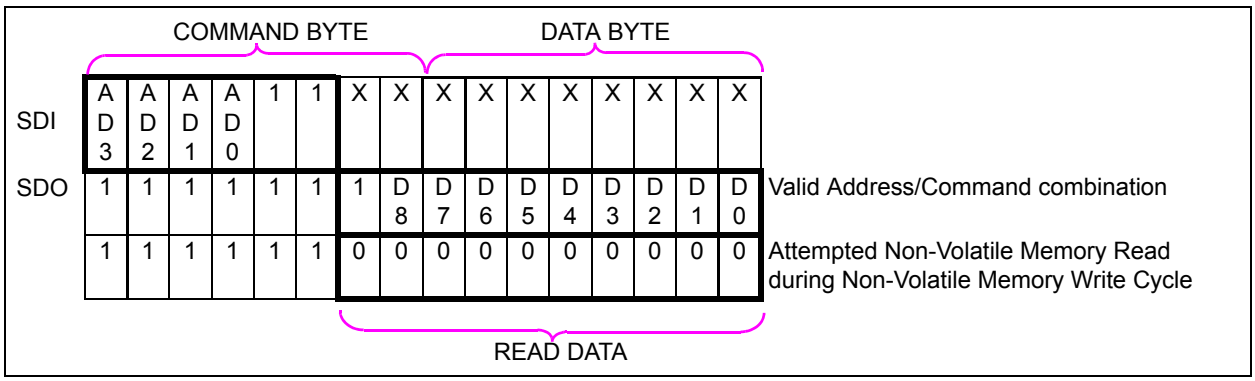
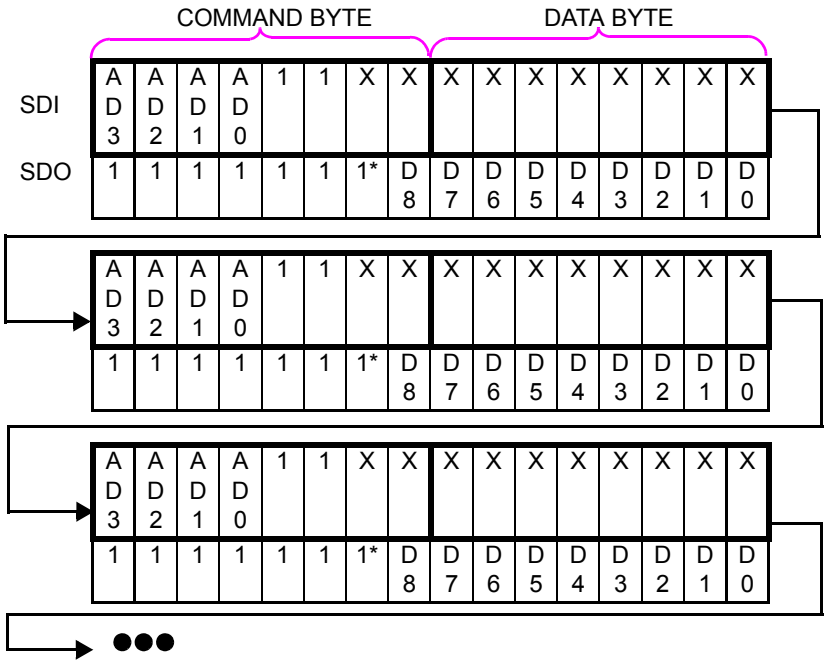



***FIGURE 7-4:*** *Read Command - SDI and SDO States.*

### 7.6.2 CONTINUOUS READS

Continuous reads allows the devices memory to be read quickly. Continuous reads are possible to all memory locations. If a non-volatile memory write cycle is occurring, then Read commands may only access the volatile memory locations.

Figure 7-5 shows the sequence for three continuous reads. The reads do not need to be to the same memory address.




**Note 1:** If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the $\overline{CS}$ pin is driven inactive ($V_{IH}$).

***FIGURE 7-5:*** *Continuous Read Sequence.*

## 7.7 Increment Wiper Normal and High Voltage

The Increment Command is an 8-bit command. The Increment Command can only be issued to volatile memory locations. The format of the command is shown in Figure 7-6.

An Increment Command to the volatile memory location changes that location after a properly formatted command (8-clocks) have been received.

Increment commands provide a quick and easy method to modify the value of the volatile wiper location by +1 with minimal overhead.

COMMAND BYTE

(INCR COMMAND (n+1) )

| | AD3 | AD2 | AD1 | AD0 | 0 | 1 | X | X | |
|---|---|---|---|---|---|---|---|---|---|
| SDI | | | | | | | | | |
| SDO | 1 | 1 | 1 | 1 | 1 | 1 | 1* | 1 | **Note 1, 2** |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **Note 1, 3** |

**Note 1:** Only functions when writing the volatile wiper registers (AD3:AD0) 0h and 1h.

**2:** Valid Address/Command combination.

**3:** Invalid Address/Command combination all following SDO bits will be low until the CMDERR condition is cleared. (the $\overline{CS}$ pin is forced to the inactive state).

**4:** If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the $\overline{CS}$ pin is driven inactive ($V_{IH}$).

***FIGURE 7-6:*** *Increment Command - SDI and SDO States.*

**Note:** Table 7-2 shows the valid addresses for the Increment Wiper command. Other addresses are invalid.

### 7.7.1 SINGLE INCREMENT

Typically, the $\overline{CS}$ pin starts at the inactive state ($V_{IH}$), but may be already be in the active state due to the completion of another command.

Figure 6-7 through Figure 6-8 show possible waveforms for a single increment. The increment operation requires that the $\overline{CS}$ pin be in the active state ($V_{IL}$ or $V_{IHH}$). Typically, the $\overline{CS}$ pin will be in the inactive state ($V_{IH}$) and is driven to the active state ($V_{IL}$ or $V_{IHH}$). The 8-bit Increment Command (Command Byte) is then clocked in on the SDI pin by the SCK pins. The SDO pin drives the CMDERR bit on the 7th clock.

The wiper value will increment up to 100h on 8-bit devices and 80h on 7-bit devices. After the wiper value has reached Full Scale (8-bit =100h, 7-bit =80h), the wiper value will not be incremented further. If the Wiper register has a value between 101h and 1FFh, the Increment command is disabled. See Table 7-4 for additional information on the Increment Command versus the current volatile wiper value.

The Increment operations only require the Increment command byte while the $\overline{CS}$ pin is active ($V_{IL}$ or $V_{IHH}$) for a single increment.

After the wiper is incremented to the desired position, the $\overline{CS}$ pin should be forced to $V_{IH}$ to ensure that unexpected transitions on the SCK pin do not cause the wiper setting to change. Driving the $\overline{CS}$ pin to $V_{IH}$ should occur as soon as possible (within device specifications) after the last desired increment occurs.

**TABLE 7-4: INCREMENT OPERATION VS. VOLATILE WIPER VALUE**

| Current Wiper Setting | | Wiper (W) Properties | Increment Command Operates? |
|---|---|---|---|
| 7-bit Pot | 8-bit Pot | | |
| 3FFh<br>081h | 3FFh<br>101h | Reserved<br>(Full-Scale (W = A)) | No |
| 080h | 100h | Full-Scale (W = A) | No |
| 07Fh<br>041h | 0FFh<br>081 | W = N | Yes |
| 040h | 080h | W = N (Mid-Scale) | |
| 03Fh<br>001h | 07Fh<br>001 | W = N | |
| 000h | 000h | Zero Scale (W = B) | Yes |

### 7.7.2 CONTINUOUS INCREMENTS

Continuous Increments are possible only when writing to the volatile memory registers (address 00h, and 01h).

Figure 7-7 shows a Continuous Increment sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

When executing an continuous Increment commands, the selected wiper will be altered from n to n+1 for each Increment command received. The wiper value will increment up to 100h on 8-bit devices and 80h on 7-bit devices. After the wiper value has reached Full-Scale (8-bit =100h, 7-bit =80h), the wiper value will not be incremented further. If the Wiper register has a value between 101h and 1FFh, the Increment command is disabled.

Increment commands can be sent repeatedly without raising $\overline{CS}$ until a desired condition is met. The value in the Volatile Wiper register can be read using a Read Command and written to the corresponding Non-Volatile Wiper EEPROM using a Write Command.

When executing a continuous command string, The Increment command can be followed by any other valid command.

The wiper terminal will move after the command has been received (8th clock).

After the wiper is incremented to the desired position, the $\overline{CS}$ pin should be forced to $V_{IH}$ to ensure that unexpected transitions (on the SCK pin do not cause the wiper setting to change). Driving the $\overline{CS}$ pin to $V_{IH}$ should occur as soon as possible (within device specifications) after the last desired increment occurs.

| | COMMAND BYTE (INCR COMMAND (n+1) ) | | | | | | | | COMMAND BYTE (INCR COMMAND (n+2) ) | | | | | | | | COMMAND BYTE (INCR COMMAND (n+3) ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SDI | AD3 | AD2 | AD1 | AD0 | 0 | 1 | X | X | AD3 | AD2 | AD1 | AD0 | 0 | 1 | X | X | AD3 | AD2 | AD1 | AD0 | 0 | 1 | X | X | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1* | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1* | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1* | 1 | **Note 1, 2** |
| SDO | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Note 3, 4** |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Note 3, 4** |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **Note 3, 4** |

**Note 1:** Only functions when writing the volatile wiper registers (AD3:AD0) 0h and 1h.

**2:** Valid Address/Command combination.

**3:** Invalid Address/Command combination.

**4:** If an Error Condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

***FIGURE 7-7:*** *Continuous Increment Command - SDI and SDO States.*

## 7.8 Decrement Wiper Normal and High Voltage

The Decrement Command is an 8-bit command. The Decrement Command can only be issued to volatile memory locations. The format of the command is shown in Figure 7-6.

An Decrement Command to the volatile memory location changes that location after a properly formatted command (8-clocks) have been received.

Decrement commands provide a quick and easy method to modify the value of the volatile wiper location by -1 with minimal overhead.

COMMAND BYTE

(DECR COMMAND (n+1))

| | AD3 | AD2 | AD1 | AD0 | 1 | 0 | X | X | |
|---|---|---|---|---|---|---|---|---|---|
| SDI | | | | | | | | | |
| SDO | 1 | 1 | 1 | 1 | 1 | 1 | 1* | 1 | **Note 1, 2** |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **Note 1, 3** |

**Note 1:** Only functions when writing the volatile wiper registers (AD3:AD0) 0h and 1h.

**2:** Valid Address/Command combination.

**3:** Invalid Address/Command combination all following SDO bits will be low until the CMDERR condition is cleared. (the $\overline{CS}$ pin is forced to the inactive state).

**4:** If a Command Error (CMDERR) occurs at this bit location (*), then all following SDO bits will be driven low until the $\overline{CS}$ pin is driven inactive ($V_{IH}$).

***FIGURE 7-8:*** *Decrement Command - SDI and SDO States.*

**Note:** Table 7-2 shows the valid addresses for the Decrement Wiper command. Other addresses are invalid.

### 7.8.1 SINGLE DECREMENT

Typically the $\overline{CS}$ pin starts at the inactive state ($V_{IH}$), but may be already be in the active state due to the completion of another command.

Figure 6-7 through Figure 6-8 show possible waveforms for a single Decrement. The decrement operation requires that the $\overline{CS}$ pin be in the active state ($V_{IL}$ or $V_{IHH}$). Typically the $\overline{CS}$ pin will be in the inactive state ($V_{IH}$) and is driven to the active state ($V_{IL}$ or $V_{IHH}$). Then the 8-bit Decrement Command (Command Byte) is clocked in on the SDI pin by the SCK pins. The SDO pin drives the CMDERR bit on the 7th clock.

The wiper value will decrement from the wipers Full Scale value (100h on 8-bit devices and 80h on 7-bit devices). Above the wipers Full Scale value (8-bit =101h to 1FFh, 7-bit = 81h to FFh), the decrement command is disabled. If the Wiper register has a Zero Scale value (000h), then the wiper value will not decrement. See Table 7-4 for additional information on the Decrement Command vs. the current volatile wiper value.

The Decrement commands only require the Decrement command byte, while the $\overline{CS}$ pin is active ($V_{IL}$ or $V_{IHH}$) for a single decrement.

After the wiper is decremented to the desired position, the $\overline{CS}$ pin should be forced to $V_{IH}$ to ensure that unexpected transitions on the SCK pin do not cause the wiper setting to change. Driving the $\overline{CS}$ pin to $V_{IH}$ should occur as soon as possible (within device specifications) after the last desired decrement occurs.

**TABLE 7-5: DECREMENT OPERATION VS. VOLATILE WIPER VALUE**

| Current Wiper Setting | | Wiper (W) Properties | Decrement Command Operates? |
|---|---|---|---|
| 7-bit Pot | 8-bit Pot | | |
| 3FFh<br>081h | 3FFh<br>101h | Reserved<br>(Full-Scale (W = A)) | No |
| 080h | 100h | Full-Scale (W = A) | Yes |
| 07Fh<br>041h | 0FFh<br>081 | W = N | Yes |
| 040h | 080h | W = N (Mid-Scale) | |
| 03Fh<br>001h | 07Fh<br>001 | W = N | |
| 000h | 000h | Zero Scale (W = B) | No |

### 7.8.2 CONTINUOUS DECREMENTS

Continuous Decrements are possible only when writing to the volatile memory registers (address 00h, 01h, and 04h).

Figure 7-9 shows a continuous Decrement sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

When executing an continuous Decrement commands, the selected wiper will be altered from n to n-1 for each Decrement command received. The wiper value will decrement from the wipers Full Scale value (100h on 8-bit devices and 80h on 7-bit devices). Above the wipers Full-Scale value (8-bit =101h to 1FFh, 7-bit = 81h to FFh), the decrement command is disabled. If the Wiper register has a Zero Scale value (000h), then the wiper value will not decrement. See Table 7-4 for additional information on the Decrement Command vs. the current volatile wiper value.

Decrement commands can be sent repeatedly without raising $\overline{CS}$ until a desired condition is met. The value in the Volatile Wiper register can be read using a Read Command and written to the corresponding Non-Volatile Wiper EEPROM using a Write Command.

When executing a continuous command string, The Decrement command can be followed by any other valid command.

The wiper terminal will move after the command has been received (8th clock).

After the wiper is decremented to the desired position, the $\overline{CS}$ pin should be forced to $V_{IH}$ to ensure that "unexpected" transitions (on the SCK pin do not cause the wiper setting to change). Driving the $\overline{CS}$ pin to $V_{IH}$ should occur as soon as possible (within device specifications) after the last desired decrement occurs.

| | COMMAND BYTE (DECR COMMAND (n-1) ) | | | | | | | | COMMAND BYTE (DECR COMMAND (n-1) ) | | | | | | | | COMMAND BYTE (DECR COMMAND (n-1) ) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SDI | AD3 | AD2 | AD1 | AD0 | 1 | 0 | X | X | AD3 | AD2 | AD1 | AD0 | 1 | 0 | X | X | AD3 | AD2 | AD1 | AD0 | 1 | 0 | X | X | |
| SDO | 1 | 1 | 1 | 1 | 1 | 1 | 1* | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1* | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1* | 1 | **Note 1, 2** |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Note 3, 4** |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Note 3, 4** |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **Note 3, 4** |

**Note 1:** Only functions when writing the volatile wiper registers (AD3:AD0) 0h and 1h.

**2:** Valid Address/Command combination.

**3:** Invalid Address/Command combination.

**4:** If an Error Condition occurs (CMDERR = L), all following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the inactive state).

***FIGURE 7-9:*** *Continuous Decrement Command - SDI and SDO States.*

## 7.9 Modify Write Protect or WiperLock Technology (High Voltage) Enable and Disable

This command is a special case of the High Voltage **Decrement Wiper** and High Voltage **Increment Wiper** commands to the non-volatile memory locations 02h, 03h, and 0Fh. This command is used to enable or disable either the software Write Protect, wiper 0 WiperLock Technology, or wiper 1 WiperLock Technology. Table 7-6 shows the memory addresses, the High Voltage command and the result of those commands on the non-volatile WP, WL0, 0r WL1 bits. The format of the command is shown in Figure 7-8 (Enable) or Figure 7-6 (Disable).

### 7.9.1 SINGLE ENABLE WRITE PROTECT OR WIPERLOCK TECHNOLOGY (HIGH VOLTAGE)

Figure 6-7 through Figure 6-8 show possible waveforms for a single Modify Write Protect or WiperLock Technology command.

A Modify Write Protect or WiperLock Technology Command will only start an EEPROM write cycle ($t_{WC}$) after a properly formatted Command (8-clocks) has been received and the $\overline{CS}$ pin transitions to the inactive state ($V_{IH}$).

After the $\overline{CS}$ pin is driven inactive ($V_{IH}$), the serial interface may immediately be re-enabled by driving the $\overline{CS}$ pin to the active state ($V_{IL}$or $V_{IHH}$).

During an EEPROM write cycle, only serial commands to Volatile memory (addresses 00h, 01h, 04h, and 05h) are accepted. All other serial commands are ignored until the EEPROM write cycle ($t_{WC}$) completes. This allows the Host Controller to operate on the Volatile Wiper registers and the TCON register, and to Read the Status Register. The EEWA bit in the Status register indicates the status of an EEPROM Write Cycle.

**TABLE 7-6: ADDRESS MAP TO MODIFY WRITE PROTECT AND WIPERLOCK TECHNOLOGY**

| Memory Address | Command's and Result | |
|---|---|---|
| | **High Voltage Decrement Wiper** | **High Voltage Increment Wiper** |
| 00h | Wiper 0 register is decremented | Wiper 0 register is incremented |
| 01h | Wiper 1 register is decremented | Wiper 1 register is incremented |
| 02h | WL0 is enabled | WL0 is disabled |
| 03h | WL1 is enabled | WL1 is disabled |
| 04h (1) | TCON register not changed, CMDERR bit is set | TCON register not changed, CMDERR bit is set |
| 05h - 0Eh (1) | Reserved | Reserved |
| 0Fh | WP is enabled | WP is disabled |

**Note 1: Reserved addresses:** Increment or Decrement commands are invalid for these addresses.

**NOTES:**

## 8.0 APPLICATIONS EXAMPLES

Non-volatile digital potentiometers have a multitude of practical uses in modern electronic circuits. The most popular uses include precision calibration of set point thresholds, sensor trimming, LCD bias trimming, audio attenuation, adjustable power supplies, motor control overcurrent trip setting, adjustable gain amplifiers and offset trimming. The MCP414X/416X/424X/426X devices can be used to replace the common mechanical trim pot in applications where the operating and terminal voltages are within CMOS process limitations ($V_{DD}$ = 2.7V to 5.5V).

### 8.1 Split Rail Applications

All inputs that would be used to interface to a Host Controller support High Voltage on their input pin. This allows the MCP4XXX device to be used in split power rail applications.

An example of this is a battery application where the PIC® MCU is directly powered by the battery supply (4.8V) and the MCP4XXX device is powered by the 3.3V regulated voltage.

For SPI applications, these inputs are:

- $\overline{CS}$
- SCK
- SDI (or SDI/SDO)
- $\overline{WP}$
- $\overline{SHDN}$

Figure 8-1 through Figure 8-2 show three example split rail systems. In this system, the MCP4XXX interface input signals need to be able to support the PIC MCU output high voltage ($V_{OH}$).

In Example #1 (Figure 8-1), the MCP4XXX interface input signals need to be able to support the PIC MCU output high voltage ($V_{OH}$). If the split rail voltage delta becomes too large, then the customer may be required to do some level shifting due to MCP4XXX $V_{OH}$ levels related to Host Controller $V_{IH}$ levels.

In Example #2 (Figure 8-2), the MCP4XXX interface input signals need to be able to support the lower voltage of the PIC MCU output high voltage level ($V_{OH}$).

Table 8-1 shows an example PIC microcontroller I/O voltage specifications and the MCP4XXX specifications. So this PIC MCU operating at 3.3V will drive a $V_{OH}$ at 2.64V, and for the MCP4XXX operating at 5.5V, the $V_{IH}$ is 2.47V. Therefore, the interface signals meet specifications.

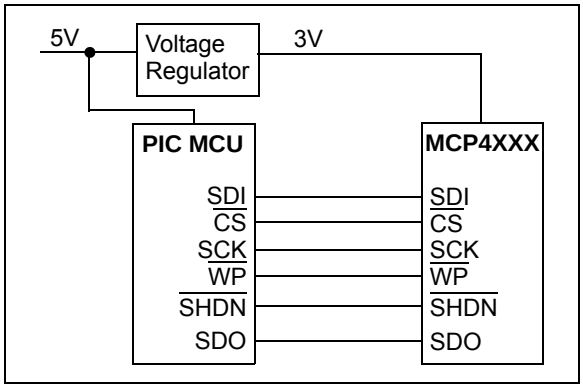



***FIGURE 8-1:*** *Example Split Rail System 1.*

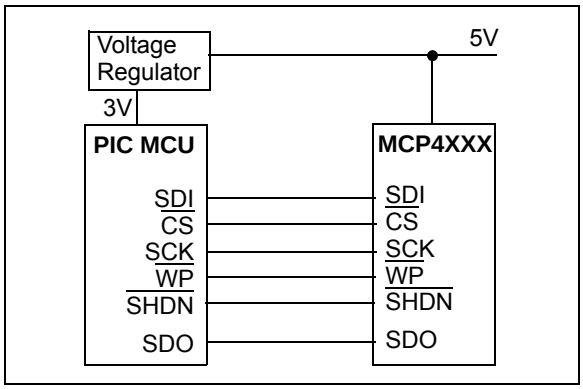



***FIGURE 8-2:*** *Example Split Rail System 2.*

**TABLE 8-1: $V_{OH}$ - $V_{IH}$ COMPARISONS**

| PIC (1) | | | MCP4XXX (2) | | | Comment |
|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{IH}$ | $V_{OH}$ | $V_{DD}$ | $V_{IH}$ | $V_{OH}$ | |
| 5.5 | 4.4 | 4.4 | 2.7 | 1.215 | — (3) | |
| 5.0 | 4.0 | 4.0 | 3.0 | 1.35 | — (3) | |
| 4.5 | 3.6 | 3.6 | 3.3 | 1.485 | — (3) | |
| 3.3 | 2.64 | 2.64 | 4.5 | 2.025 | — (3) | |
| 3.0 | 2.4 | 2.4 | 5.0 | 2.25 | — (3) | |
| 2.7 | 2.16 | 2.16 | 5.5 | 2.475 | — (3) | |

**Note 1:** $V_{OH}$ minimum = 0.8 * $V_{DD}$;
$V_{OL}$ maximum = 0.6V
$V_{IH}$ minimum = 0.8 * $V_{DD}$;
$V_{IL}$ maximum = 0.2 * $V_{DD}$;

**2:** $V_{OH}$ minimum (SDA only) =;
$V_{OL}$ maximum = 0.2 * $V_{DD}$
$V_{IH}$ minimum = 0.45 * $V_{DD}$;
$V_{IL}$ maximum = 0.2 * $V_{DD}$

**3:** The only MCP4XXX output pin is SDO, which is Open-Drain (or Open-Drain with Internal Pull-up) with High Voltage Support

## 8.2 Techniques to force the $\overline{CS}$ pin to $V_{IHH}$

The circuit in Figure 8-3 shows a method using the TC1240A doubling charge pump. When the $\overline{SHDN}$ pin is high, the TC1240A is off, and the level on the $\overline{CS}$ pin is controlled by the PIC® microcontrollers (MCUs) IO2 pin.

When the SHDN pin is low, the TC1240A is on and the $V_{OUT}$ voltage is 2 * $V_{DD}$. The resistor $R_1$ allows the $\overline{CS}$ pin to go higher than the voltage such that the PIC MCU's IO2 pin "clamps" at approximately $V_{DD}$.

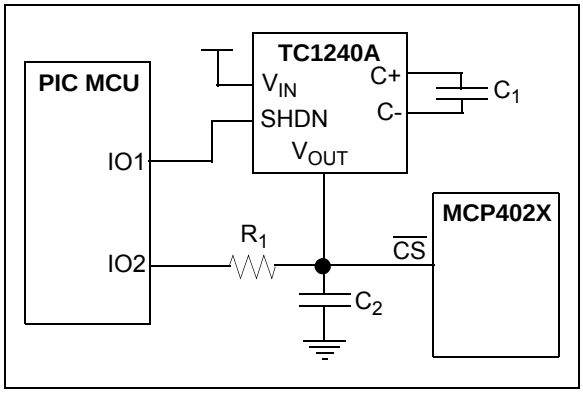



***FIGURE 8-3:*** *Using the TC1240A to generate the $V_{IHH}$ voltage.*

The circuit in Figure 8-4 shows the method used on the MCP402X Non-volatile Digital Potentiometer Evaluation Board (Part Number: MCP402XEV). This method requires that the system voltage be approximately 5V. This ensures that when the PIC10F206 enters a brown-out condition, there is an insufficient voltage level on the $\overline{CS}$ pin to change the stored value of the wiper. The MCP402X Non-volatile Digital Potentiometer Evaluation Board User's Guide (DS51546) contains a complete schematic.

GP0 is a general purpose I/O pin, while GP2 can either be a general purpose I/O pin or it can output the internal clock.

For the serial commands, configure the GP2 pin as an input (high impedance). The output state of the GP0 pin will determine the voltage on the $\overline{CS}$ pin ($V_{IL}$ or $V_{IH}$).

For high-voltage serial commands, force the GP0 output pin to output a high level ($V_{OH}$) and configure the GP2 pin to output the internal clock. This will form a charge pump and increase the voltage on the $\overline{CS}$ pin (when the system voltage is approximately 5V).

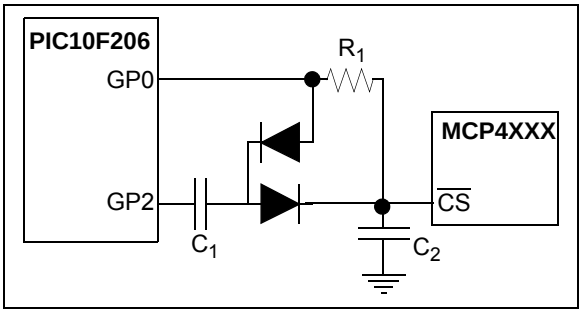



***FIGURE 8-4:*** *MCP4XXX Non-volatile Digital Potentiometer Evaluation Board (MCP402XEV) implementation to generate the $V_{IHH}$ voltage.*

## 8.3 Using Shutdown Modes

Figure 8-5 shows a possible application circuit where the independent terminals could be used. Disconnecting the wiper allows the transistor input to be taken to the Bias voltage level (disconnecting A and or B may be desired to reduce system current). Disconnecting Terminal A modifies the transistor input by the $R_{BW}$ rheostat value to the Common B. Disconnecting Terminal B modifies the transistor input by the $R_{AW}$ rheostat value to the Common A. The Common A and Common B connections could be connected to $V_{DD}$ and $V_{SS}$.

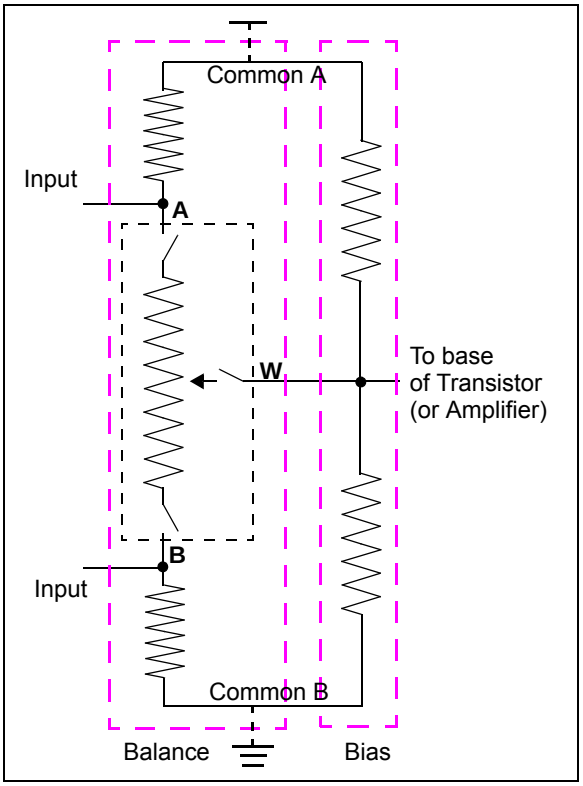



***FIGURE 8-5:*** *Example Application Circuit using Terminal Disconnects.*

## 8.4 Design Considerations

In the design of a system with the MCP4XXX devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

### 8.4.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-6 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin ($V_{DD}$) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, $V_{DD}$ and $V_{SS}$ should reside on the analog plane.

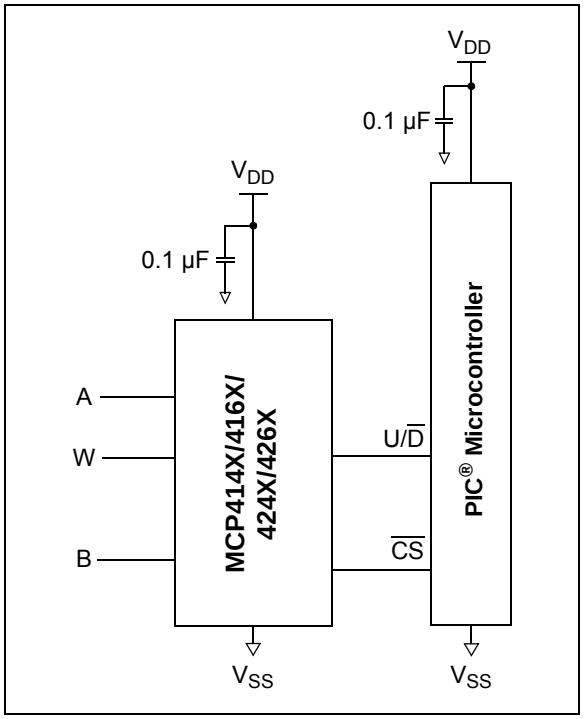



***FIGURE 8-6:*** *Typical Microcontroller Connections.*

### 8.4.2 LAYOUT CONSIDERATIONS

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP4XXX's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

If low noise is desired, breadboards and wire-wrapped boards are not recommended.

### 8.4.3 RESISTOR TEMPCO

Characterization curves of the resistor temperature coefficient (Tempco) are shown in Figure 2-8, Figure 2-19, Figure 2-29, and Figure 2-39.

These curves show that the resistor network is designed to correct for the change in resistance as temperature increases. This technique reduces the end to end change is $R_{AB}$ resistance.

### 8.4.4 HIGH VOLTAGE TOLERANT PINS

High Voltage support ($V_{IHH}$) on the Serial Interface pins supports two features. These are:

- In-Circuit Accommodation of split rail applications and power supply sync issues
- User configuration of the Non-Volatile EEPROM, Write Protect, and WiperLock feature

| **Note:** | In many applications, the High Voltage will only be present at the manufacturing stage so as to "lock" the Non-Volatile wiper value (after calibration) and the contents of the EEPROM. This ensures that the since High Voltage is not present under normal operating conditions, that these values can not be modified. |
|---|---|

**NOTES:**

# 9.0 DEVELOPMENT SUPPORT

## 9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP4XXX devices. The currently available tools are shown in Table 9-1.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

## 9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-2 shows some of these documents.

**TABLE 9-1: DEVELOPMENT TOOLS**

| Board Name | Part # | Supported Devices |
|---|---|---|
| MCP42XX Digital Potentiometer PICtail Plus Demo Board | MCP42XXDM-PTPLS | MCP42XX |
| MCP4XXX Digital Potentiometer Daughter Board (1) | MCP4XXXDM-DB | MCP42XXX, MCP42XX, MCP4021, and MCP4011 |
| 8-pin SOIC/MSOP/TSSOP/DIP Evaluation Board | SOIC8EV | Any 8-pin device in DIP, SOIC, MSOP, or TSSOP package |
| 14-pin SOIC/MSOP/DIP Evaluation Board | SOIC14EV | Any 14-pin device in DIP, SOIC, or MSOP package |

**Note 1:** Requires the use of a PICDEM Demo board (see User's Guide for details)

**TABLE 9-2: TECHNICAL DOCUMENTATION**

| Application Note Number | Title | Literature # |
|---|---|---|
| AN1080 | Understanding Digital Potentiometers Resistor Variations | DS01080 |
| AN737 | Using Digital Potentiometers to Design Low Pass Adjustable Filters | DS00737 |
| AN692 | Using a Digital Potentiometer to Optimize a Precision Single Supply Photo Detect | DS00692 |
| AN691 | Optimizing the Digital Potentiometer in Precision Circuits | DS00691 |
| AN219 | Comparing Digital Potentiometers to Mechanical Potentiometers | DS00219 |
| — | Digital Potentiometer Design Guide | DS22017 |
| — | Signal Chain Design Guide | DS21825 |

**NOTES:**

## 10.0 PACKAGING INFORMATION

### 10.1 Package Marking Information

8-Lead DFN (3x3)


| Part Number | Code | Part Number | Code |
|---|---|---|---|
| MCP4141-502E/MF | DAAJ | MCP4142-502E/MF | DABC |
| MCP4141-103E/MF | DAAK | MCP4142-103E/MF | DABD |
| MCP4141-104E/MF | DAAM | MCP4142-104E/MF | DABF |
| MCP4141-503E/MF | DAAL | MCP4142-503E/MF | DABE |
| MCP4161-502E/MF | DAAT | MCP4162-502E/MF | DABG |
| MCP4161-103E/MF | DAAU | MCP4162-103E/MF | DABH |
| MCP4161-104E/MF | DAAW | MCP4162-104E/MF | DABK |
| MCP4161-503E/MF | DAAV | MCP4162-503E/MF | DABJ |

Example:


8-Lead MSOP


| Part Number | Code | Part Number | Code |
|---|---|---|---|
| MCP4141-502E/MS | 414152 | MCP4142-502E/MS | 414252 |
| MCP4141-103E/MS | 414113 | MCP4142-103E/MS | 414213 |
| MCP4141-104E/MS | 414114 | MCP4142-104E/MS | 414214 |
| MCP4141-503E/MS | 414153 | MCP4142-503E/MS | 414253 |
| MCP4161-502E/MS | 416152 | MCP4162-502E/MS | 416252 |
| MCP4161-103E/MS | 416113 | MCP4162-103E/MS | 416213 |
| MCP4161-104E/MS | 416114 | MCP4162-104E/MS | 416214 |
| MCP4161-503E/MS | 416153 | MCP4162-503E/MS | 416253 |

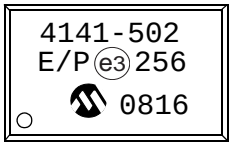
Example


| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

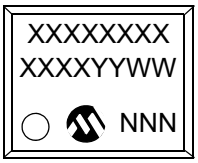
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead PDIP

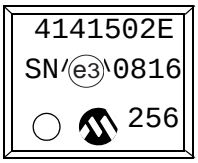

Example




8-Lead SOIC




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## Package Marking Information (Continued)

10-Lead DFN (3x3)


| Part Number | Code | Part Number | Code |
|---|---|---|---|
| MCP4242-502E/MF | BAEM | MCP4262-502E/MF | BAEW |
| MCP4242-103E/MF | BAEP | MCP4262-103E/MF | BAEX |
| MCP4242-104E/MF | BAER | MCP4262-104E/MF | BAEZ |
| MCP4242-503E/MF | BAEQ | MCP4262-503E/MF | BAEY |

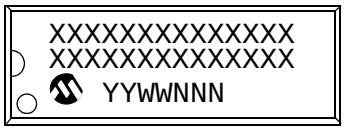
Example:


10-Lead MSOP

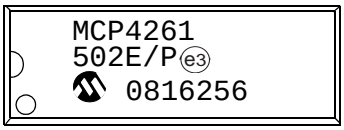

| Part Number | Code | Part Number | Code |
|---|---|---|---|
| MCP4242-502E/MS | 424252 | MCP4262-502E/MS | 426252 |
| MCP4242-103E/MS | 424213 | MCP4262-103E/MS | 426213 |
| MCP4242-104E/MS | 424214 | MCP4262-104E/MS | 426214 |
| MCP4242-503E/MS | 424253 | MCP4262-503E/MS | 426253 |

Example


14-Lead PDIP

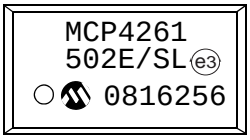



Example

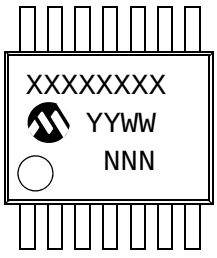



14-Lead SOIC (.150”)

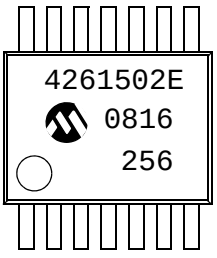

Example



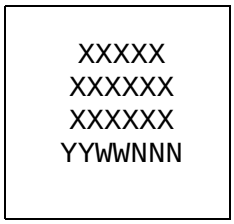

14-Lead TSSOP



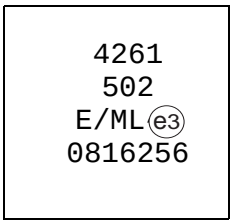

Example




16-Lead QFN (4x4)

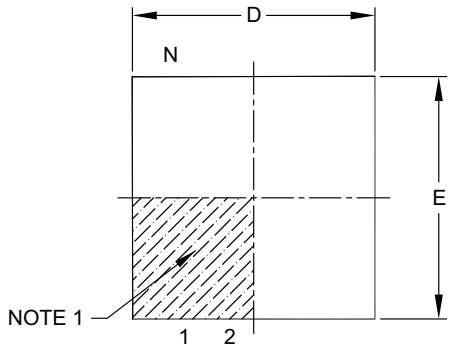



Example

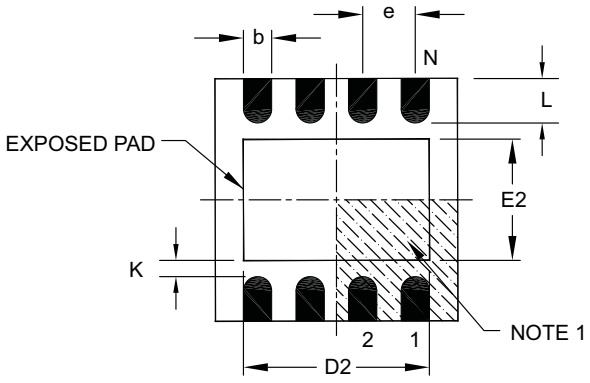


## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

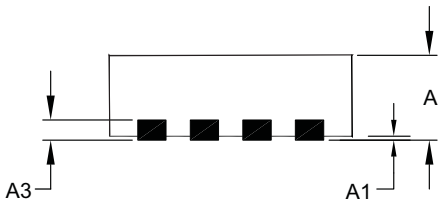
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

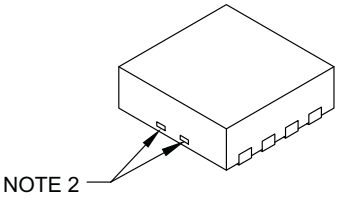



TOP VIEW




BOTTOM VIEW




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Width | E2 | 0.00 | – | 1.60 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 0.00 | – | 2.40 |
| Contact Width | b | 0.25 | 0.30 | 0.35 |
| Contact Length | L | 0.20 | 0.30 | 0.55 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

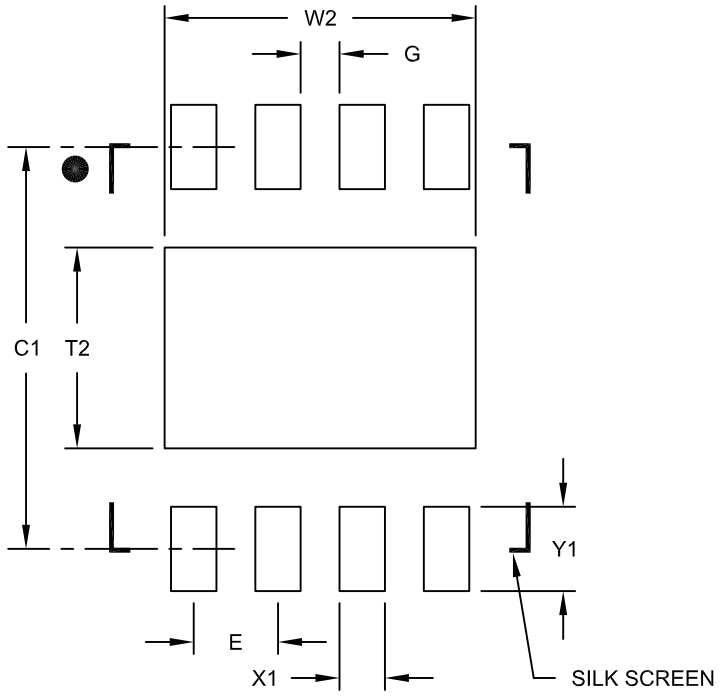
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B

## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 2.40 |
| Optional Center Pad Length | T2 | | | 1.55 |
| Contact Pad Spacing | C1 | | 3.10 | |
| Contact Pad Width (X8) | X1 | | | 0.35 |
| Contact Pad Length (X8) | Y1 | | | 0.65 |
| Distance Between Pads | G | 0.30 | | |

Notes:

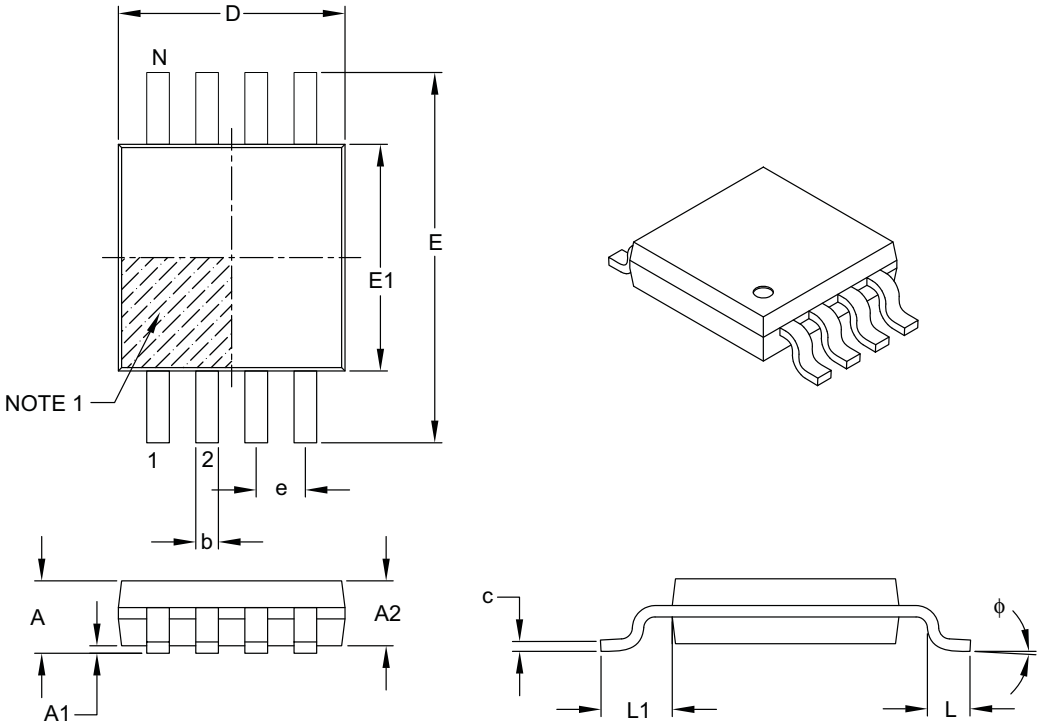
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062A

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Overall Length | D | | 3.00 BSC | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.22 | – | 0.40 |

**Notes:**

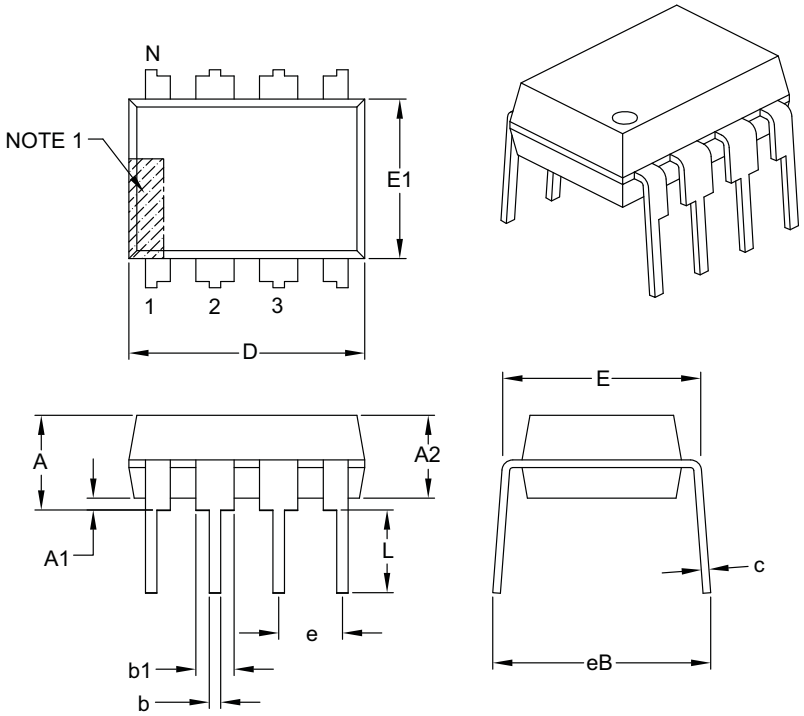
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

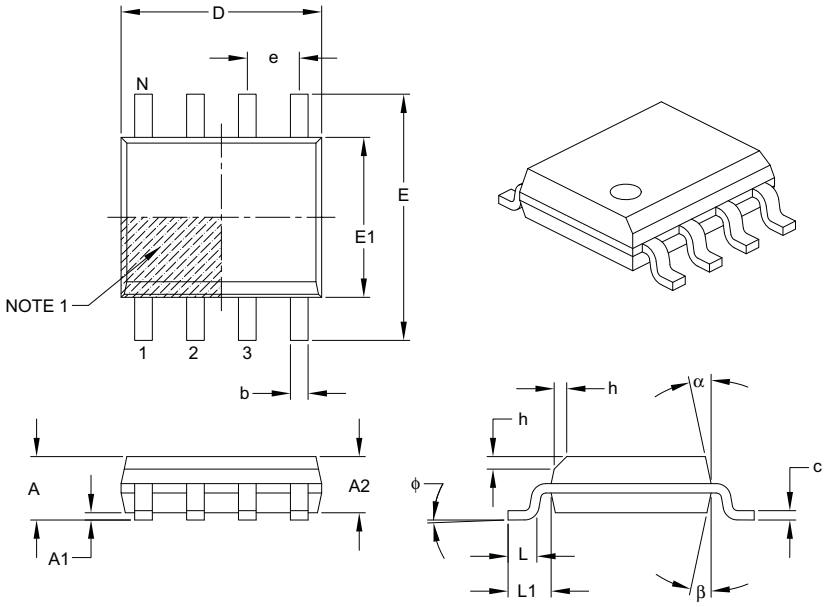
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

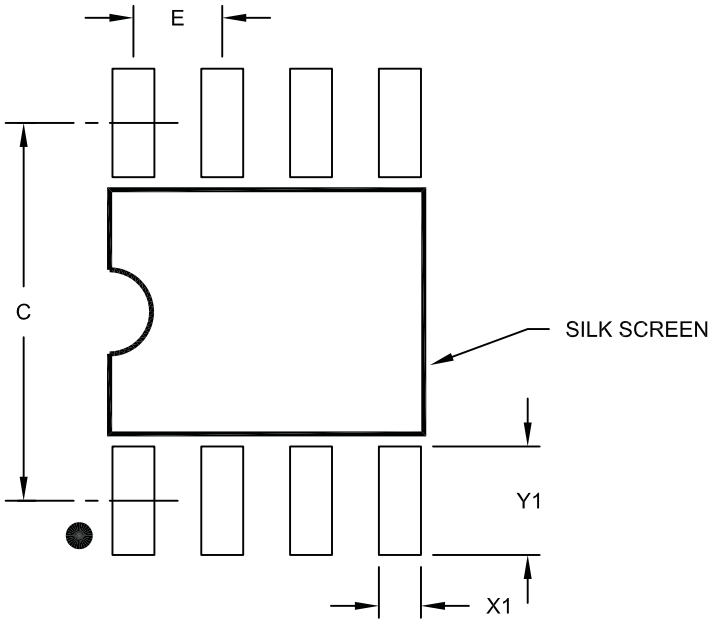
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

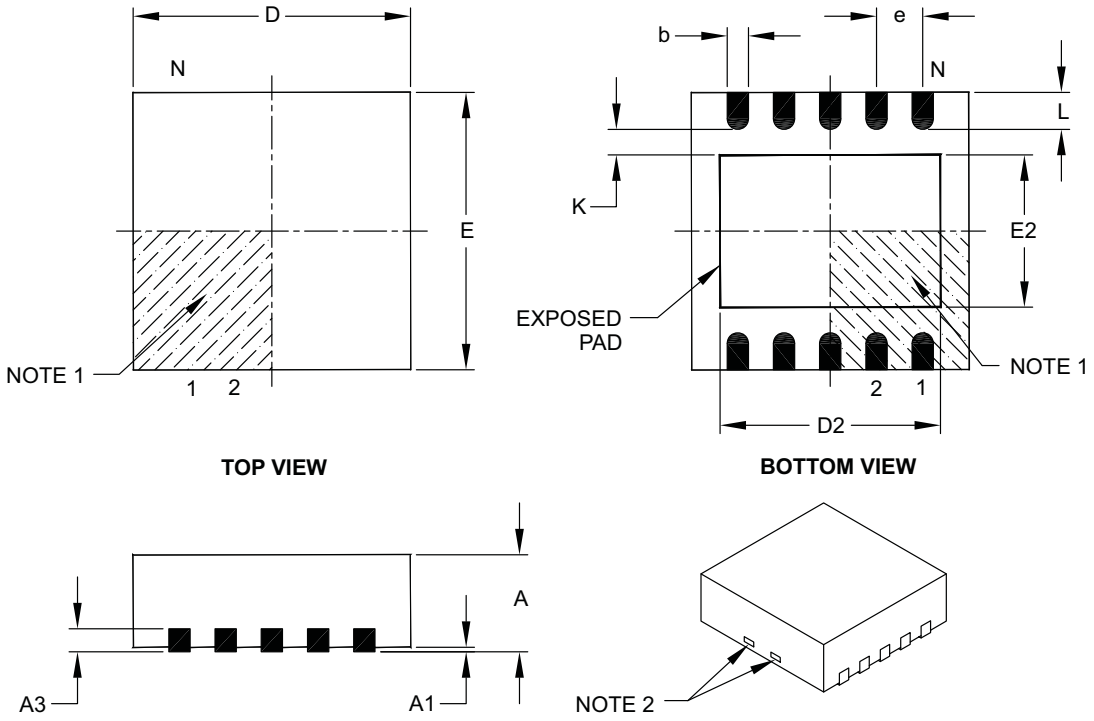
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

## 10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 10 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 2.20 | 2.35 | 2.48 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.40 | 1.58 | 1.75 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

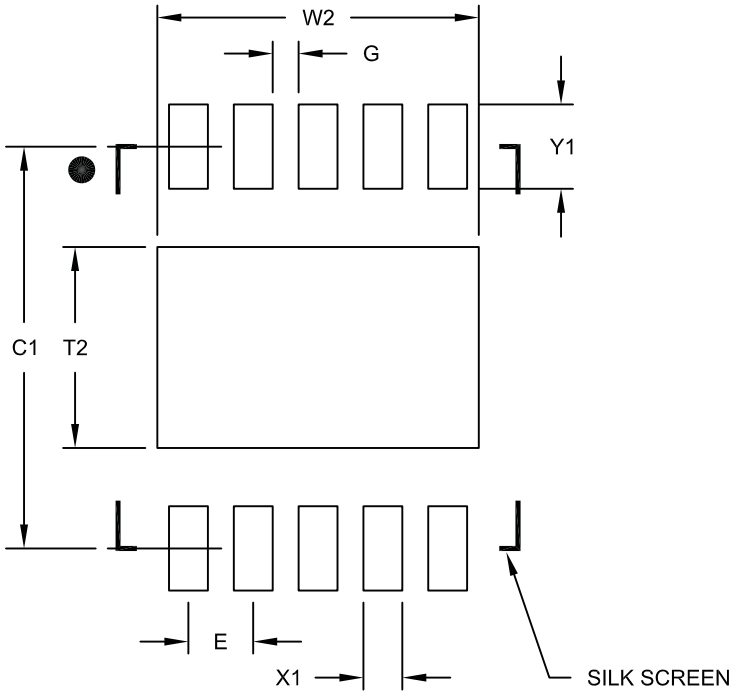
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-063B

## 10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 2.48 |
| Optional Center Pad Length | T2 | | | 1.55 |
| Contact Pad Spacing | C1 | | 3.10 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.65 |
| Distance Between Pads | G | 0.20 | | |

Notes:

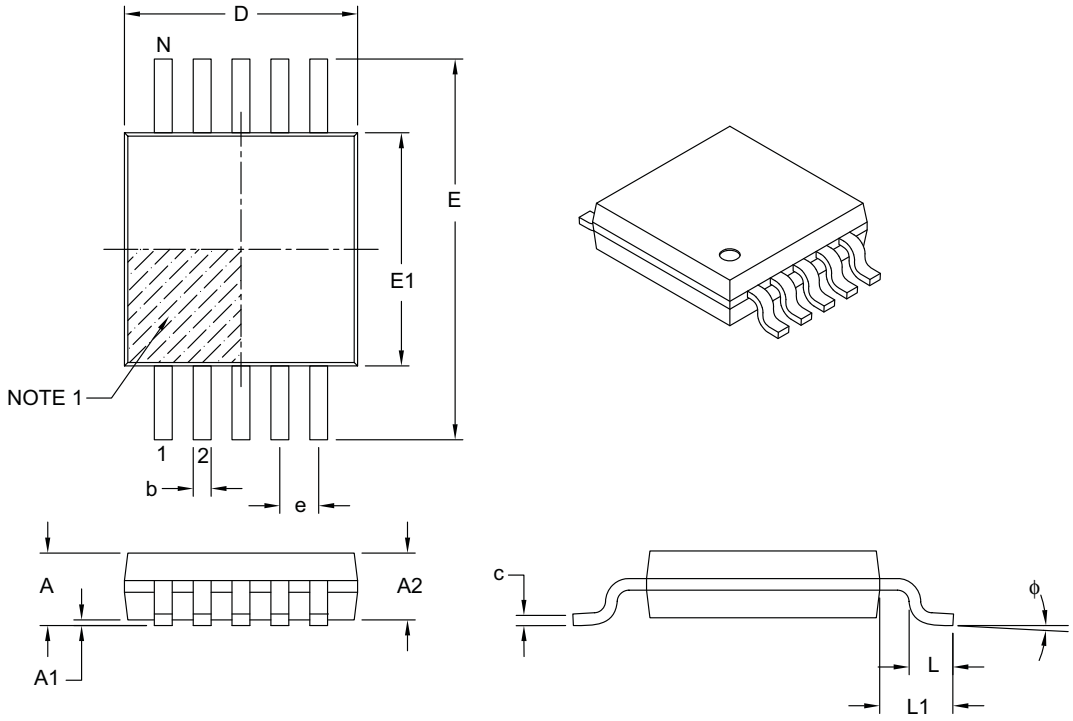
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063A

## 10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 10 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Overall Length | D | | 3.00 BSC | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.15 | – | 0.33 |

**Notes:**

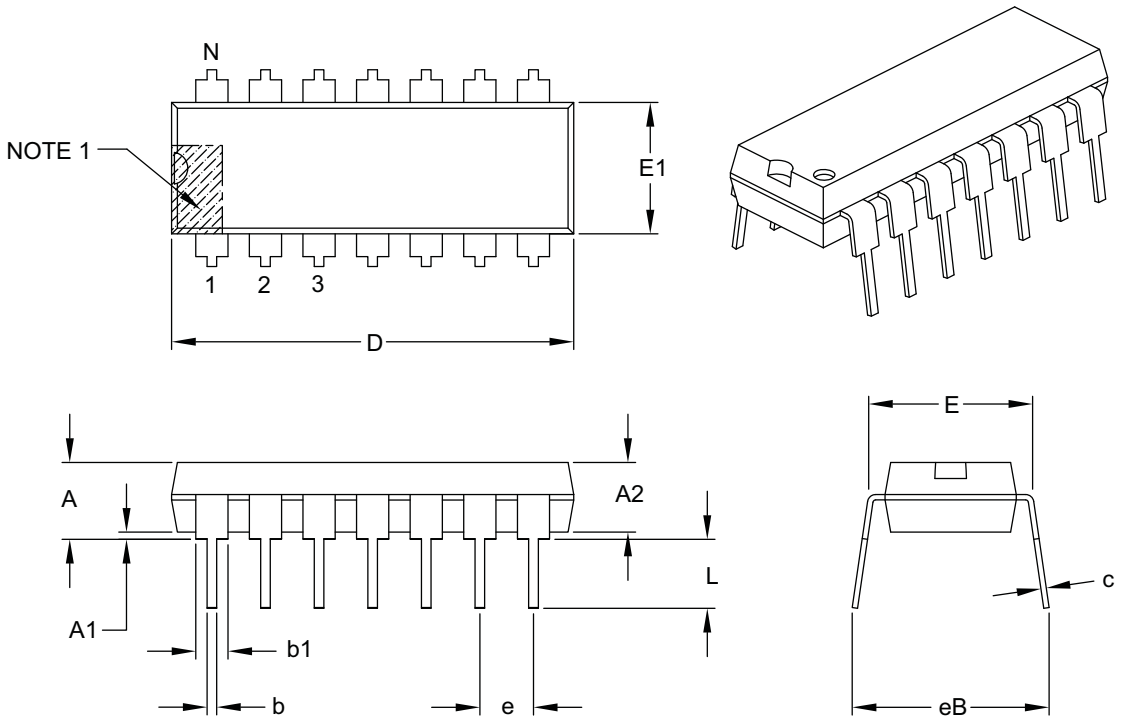
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021B

## 14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 14 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .735 | .750 | .775 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .045 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

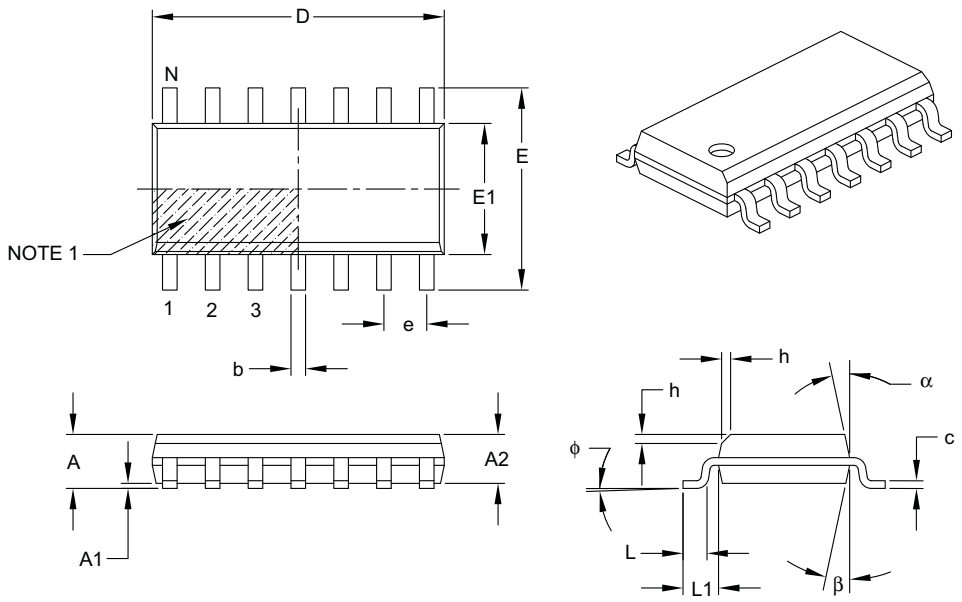
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

## 14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 14 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 8.65 BSC | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

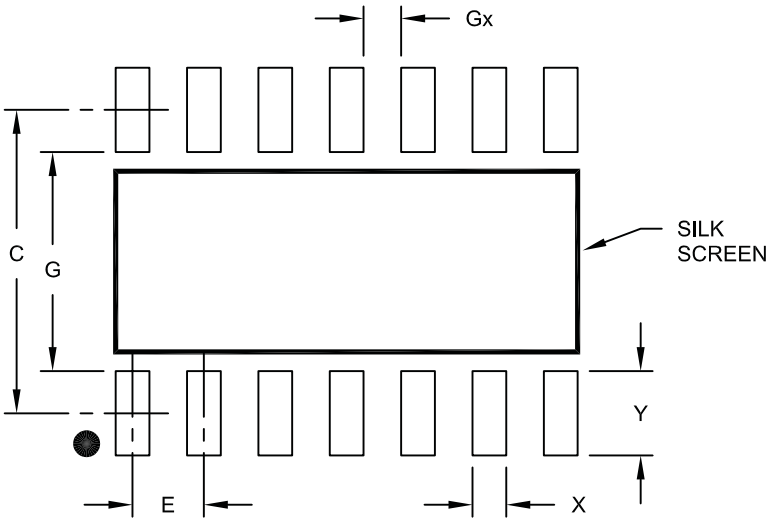
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width | X | | | 0.60 |
| Contact Pad Length | Y | | | 1.50 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 3.90 | | |

Notes:

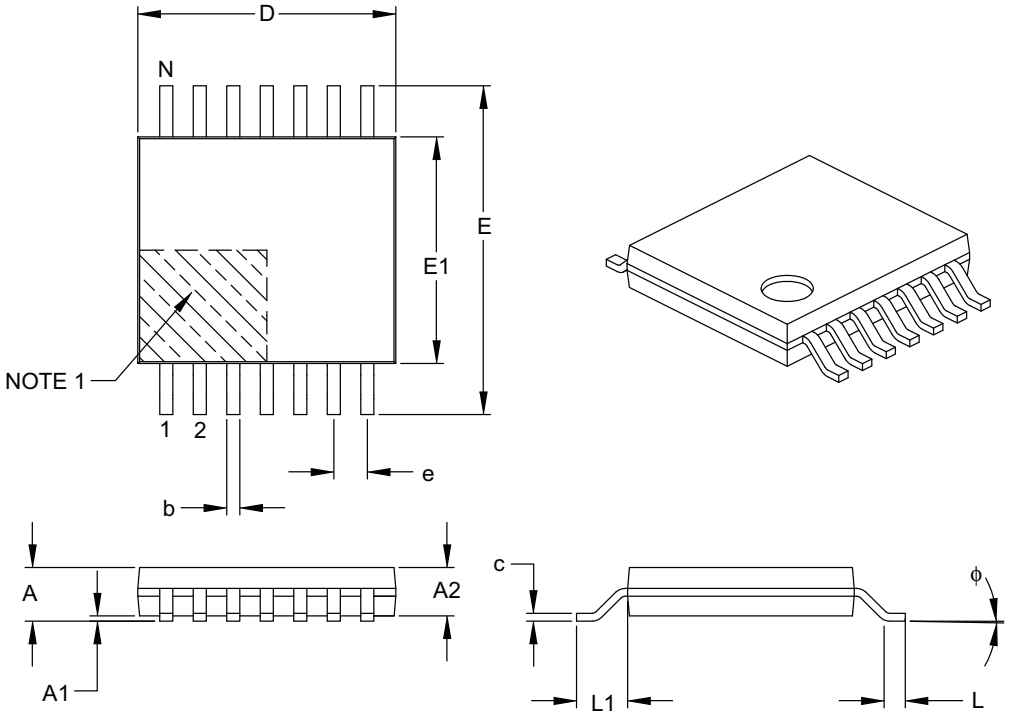
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 14 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 4.90 | 5.00 | 5.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.19 | – | 0.30 |

**Notes:**

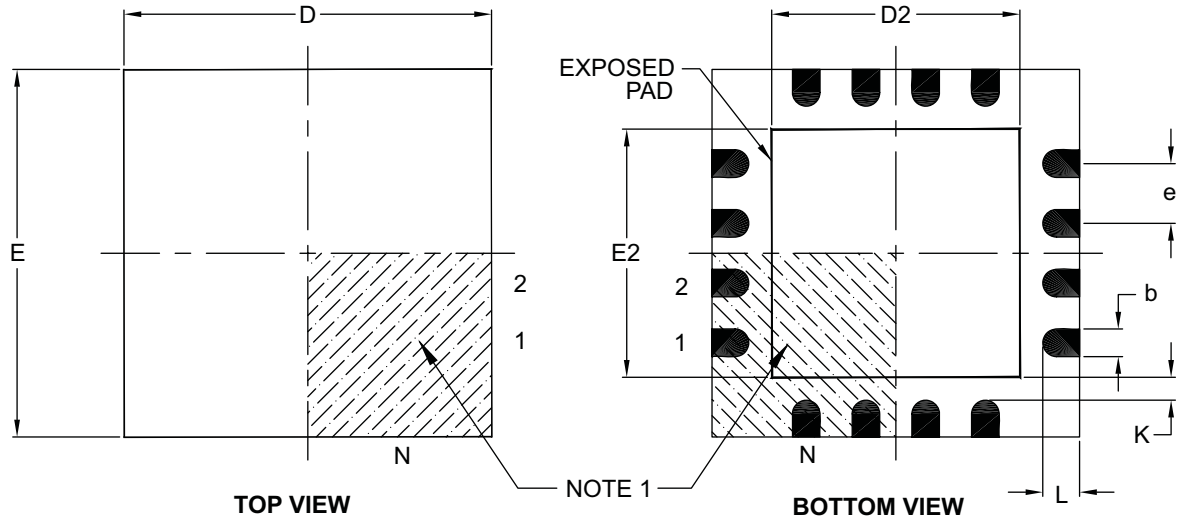
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

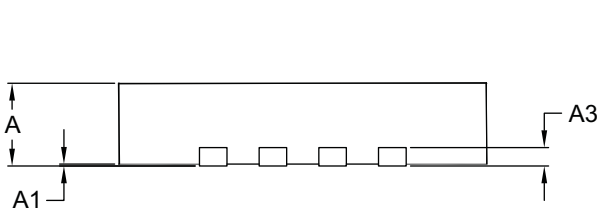
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

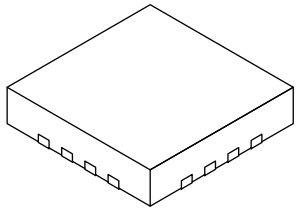
Microchip Technology Drawing C04-087B

## 16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 16 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 4.00 BSC | |
| Exposed Pad Width | E2 | 2.50 | 2.65 | 2.80 |
| Overall Length | D | | 4.00 BSC | |
| Exposed Pad Length | D2 | 2.50 | 2.65 | 2.80 |
| Contact Width | b | 0.25 | 0.30 | 0.35 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

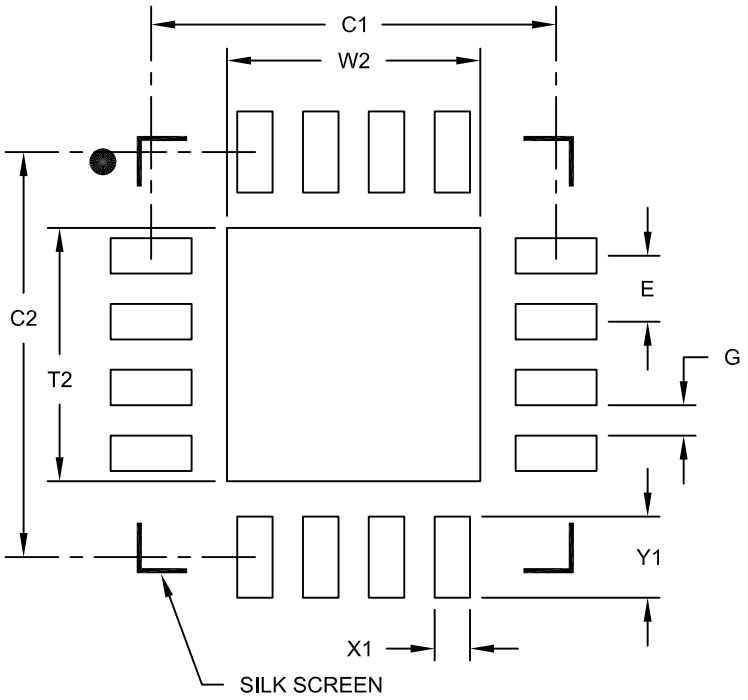
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

16-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | W2 | | | 2.50 |
| Optional Center Pad Length | T2 | | | 2.50 |
| Contact Pad Spacing | C1 | | 4.00 | |
| Contact Pad Spacing | C2 | | 4.00 | |
| Contact Pad Width (X28) | X1 | | | 0.35 |
| Contact Pad Length (X28) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.30 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2127A

# APPENDIX A: REVISION HISTORY

## Revision B (December 2008)

The following is the list of modifications:

1. Updated $I_{PU}$ specifications to specify test conditions and new limit.
2. Updated DFN and QFN package in **"Package Types (top view)"**, to include Exposed Thermal Pad samples (EP).
3. Added new descriptions in **Section 3.0 "Pin Descriptions"**.
4. Added new Development Tool support item.
5. Updated Package Outline section.

## Revision A (August 2007)

- Original Release of this Document.

# APPENDIX B: MIGRATING FROM THE MCP41XXX AND MCP42XXX DEVICES

This is intended to give an overview of some of the differences to be aware of when migrating from the MCP41XXX and MCP42XXX devices.

## B.1 MCP41XXX to MCP41XX Differences

Here are some of the differences to be aware of:

1. SI pin is now SDI/SDO pin, and the contents of the device memory can be read
2. Need to address the Terminal Connect Feature (TCON register) of MCP41XX
3. MCP41XX supports software Shutdown mode
4. New 5 kΩ version
5. MCP41XX have 7-bit resolution options
6. MCP41XX are Non-Volatile
7. Alternate pinout versions (for Rheostat configuration)
8. Verify device's electrical specifications
9. Interface signals are now high voltage tolerant
10. Interface signals now have internal pull-up resistors

## B.2 MCP42XXX to MCP42XX Differences

Here are some of the differences to be aware of:

1. Hardware Reset ($\overline{RS}$) pin replace by Hardware Write Protect ($\overline{WP}$) pin
2. Daisy chaining of devices is no longer supported
3. SDO pin allows contents of device memory to be read
4. Need to address the Terminal Connect Feature (TCON register) of MCP42XX
5. MCP42XX supports software Shutdown mode
6. New 5 kΩ version
7. MCP42XX have 7-bit resolution options
8. MCP42XX are Non-Volatile
9. Alternate package/pinout versions (for Rheostat configuration)
10. Verify device's electrical specifications
11. Interface signals are now high voltage tolerant
12. Interface signals now have internal pull-up resistors

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | -XXX | X | /XX |
|---|---|---|---|
| Device | Resistance Version | Temperature Range | Package |

| | | |
|---|---|---|
| Device | MCP4141: | Single Non-Volatile 7-bit Potentiometer |
| | MCP4141T: | Single Non-Volatile 7-bit Potentiometer (Tape and Reel) |
| | MCP4142: | Single Non-Volatile 7-bit Rheostat |
| | MCP4142T: | Single Non-Volatile 7-bit Rheostat (Tape and Reel) |
| | MCP4161: | Single Non-Volatile 8-bit Potentiometer |
| | MCP4161T: | Single Non-Volatile 8-bit Potentiometer (Tape and Reel) |
| | MCP4162: | Single Non-Volatile 8-bit Rheostat |
| | MCP4162T: | Single Non-Volatile 8-bit Rheostat (Tape and Reel) |
| | MCP4241: | Dual Non-Volatile 7-bit Potentiometer |
| | MCP4241T: | Dual Non-Volatile 7-bit Potentiometer (Tape and Reel) |
| | MCP4242: | Dual Non-Volatile 7-bit Rheostat |
| | MCP4242T: | Dual Non-Volatile 7-bit Rheostat (Tape and Reel) |
| | MCP4261: | Dual Non-Volatile 8-bit Potentiometer |
| | MCP4261T: | Dual Non-Volatile 8-bit Potentiometer (Tape and Reel) |
| | MCP4262: | Dual Non-Volatile 8-bit Rheostat |
| | MCP4262T: | Dual Non-Volatile 8-bit Rheostat (Tape and Reel) |
| Resistance Version: | 502 | = 5 kΩ |
| | 103 | = 10 kΩ |
| | 503 | = 50 kΩ |
| | 104 | = 100 kΩ |
| Temperature Range | I | = -40°C to +85°C (Industrial) |
| | E | = -40°C to +125°C (Extended) |
| Package | MF | = Plastic Dual Flat No-lead (3x3 DFN), 8/10-lead |
| | ML | = Plastic Quad Flat No-lead (4x4 QFN), 16-lead |
| | MS | = Plastic Micro Small Outline (MSOP), 8-lead |
| | P | = Plastic Dual In-line (PDIP) (300 mil), 8/14-lead |
| | SN | = Plastic Small Outline (SOIC), (150 mil), 8-lead |
| | SL | = Plastic Small Outline (SOIC), (150 mil), 14-lead |
| | ST | = Plastic Thin Shrink Small Outline (TSSOP), 14-lead |
| | UN | = Plastic Micro Small Outline (MSOP), 10-lead |

**Examples:**

a) MCP4141-502E/XX: 5 kΩ, 8LD Device
b) MCP4141T-502E/XX: T/R, 5 kΩ, 8LD Device
c) MCP4141-103E/XX: 10 kΩ, 8-LD Device
d) MCP4141T-103E/XX: T/R, 10 kΩ, 8LD Device
e) MCP4141-503E/XX: 50 kΩ, 8LD Device
f) MCP4141T-503E/XX: T/R, 50 kΩ, 8LD Device
g) MCP4141-104E/XX: 100 kΩ, 8LD Device
h) MCP4141T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4142-502E/XX: 5 kΩ, 8LD Device
b) MCP4142T-502E/XX: T/R, 5 kΩ, 8LD Device
c) MCP4142-103E/XX: 10 kΩ, 8-LD Device
d) MCP4142T-103E/XX: T/R, 10 kΩ, 8LD Device
e) MCP4142-503E/XX: 50 kΩ, 8LD Device
f) MCP4142T-503E/XX: T/R, 50 kΩ, 8LD Device
g) MCP4142-104E/XX: 100 kΩ, 8LD Device
h) MCP4142T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4161-502E/XX: 5 kΩ, 8LD Device
b) MCP4161T-502E/XX: T/R, 5 kΩ, 8LD Device
c) MCP4161-103E/XX: 10 kΩ, 8-LD Device
d) MCP4161T-103E/XX: T/R, 10 kΩ, 8LD Device
e) MCP4161-503E/XX: 50 kΩ, 8LD Device
f) MCP4161T-503E/XX: T/R, 50 kΩ, 8LD Device
g) MCP4161-104E/XX: 100 kΩ, 8LD Device
h) MCP4161T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4162-502E/XX: 5 kΩ, 8LD Device
b) MCP4162T-502E/XX: T/R, 5 kΩ, 8LD Device
c) MCP4162-103E/XX: 10 kΩ, 8-LD Device
d) MCP4162T-103E/XX: T/R, 10 kΩ, 8LD Device
e) MCP4162-503E/XX: 50 kΩ, 8LD Device
f) MCP4162T-503E/XX: T/R, 50 kΩ, 8LD Device
g) MCP4162-104E/XX: 100 kΩ, 8LD Device
h) MCP4162T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4241-502E/XX: 5 kΩ, 8LD Device
b) MCP4241T-502E/XX: T/R, 5 kΩ, 8LD Device
c) MCP4241-103E/XX: 10 kΩ, 8-LD Device
d) MCP4241T-103E/XX: T/R, 10 kΩ, 8LD Device
e) MCP4241-503E/XX: 50 kΩ, 8LD Device
f) MCP4241T-503E/XX: T/R, 50 kΩ, 8LD Device
g) MCP4241-104E/XX: 100 kΩ, 8LD Device
h) MCP4241T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4242-502E/XX: 5 kΩ, 8LD Device
b) MCP4242T-502E/XX: T/R, 5 kΩ, 8LD Device
c) MCP4242-103E/XX: 10 kΩ, 8-LD Device
d) MCP4242T-103E/XX: T/R, 10 kΩ, 8LD Device
e) MCP4242-503E/XX: 50 kΩ, 8LD Device
f) MCP4242T-503E/XX: T/R, 50 kΩ, 8LD Device
g) MCP4242-104E/XX: 100 kΩ, 8LD Device
h) MCP4242T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4261-502E/XX: 5 kΩ, 8LD Device
b) MCP4261T-502E/XX: T/R, 5 kΩ, 8LD Device
c) MCP4261-103E/XX: 10 kΩ, 8-LD Device
d) MCP4261T-103E/XX: T/R, 10 kΩ, 8LD Device
e) MCP4261-503E/XX: 50 kΩ, 8LD Device
f) MCP4261T-503E/XX: T/R, 50 kΩ, 8LD Device
g) MCP4261-104E/XX: 100 kΩ, 8LD Device
h) MCP4261T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4262-502E/XX: 5 kΩ, 8LD Device
b) MCP4262T-502E/XX: T/R, 5 kΩ, 8LD Device
c) MCP4262-103E/XX: 10 kΩ, 8-LD Device
d) MCP4262T-103E/XX: T/R, 10 kΩ, 8LD Device
e) MCP4262-503E/XX: 50 kΩ, 8LD Device
f) MCP4262T-503E/XX: T/R, 50 kΩ, 8LD Device
g) MCP4262-104E/XX: 100 kΩ, 8LD Device
h) MCP4262T-104E/XX: T/R, 100 kΩ, 8LD Device

XX = MF for 8/10-lead 3x3 DFN
= ML for 16-lead QFN
= MS for 8-lead MSOP
= P for 8/14-lead PDIP
= SN for 8-lead SOIC
= SL for 14-lead SOIC
= ST for 14-lead TSSOP
= UN for 10-lead MSOP

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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