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MB91F527R/MB91F527U/MB91F527M/MB91F527Y
MB91F528R/MB91F528U/MB91F528M/MB91F528Y

32-bit FR81S Microcontroller

The MB91520 series is a Cypress 32-bit microcontroller designed for automotive devices. This series contains the FR81S CPU which is compatible with the FR family.

Note: This series is a composition of the end of the above-mentioned each name of articles of presence, According to Presence of sub-clock, CSV initial value and LVD initial value. Please see "ORDERING INFORMATION" for details.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Maximum operating frequency:
  - MB91F52xR/MB91F52xU(LQS144/LQN144/LQP176): 80 MHz (Source oscillation = 4.0 MHz and 20 multiplied (PLL clock multiplication system))
  - MB91F52xR/MB91F52xU(LES144/LEP176): 128 MHz (Source oscillation = 4.0 MHz and 32 multiplied (PLL clock multiplication system))
  - MB91F52xM/ MB91F52xY: 128 MHz (Source oscillation = 4.0 MHz and 32 multiplied (PLL clock multiplication system))
- General-purpose register : 32-bit ×16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instruction
  - Bit processing instruction
  - Barrel shift instruction etc.
- High-level language support instructions
  - Function entry/exit instructions
  - Register content multi-load and store instructions
- Bit search instructions
  - Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
  - Decrease overhead during branch process
- Register interlock function
  - Easy assembler writing
- Built-in multiplier and instruction level support
  - Signed 32-bit multiplication : 5 cycles
  - Signed 16-bit multiplication : 3 cycles
- Interrupt (PC/PS saving)
  - 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and the data.
  - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
  - IEEE754 compliant
  - Floating-point register 32-bit × 16 sets

Peripheral Functions

- Clock generation (equipped with SSCG function)
- Main oscillation (4MHz to 16MHz)
  - Sub oscillation (32kHz) or no sub oscillation
    PLL multiplication rate
    : 1 to 20 times for MB91F52xR/MB91F52xU (LQS144/LQN144/LQP176)
    : 1 to 32 times for MB91F52xR/MB91F52xU (LES144/LEP176)
    : 1 to 32 times for MB91F52xM/MB91F52xY
- 100 kHz CR oscillator mounted
- Maximum operating frequency:
- Peripheral bus clock: 40MHz
- External bus clock: 40MHz
- Built-in Program flash capacity
- MB91F527 : 1536KB + 64KB
- MB91F528 : 2048KB + 64KB
- Built-in Data flash (WorkFlash) 64KB
- Built-in RAM capacity
  - Main RAM
    MB91F527 : 192KB
    MB91F528 : 192KB + 128KB (128KB located in the AHB area, a penalty given at access)
  - Backup RAM 16KB
- General-purpose ports :
  MB91F527R/MB91F528R : 115 (none sub oscillation), 113 (with sub oscillation)
  MB91F527U/MB91F528U : 147 (none sub oscillation), 145 (with sub oscillation)
  MB91F527M/MB91F528M : 177 (none sub oscillation), 175 (with sub oscillation)
  MB91F527Y/MB91F528Y 219 (none sub oscillation), 217 (with sub oscillation)
  Included I^2C pseudo open drain ports : Max. 30
- External bus interface
  - 22-bit address, 8/16-bit data
- DMA Controller
  - Up to 16 channels can be started simultaneously.

- 2 transfer factors (Internal peripheral request and software)

- A/D converter (successive approximation type)
  - 12-bit resolution : Max. 64 channels (32 channels +32 channels)
  - Conversion time : 1.4µs
- D/A converter (R-2R type)
  - 8-bit resolution : 2 channels
- External interrupt input: Max. 24 channels
  - Level ("H" / "L"), or edge detection (rising or falling) supported
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max. 20 channels
  5V tolerant input 8 channels (ch.6, ch.8, ch.9, ch.11, ch.16 to ch.19) CMOS hysteresis input
  < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - The external clock can be used as the transfer clock
  - Parity, frame, and overrun error detect functions provided
  - DMA transfer support

  <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 64-byte transmission FIFO, memory, 64-byte reception FIFO memory
  - SPI supported; master and slave systems supported; 5-bit to 16-bit, 20-bit, 24-bit, 32-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - The external clock can be entered. (Slave operation)
  - Overrun error detection function is provided
  - DMA transfer support
  - Serial chip select SPI function
  - <LIN (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
  - LIN protocol revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - The external clock can be adjusted by the reload counter
  - DMA transfer support
  - Hardware assist function

  < I2C >
  - 10 channels (ch.3, ch.4, ch.12 to ch.19) Standard mode / Fast mode supported
  - 5 channels (ch.5 to ch.8, ch.11) Standard mode supported
  - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
  - Standard mode (Max. 100kbps) / Fast mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)
- CAN : 6 channels
  - Transfer speed : Up to 1Mbps
  - 128-transmission/reception message buffering : 6 channels
- FlexRay controller: 1 unit (ch.A/ch.B)
- FlexRay specification version 2.1 supported
  - Max. 128-message buffer configuration
  - 8KB message RAM
  - Variable-length message buffer configuration
  - Each message buffer can be configured as a part of a reception buffer, transmission buffer, or reception FIFO.
  - Host access to message buffers through input and output buffers
  - Filtering the slot counter, cycle counter, and channels
  - Maskable interrupts
- PPG : 16-bit × Max. 88 channels
  - LED drive output 4 channels (ch.11 to ch.14)
- Reload timer : 16-bit × 8 channels
- Free-run timer :
  16-bit × 3 channels
  32-bit × Max. 8 channels
- Input capture :
  16-bit × 4 channels (linked to the free-run timer)
  32-bit × Max. 8 channels (linked to the free-run timer)
- Output compare :
  16-bit × 6 channels (linked to the free-run timer)
  32-bit × Max. 8 channels (linked to the free-run timer)
- Wave generator : 6 channels
- U/D counter:
  - 8/16-bit up/down counter × Max. 4 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main oscillation / sub oscillation frequency can be selected for the operation clock.
- Calibration: A real-time clock (RTC) of the sub clock drive.
  - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (damage of crystal etc.) of sub oscillation (32kHz) (dual clock products) and main oscillation (4 MHz).
  - When abnormality is detected, it switches to the CR clock.
- For some devices, ON/OFF can be selected as the initial value.
- Base timer : 2 channels
  - 16-bit timer
  - The timer mode is selected from PWM/PPG/PWC/reload.
  - In the cascaded mode, a pair of 16-bit timers can be used as one 32-bit timer.
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog (An effective range of a clear counter can be set.)
- NMI

- Interrupt controller
- Interrupt request batch read
  - Multiple interrupts from peripherals can be read by a series of registers.
- I/O relocation
- Peripheral function pins can be reassigned.
- Low-power consumption mode
  - Sleep / Stop / Watch / Sub RUN mode
  - Stop (power shutdown) / Watch (power shutdown) mode
- Power on reset
- Low-voltage detection reset (External power supply and Internal power supply are independently observed.)
- For some devices, ON/OFF can be selected as the initial value for external power supply.
- Tuning RAM
- Capacity: 128 KB
- Can be used as RAM for data tuning.
- JTAG pins (TRST, TCK, TMS, TDI, TDO)
- Device Package : 144/176/208/416
- CMOS 90nm Technology
- Power supplies
  - 5V or 3V Power supply
  - The internal 1.2V is generated from 5V with the voltage step-down regulator.
  - Restriction on the power-on sequence (from VCC to VCCE)
  - Applying a voltage higher than the power supply voltage to an analog signal input is prohibited.
- Operation guaranteed voltage range (recommended): 3.0V to 5.5V (within the range guaranteed by AC and DC spec)
- Operation guaranteed voltage range: 2.7V to 5.5V

Contents

1. Product Lineup

Product lineup comparison 144 pins

	MB91F527R	MB91F528R
System Clock	On-chip PLL Clock multiple method	
Minimum instruction execution time	12.5ns(80MHz) (LQS144/LQN144) 8.0ns(128MHz) (LES144)	
FLASH Capacity (Program)	1536KB + 64KB	2048KB + 64KB
FLASH Capacity (Data)	64KB	
RAM Capacity	192KB + 16KB	(192KB + 128KB) + 16KB
External Bus I/F (22 address/16 data/4cs)	Yes	
DMA Transfer	16 channels	
16-bit Base Timer	2 channels	
Free-run Timer	16-bit × 3 channels, 32-bit × 3 channels	
Input capture	16-bit × 4 channels, 32-bit × 6 channels	
Output Compare	16-bit × 6 channels, 32-bit × 6 channels	
16-bit Reload Timer	8 channels	
PPG	16-bit × 44 channels *2	
Up/down Counter	2 channels	
Clock Supervisor	Yes	
External interrupt	8 channels × 2 units	
A/D	12-bit × 32 channels (1 unit), 12-bit × 16 channels (1 unit)	
D/A (8-bit)	2 channels	
Multi-Function Serial	12 channels *3	
CAN	128msg × 6 channels	
FlexRay	1 channel	
Hardware watchdog	Yes	
CRC generation	Yes	
Low-voltage detection reset	Yes	

	MB91F527R	MB91F528R
Flash Security	Yes	
ECC Flash/WorkFlash	Yes	
ECC RAM	Yes	
Memory Protection Function (MPU)	Yes	
Floating-point arithmetic (FPU)	Yes	
Real Time Clock (RTC)	Yes	
General-purpose port (#GPIOs)	115 ports (no sub clock) / 113 ports (with sub clock)	
SSCG	Yes	
Sub clock	Yes	
CR oscillator	Yes	
NMI request function	Yes	
OCD (On Chip Debug)	Yes	
TPU (Timing Protection Unit)	Yes	
Key Code Register	Yes	
Wave Generator	6 channels	
Tuning RAM	None	Yes
JTAG	Yes	
Operation guaranteed temperature (Ta)	-40°C to +125°C *1	
Power supply	2.7 V to 5.5 V *4 VCCE = 5.0 V±10% or VCCE = 3.0 V to 3.6 V (VCCE: 1-pin to 39-pin and 128-pin to 144-pin power supply) (External bus I/F: 3.0 V to 3.6 V)	
Package	LQS144 / LQN144 / LES144	

*1: The limitation with the package has been described by the item of the power consumption of "Absolute maximum ratings".
*2: PPG output pins on ch.38 and ch.39 do not exist. See "Pins of PPG (ch.0 to ch.87)."
*3: Only channel 3 and channel 4 support the I^2C (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
*4: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).
This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 176 pins

	MB91F527U	MB91F528U
System Clock	On-chip PLL Clock multiple method	
Minimum instruction execution time	12.5ns(80MHz) (LQP176) 8.0ns(128MHz) (LEP176)	
FLASH Capacity (Program)	1536KB + 64KB	2048KB + 64KB
FLASH Capacity (Data)	64KB	
RAM Capacity	192KB + 16KB	(192KB + 128KB) + 16KB
External Bus I/F (22 address/16 data/4cs)	Yes	
DMA Transfer	16 channels	
16-bit Base Timer	2 channels	
Free-run Timer	16-bit × 3 channels, 32-bit × 3 channels	
Input capture	16-bit × 4 channels, 32-bit × 6 channels	
Output Compare	16-bit × 6 channels, 32-bit × 6 channels	
16-bit Reload Timer	8 channels	
PPG	16-bit × 48 channels	
Up/down Counter	2 channels	
Clock Supervisor	Yes	
External interrupt	8 channels × 2 units	
A/D	12-bit × 32 channels (1 unit), 12-bit × 16 channels (1 unit)	
D/A (8-bit)	2 channels	
Multi-Function Serial	12 channels [*2]	
CAN	128msg × 6 channels	
FlexRay	1 channel	
Hardware watchdog	Yes	
CRC generation	Yes	
Low-voltage detection reset	Yes	

	MB91F527U	MB91F528U
Flash Security	Yes	
ECC Flash/WorkFlash	Yes	
ECC RAM	Yes	
Memory Protection Function (MPU)	Yes	
Floating-point arithmetic (FPU)	Yes	
Real Time Clock (RTC)	Yes	
General-purpose port (#GPIOs)	147 ports (no sub clock) / 145 ports (with sub clock)	
SSCG	Yes	
Sub clock	Yes	
CR oscillator	Yes	
NMI request function	Yes	
OCD (On Chip Debug)	Yes	
TPU (Timing Protection Unit)	Yes	
Key Code Register	Yes	
Wave Generator	6 channels	
Tuning RAM	None	Yes
JTAG	Yes	
Operation guaranteed temperature (Ta)	-40°C to +125°C *1	
Power supply	2.7 V to 5.5 V *3 VCCE = 5.0 V±10% or VCCE = 3.0 V to 3.6 V (VCCE: 1-pin to 49-pin and 156-pin to 176-pin power supply) (External bus I/F: 3.0 V to 3.6 V)	
Package	LQP176 / LEP176	

*1: The limitation with the package has been described by the item of the power consumption of "Absolute maximum ratings".
*2: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 208 pins

	MB91F527M	MB91F528M
System Clock	On-chip PLL Clock multiple method	
Minimum instruction execution time	8.0ns (128MHz)	
FLASH Capacity (Program)	1536KB + 64KB	2048KB + 64KB
FLASH Capacity (Data)	64KB	
RAM Capacity	192KB + 16KB	(192KB + 128KB) + 16KB
External Bus I/F (22 address/16 data/4cs)	Yes	
DMA Transfer	16 channels	
16-bit Base Timer	2 channels	
Free-run Timer	16-bit × 3 channels, 32-bit × 8 channels	
Input capture	16-bit × 4 channels, 32-bit × 8 channels	
Output Compare	16-bit × 6 channels, 32-bit × 8 channels	
16-bit Reload Timer	8 channels	
PPG	16-bit × 64 channels	
Up/down Counter	4 channels	
Clock Supervisor	Yes	
External interrupt	8 channels × 3 units	
A/D	12-bit × 32 channels (2 units)	
D/A (8-bit)	2 channels	
Multi-Function Serial	20 channels *2	
CAN	128msg × 6 channels	
FlexRay	1 channel	
Hardware watchdog	Yes	
CRC generation	Yes	
Low-voltage detection reset	Yes	

	MB91F527M	MB91F528M
Flash Security	Yes	
ECC Flash/WorkFlash	Yes	
ECC RAM	Yes	
Memory Protection Function (MPU)	Yes	
Floating-point arithmetic (FPU)	Yes	
Real Time Clock (RTC)	Yes	
General-purpose port (#GPIOs)	177 ports (no sub clock) / 175 ports (with sub clock)	
SSCG	Yes	
Sub clock	Yes	
CR oscillator	Yes	
NMI request function	Yes	
OCD(On Chip Debug)	Yes	
TPU (Timing Protection Unit)	Yes	
Key Code Register	Yes	
Wave Generator	6 channels	
Tuning RAM	None	Yes
JTAG	Yes	
Operation guaranteed temperature (Ta)	-40°C to +125°C *1	
Power supply	2.7 V to 5.5 V *3 VCCE = 5.0 V±10% or VCCE = 3.0 V to 3.6 V (VCCE: 1-pin to 57-pin and 188-pin to 208-pin power supply) (External bus I/F: 3.0 V to 3.6 V)	
Package	LQR208 / LER208	

*1: The limitation with the package has been described by the item of the power consumption of "Absolute maximum ratings".
*2: Only channel 3, channel 4 and channel 12 to channel 19 support the I^2C (high-speed mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode)
*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).
This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 416 pins

	MB91F527Y	MB91F528Y
System Clock	On-chip PLL Clock multiple method	
Minimum instruction execution time	8.0ns (128MHz)	
FLASH Capacity (Program)	1536KB + 64KB	2048KB + 64KB
FLASH Capacity (Data)	64KB	
RAM Capacity	192KB + 16KB	(192KB + 128KB) + 16KB
External Bus I/F (22 address/16 data/4cs)	Yes	
DMA Transfer	16 channels	
16-bit Base Timer	2 channels	
Free-run Timer	16-bit × 3 channels, 32-bit × 8 channels	
Input capture	16-bit × 4 channels, 32-bit × 8 channels	
Output Compare	16-bit × 6 channels, 32-bit × 8 channels	
16-bit Reload Timer	8 channels	
PPG	16-bit × 88 channels	
Up/down Counter	4 channels	
Clock Supervisor	Yes	
External interrupt	8 channels × 3 units	
A/D	12-bit × 32 channels (2 units)	
D/A (8-bit)	2 channels	
Multi-Function Serial	20 channels *1	
CAN	128msg × 6 channels	
FlexRay	1 channel	
Hardware watchdog	Yes	
CRC generation	Yes	
Low-voltage detection reset	Yes	
Flash Security	Yes	
ECC Flash/WorkFlash	Yes	

	MB91F527Y	MB91F528Y
ECC RAM	Yes	
Memory Protection Function (MPU)	Yes	
Floating-point arithmetic (FPU)	Yes	
Real Time Clock (RTC)	Yes	
General-purpose port (#GPIOs)	219 ports (no sub clock) / 217 ports (with sub clock)	
SSCG	Yes	
Sub clock	Yes	
CR oscillator	Yes	
NMI request function	Yes	
OCD(On Chip Debug)	Yes	
TPU (Timing Protection Unit)	Yes	
Key Code Register	Yes	
Wave Generator	6 channels	
Tuning RAM	None	Yes
JTAG	Yes	
Operation guaranteed temperature (Ta)	-40°C to +125°C	
Power supply	2.7 V to 5.5 V *2 VCCE = 5.0 V±10% or VCCE = 3.0 V to 3.6 V (VCCE: See pin assignment) (External bus I/F: 3.0 V to 3.6 V)	
Package	PAB416	

*1: Only channel 3, channel 4 and channel 12 to channel 19 support the I^2C (high-speed mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).
This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operationvoltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Table for Clock Supervisor and External Low Voltage Detection Reset Initial Value ON/OFF

Clock	Initial value of clock supervisor	Initial value of external low-voltage detection reset	Function
Single	ON	ON	S
		OFF	U
	OFF	ON	H
		OFF	K
Dual	ON	ON	W
		OFF	Y
	OFF	ON	J
		OFF	L

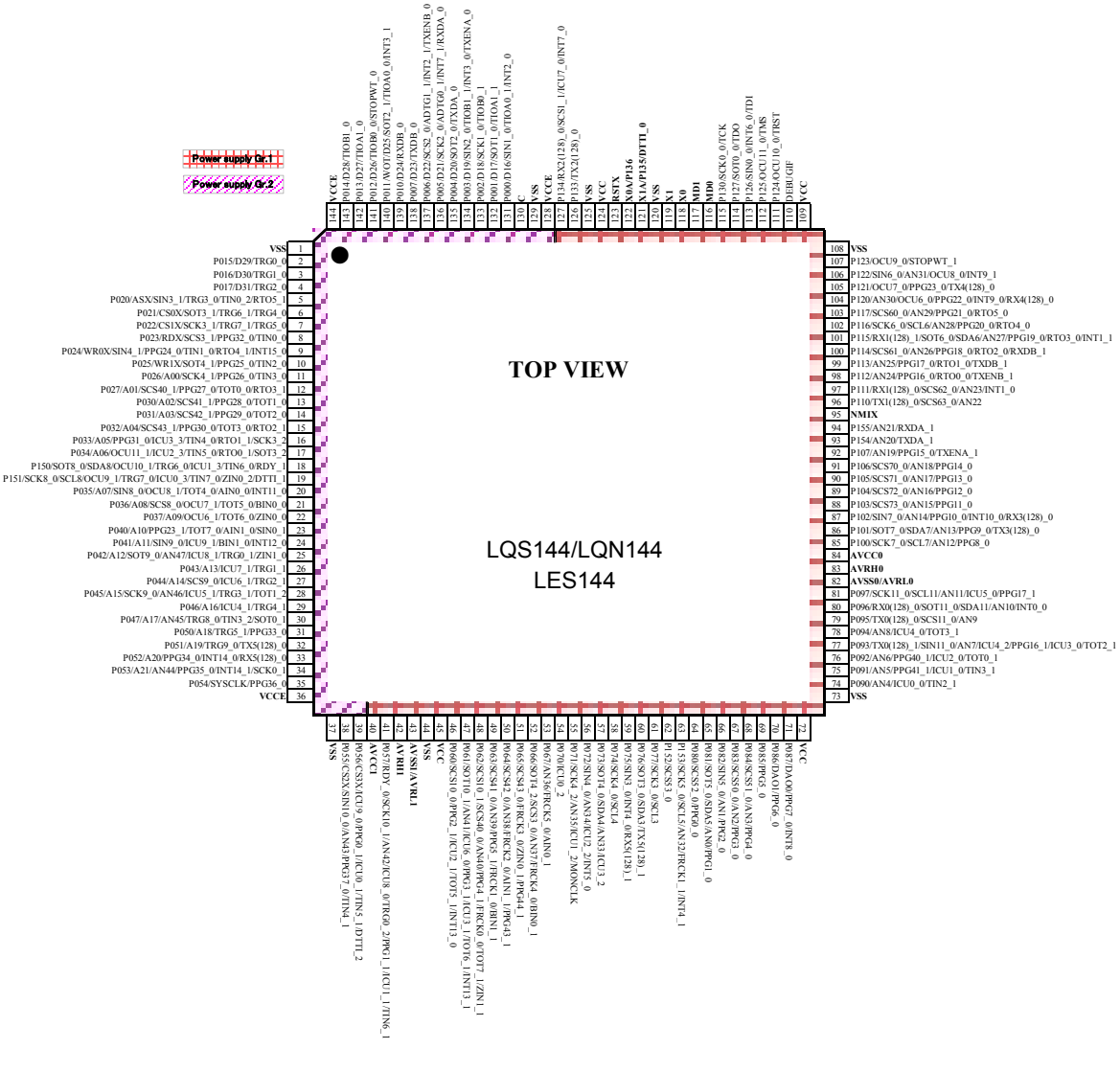
MB91F52Xxyz
- Revision: C, D, E
- Function: See Table 3-5
- PKG Type: R 144 pin
  U 176 pin
  M 208 pin
  Y PAB 416 pin
- Memory Size: 7 1.5MB
  8 2MB

2. Pin Assignment

MB91F52xR

MB91F527R, MB91F528R

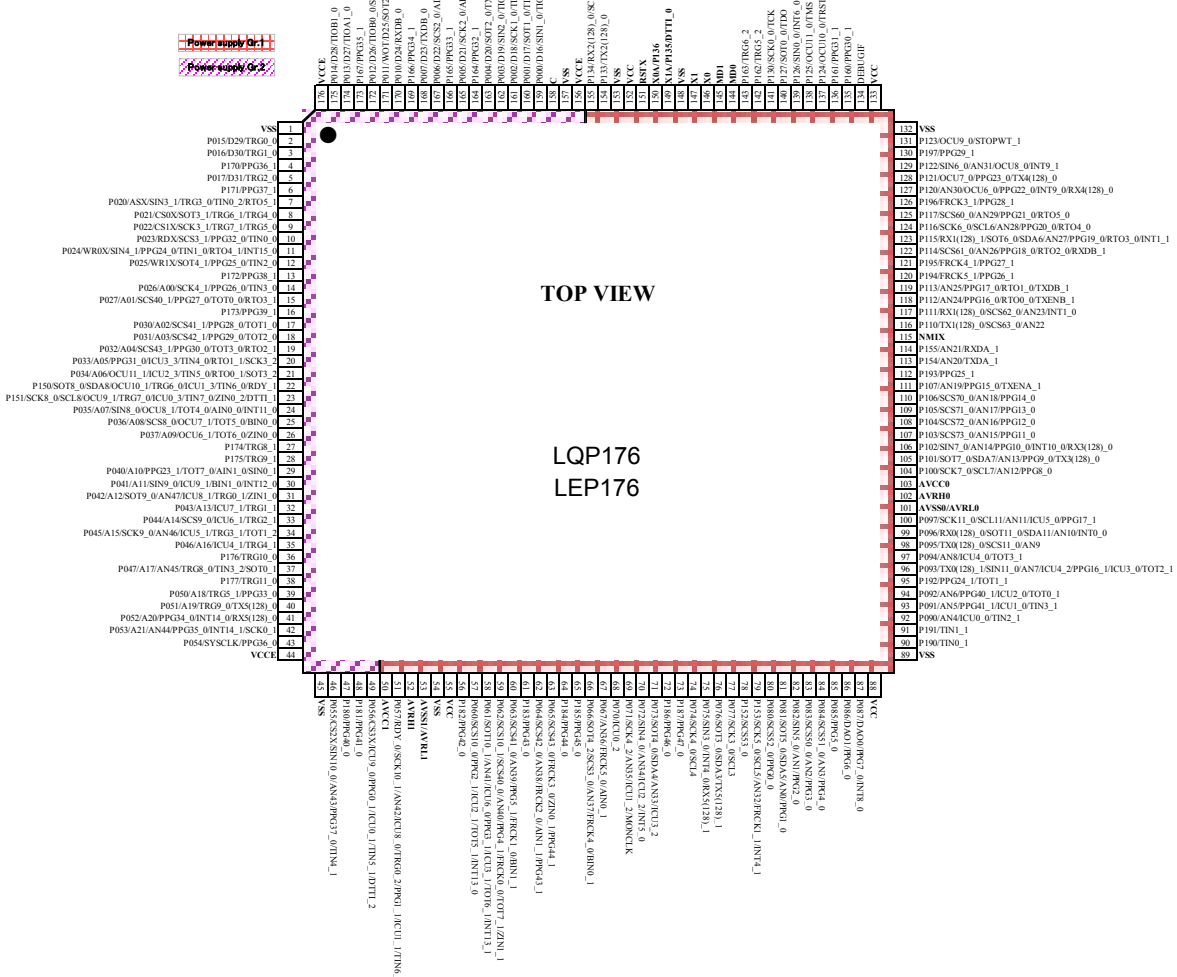
(TOP VIEW)



MB91F52xU

MB91F527U, MB91F528U

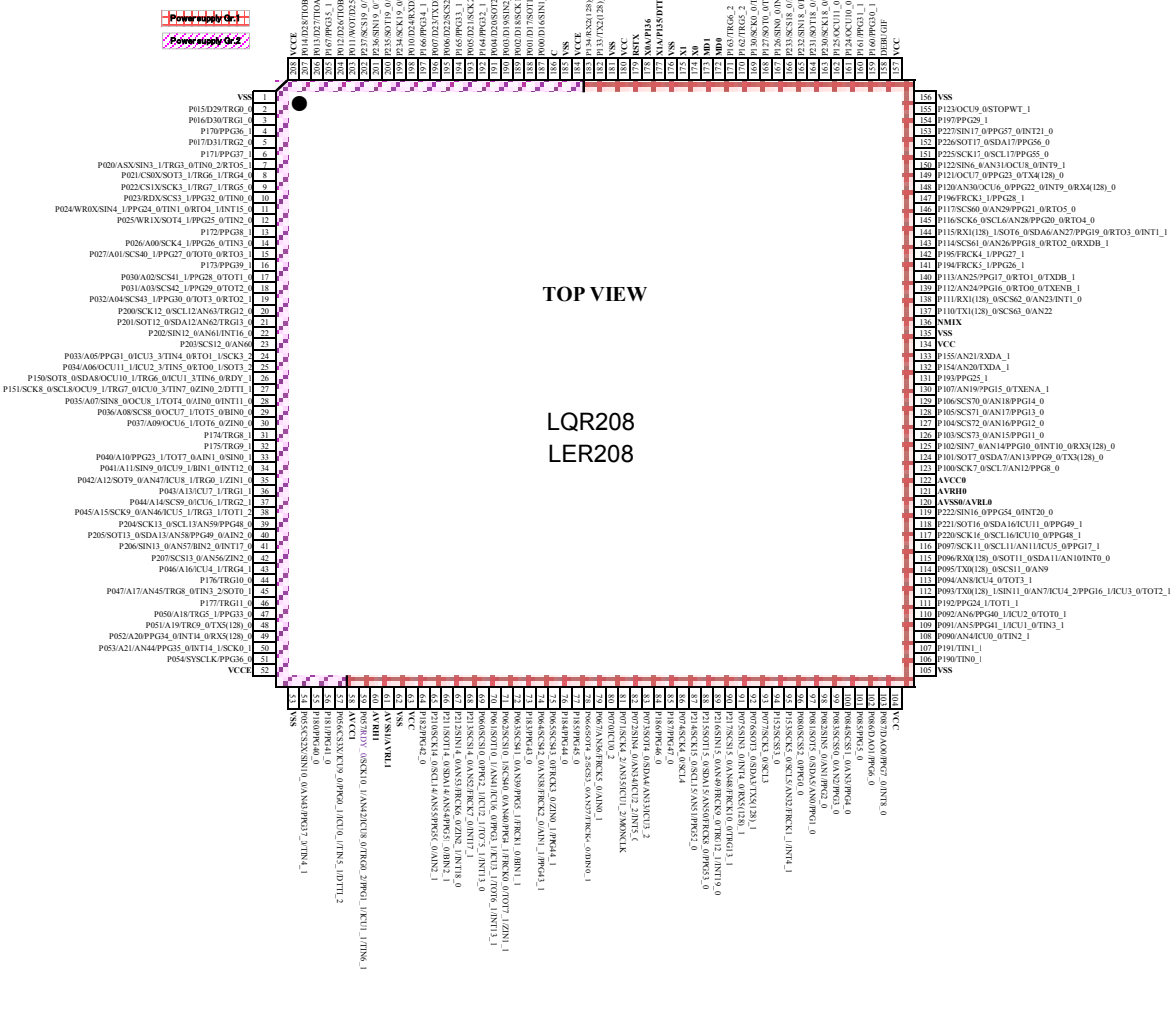
(TOP VIEW)



MB91F52xM

MB91F527M, MB91F528M

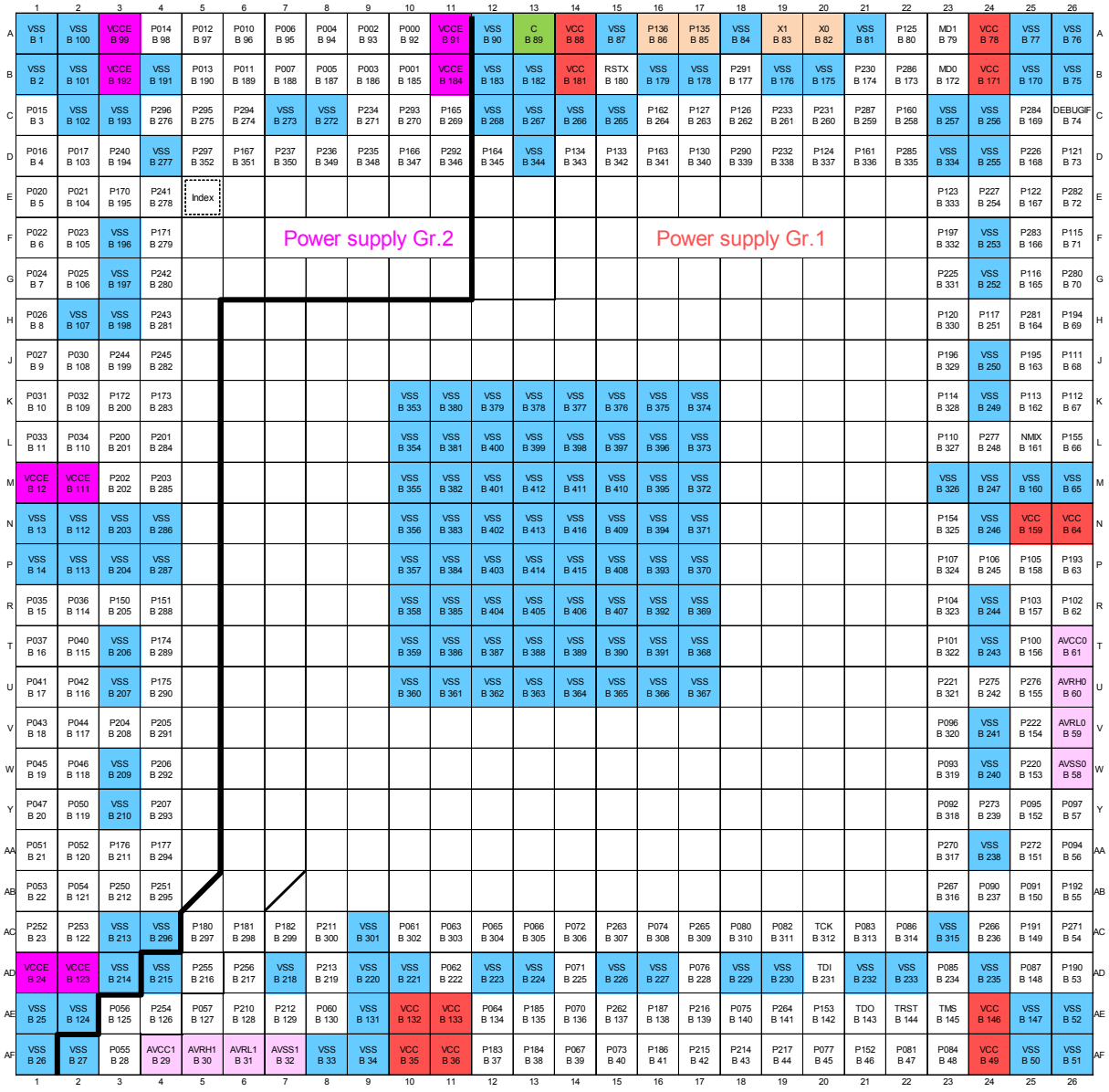
(TOP VIEW)



MB91F52xY

MB91F527Y, MB91F528Y

Top view



PAB416

3. Pin Description

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	D3	P240	-	A	General-purpose I/O port
-	-	-	E4	P241	-	A	General-purpose I/O port
2	2	2	C1	P015	-	R	General-purpose I/O port
				D29	-		External Bus data bit29 I/O pin
				TRG0_0	-		PPG trigger 0 input pin(0)
3	3	3	D1	P016	-	R	General-purpose I/O port
				D30	-		External Bus data bit30 I/O pin
				TRG1_0	-		PPG trigger 1 input pin(0)
-	4	4	E3	P170	-	A	General-purpose I/O port
				PPG36_1	-		PPG ch.36 output pin(1)
4	5	5	D2	P017	-	R	General-purpose I/O port
				D31	-		External Bus data bit31 I/O pin
				TRG2_0	-		PPG trigger 2 input pin(0)
-	6	6	F4	P171	-	A	General-purpose I/O port
				PPG37_1	-		PPG ch.37 output pin(1)
-	-	-	G4	P242	-	A	General-purpose I/O port
				TRG16_0	-		PPG trigger 16 input pin(0)
-	-	-	H4	P243	-	A	General-purpose I/O port
				TRG17_0	-		PPG trigger 17 input pin(0)
5	7	7	E1	P020	-	F	General-purpose I/O port
				ASX	-		External Bus address strobe output pin
				SIN3_1	-		Multi-function serial ch.3 serial data input pin(1)
				TRG3_0	-		PPG trigger 3 input pin(0)
				TIN0_2	-		Reload timer ch.0 event input pin(2)
				RTO5_1	-		Waveform generator ch.5 output pin(1)
6	8	8	E2	P021	-	A	General-purpose I/O port
				CS0X	-		External Bus chip select 0 output pin
				SOT3_1	-		Multi-function serial ch.3 serial data output pin(1)
				TRG6_1	-		PPG trigger 6 input pin(1)
				TRG4_0	-		PPG trigger 4 input pin(0)
7	9	9	F1	P022	-	F	General-purpose I/O port
				CS1X	-		External Bus chip select 1 output pin
				SCK3_1	-		Multi-function serial ch.3 clock I/O pin(1)
				TRG7_1	-		PPG trigger 7 input pin(1)
				TRG5_0	-		PPG trigger 5 input pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
8	10	10	F2	P023	-	A	General-purpose I/O port
				RDX	-		External Bus read strobe output pin
				SCS3_1	-		Serial chip select 3 I/O pin(1)
				PPG32_0	-		PPG ch.32 output pin(0)
				TIN0_0	-		Reload timer ch.0 event input pin(0)
-	-	-	J3	P244	-	A	General-purpose I/O port
				PPG64_0	-		PPG ch.64 output pin(0)
-	-	-	J4	P245	-	A	General-purpose I/O port
				PPG65_0	-		PPG ch.65 output pin(0)
9	11	11	G1	P024	-	F	General-purpose I/O port
				WR0X	-		External Bus write strobe 0 output pin
				SIN4_1	-		Multi-function serial ch.4 serial data input pin(1)
				PPG24_0	-		PPG ch.24 output pin(0)
				TIN1_0	-		Reload timer ch.1 event input pin(0)
				RTO4_1	-		Waveform generator ch.4 output pin(1)
				INT15_0	-		INT15 external interrupt input pin(0)
10	12	12	G2	P025	-	A	General-purpose I/O port
				WR1X	-		External Bus write strobe 1 output pin
				SOT4_1	-		Multi-function serial ch.4 serial data output pin(1)
				PPG25_0	-		PPG ch.25 output pin(0)
				TIN2_0	-		Reload timer ch.2 event input pin(0)
-	13	13	K3	P172	-	A	General-purpose I/O port
				PPG38_1	-		PPG ch.38 output pin(1)
11	14	14	H1	P026	-	F	General-purpose I/O port
				A00	-		External Bus address bit0 output pin
				SCK4_1	-		Multi-function serial ch.4 clock I/O pin(1)
				PPG26_0	-		PPG ch.26 output pin(0)
				TIN3_0	-		Reload timer ch.3 event input pin(0)
12	15	15	J1	P027	-	A	General-purpose I/O port
				A01	-		External Bus address bit1 output pin
				SCS40_1	-		Serial chip select 40 I/O pin(1)
				PPG27_0	-		PPG ch.27 output pin(0)
				TOT0_0	-		Reload timer ch.0 output pin(0)
				RTO3_1	-		Waveform generator ch.3 output pin(1)
-	16	16	K4	P173	-	A	General-purpose I/O port
				PPG39_1	-		PPG ch.39 output pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
13	17	17	J2	P030	-	A	General-purpose I/O port
				A02	-		External Bus address bit2 output pin
				SCS41_1	-		Serial chip select 41 output pin(1)
				PPG28_0	-		PPG ch.28 output pin(0)
				TOT1_0	-		Reload timer ch.1 output pin(0)
14	18	18	K1	P031	-	A	General-purpose I/O port
				A03	-		External Bus address bit3 output pin
				SCS42_1	-		Serial chip select 42 output pin(1)
				PPG29_0	-		PPG ch.29 output pin(0)
				TOT2_0	-		Reload timer ch.2 output pin(0)
15	19	19	K2	P032	-	A	General-purpose I/O port
				A04	-		External Bus address bit4 output pin
				SCS43_1	-		Serial chip select 43 output pin(1)
				PPG30_0	-		PPG ch.30 output pin(0)
				TOT3_0	-		Reload timer ch.3 output pin(0)
				RTO2_1	-		Waveform generator ch.2 output pin(1)
-	-	20	L3	P200	-	Q	General-purpose I/O port
				SCK12_0/SCL12	-		Multi-function serial ch.12 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				AN63	-		ADC analog 63 input pin
				TRG12_0	-		PPG trigger 12 input pin(0)
-	-	21	L4	P201	-	Q	General-purpose I/O port
				SOT12_0/SDA12	-		Multi-function serial ch.12 serial data output pin(0)/I^2C bus serial data I/O pin
				AN62	-		ADC analog 62 input pin
				TRG13_0	-		PPG trigger 13 input pin(0)
-	-	22	M3	P202	-	G	General-purpose I/O port
				SIN12_0	-		Multi-function serial ch.12 serial data input pin(0)
				AN61	-		ADC analog 61 input pin
				INT16_0	-		INT16 external interrupt input pin(0)
-	-	23	M4	P203	-	B	General-purpose I/O port
				SCS12_0	-		Serial chip select 12 I/O pin(0)
				AN60	-		ADC analog 60 input pin

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
16	20	24	L1	P033	-	A	General-purpose I/O port
				A05	-		External Bus address bit5 output pin
				PPG31_0	-		PPG ch.31 output pin(0)
				ICU3_3	-		Input capture ch.3 input pin(3)
				TIN4_0	-		Reload timer ch.4 event input pin(0)
				RTO1_1	-		Waveform generator ch.1 output pin(1)
				SCK3_2	-		Multi-function serial ch.3 clock I/O pin(2)
17	21	25	L2	P034	-	A	General-purpose I/O port
				A06	-		External Bus address bit6 output pin
				OCU11_1	-		Output compare ch.11 output pin(1)
				ICU2_3	-		Input capture ch.2 input pin(3)
				TIN5_0	-		Reload timer ch.5 event input pin(0)
				RTO0_1	-		Waveform generator ch.0 output pin(1)
				SOT3_2	-		Multi-function serial ch.3 serial data output pin(2)
18	22	26	R3	P150	-	F	General-purpose I/O port
				RDY_1	-		External Bus RDY input pin (1)
				SOT8_0/SDA8	-		Multi-function serial ch.8 serial data output pin(0)/I^2C bus serial data I/O pin
				OCU10_1	-		Output compare ch.10 output pin(1)
				TRG6_0	-		PPG trigger 6 input pin(0)
				ICU1_3	-		Input capture ch.1 input pin(3)
				TIN6_0	-		Reload timer ch.6 event input pin(0)
19	23	27	R4	P151	-	F	General-purpose I/O port
				SCK8_0/SCL8	-		Multi-function serial ch.8 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				OCU9_1	-		Output compare ch.9 output pin(1)
				TRG7_0	-		PPG trigger 7 input pin(0)
				ICU0_3	-		Input capture ch.0 input pin(3)
				TIN7_0	-		Reload timer ch.7 event input pin(0)
				ZIN0_2	-		U/D counter ch.0 ZIN input pin(2)
				DTTI_1	-		Waveform generator ch.0-ch.5 input pin(1)
20	24	28	R1	P035	-	I	General-purpose I/O port
				A07	-		External Bus address bit7 output pin
				SIN8_0	-		Multi-function serial ch.8 serial data input pin(0)
				OCU8_1	-		Output compare ch.8 output pin(1)
				TOT4_0	-		Reload timer ch.4 output pin(0)
				AIN0_0	-		U/D counter ch.0 AIN input pin(0)
				INT11_0	-		INT11 external interrupt input pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
21	25	29	R2	P036	-	A	General-purpose I/O port
				A08	-		External Bus address bit8 output pin
				SCS8_0	-		Serial chip select 8 I/O pin(0)
				OCU7_1	-		Output compare ch.7 output pin(1)
				TOT5_0	-		Reload timer ch.5 output pin(0)
				BIN0_0	-		U/D counter ch.0 BIN input pin(0)
22	26	30	T1	P037	-	A	General-purpose I/O port
				A09	-		External Bus address bit9 output pin
				OCU6_1	-		Output compare ch.6 output pin(1)
				TOT6_0	-		Reload timer ch.6 output pin(0)
				ZIN0_0	-		U/D counter ch.0 ZIN input pin(0)
-	27	31	T4	P174	-	A	General-purpose I/O port
				TRG8_1	-		PPG trigger 8 input pin(1)
-	28	32	U4	P175	-	A	General-purpose I/O port
				TRG9_1	-		PPG trigger 9 input pin(1)
23	29	33	T2	P040	-	A	General-purpose I/O port
				A10	-		External Bus address bit10 output pin
				PPG23_1	-		PPG ch.23 output pin(1)
				TOT7_0	-		Reload timer ch.7 output pin(0)
				AIN1_0	-		U/D counter ch.1 AIN input pin(0)
				SIN0_1	-		Multi-function serial ch.0 serial data input pin(1)
24	30	34	U1	P041	-	I	General-purpose I/O port
				A11	-		External Bus address bit11 output pin
				SIN9_0	-		Multi-function serial ch.9 serial data input pin(0)
				ICU9_1	-		Input capture ch.9 input pin(1)
				BIN1_0	-		U/D counter ch.1 BIN input pin(0)
				INT12_0	-		INT12 external interrupt input pin(0)
25	31	35	U2	P042	-	B	General-purpose I/O port
				A12	-		External Bus address bit12 output pin
				SOT9_0	-		Multi-function serial ch.9 serial data output pin(0)
				AN47	-		ADC analog 47 input pin
				ICU8_1	-		Input capture ch.8 input pin(1)
				TRG0_1	-		PPG trigger 0 input pin(1)
				ZIN1_0	-		U/D counter ch.1 ZIN input pin(0)
26	32	36	V1	P043	-	A	General-purpose I/O port
				A13	-		External Bus address bit13 output pin
				ICU7_1	-		Input capture ch.7 input pin(1)
				TRG1_1	-		PPG trigger 1 input pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
27	33	37	V2	P044	-	A	General-purpose I/O port
				A14	-		External Bus address bit14 output pin
				SCS9_0	-		Serial chip select 9 I/O pin(0)
				ICU6_1	-		Input capture ch.6 input pin(1)
				TRG2_1	-		PPG trigger 2 input pin(1)
28	34	38	W1	P045	-	G	General-purpose I/O port
				A15	-		External Bus address bit15 output pin
				SCK9_0	-		Multi-function serial ch.9 clock I/O pin(0)
				AN46	-		ADC analog 46 input pin
				ICU5_1	-		Input capture ch.5 input pin(1)
				TRG3_1	-		PPG trigger 3 input pin(1)
				TOT1_2	-		Reload timer ch.1 output pin(2)
-	-	39	V3	P204	-	Q	General-purpose I/O port
				SCK13_0/SCL13	-		Multi-function serial ch.13 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				AN59	-		ADC analog 59 input pin
				PPG48_0	-		PPG ch.48 output pin(0)
-	-	40	V4	P205	-	Q	General-purpose I/O port
				SOT13_0/SDA13	-		Multi-function serial ch.13 serial data output pin(0)/I^2C bus serial data I/O pin
				AN58	-		ADC analog 58 input pin
				PPG49_0	-		PPG ch.49 output pin(0)
				AIN2_0	-		U/D counter ch.2 AIN input pin(0)
-	-	41	W4	P206	-	G	General-purpose I/O port
				SIN13_0	-		Multi-function serial ch.13 serial data input pin(0)
				AN57	-		ADC analog 57 input pin
				BIN2_0	-		U/D counter ch.2 BIN input pin(0)
				INT17_0	-		INT17 external interrupt input pin(0)
-	-	42	Y4	P207	-	B	General-purpose I/O port
				SCS13_0	-		Serial chip select 13 I/O pin(0)
				AN56	-		ADC analog 56 input pin
				ZIN2_0	-		U/D counter ch.2 ZIN input pin(0)
29	35	43	W2	P046	-	A	General-purpose I/O port
				A16	-		External Bus address bit16 output pin
				ICU4_1	-		Input capture ch.4 input pin(1)
				TRG4_1	-		PPG trigger 4 input pin(1)
-	36	44	AA3	P176	-	A	General-purpose I/O port
				TRG10_0	-		PPG trigger 10 input pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
30	37	45	Y1	P047	-	B	General-purpose I/O port
				A17	-		External Bus address bit17 output pin
				AN45	-		ADC analog 45 input pin
				TRG8_0	-		PPG trigger 8 input pin(0)
				TIN3_2	-		Reload timer ch.3 event input pin(2)
				SOT0_1	-		Multi-function serial ch.0 serial data output pin(1)
-	38	46	AA4	P177	-	A	General-purpose I/O port
				TRG11_0	-		PPG trigger 11 input pin(0)
31	39	47	Y2	P050	-	A	General-purpose I/O port
				A18	-		External Bus address bit18 output pin
				TRG5_1	-		PPG trigger 5 input pin(1)
				PPG33_0	-		PPG ch.33 output pin(0)
32	40	48	AA1	P051	-	A	General-purpose I/O port
				A19	-		External Bus address bit19 output pin
				TRG9_0	-		PPG trigger 9 input pin(0)
				TX5(128)_0	-		CAN transmission data 5 output pin(0)
-	-	-	AB3	P250	-	A	General-purpose I/O port
				PPG66_0	-		PPG ch.66 output pin(0)
-	-	-	AB4	P251	-	A	General-purpose I/O port
				PPG67_0	-		PPG ch.67 output pin(0)
33	41	49	AA2	P052	-	R	General-purpose I/O port
				A20			External Bus address bit20 output pin
				PPG34_0	-		PPG ch.34 output pin(0)
				INT14_0	-		INT14 external interrupt input pin(0)
				RX5(128)_0	-		CAN reception data 5 input pin(0)
34	42	50	AB1	P053	-	B	General-purpose I/O port
				A21	-		External Bus address bit21 output pin
				AN44	-		ADC analog 44 input pin
				PPG35_0	-		PPG ch.35 output pin(0)
				INT14_1	-		INT14 external interrupt input pin(1)
				SCK0_1	-		Multi-function serial ch.0 clock I/O pin(1)
35	43	51	AB2	P054	-	A	General-purpose I/O port
				SYSCLK	-		External Bus system clock output pin
				PPG36_0	-		PPG ch.36 output pin(0)
-	-	-	AC1	P252	-	A	General-purpose I/O port
-	-	-	AC2	P253	-	A	General-purpose I/O port
-	-	-	AE4	P254	-	A	General-purpose I/O port
				PPG68_0	-		PPG ch.68 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	AD5	P255	-	A	General-purpose I/O port
				PPG69_0	-		PPG ch.69 output pin(0)
38	46	54	AF3	P055	-	G	General-purpose I/O port
				CS2X	-		External Bus chip select 2 output pin
				SIN10_0	-		Multi-function serial ch.10 serial data input pin(0)
				AN43	-		ADC analog 43 input pin
				PPG37_0	-		PPG ch.37 output pin(0)
				TIN4_1	-		Reload timer ch.4 event input pin(1)
-	47	55	AC5	P180	-	A	General-purpose I/O port
				PPG40_0	-		PPG ch.40 output pin(0)
-	48	56	AC6	P181	-	A	General-purpose I/O port
				PPG41_0	-		PPG ch.41 output pin(0)
39	49	57	AE3	P056	-	A	General-purpose I/O port
				CS3X	-		External Bus chip select 3 output pin
				ICU9_0	-		Input capture ch.9 input pin(0)
				PPG0_1	-		PPG ch.0 output pin(1)
				ICU0_1	-		Input capture ch.0 input pin(1)
				TIN5_1	-		Reload timer ch.5 event input pin(1)
				DTTI_2	-		Waveform generator ch.0 to ch.5 input pin(2)
-	-	-	AD6	P256	-	A	General-purpose I/O port
				PPG66_1	-		PPG ch.66 output pin(1)
41	51	59	AE5	P057	-	G	General-purpose I/O port
				RDY_0	-		External Bus RDY input pin (0)
				SCK10_1	-		Multi-function serial ch.10 clock I/O pin(1)
				AN42	-		ADC analog 42 input pin
				ICU8_0	-		Input capture ch.8 input pin(0)
				TRG0_2	-		PPG trigger 0 input pin(2)
				PPG1_1	-		PPG ch.1 output pin(1)
				ICU1_1	-		Input capture ch.1 input pin(1)
				TIN6_1	-		Reload timer ch.6 event input pin(1)
-	56	64	AC7	P182	-	A	General-purpose I/O port
				PPG42_0	-		PPG ch.42 output pin(0)
-	-	65	AE6	P210	-	Q	General-purpose I/O port
				SCK14_0/SCL14	-		Multi-function serial ch.14 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				AN55	-		ADC analog 55 input pin
				PPG50_0	-		PPG ch.50 output pin(0)
				AIN2_1	-		U/D counter ch.2 AIN input pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	66	AC8	P211	-	Q	General-purpose I/O port
				SOT14_0/SDA14	-		Multi-function serial ch.14 serial data output pin(0)/I2C bus serial data I/O pin
				AN54	-		ADC analog 54 input pin
				PPG51_0	-		PPG ch.51 output pin(0)
				BIN2_1	-		U/D counter ch.2 BIN input pin(1)
-	-	67	AE7	P212	-	G	General-purpose I/O port
				SIN14_0	-		Multi-function serial ch.14 serial data input pin(0)
				AN53	-		ADC analog 53 input pin
				FRCK6_0	-		Free-run timer 6 clock input pin(0)
				ZIN2_1	-		U/D counter ch.2 ZIN input pin(1)
				INT18_0	-		INT18 external interrupt input pin(0)
-	-	68	AD8	P213	-	B	General-purpose I/O port
				SCS14_0	-		Serial chip select 14 I/O pin(0)
				AN52	-		ADC analog 52 input pin
				FRCK7_0	-		Free-run timer 7 clock input pin(0)
				INT17_1	-		INT17 external interrupt input pin(1)
46	57	69	AE8	P060	-	A	General-purpose I/O port
				SCS10_0	-		Serial chip select 10 I/O pin(0)
				PPG2_1	-		PPG ch.2 output pin(1)
				ICU2_1	-		Input capture ch.2 input pin(1)
				TOT5_1	-		Reload timer ch.5 output pin(1)
				INT13_0	-		INT13 external interrupt input pin(0)
47	58	70	AC10	P061	-	B	General-purpose I/O port
				SOT10_1	-		Multi-function serial ch.10 serial data output pin(1)
				AN41	-		ADC analog 41 input pin
				ICU6_0	-		Input capture ch.6 input pin(0)
				PPG3_1	-		PPG ch.3 output pin(1)
				ICU3_1	-		Input capture ch.3 input pin(1)
				TOT6_1	-		Reload timer ch.6 output pin(1)
				INT13_1	-		INT13 external interrupt input pin(1)
48	59	71	AD11	P062	-	B	General-purpose I/O port
				SCS10_1	-		Serial chip select 10 I/O pin(1)
				SCS40_0	-		Serial chip select 40 I/O pin(0)
				AN40	-		ADC analog 40 input pin
				PPG4_1	-		PPG ch.4 output pin(1)
				FRCK0_0	-		Free-run timer 0 clock input pin(0)
				TOT7_1	-		Reload timer ch.7 output pin(1)
				ZIN1_1	-		U/D counter ch.1 ZIN input pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
49	60	72	AC11	P063	-	B	General-purpose I/O port
				SCS41_0	-		Serial chip select 41 output pin(0)
				AN39	-		ADC analog 39 input pin
				PPG5_1	-		PPG ch.5 output pin(1)
				FRCK1_0	-		Free-run timer 1 clock input pin(0)
				BIN1_1	-		U/D counter ch.1 BIN input pin(1)
-	61	73	AF12	P183	-	A	General-purpose I/O port
				PPG43_0	-		PPG ch.43 output pin(0)
50	62	74	AE12	P064	-	B	General-purpose I/O port
				SCS42_0	-		Serial chip select 42 output pin(0)
				AN38	-		ADC analog 38 input pin
				FRCK2_0	-		Free-run timer 2 clock input pin(0)
				AIN1_1	-		U/D counter ch.1 AIN input pin(1)
				PPG43_1	-		PPG ch.43 output pin(1)
51	63	75	AC12	P065	-	A	General-purpose I/O port
				SCS43_0	-		Serial chip select 43 output pin(0)
				FRCK3_0	-		Free-run timer 3 clock input pin(0)
				ZIN0_1	-		U/D counter ch.0 ZIN input pin(1)
				PPG44_1	-		PPG ch.44 output pin(1)
-	64	76	AF13	P184	-	A	General-purpose I/O port
				PPG44_0	-		PPG ch.44 output pin(0)
-	65	77	AE13	P185	-	A	General-purpose I/O port
				PPG45_0	-		PPG ch.45 output pin(0)
52	66	78	AC13	P066	-	B	General-purpose I/O port
				SOT4_2	-		Multi-function serial ch.4 serial data output pin(2)
				SCS3_0	-		Serial chip select 3 I/O pin(0)
				AN37	-		ADC analog 37 input pin
				FRCK4_0	-		Free-run timer 4 clock input pin(0)
				BIN0_1	-		U/D counter ch.0 BIN input pin(1)
53	67	79	AF14	P067	-	B	General-purpose I/O port
				AN36	-		ADC analog 36 input pin
				FRCK5_0	-		Free-run timer 5 clock input pin(0)
				AIN0_1	-		U/D counter ch.0 AIN input pin(1)
54	68	80	AE14	P070	-	A	General-purpose I/O port
				ICU0_2	-		Input capture ch.0 input pin(2)
55	69	81	AD14	P071	-	G	General-purpose I/O port
				SCK4_2	-		Multi-function serial ch.4 clock I/O pin(2)
				AN35	-		ADC analog 35 input pin
				ICU1_2	-		Input capture ch.1 input pin(2)
				MONCLK	-		Clock monitor output pin

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
56	70	82	AC14	P072	-	G	General-purpose I/O port
				SIN4_0	-		Multi-function serial ch.4 serial data input pin(0)
				AN34	-		ADC analog 34 input pin
				ICU2_2	-		Input capture ch.2 input pin(2)
				INT5_0	-		INT5 external interrupt input pin(0)
57	71	83	AF15	P073	-	D	General-purpose I/O port
				SOT4_0/SDA4	-		Multi-function serial ch.4 serial data output pin(0)/I^2C bus serial data I/O pin
				AN33	-		ADC analog 33 input pin
				ICU3_2	-		Input capture ch.3 input pin(2)
-	-	-	AE15	P262	-	A	General-purpose I/O port
				PPG70_0	-		PPG ch.70 output pin(0)
-	-	-	AC15	P263	-	A	General-purpose I/O port
				PPG71_0	-		PPG ch.71 output pin(0)
-	72	84	AF16	P186	-	A	General-purpose I/O port
				PPG46_0	-		PPG ch.46 output pin(0)
-	73	85	AE16	P187	-	A	General-purpose I/O port
				PPG47_0	-		PPG ch.47 output pin(0)
58	74	86	AC16	P074	-	E	General-purpose I/O port
				SCK4_0/SCL4	-		Multi-function serial ch.4 clock I/O pin(0) / I^2C bus serial clock I/O pin
-	-	87	AF18	P214	-	Q	General-purpose I/O port
				SCK15_0/SCL15	-		Multi-function serial ch.15 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				AN51	-		ADC analog 51 input pin
				PPG52_0	-		PPG ch.52 output pin(0)
-	-	88	AF17	P215	-	Q	General-purpose I/O port
				SOT15_0/SDA15	-		Multi-function serial ch.15 serial data output pin(0)/I^2C bus serial data I/O pin
				AN50	-		ADC analog 50 input pin
				FRCK8_0	-		Free-run timer 8 clock input pin(0)
				PPG53_0	-		PPG ch.53 output pin(0)
-	-	89	AE17	P216	-	G	General-purpose I/O port
				SIN15_0	-		Multi-function serial ch.15 serial data input pin(0)
				AN49	-		ADC analog 49 input pin
				FRCK9_0	-		Free-run timer 9 clock input pin(0)
				TRG12_1	-		PPG trigger 12 input pin(1)
				INT19_0	-		INT19 external interrupt input pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	90	AF19	P217	-	B	General-purpose I/O port
				SCS15_0	-		Serial chip select 15 I/O pin(0)
				AN48	-		ADC analog 48 input pin
				FRCK10_0	-		Free-run timer 10 clock input pin(0)
				TRG13_1	-		PPG trigger 13 input pin(1)
59	75	91	AE18	P075	-	F	General-purpose I/O port
				SIN3_0	-		Multi-function serial ch.3 serial data input pin(0)
				INT4_0	-		INT4 external interrupt input pin(0)
				RX5(128)_1	-		CAN reception data 5 input pin(1)
60	76	92	AD17	P076	-	P	General-purpose I/O port
				SOT3_0/SDA3	-		Multi-function serial ch.3 serial data output pin(0)/I^2C bus serial data I/O pin
				TX5(128)_1	-		CAN transmission data 5 output pin(1)
61	77	93	AF20	P077	-	E	General-purpose I/O port
				SCK3_0/SCL3	-		Multi-function serial ch.3 clock I/O pin(0)/ I^2C bus serial clock I/O pin
-	-	-	AE19	P264	-	A	General-purpose I/O port
				PPG72_0	-		PPG ch.72 output pin(0)
-	-	-	AC17	P265	-	A	General-purpose I/O port
				PPG73_0	-		PPG ch.73 output pin(0)
62	78	94	AF21	P152	-	A	General-purpose I/O port
				SCS53_0	-		Serial chip select 53 output pin(0)
63	79	95	AE20	P153	-	G	General-purpose I/O port
				SCK5_0/SCL5	-		Multi-function serial ch.5 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				AN32	-		ADC analog 32 input pin
				FRCK1_1	-		Free-run timer 1 clock input pin(1)
				INT4_1	-		INT4 external interrupt input pin(1)
64	80	96	AC18	P080	-	A	General-purpose I/O port
				SCS52_0	-		Serial chip select 52 output pin(0)
				PPG0_0	-		PPG ch.0 output pin(0)
65	81	97	AF22	P081	-	G	General-purpose I/O port
				SOT5_0/SDA5	-		Multi-function serial ch.5 serial data output pin(0)/I^2C bus serial data I/O pin
				AN0	-		ADC analog 0 input pin
				PPG1_0	-		PPG ch.1 output pin(0)
-	-	-	AE21	TDO	-	W	JTAG test data output
-	-	-	AD20	TDI	-	V	JTAG test data input

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
66	82	98	AC19	P082	-	G	General-purpose I/O port
				SIN5_0	-		Multi-function serial ch.5 serial data input pin(0)
				AN1	-		ADC analog 1 input pin
				PPG2_0	-		PPG ch.2 output pin(0)
-	-	-	AE22	TRST	-	V	JTAG test reset input
-	-	-	AC20	TCK	-	V	JTAG test clock input
-	-	-	AE23	TMS	-	V	JTAG test mode state input
67	83	99	AC21	P083	-	B	General-purpose I/O port
				SCS50_0	-		Serial chip select 50 I/O pin(0)
				AN2	-		ADC analog 2 input pin
				PPG3_0	-		PPG ch.3 output pin(0)
68	84	100	AF23	P084	-	B	General-purpose I/O port
				SCS51_0	-		Serial chip select 51 output pin(0)
				AN3	-		ADC analog 3 input pin
				PPG4_0	-		PPG ch.4 output pin(0)
69	85	101	AD23	P085	-	A	General-purpose I/O port
				PPG5_0	-		PPG ch.5 output pin(0)
70	86	102	AC22	P086	-	C	General-purpose I/O port
				DAO1	-		DAC analog 1 output pin
				PPG6_0	-		PPG ch.6 output pin(0)
71	87	103	AD25	P087	-	C	General-purpose I/O port
				DAO0	-		DAC analog 0 output pin
				PPG7_0	-		PPG ch.7 output pin(0)
				INT8_0	-		INT8 external interrupt input pin(0)
-	-	-	AC24	P266	-	A	General-purpose I/O port
				PPG74_0	-		PPG ch.74 output pin(0)
-	-	-	AB23	P267	-	A	General-purpose I/O port
				PPG75_0	-		PPG ch.75 output pin(0)
-	90	106	AD26	P190	-	A	General-purpose I/O port
				TIN0_1	-		Reload timer ch.0 event input pin(1)
-	91	107	AC25	P191	-	A	General-purpose I/O port
				TIN1_1	-		Reload timer ch.1 event input pin(1)
74	92	108	AB24	P090	-	B	General-purpose I/O port
				AN4	-		ADC analog 4 input pin
				ICU0_0	-		Input capture ch.0 input pin(0)
				TIN2_1	-		Reload timer ch.2 event input pin(1)
-	-	-	AA23	P270	-	A	General-purpose I/O port
				PPG76_0	-		PPG ch.76 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	AC26	P271	-	A	General-purpose I/O port
				PPG77_0	-		PPG ch.77 output pin(0)
75	93	109	AB25	P091	-	B	General-purpose I/O port
				AN5	-		ADC analog 5 input pin
				PPG41_1	-		PPG ch.41 output pin(1)
				ICU1_0	-		Input capture ch.1 input pin(0)
				TIN3_1	-		Reload timer ch.3 event input pin(1)
76	94	110	Y23	P092	-	B	General-purpose I/O port
				AN6	-		ADC analog 6 input pin
				PPG40_1	-		PPG ch.40 output pin(1)
				ICU2_0	-		Input capture ch.2 input pin(0)
				TOT0_1	-		Reload timer ch.0 output pin(1)
-	95	111	AB26	P192	-	A	General-purpose I/O port
				PPG24_1	-		PPG ch.24 output pin(1)
				TOT1_1	-		Reload timer ch.1 output pin(1)
-	-	-	AA25	P272	-	A	General-purpose I/O port
				PPG78_0	-		PPG ch.78 output pin(0)
-	-	-	Y24	P273	-	A	General-purpose I/O port
				PPG79_0	-		PPG ch.79 output pin(0)
77	96	112	W23	P093	-	J	General-purpose I/O port
				TX0(128)_1	-		CAN transmission data 0 output pin(1)
				SIN11_0	-		Multi-function serial ch.11 serial data input pin(0)
				AN7	-		ADC analog 7 input pin
				ICU4_2	-		Input capture ch.4 input pin(2)
				PPG16_1	-		PPG ch.16 output pin(1)
				ICU3_0	-		Input capture ch.3 input pin(0)
				TOT2_1	-		Reload timer ch.2 output pin(1)
78	97	113	AA26	P094	-	B	General-purpose I/O port
				AN8	-		ADC analog 8 input pin
				ICU4_0	-		Input capture ch.4 input pin(0)
				TOT3_1	-		Reload timer ch.3 output pin(1)
79	98	114	Y25	P095	-	B	General-purpose I/O port
				TX0(128)_0	-		CAN transmission data 0 output pin(0)
				SCS11_0	-		Serial chip select 11 I/O pin(0)
				AN9	-		ADC analog 9 input pin

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
80	99	115	V23	P096	-	G	General-purpose I/O port
				RX0(128)_0	-		CAN reception data 0 input pin(0)
				SOT11_0/SDA11	-		Multi-function serial ch.11 serial data output pin(0)/I2C bus serial data I/O pin
				AN10	-		ADC analog 10 input pin
				INT0_0	-		INT0 external interrupt input pin(0)
81	100	116	Y26	P097	-	G	General-purpose I/O port
				SCK11_0/SCL11	-		Multi-function serial ch.11 clock I/O pin(0)/ I2C bus serial clock I/O pin
				AN11	-		ADC analog 11 input pin
				ICU5_0	-		Input capture ch.5 input pin(0)
				PPG17_1	-		PPG ch.17 output pin(1)
-	-	117	W25	P220	-	P	General-purpose I/O port
				SCK16_0/SCL16	-		Multi-function serial ch.16 clock I/O pin(0)/ I2C bus serial clock I/O pin
				ICU10_0	-		Input capture ch.10 input pin(0)
				PPG48_1	-		PPG ch.48 output pin(1)
-	-	118	U23	P221	-	P	General-purpose I/O port
				SOT16_0/SDA16	-		Multi-function serial ch.16 serial data output pin(0)/I2C bus serial data I/O pin
				ICU11_0	-		Input capture ch.11 input pin(0)
				PPG49_1	-		PPG ch.49 output pin(1)
-	-	119	V25	P222	-	I	General-purpose I/O port
				SIN16_0	-		Multi-function serial ch.16 serial data input pin(0)
				PPG54_0	-		PPG ch.54 output pin(0)
				INT20_0	-		INT20 external interrupt input pin(0)
-	-	-	U24	P275	-	A	General-purpose I/O port
				PPG67_1	-		PPG ch.67 output pin(1)
-	-	-	U25	P276	-	A	General-purpose I/O port
				TRG16_1	-		PPG trigger 16 input pin(1)
				PPG86_1	-		PPG ch.86 output pin(1)
85	104	123	T25	P100	-	G	General-purpose I/O port
				SCK7_0/SCL7	-		Multi-function serial ch.7 clock I/O pin(0)/ I2C bus serial clock I/O pin
				AN12	-		ADC analog 12 input pin
				PPG8_0	-		PPG ch.8 output pin(0)
86	105	124	T23	P101	-	G	General-purpose I/O port
				SOT7_0/SDA7	-		Multi-function serial ch.7 serial data output pin(0)/I2C bus serial data I/O pin
				AN13	-		ADC analog 13 input pin
				PPG9_0	-		PPG ch.9 output pin(0)
				TX3(128)_0	-		CAN transmission data 3 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
87	106	125	R26	P102	-	G	General-purpose I/O port
				SIN7_0	-		Multi-function serial ch.7 serial data input pin(0)
				AN14	-		ADC analog 14 input pin
				PPG10_0	-		PPG ch.10 output pin(0)
				INT10_0	-		INT10 external interrupt input pin(0)
				RX3(128)_0	-		CAN reception data 3 input pin(0)
88	107	126	R25	P103	-	H	General-purpose I/O port
				SCS73_0	-		Serial chip select 73 output pin(0)
				AN15	-		ADC analog 15 input pin
				PPG11_0	-		PPG ch.11 output pin(0)
89	108	127	R23	P104	-	H	General-purpose I/O port
				SCS72_0	-		Serial chip select 72 output pin(0)
				AN16	-		ADC analog 16 input pin
				PPG12_0	-		PPG ch.12 output pin(0)
90	109	128	P25	P105	-	H	General-purpose I/O port
				SCS71_0	-		Serial chip select 71 output pin(0)
				AN17	-		ADC analog 17 input pin
				PPG13_0	-		PPG ch.13 output pin(0)
91	110	129	P24	P106	-	H	General-purpose I/O port
				SCS70_0	-		Serial chip select 70 I/O pin(0)
				AN18	-		ADC analog 18 input pin
				PPG14_0	-		PPG ch.14 output pin(0)
92	111	130	P23	P107	-	U	General-purpose I/O port
				AN19	-		ADC analog 19 input pin
				PPG15_0	-		PPG ch.15 output pin(0)
				TXENA_1	-		FlexRay ch.A operation enable output(1)
-	112	131	P26	P193	-	A	General-purpose I/O port
				PPG25_1	-		PPG ch.25 output pin(1)
93	113	132	N23	P154	-	U	General-purpose I/O port
				AN20	-		ADC analog 20 input pin
				TXDA_1	-		FlexRay ch.A data output(1)
94	114	133	L26	P155	-	S	General-purpose I/O port
				AN21	-		ADC analog 21 input pin
				RXDA_1	-		FlexRay ch.A data input(1)
95	115	136	L25	NMIX	N	M	Non-maskable interrupt input pin
-	-	-	L24	P277	-	A	General-purpose I/O port
				TRG17_1	-		PPG trigger 17 input pin(1)
				PPG87_1	-		PPG ch.87 output pin(1)
96	116	137	L23	P110	-	B	General-purpose I/O port
				TX1(128)_0	-		CAN transmission data 1 output pin(0)
				SCS63_0	-		Serial chip select 63 output pin(0)
				AN22	-		ADC analog 22 input pin

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
97	117	138	J26	P111	-	G	General-purpose I/O port
				RX1(128)_0	-		CAN reception data 1 input pin(0)
				SCS62_0	-		Serial chip select 62 output pin(0)
				AN23	-		ADC analog 23 input pin
				INT1_0	-		INT1 external interrupt input pin(0)
98	118	139	K26	P112	-	U	General-purpose I/O port
				AN24	-		ADC analog 24 input pin
				PPG16_0	-		PPG ch.16 output pin(0)
				RTO0_0	-		Waveform generator ch.0 output pin(0)
				TXENB_1	-		FlexRay ch.B operation enable output(1)
99	119	140	K25	P113	-	U	General-purpose I/O port
				AN25	-		ADC analog 25 input pin
				PPG17_0	-		PPG ch.17 output pin(0)
				RTO1_0	-		Waveform generator ch.1 output pin(0)
				TXDB_1	-		FlexRay ch.B data output(1)
-	120	141	H26	P194	-	A	General-purpose I/O port
				FRCK5_1	-		Free-run timer 5 clock input pin(1)
				PPG26_1	-		PPG ch.26 output pin(1)
-	121	142	J25	P195	-	A	General-purpose I/O port
				FRCK4_1	-		Free-run timer 4 clock input pin(1)
				PPG27_1	-		PPG ch.27 output pin(1)
-	-	-	G26	P280	-	A	General-purpose I/O port
				PPG80_0	-		PPG ch.80 output pin(0)
-	-	-	H25	P281	-	A	General-purpose I/O port
				PPG81_0	-		PPG ch.81 output pin(0)
100	122	143	K23	P114	-	S	General-purpose I/O port
				SCS61_0	-		Serial chip select 61 output pin(0)
				AN26	-		ADC analog 26 input pin
				PPG18_0	-		PPG ch.18 output pin(0)
				RTO2_0	-		Waveform generator ch.2 output pin(0)
				RXDB_1	-		FlexRay ch.B data input(1)
101	123	144	F26	P115	-	G	General-purpose I/O port
				RX1(128)_1	-		CAN reception data 1 input pin(1)
				SOT6_0/SDA6	-		Multi-function serial ch.6 serial data output pin(0)/I^2C bus serial data I/O pin
				AN27	-		ADC analog 27 input pin
				PPG19_0	-		PPG ch.19 output pin(0)
				RTO3_0	-		Waveform generator ch.3 output pin(0)
				INT1_1	-		INT1 external interrupt input pin(1)
102	124	145	G25	P116	-	G	General-purpose I/O port
				SCK6_0/SCL6	-		Multi-function serial ch.6 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				AN28	-		ADC analog 28 input pin
				PPG20_0	-		PPG ch.20 output pin(0)
				RTO4_0	-		Waveform generator ch.4 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
103	125	146	H24	P117	-	B	General-purpose I/O port
				SCS60_0	-		Serial chip select 60 I/O pin(0)
				AN29	-		ADC analog 29 input pin
				PPG21_0	-		PPG ch.21 output pin(0)
				RTO5_0	-		Waveform generator ch.5 output pin(0)
-	126	147	J23	P196	-	A	General-purpose I/O port
				FRCK3_1	-		Free-run timer 3 clock input pin(1)
				PPG28_1	-		PPG ch.28 output pin(1)
-	-	-	E26	P282	-	A	General-purpose I/O port
				PPG82_0	-		PPG ch.82 output pin(0)
-	-	-	F25	P283	-	A	General-purpose I/O port
				PPG83_0	-		PPG ch.83 output pin(0)
104	127	148	H23	P120	-	S	General-purpose I/O port
				AN30			ADC analog 30 input pin
				OCU6_0	-		Output compare ch.6 output pin(0)
				PPG22_0	-		PPG ch.22 output pin(0)
				INT9_0	-		INT9 external interrupt input pin(0)
				RX4(128)_0	-		CAN reception data 4 input pin(0)
105	128	149	D26	P121	-	A	General-purpose I/O port
				OCU7_0	-		Output compare ch.7 output pin(0)
				PPG23_0	-		PPG ch.23 output pin(0)
				TX4(128)_0	-		CAN transmission data 4 output pin(0)
106	129	150	E25	P122	-	J	General-purpose I/O port
				SIN6_0	-		Multi-function serial ch.6 serial data input pin(0)
				AN31	-		ADC analog 31 input pin
				OCU8_0	-		Output compare ch.8 output pin(0)
				INT9_1	-		INT9 external interrupt input pin(1)
-	-	151	G23	P225	-	P	General-purpose I/O port
				SCK17_0/SCL17	-		Multi-function serial ch.17 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				PPG55_0	-		PPG ch.55 output pin(0)
-	-	152	D25	P226	-	P	General-purpose I/O port
				SOT17_0/SDA17	-		Multi-function serial ch.17 serial data output pin(0)/I^2C bus serial data I/O pin
				PPG56_0	-		PPG ch.56 output pin(0)
-	-	153	E24	P227	-	I	General-purpose I/O port
				SIN17_0	-		Multi-function serial ch.17 serial data input pin(0)
				PPG57_0	-		PPG ch.57 output pin(0)
				INT21_0	-		INT21 external interrupt input pin(0)
-	130	154	F23	P197	-	A	General-purpose I/O port
				PPG29_1	-		PPG ch.29 output pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
107	131	155	E23	P123	-	R	General-purpose I/O port
				OCU9_0	-		Output compare ch.9 output pin(0)
				STOPWT_1	-		FlexRay stopwatch input(1)
110	134	158	C26	DEBUGIF	-	L	DEBUGIF I/O pin for debug (OCD)
-	-	-	C25	P284	-	A	General-purpose I/O port
				PPG84_0	-		PPG ch.84 output pin(0)
-	-	-	D22	P285	-	A	General-purpose I/O port
				PPG85_0	-		PPG ch.85 output pin(0)
-	135	159	C22	P160	-	A	General-purpose I/O port
				PPG30_1	-		PPG ch.30 output pin(1)
-	136	160	D21	P161	-	A	General-purpose I/O port
				PPG31_1	-		PPG ch.31 output pin(1)
-	-	-	B22	P286	-	A	General-purpose I/O port
				TRG18_0	-		PPG trigger 18 input pin(0)
-	-	-	C21	P287	-	A	General-purpose I/O port
				TRG19_0	-		PPG trigger 19 input pin(0)
111	137	161	-	P124	-	A	General-purpose I/O port
				OCU10_0	-		Output compare ch.10 output pin(0)
				TRST	-		JTAG test reset input
-	-	-	D20	P124	-	A	General-purpose I/O port
				OCU10_0	-		Output compare ch.10 output pin(0)
112	138	162	-	P125	-	A	General-purpose I/O port
				OCU11_0	-		Output compare ch.11 output pin(0)
				TMS	-		JTAG test mode state input
-	-	-	A22	P125	-	A	General-purpose I/O port
				OCU11_0	-		Output compare ch.11 output pin(0)
-	-	163	B21	P230	-	P	General-purpose I/O port
				SCK18_0/SCL18	-		Multi-function serial ch.18 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				OCU12_0	-		Output compare ch.12 output pin(0)
				PPG58_0	-		PPG ch.58 output pin(0)
-	-	164	C20	P231	-	P	General-purpose I/O port
				SOT18_0/SDA18	-		Multi-function serial ch.18 serial data output pin(0)/I^2C bus serial data I/O pin
				OCU13_0	-		Output compare ch.13 output pin(0)
				PPG59_0	-		PPG ch.59 output pin(0)
-	-	165	D19	P232	-	I	General-purpose I/O port
				SIN18_0	-		Multi-function serial ch.18 serial data input pin(0)
				PPG60_0	-		PPG ch.60 output pin(0)
				INT22_0	-		INT22 external interrupt input pin(0)
-	-	166	C19	P233	-	A	General-purpose I/O port
				SCS18_0	-		Serial chip select 18 I/O pin(0)
				PPG61_0	-		PPG ch.61 output pin(0)
				INT16_1	-		INT16 external interrupt input pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	D18	P290	-	A	General-purpose I/O port
				TRG20_0	-		PPG trigger 20 input pin(0)
				PPG64_1	-		PPG ch.64 output pin(1)
-	-	-	B18	P291	-	A	General-purpose I/O port
				TRG21_0	-		PPG trigger 21 input pin(0)
				PPG65_1	-		PPG ch.65 output pin(1)
113	139	167	-	P126	-	F	General-purpose I/O port
				SIN0_0	-		Multi-function serial ch.0 serial data input pin(0)
				INT6_0	-		INT6 external interrupt input pin(0)
				TDI	-		JTAG test data input
-	-	-	C18	P126	-	F	General-purpose I/O port
				SIN0_0	-		Multi-function serial ch.0 serial data input pin(0)
				INT6_0	-		INT6 external interrupt input pin(0)
114	140	168	-	P127	-	A	General-purpose I/O port
				SOT0_0	-		Multi-function serial ch.0 serial data output pin(0)
				TDO	-		JTAG test data output
-	-	-	C17	P127	-	A	General-purpose I/O port
				SOT0_0	-		Multi-function serial ch.0 serial data output pin(0)
115	141	169	-	P130	-	F	General-purpose I/O port
				SCK0_0	-		Multi-function serial ch.0 clock I/O pin(0)
				TCK	-		JTAG test clock input
-	-	-	D17	P130	-	F	General-purpose I/O port
				SCK0_0	-		Multi-function serial ch.0 clock I/O pin(0)
-	142	170	C16	P162	-	A	General-purpose I/O port
				TRG5_2	-		PPG trigger 5 input pin(2)
-	143	171	D16	P163	-	A	General-purpose I/O port
				TRG6_2	-		PPG trigger 6 input pin(2)
116	144	172	B23	MD0	-	K	Mode pin 0
117	145	173	A23	MD1	-	K	Mode pin 1
118	146	174	A20	X0	-	N	Main clock oscillation input pin
119	147	175	A19	X1	-	N	Main clock oscillation output pin
121	149	177	A17	P135	-	A	General-purpose I/O port
				DTTI_0	-		Waveform generator ch.0 to ch.5 input pin(0)
				X1A	-	O	Sub clock oscillation output pin
122	150	178	A16	P136	-	A	General-purpose I/O port
				X0A	-	O	Sub clock oscillation input pin
123	151	179	B15	RSTX	N	M	External reset input pin
126	154	182	D15	P133	-	A	General-purpose I/O port
				TX2(128)_0	-		CAN transmission data 2 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
127	155	183	D14	P134	-	F	General-purpose I/O port
				RX2(128)_0	-		CAN reception data 2 input pin(0)
				SCS1_1	-		Serial chip select 1 I/O pin(1)
				ICU7_0	-		Input capture ch.7 input pin(0)
				INT7_0	-		INT7 external interrupt input pin(0)
131	159	187	A10	P000	-	F	General-purpose I/O port
				D16	-		External Bus data bit16 I/O pin
				SIN1_0	-		Multi-function serial ch.1 serial data input pin(0)
				TIOA0_1	-		Base timer ch.0 TIOA output pin(1)
				INT2_0	-		INT2 external interrupt input pin(0)
132	160	188	B10	P001	-	R	General-purpose I/O port
				D17	-		External Bus data bit17 I/O pin
				SOT1_0	-		Multi-function serial ch.1 serial data output pin(0)
				TIOA1_1	-		Base timer ch.1 TIOA I/O pin(1)
133	161	189	A9	P002	-	F	General-purpose I/O port
				D18	-		External Bus data bit18 I/O pin
				SCK1_0	-		Multi-function serial ch.1 clock I/O pin(0)
				TIOB0_1	-		Base timer ch.0 TIOB input pin(1)
134	162	190	B9	P003	-	T	General-purpose I/O port
				D19	-		External Bus data bit19 I/O pin
				SIN2_0	-		Multi-function serial ch.2 serial data input pin(0)
				TIOB1_1	-		Base timer ch.1 TIOB input pin(1)
				INT3_0	-		INT3 external interrupt input pin(0)
				TXENA_0	-		FlexRay ch.A operation enable output(0)
135	163	191	A8	P004	-	R	General-purpose I/O port
				D20	-		External Bus data bit20 I/O pin
				SOT2_0	-		Multi-function serial ch.2 serial data output pin(0)
				TXDA_0	-		FlexRay ch.A data output(0)
-	164	192	D12	P164	-	A	General-purpose I/O port
				PPG32_1	-		PPG ch.32 output pin(1)
136	165	193	B8	P005	-	F	General-purpose I/O port
				D21	-		External Bus data bit21 I/O pin
				SCK2_0	-		Multi-function serial ch.2 clock I/O pin(0)
				ADTG0_1	-		A/D converter external trigger input pin 0(1)
				INT7_1	-		INT7 external interrupt input pin(1)
				RXDA_0	-		FlexRay ch.A data input(0)
-	166	194	C11	P165	-	A	General-purpose I/O port
				PPG33_1	-		PPG ch.33 output pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
137	167	195	A7	P006	-	R	General-purpose I/O port
				D22	-		External Bus data bit22 I/O pin
				SCS2_0	-		Serial chip select 2 I/O pin(0)
				ADTG1_1	-		A/D converter external trigger input pin 1(1)
				INT2_1	-		INT2 external interrupt input pin(1)
				TXENB_0	-		FlexRay ch.B operation enable output(0)
138	168	196	B7	P007	-	R	General-purpose I/O port
				D23	-		External Bus data bit23 I/O pin
				TXDB_0	-		FlexRay ch.B data output(0)
-	-	-	D11	P292	-	A	General-purpose I/O port
-	-	-	C10	P293	-	A	General-purpose I/O port
-	169	197	D10	P166	-	A	General-purpose I/O port
				PPG34_1	-		PPG ch.34 output pin(1)
139	170	198	A6	P010	-	R	General-purpose I/O port
				D24	-		External Bus data bit24 I/O pin
				RXDB_0	-		FlexRay ch.B data input(0)
-	-	199	C9	P234	-	P	General-purpose I/O port
				SCK19_0/SCL19	-		Multi-function serial ch.19 clock I/O pin(0)/ I^2C bus serial clock I/O pin
				PPG62_0	-		PPG ch.62 output pin(0)
-	-	200	D9	P235	-	P	General-purpose I/O port
				SOT19_0/SDA19	-		Multi-function serial ch.19 serial data output pin(0)/I^2C bus serial data I/O pin
				PPG63_0	-		PPG ch.63 output pin(0)
				AIN3_0	-		U/D counter ch.3 AIN input pin(0)
-	-	201	D8	P236	-	I	General-purpose I/O port
				SIN19_0	-		Multi-function serial ch.19 serial data input pin(0)
				TRG14_0	-		PPG trigger 14 input pin(0)
				BIN3_0	-		U/D counter ch.3 BIN input pin(0)
				INT23_0	-		INT23 external interrupt input pin(0)
-	-	202	D7	P237	-	A	General-purpose I/O port
				SCS19_0	-		Serial chip select 19 I/O pin(0)
				TRG15_0	-		PPG trigger 15 input pin(0)
				ZIN3_0	-		U/D counter ch.3 ZIN input pin(0)
140	171	203	B6	P011	-	R	General-purpose I/O port
				WOT	-		RTC output pin
				D25	-		External Bus data bit25 I/O pin
				SOT2_1	-		Multi-function serial ch.2 serial data output pin(1)
				TIOA0_0	-		Base timer ch.0 TIOA output pin(0)
				INT3_1	-		INT3 external interrupt input pin(1)
141	172	204	A5	P012	-	R	General-purpose I/O port
				D26	-		External Bus data bit26 I/O pin
				TIOB0_0	-		Base timer ch.0 TIOB input pin(0)
				STOPWT_0	-		FlexRay stopwatch input(0)

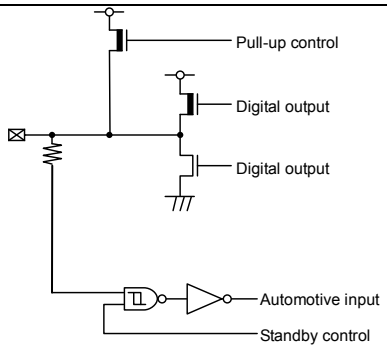
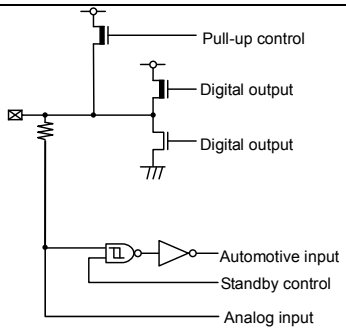
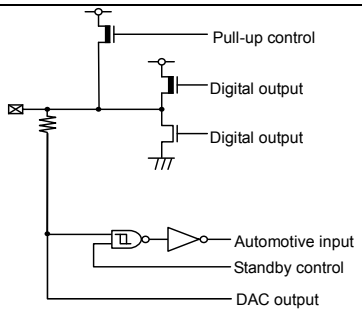
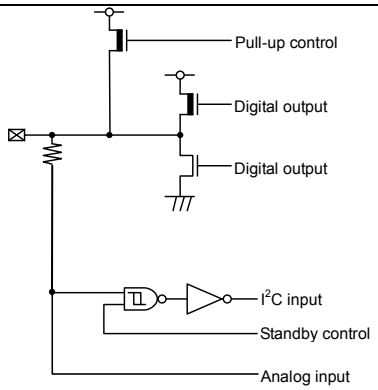
Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	C6	P294	-	A	General-purpose I/O port
				PPG86_0	-		PPG ch.86 output pin(0)
-	-	-	C5	P295	-	A	General-purpose I/O port
				PPG87_0	-		PPG ch.87 output pin(0)
-	173	205	D6	P167	-	A	General-purpose I/O port
				PPG35_1	-		PPG ch.35 output pin(1)
-	-	-	C4	P296	-	A	General-purpose I/O port
-	-	-	D5	P297	-	A	General-purpose I/O port
142	174	206	B5	P013	-	R	General-purpose I/O port
				D27	-		External Bus data bit27 I/O pin
				TIOA1_0	-		Base timer ch.1 TIOA I/O pin(0)
143	175	207	A4	P014	-	R	General-purpose I/O port
				D28	-		External Bus data bit28 I/O pin
				TIOB1_0	-		Base timer ch.1 TIOB input pin(0)
40	50	58	AF4	AVCC1	-	-	A/D, D/A converter unit1 analog power supply pin
84	103	122	T26	AVCC0	-	-	A/D, D/A converter unit0 analog power supply pin
42	52	60	AF5	AVRH1	-	-	A/D converter unit1 upper limit reference voltage pin
83	102	121	U26	AVRH0	-	-	A/D converter unit0 upper limit reference voltage pin
43	53	61	-	AVSS1/AVRL1	-	-	A/D, D/A converter unit1 GND / A/D converter unit1 lower limit reference voltage pin
-	-	-	AF7	AVSS1	-	-	A/D, D/A converter unit1 GND
-	-	-	AF6	AVRL1	-	-	A/D converter unit1 lower limit reference voltage pin
82	101	120	-	AVSS0/AVRL0	-	-	A/D, D/A converter unit0 GND / A/D converter unit0 lower limit reference voltage pin
-	-	-	W26	AVSS0	-	-	A/D, D/A converter unit0 GND
-	-	-	V26	AVRL0	-	-	A/D converter unit0 lower limit reference voltage pin
130	158	186	A13	C	-	-	External capacity connection output pin
-	-	63	AF10	VCC	-	-	Power supply (1)
45	55	104	AF11				
72	88	134	AE10				
109	133	157	AE11				
124	152	180	AE24				
-	-	-	AF24				
-	-	-	N25				
-	-	-	N26				
-	-	-	A24				
-	-	-	B24				
-	-	-	A14				
-			B14				

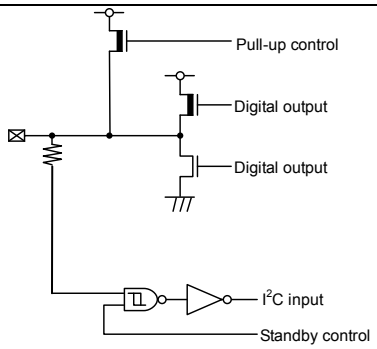
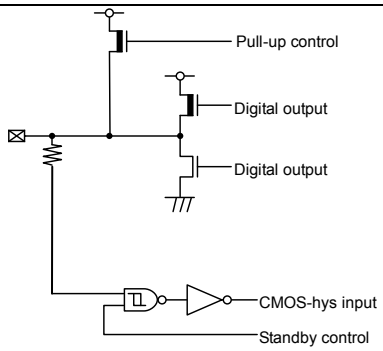
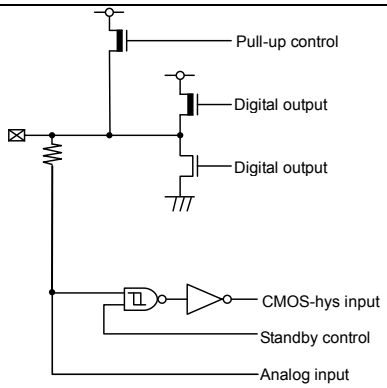
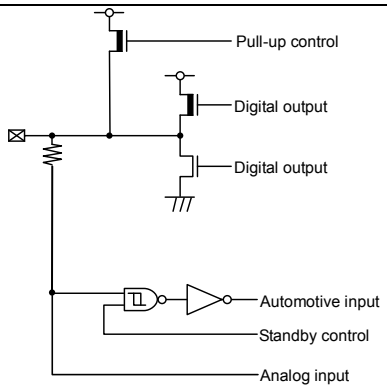
Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
36	44	52	M1	VCCE	-	-	Power supply (2)
128	156	184	M2				
144	176	208	AD2				
-	-	-	AD1				
-	-	-	A11				
-	-	-	B11				
-	-	-	B3				
-	-	-	A3				
1	1	1	A1	VSS	-	-	GND
37	45	53	B2				
44	54	62	P1				
73	89	105	P2				
108	132	135	AF1				
120	148	156	AE2				
125	153	176	AF8				
129	157	181	AF9				
-	-	185	AE9				
-	-	-	AD10				
-	-	-	AF26				
-	-	-	AE25				
-	-	-	M26				
-	-	-	M25				
-	-	-	A26				
-	-	-	B25				
-	-	-	A21				
-	-	-	A18				
-	-	-	B16				
-	-	-	A15				
-	-	-	A12				
-	-	-	B12				
-	-	-	A2,A25				
-	-	-	B1,B4				
-	-	-	B13,B17				
-	-	-	B19,B20				
-	-	-	B26				
-	-	-	C2,C3				
-	-	-	C7,C8				
-	-	-	C12,C13				
-	-	-	C14,C15				
-	-	-	C23,C24				
-	-	-	D4,D13				
-	-	-	D23,D24				
-	-	-	F3,F24				
-	-	-	G3,G24				

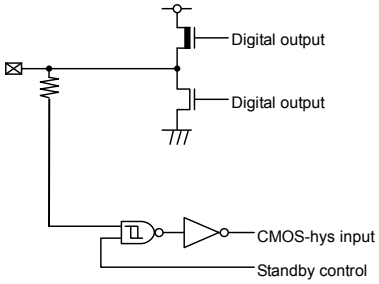
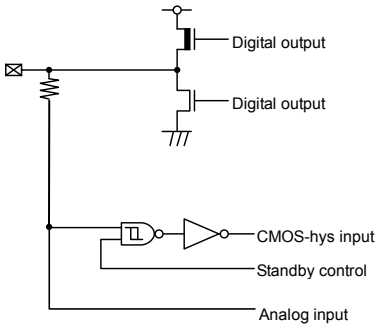
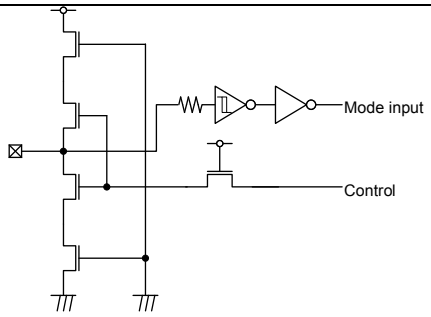
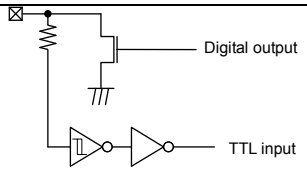
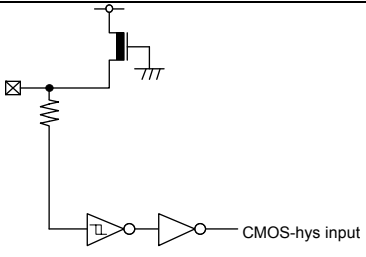
Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	H2,H3	VSS	-	-	GND
-	-	-	J24				
-	-	-	K10-K17				
-	-	-	K24				
-	-	-	L10-L17				
-	-	-	M10-M17				
-	-	-	M23,M24				
-	-	-	N1-N4				
-	-	-	N10-N17				
-	-	-	N24				
-	-	-	P3,P4				
-	-	-	P10-P17				
-	-	-	R10-R17				
-	-	-	R24				
-	-	-	T3				
-	-	-	T10-T17				
-	-	-	T24				
-	-	-	U3				
-	-	-	U10-U17				
-	-	-	V24				
-	-	-	W3,W24				
-	-	-	Y3				
-	-	-	AA24				
-	-	-	AC3,AC4				
-	-	-	AC9,AC23				
-	-	-	AD3,AD4				
-	-	-	AD7,AD9				
-	-	-	AD12,AD13				
-	-	-	AD15,AD16				
-	-	-	AD18,AD19				
-	-	-	AD21,AD22				
-	-	-	AD24				
-	-	-	AE1,AE26				
-	-	-	AF2,AF25				

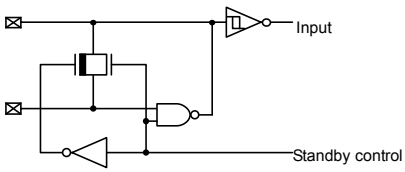
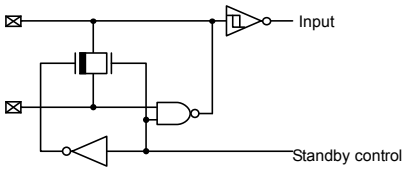
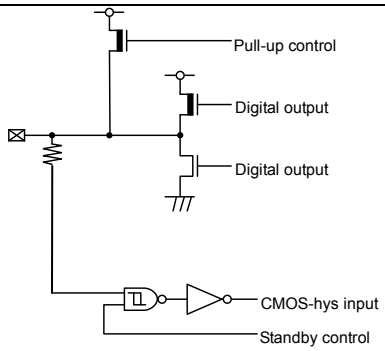
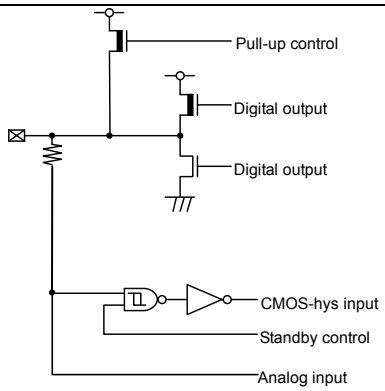
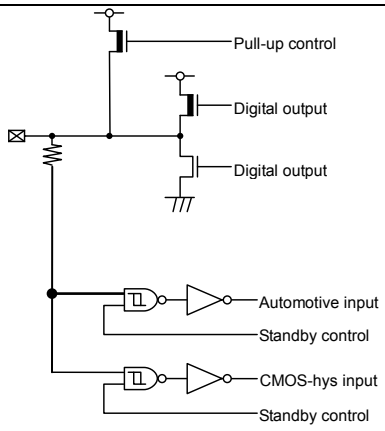
*1: For the I/O circuit types, see "4. I/O CIRCUIT TYPE".
*2: For switching, see "I/O Port" in HARDWARE MANUAL.

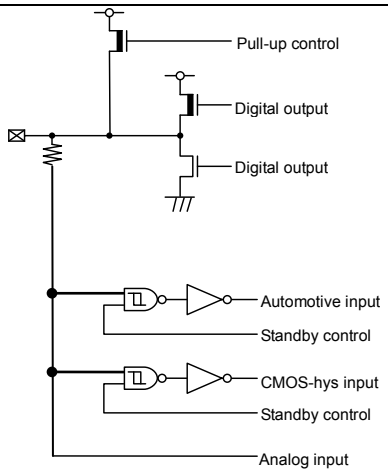
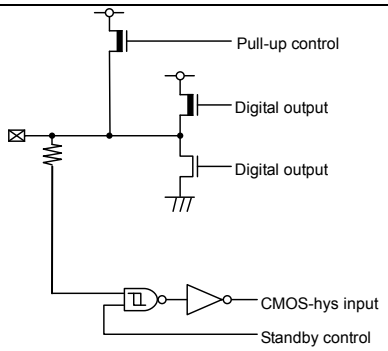
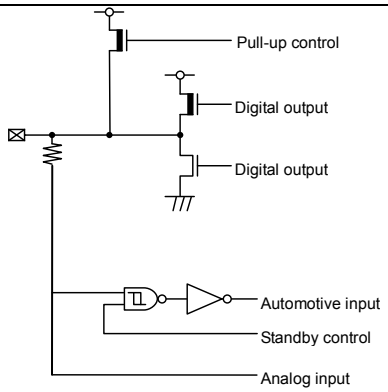
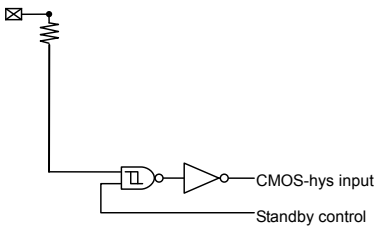
4. I/O Circuit Type

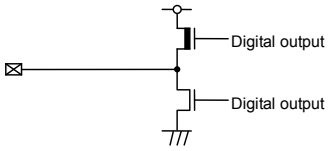
Type	Circuit	Remarks
A		- General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - Automotive input
B		- Analog input, General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - Automotive input
C		- DAC output, General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - Automotive input
D		- I²C Analog input, General-purpose I/O port - Output 3mA - Pull-up resistor control 50kΩ - I²C hysteresis input

Type	Circuit	Remarks
E		- I²C,General-purpose I/O port - Output 3mA - Pull-up resistor control 50kΩ - I²C hysteresis input
F		- General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - CMOS hysteresis input
G		- Analog input, General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - CMOS hysteresis input
H		- Analog input, General-purpose I/O port - Output 12mA - Pull-up resistor control 50kΩ - Automotive input

Type	Circuit	Remarks
I		- General-purpose I/O port (5V tolerant) - Output 4mA - CMOS hysteresis input
J		- Analog input, General-purpose I/O port (5V tolerant) - Output 4mA - CMOS hysteresis input
K		- Mode I/O - CMOS hysteresis input
L		- Open-drain I/O - Output 25mA (Nch open drain) - TTL input
M		- Hysteresis input - Pull-up resistor 50k

Type	Circuit	Remarks
N		- Main oscillation I/O
O		- Sub oscillation I/O
P		- General-purpose I/O port - Output 4mA - Output 3mA (Nch open drain) - Pull-up resistor control 50kΩ - CMOS hysteresis input
Q		- Analog input, General-purpose I/O port - Output 4mA - Output 3mA (Nch open drain) - Pull-up resistor control 50kΩ - CMOS hysteresis input
R		- General-purpose I/O port - Output 4mA - Output 4mA (FlexRay output) - Pull-up resistor control 50kΩ - Automotive input - CMOS hysteresis input

Type	Circuit	Remarks
S		- Analog input, General-purpose I/O port - Output 4mA - Output 4mA (FlexRay output) - Pull-up resistor control 50kΩ - Automotive input - CMOS hysteresis input
T		- General-purpose I/O port - Output 4mA - Output 4mA (FlexRay output) - Pull-up resistor control 50kΩ - CMOS hysteresis input
U		- Analog input, General-purpose I/O port - Output 4mA - Output 4mA (FlexRay output) - Pull-up resistor control 50kΩ - Automotive input
V		- CMOS hysteresis input

Type	Circuit	Remarks
W		- Output 4mA

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Code: DS00-00004-2Ea

Observance of Safety Regulations and Standards
Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design
Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices
Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type
Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging
CAUTION: When ball grid array (PAB) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices
Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.

When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame
CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

This section explains the latch-up prevention and pin processing.

■ **For latch-up prevention**

If a voltage higher than V_{CC} (V_{CCE} in case of terminal corresponding to V_{CCE} power supply.) or a voltage lower than V_{SS} is applied to an I/O pin, or if a voltage exceeding the ratings is applied between V_{CC} and V_{SS} pins or V_{CCE} and V_{SS} pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AV_{CC}, AVRH), analog input and digital power supply (V_{CCE}) must not be exceed the digital power supply (V_{CC}) when the power supply to the analog system and digital power supply (V_{CCE}) are turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (V_{CC}), analog power supplies (AV_{CC}, AVRH) and digital power supply (V_{CCE}) simultaneously. Or, turn on the digital power supply (V_{CC}), and then turn on analog power supplies (AV_{CC}, AVRH) and digital power supply (V_{CCE}).

■ **Treatment of unused pins**

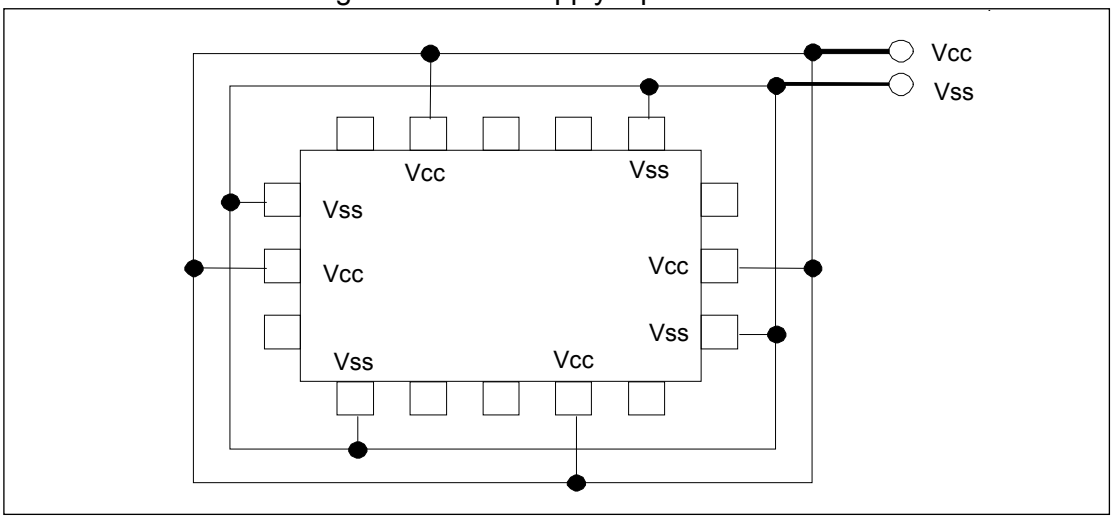
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2kΩ resistor to each of the unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

■ **Power supply pins**

The device is designed to ensure that if the device contains multiple V_{CC} or V_{SS} pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1 Power Supply Input Pins



The power supply pins should be connected to V_{CC} and V_{SS} pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between V_{CC} and V_{SS} pins.

Crystal oscillation circuit

An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

Mode pins (MD1, MD0)

Connect the MD1and MD0 mode pins to the V_{CC} or V_{SS} pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and V_{CC} or V_{SS} pin on the printed circuit board. Also, use the low-impedance pin connection.

During power-on

To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.

Notes during PLL clock operation

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

Treatment of A/D converter power supply pins

Connect the pins to have AV_{CC}=AVRH=V_{CC} and AV_{SS}/AVRL=V_{SS} even if the A/D converter is not used.

Notes on using external clock

An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

Power-on sequence of A/D converter analog inputs

Be sure to turn on the digital power supply (V_{CC}, V_{CCE}) first, and then turn on the A/D converter power supplies (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN63). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (V_{CC}, V_{CCE}). When the AVRH pin voltage is turned on or off, it must not exceed AV_{CC}. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

Treatment of C pin

This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

Note: Please see the latest data sheet for a detailed specification of the operation voltage.

Function switching of a multiplexed port

To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see " I/O PORTS" in the hardware manual.

Low-power consumption mode

To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in "Activating the sleep mode, watch mode, or stop mode" or "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL" in the hardware manual.

Take the following notes when using a monitor debugger.

Do not set a break point for the low-power consumption transition program.
Do not execute an operation step for the low-power consumption transition program.

Notes When Writing Data in a Register Having the Status Flag

When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

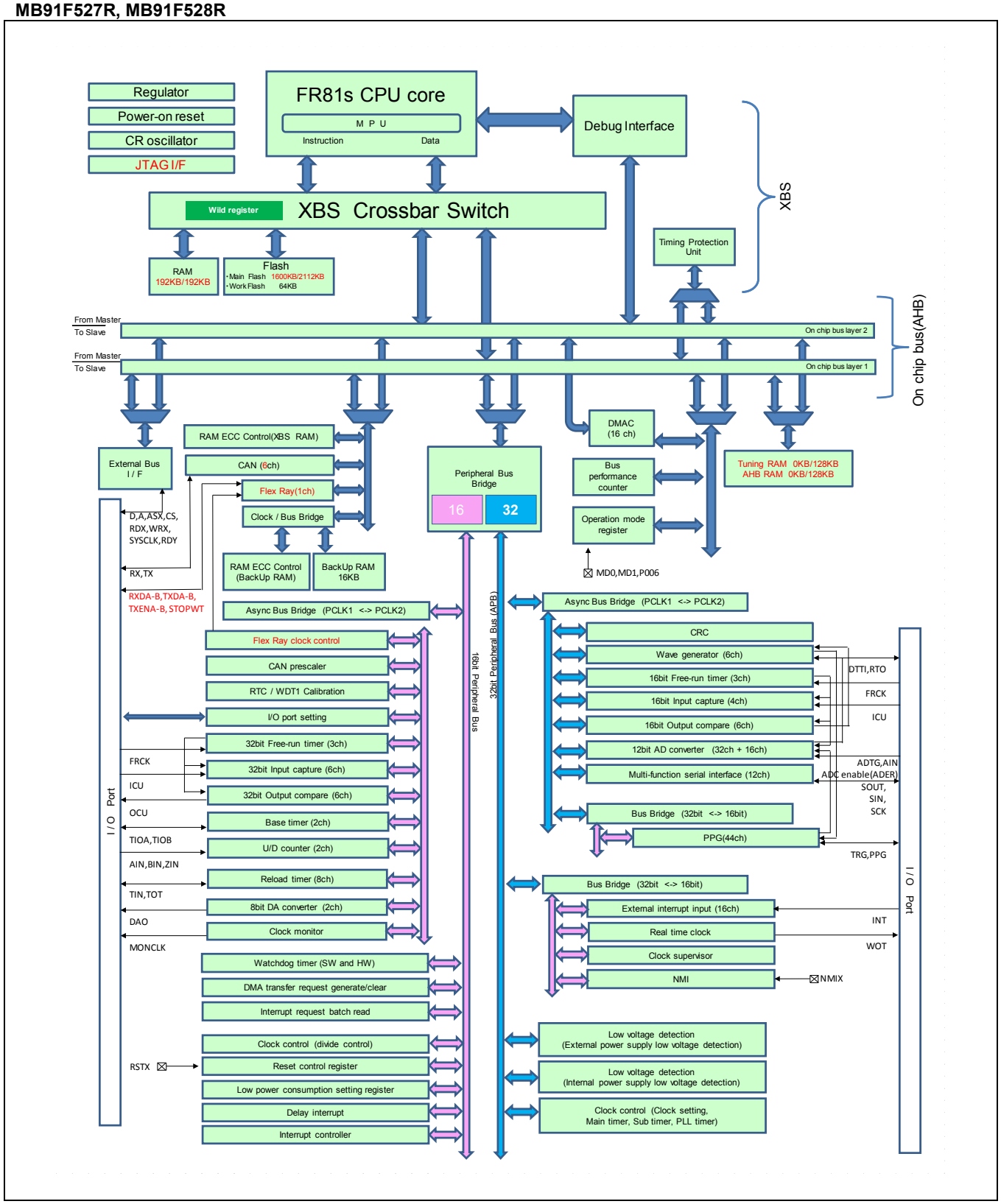
The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

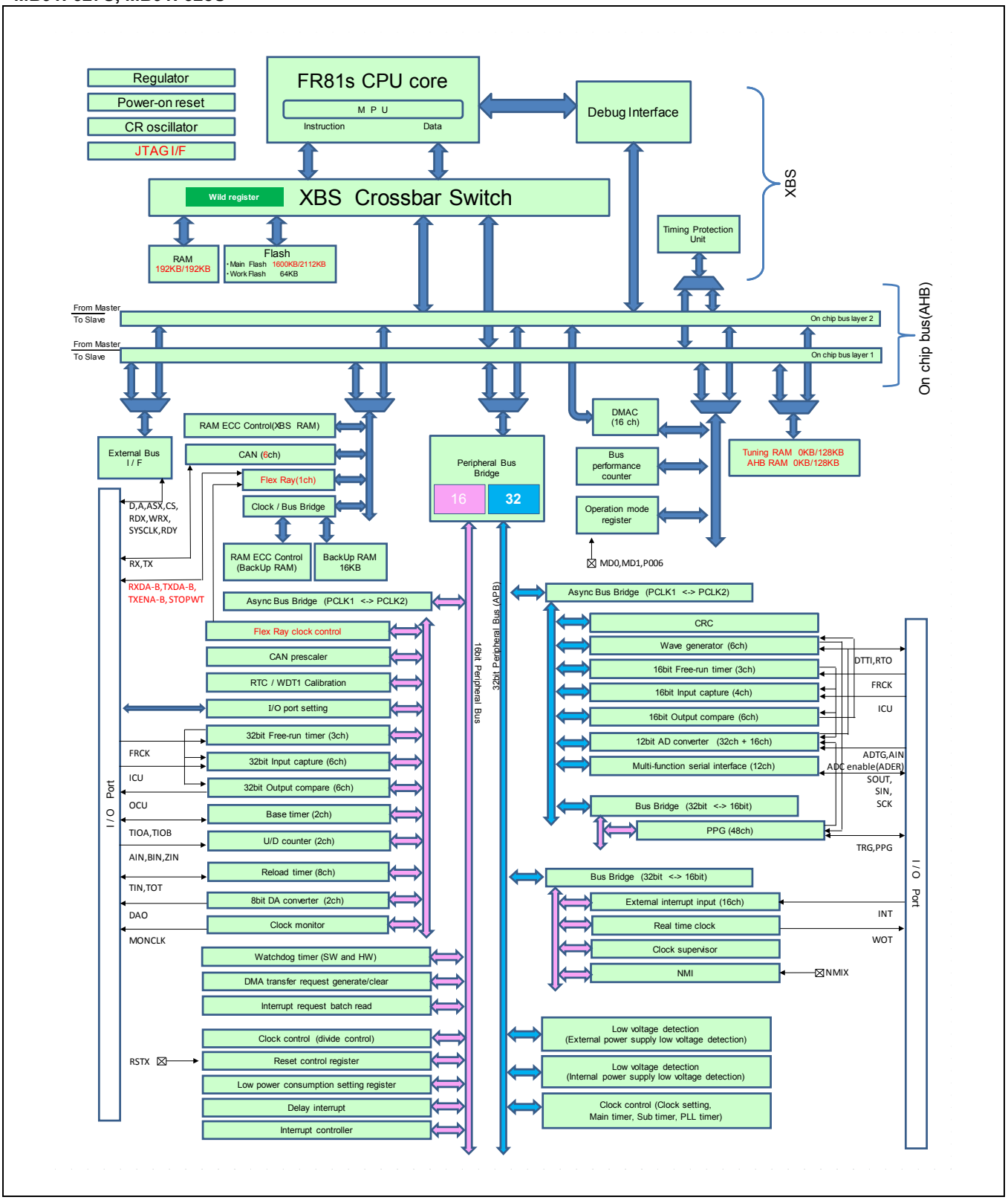
Note: These points can be ignored because the bit instructions are already taken the points into consideration.

7. Block Diagram

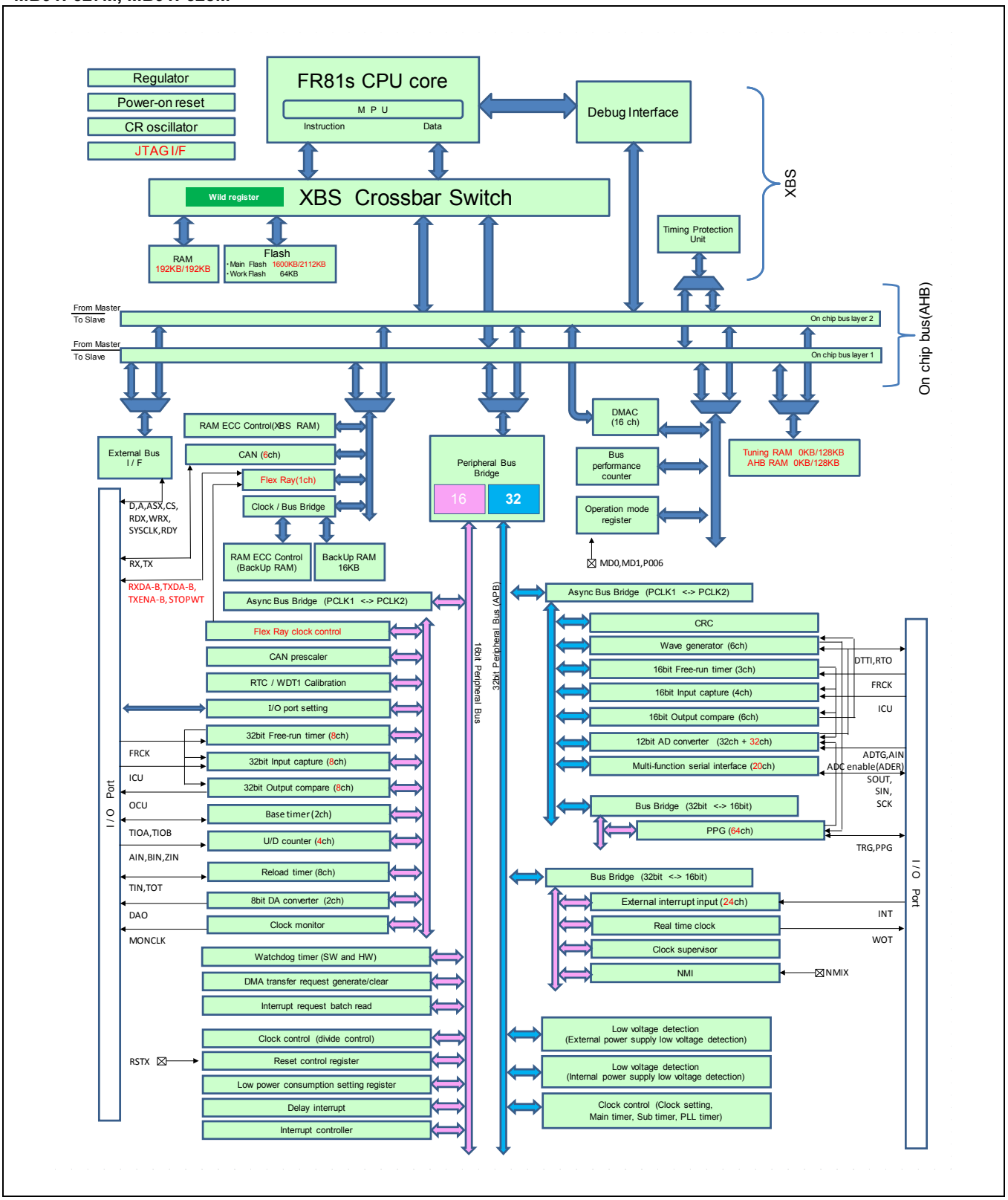
MB91F527R, MB91F528R



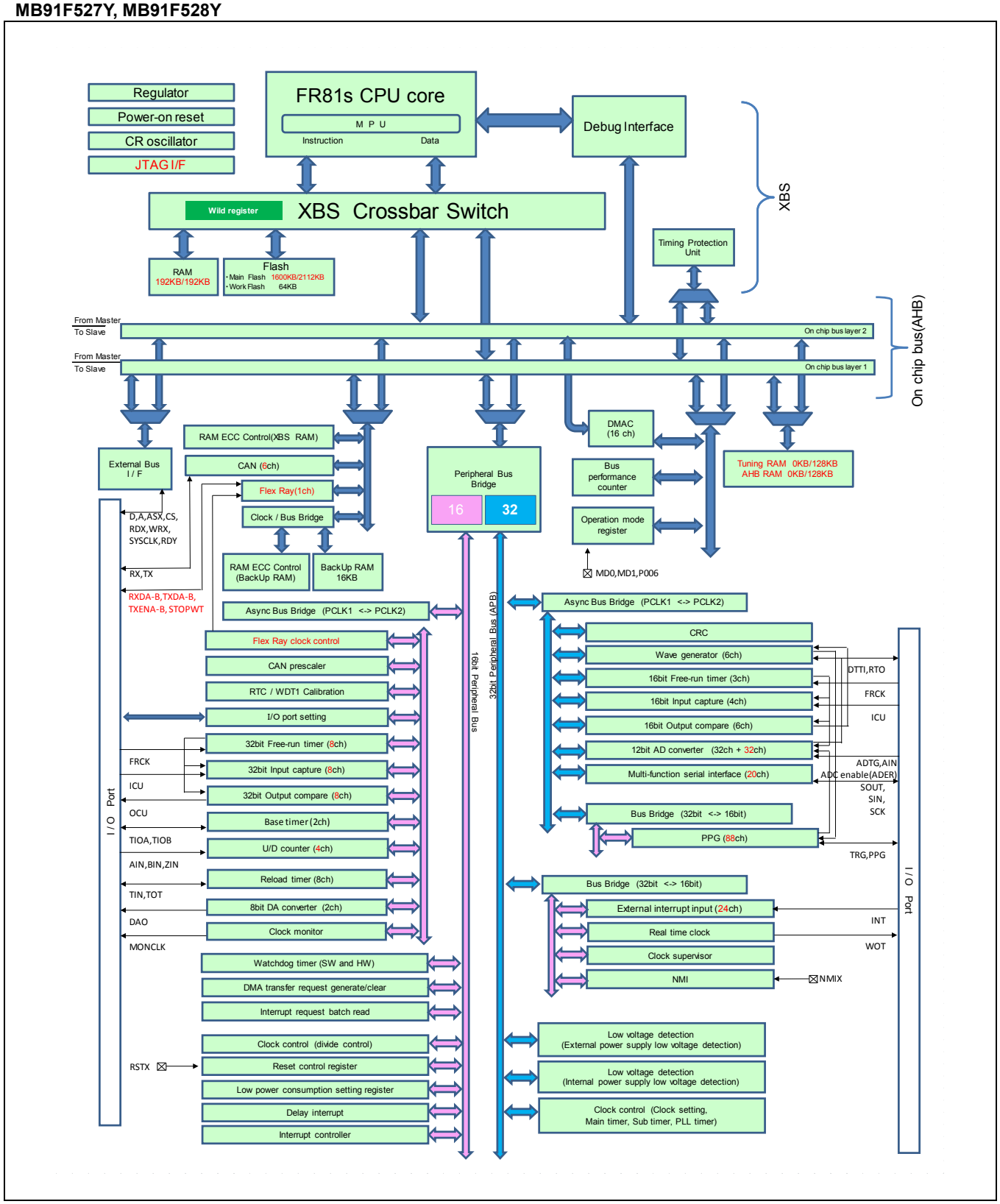
MB91F527U, MB91F528U



MB91F527M, MB91F528M

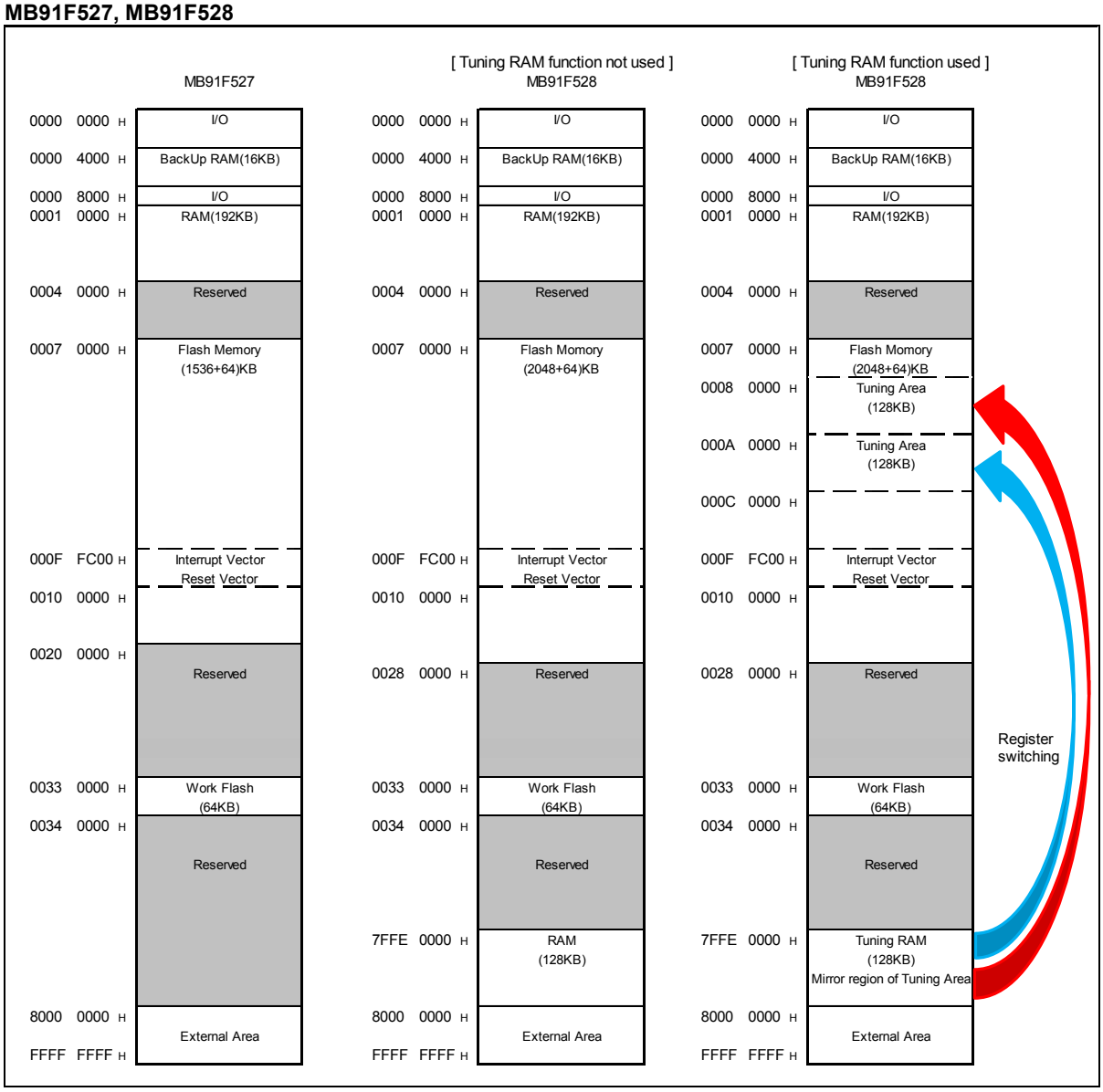


MB91F527Y, MB91F528Y



8. Memory Map

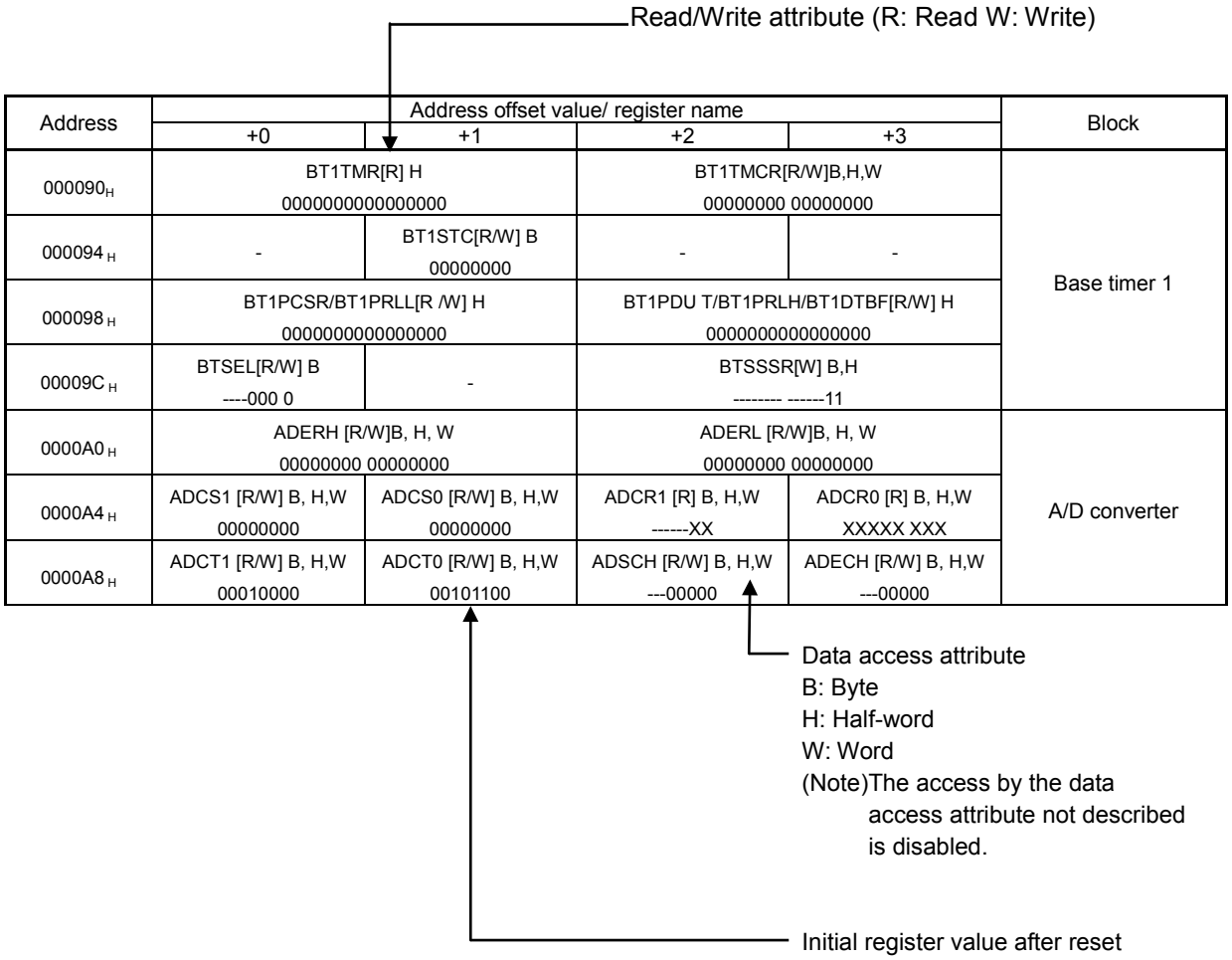
MB91F527, MB91F528



9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map



Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090H	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094H	-	BT1STC[R/W] B 00000000	-	-	
000098H	BT1PCSR/BT1PRLL[R /W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1DTBF[R/W] H 0000000000000000		
00009CH	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -------- ------11		
0000A0H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4H	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note: The access to addresses not described is disabled.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] B,H,W XXXXXXXX	PDR01 [R/W] B,H,W XXXXXXXX	PDR02 [R/W] B,H,W XXXXXXXX	PDR03 [R/W] B,H,W XXXXXXXX	Port Data Register
000004_H	PDR04 [R/W] B,H,W XXXXXXXX	PDR05 [R/W] B,H,W XXXXXXXX	PDR06 [R/W] B,H,W XXXXXXXX	PDR07 [R/W] B,H,W XXXXXXXX	
000008_H	PDR08 [R/W] B,H,W XXXXXXXX	PDR09 [R/W] B,H,W XXXXXXXX	PDR10 [R/W] B,H,W XXXXXXXX	PDR11 [R/W] B,H,W XXXXXXXX	
$00000C_H$	PDR12 [R/W] B,H,W XXXXXXXX	PDR13 [R/W] B,H,W -XXX--XX	PDR14 [R/W] B,H,W --------	PDR15 [R/W] B,H,W --XXXXXX	
000010_H	PDR20 [R/W] B,H,W XXXXXXXX	PDR21 [R/W] B,H,W XXXXXXXX	PDR22 [R/W] B,H,W XXX--XXX	PDR23 [R/W] B,H,W XXXXXXXX	
000014_H	PDR24 [R/W] B,H,W --XXXXXX	PDR25 [R/W] B,H,W -XXXXXXX	PDR26 [R/W] B,H,W XXXXXX--	PDR27 [R/W] B,H,W XXX-XXXX	
000018_H	PDR16 [R/W] B,H,W XXXXXXXX	PDR17 [R/W] B,H,W XXXXXXXX	PDR18 [R/W] B,H,W XXXXXXXX	PDR19 [R/W] B,H,W XXXXXXXX	
$00001C_H$	PDR28 [R/W] B,H,W XXXXXXXX	PDR29 [R/W] B,H,W XXXXXXXX	—	—	
000020_H	MSCY10 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 10,11 32-bit ICU
000024_H	MSCY11 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000028_H	—	—	MSCH1011 [R] B,H,W 00000000	MSCL1011 [R/W] B,H,W ------00	
$00002C_H$	IPCP10 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000030_H	IPCP11 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000034_H	—	—	—	ICS1011 [R/W] B,H,W 00000000	
000038_H	WDTECR0 [R/W] B,H,W ---00000	—	—	—	Watchdog Timer [S]
$00003C_H$	WDTCR0 [R/W] B,H,W -0--0000	WDTCPR0 [W] B,H,W 00000000	WDTCR1 [R] B,H,W ----0110	WDTCPR1 [W] B,H,W 00000000	
000040_H	—	—	—	—	Reserved
000044_H	DICR [R/W] B -------0	—	—	—	Delayed Interrupt
000048_H to $00005C_H$	—	—	—	—	Reserved
000060_H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload Timer 0
000064_H	TMRLRB0 [R/W] H XXXXXXXX XXXXXXXX		TMCSR0 [R/W] B,H,W 00000000 0-000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000068_H	TMRLRA7 [R/W] H XXXXXXXX XXXXXXXX		TMR7 [R] H XXXXXXXX XXXXXXXX		Reload Timer 7
$00006C_H$	TMRLRB7 [R/W] H XXXXXXXX XXXXXXXX		TMCSR7 [R/W] B,H,W 00000000 0-000000		
000070_H	FRS8 [R/W] B,H,W -000-000 -000-000 -000-000 -000-000				Free-run timer selection register 8
000074_H	FRS9 [R/W] B,H,W -000-000 -000-000 -000-000 -000-000				Free-run timer selection register 9
000078_H	—	—	—	OCLS67 [R/W] B,H,W ----0000	OCU67 Output level control register
$00007C_H$	—	—	—	OCLS89 [R/W] B,H,W ----0000	OCU89 Output level control register
000080_H	BT0TMR [R] H 00000000 00000000		BT0TMCR [R/W] H -000--00 -000-000		Base Timer 0
000084_H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	—	—	
000088_H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	—	—	—	—	Reserved
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -000--00 -000-000		Base Timer 1
000094_H	BT1TMCR2 [R/W] B -------0	BT1STC [R/W] B -0-0-0-0	—	—	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base Timer 0,1
$0000A0_H$ to $0000FC_H$	—	—	—	—	Reserved
000100_H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1
000104_H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108_H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2
$00010C_H$	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B,H,W 00000000 0-000000		
000110_H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3
000114_H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B,H,W 00000000 0-000000		
000118_H	MSCY4 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 Cycle measurement data register 45
$00011C_H$	MSCY5 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000120_H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 6,7 32-bit OCU
000124_H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
000128_H	—	—	OCSH67 [R/W] B,H,W ---0--00	OCSL67 [R/W] B,H,W 0000--00	
$00012C_H$	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 8,9 32-bit OCU
000130_H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000				
000134_H	—	—	OCSH89 [R/W] B,H,W ---0--00	OCSL89 [R/W] B,H,W 0000--00	
000138_H	OCCP12 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 12,13 32-bit OCU
$00013C_H$	OCCP13 [R/W] W 00000000 00000000 00000000 00000000				
000140_H	—	—	OCSH1213 [R/W] B,H,W ---0--00	OCSL1213 [R/W] B,H,W 0000--00	
000144_H to $0001B4_H$	—	—	—	—	Reserved
$0001B8_H$	EPFR64 [R/W] B,H,W -----00-	EPFR65 [R/W] B,H,W 0000-00-	EPFR66 [R/W] B,H,W --000000	EPFR67 [R/W] B,H,W ----0000	Extended port function register
$0001BC_H$	EPFR68 [R/W] B,H,W ----0000	EPFR69 [R/W] B,H,W ----0000	EPFR70 [R/W] B,H,W ---00000	EPFR71 [R/W] B,H,W -0-0-0-0	
$0001C0_H$	EPFR72 [R/W] B,H,W 000000-0	EPFR73 [R/W] B,H,W 00000000	EPFR74 [R/W] B,H,W 00000000	EPFR75 [R/W] B,H,W 00000000	
$0001C4_H$	EPFR76 [R/W] B,H,W 00000-0-	EPFR77 [R/W] B,H,W --000000	EPFR78 [R/W] B,H,W ------00	EPFR79 [R/W] B,H,W 00000000	
$0001C8_H$	EPFR80 [R/W] B,H,W ---00000	EPFR81 [R/W] B,H,W 00000000	EPFR82 [R/W] B,H,W 00000000	EPFR83 [R/W] B,H,W -0000000	
$0001CC_H$	EPFR84 [R/W] B,H,W 00000000	EPFR85 [R/W] B,H,W --000000	EPFR86 [R/W] B,H,W ---00000	EPFR87 [R/W] B,H,W --------	
$0001D0_H$	EPFR88 [R/W] B,H,W -------0	EPFR89 [R/W] B,H,W -0-00000	EPFR90 [R/W] B,H,W -0-0-0-0	EPFR91 [R/W] B,H,W -0-0-0-0	
$0001D4_H$	EPFR92 [R/W] B,H,W -0-0-0-0	EPFR93 [R/W] B,H,W 00000000	EPFR94 [R/W] B,H,W -0-0-0-0	EPFR95 [R/W] B,H,W -0-0-0-0	
$0001D8_H$	TMRLRA4 [R/W] H XXXXXXXX XXXXXXXX		TMR4 [R] H XXXXXXXX XXXXXXXX		Reload Timer 4

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0001DC$_H$	TMRLRB4 [R/W] H XXXXXXXX XXXXXXXX		TMCSR4 [R/W] B, H,W 00000000 0-000000		Reload Timer 4
0001E0$_H$	EPFR96 [R/W] B,H,W -0-0-0-0	EPFR97 [R/W] B,H,W -0-0-0-0	EPFR98 [R/W] B,H,W 0000-0-0	EPFR99 [R/W] B,H,W ----0000	Extended port function register
0001E4$_H$	EPFR100 [R/W] B,H,W -----00-	EPFR101 [R/W] B,H,W -----00-	EPFR102 [R/W] B,H,W -----00-	EPFR103 [R/W] B,H,W -----00-	
0001E8$_H$	EPFR104 [R/W] B,H,W -----00-	EPFR105 [R/W] B,H,W -----00-	EPFR106 [R/W] B,H,W -----00-	EPFR107 [R/W] B,H,W -----00-	
0001EC$_H$	EPFR108 [R/W] B,H,W ---00000	EPFR109 [R/W] B,H,W --000000	EPFR110 [R/W] B,H,W --000000	EPFR111 [R/W] B,H,W -------0	
0001F0$_H$	TMRLRA5 [R/W] H XXXXXXXX XXXXXXXX		TMR5 [R] H XXXXXXXX XXXXXXXX		Reload Timer 5
0001F4$_H$	TMRLRB5 [R/W] H XXXXXXXX XXXXXXXX		TMCSR5 [R/W] B, H,W 00000000 0-000000		
0001F8$_H$	TMRLRA6 [R/W] H XXXXXXXX XXXXXXXX		TMR6 [R] H XXXXXXXX XXXXXXXX		Reload Timer 6
0001FC$_H$	TMRLRB6 [R/W] H XXXXXXXX XXXXXXXX		TMCSR6 [R/W] B, H,W 00000000 0-000000		
000200$_H$ to 000238$_H$	—	—	—	—	Reserved
00023C$_H$	DACR0 [R/W] B,H,W -------0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W -------0	DADR1 [R/W] B,H,W XXXXXXXX	DA Converter
000240$_H$	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 3 32-bit FRT
000244$_H$	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000248$_H$	TCCSH3 [R/W] B,H,W 0-----00	TCCSL3 [R/W] B,H,W -1-00000	—	—	
00024C$_H$	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 4 32-bit FRT
000250$_H$	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000254$_H$	TCCSH4 [R/W] B,H,W 0-----00	TCCSL4 [R/W] B,H,W -1-00000	—	—	
000258$_H$ to 0002C0$_H$	—	—	—	—	Reserved
0002C4$_H$ to 0002FC$_H$	—	—	—	—	Reserved
000300$_H$ to 00030C$_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000310_H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only CPU core can access this area)
000314_H	—	—	—	—	
000318_H	—				
$00031C_H$	—	—	—		
000320_H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	—	—	DPVSR [R/W] H -------- 00000--0		
000328_H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	—	—	DESR [R/W] H -------- 00000--0		
000330_H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338_H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340_H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348_H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only CPU core can access this area)
$00034C_H$	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350_H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354_H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358_H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360_H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368_H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	—	—	PACR7 [R/W] H 000000-0 00000--0		
000370_H to $0003AC_H$	—				Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0003B0$_H$ to 0003FC$_H$	—	—	—	—	Reserved [S]
000400$_H$	ICSEL0 [R/W] B,H,W -----000	ICSEL1 [R/W] B,H,W ----0000	ICSEL2 [R/W] B,H,W -------0	ICSEL3 [R/W] B,H,W -------0	DMA request generation and clear
000404$_H$	ICSEL4 [R/W] B,H,W -------0	ICSEL5 [R/W] B,H,W -----000	ICSEL6 [R/W] B,H,W ----0000	ICSEL7 [R/W] B,H,W ----0000	
000408$_H$	ICSEL8 [R/W] B,H,W ------00	ICSEL9 [R/W] B,H,W ------00	ICSEL10 [R/W] B,H,W ------00	ICSEL11 [R/W] B,H,W -----000	
00040C$_H$	ICSEL12 [R/W] B,H,W -------0	ICSEL13 [R/W] B,H,W ------00	ICSEL14 [R/W] B,H,W ------00	ICSEL15 [R/W] B,H,W ------00	
000410$_H$	ICSEL16 [R/W] B,H,W ----0000	ICSEL17 [R/W] B,H,W ------00	ICSEL18 [R/W] B,H,W --000000	ICSEL19 [R/W] B,H,W -----000	
000414$_H$	ICSEL20 [R/W] B,H,W -----000	ICSEL21 [R/W] B,H,W ------00	ICSEL22 [R/W] B,H,W ------00	ICSEL23 [R/W] B,H,W ------00	
000418$_H$	IRPR0H [R] B,H,W 00------	IRPR0L [R] B,H,W 00------	IRPR1H [R] B,H,W 00------	IRPR1L [R] B,H,W 00------	Interrupt Request Batch Reading Register
00041C$_H$	—	—	IRPR3H [R] B,H,W 000000--	IRPR3L [R] B,H,W 000000--	
000420$_H$	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 0000----	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 0000000-	
000424$_H$	IRPR6H [R] B,H,W --00----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W -0-00---	IRPR7L [R] B,H,W ------00	
000428$_H$	IRPR8H [R] B,H,W --0-----	IRPR8L [R] B,H,W -00-----	IRPR9H [R] B,H,W -0------	IRPR9L [R] B,H,W -0------	
00042C$_H$	IRPR10H [R] B,H,W -0------	IRPR10L [R] B,H,W -0------	IRPR11H [R] B,H,W 0-------	IRPR11L [R] B,H,W 0-------	
000430$_H$	IRPR12H [R] B,H,W --0000--	IRPR12L [R] B,H,W ----00--	IRPR13H [R] B,H,W 00------	IRPR13L [R] B,H,W 00------	Interrupt Request Batch Reading Register
000434$_H$	IRPR14H [R] B,H,W 00000000	IRPR14L [R] B,H,W 00000000	IRPR15H [R] B,H,W 000-----	IRPR15L [R] B,H,W 00000000	
000438$_H$	ICSEL24 [R/W] B,H,W ------00	ICSEL25 [R/W] B,H,W ---00000	ICSEL26 [R/W] B,H,W -------0	ICSEL27 [R/W] B,H,W -------0	DMA request generation and clear
00043C$_H$	IRPR16H [R] B,H,W 000-----	IRPR16L [R] B,H,W 00000---	IRPR17H [R] B,H,W 000-----	IRPR17L [R] B,H,W 000-----	Interrupt Request Batch Reading Register

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444_H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448_H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
$00044C_H$	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450_H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454_H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458_H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
$00045C_H$	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460_H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464_H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468_H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
$00046C_H$	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	
000470_H to $00047C_H$	—	—	—	—	Reserved [S]
000480_H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484_H	—	—	—	—	Reserved [S]
000488_H	DIVR0 [R/W] B,H,W 000-----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
$00048C_H$	—	—	—	—	Reserved [S]
000490_H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral [S]
000494_H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498_H	IORR8 [R/W] B,H,W -0000000	IORR9 [R/W] B,H,W -0000000	IORR10 [R/W] B,H,W -0000000	IORR11 [R/W] B,H,W -0000000	
$00049C_H$	IORR12 [R/W] B,H,W -0000000	IORR13 [R/W] B,H,W -0000000	IORR14 [R/W] B,H,W -0000000	IORR15 [R/W] B,H,W -0000000	
$0004A0_H$	—	—	—	—	Reserved
$0004A4_H$	CANPRE [R/W] B,H,W ---00000	—	—	—	CAN prescaler
$0004A8_H$	—	—	CSCFG[R/W]B,H,W ---0----	CMCFG[R/W]B,H,W 00000000	Clock monitor control register

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0004AC$_H$	ADERH0[R/W] B,H 11111111 11111111		ADERL0[R/W] B,H 11111111 11111111		Analog input control register 0
0004B0$_H$	ADERH1[R/W] B,H 11111111 11111111		ADERL1[R/W] B,H 11111111 11111111		Analog input control register 1
0004B4$_H$	—	—	—	—	Reserved
0004B8$_H$	CUCR0 [R/W] B,H,W -------- ---0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration
0004BC$_H$	CUTR0 [R] B,H,W -------- 00000000 00000000 00000000				
0004C0$_H$	—	—	—	—	
0004C4$_H$	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1 [R/W] B,H,W 11000011 01010000		
0004C8$_H$	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
0004CC$_H$	—	—	—	—	Reserved
0004D0$_H$	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	Clock control for FlexRay
0004D4$_H$	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -------0	CLKR2[R/W] B,H,W 000--000	—	
0004D8$_H$	ICSEL28 [R/W] B,H,W -------0	ICSEL29 [R/W] B,H,W -------0	ICSEL30 [R/W] B,H,W -------0	ICSEL31 [R/W] B,H,W -------0	DMA request generation and clear
0004DC$_H$	ICSEL32 [R/W] B,H,W -------0	ICSEL33 [R/W] B,H,W -------0	—	—	
0004E0$_H$ to 00050C$_H$	—	—	—	—	Reserved
000510$_H$	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock Control [S]
000514$_H$	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518$_H$	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset Control [S]
00051C$_H$	—	—	—	—	Reserved [S]
000520$_H$	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock Control 2 [S]
000524$_H$	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528$_H$	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		
00052C$_H$	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000530_H	CCRTSELR [R/W] B,H,W 0------0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	Clock Control 2 [S]
000534_H to $00053C_H$	—	—	—	—	Reserved
000540_H	EIRR2 [R/W] B,H,W XXXXXXXX	ENIR2 [R/W] B,H,W 00000000	ELVR2 [R/W] B,H,W 00000000 00000000	External Interrupt (INT16 to 23)	
000544_H to $00054C_H$	—	—	—	—	Reserved
000550_H	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External Interrupt (INT0 to 7)
000554_H	EIRR1 [R/W] B,H,W XXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External Interrupt (INT8 to 15)
000558_H	—	—	—	—	Reserved
$00055C_H$	—	—	WTDR [R/W] H 00000000 00000000		Real Time Clock (RTC)
000560_H	—	WTCRH [R/W] B ------00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564_H	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX	
000568_H	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
$00056C_H$	—	CSVCR [R/W] B 000111--	—	—	Clock Supervisor
000570_H to $00057C_H$	—	—	—	—	Reserved
000580_H	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator Control / Low Voltage Detection
000584_H	LVD5R [R/W] B,H,W -------1	LVD5F [R/W] B,H,W 00000001	LVD [R/W] B,H,W 01000--0	—	
000588_H, $00058C_H$	—	—	—	—	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594_H	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	PMUINTF3 [R/W] B,H,W 00000000	PMU
000598_H	—	—	—	—	
$00059C_H$ to $0005FC_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000600_H	ASR0 [R/W] W 00000000 00000000 -------- 1111-001				External Bus Interface [S]
000604_H	ASR1 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608_H	ASR2 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
$00060C_H$	ASR3 [R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				External Bus Interface [S]
000610_H to $00063C_H$	—	—	—	—	Reserved [S]
000640_H	ACR0 [R/W] W -------- -------- -------- 01--00--				External Bus Interface [S]
000644_H	ACR1 [R/W] W -------- -------- -------- XX--XX--				
000648_H	ACR2 [R/W] W -------- -------- -------- XX--XX--				
$00064C_H$	ACR3 [R/W] W -------- -------- -------- XX--XX--				
000650_H to $00067C_H$	—	—	—	—	Reserved [S]
000680_H	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				External Bus Interface [S]
000684_H	AWR1 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688_H	AWR2 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
$00068C_H$	AWR3 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690_H to $0006FC_H$	—	—	—	—	Reserved [S]
000700_H to $00070C_H$	—	—	—	—	Reserved
000710_H	BPCCRA [R/W] B 00000000	BPCCRB [R/W] B 00000000	BPCCRC [R/W] B 00000000	—	Bus Performance Counter
000714_H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB [R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC [R/W] W 00000000 00000000 00000000 00000000				
000720_H to $0007F8_H$	—	—	—	—	Reserved
$0007FC_H$	BMODR [R] B, H, W XXXXXXXX	—	—	—	Mode Register

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000800_H to $00083C_H$	—	—	—	—	Reserved [S]
000840_H	FCTLR [R/W] H -0--1000 0--0----		—	FSTR [R/W] B -----001	Flash Memory Register [S]
000844_H to 000854_H	—	—	—	—	Reserved [S]
000858_H	—	—	WREN [R/W] H 00000000 00000000		Wild Register [S]
$00085C_H$ to $00087C_H$	—	—	—	—	Reserved [S]
000880_H	WRAR00 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
000884_H	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A0_H$	WRAR04 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008A4_H$	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0008C8_H$	WRAR09 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
$0008CC_H$	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D0_H$	WRAR10 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008D4_H$	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D8_H$	WRAR11 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008DC_H$	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E0_H$	WRAR12 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008E4_H$	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E8_H$	WRAR13 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008EC_H$	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008F4_H$	WRDR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F8_H$	WRAR15 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008FC_H$	WRDR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900_H	TPUUNLOCK [R/W] W 00000000 00000000 00000000 00000000				Time Protection Unit [S]
000904_H	TPULST [R] B,H,W -------0	—	TPUVST [R/W] B,H,W -----000	—	
000908_H	TPUCFG [R/W] B,H,W -------0 0-000000 -------- -------0				
$00090C_H$	TPUTIR [R] B,H,W 00000000	—	—	—	
000910_H	TPUTST [R] B,H,W 00000000	—	—	—	
000914_H	TPUTIE [R/W] B,H,W 00000000	—	—	—	
000918_H	TPUTMID [R] B,H,W 00000000 00000000 00000000 00000000				
$00091C_H$ to $00092C_H$	—	—	—	—	
000930_H	TPUTCN00 [R/W] B,H,W 000000-- 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000934_H	TPUTCN01 [R/W] B,H,W 000000-- 00000000 00000000 00000000				Time Protection Unit [S]
000938_H	TPUTCN02 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
$00093C_H$	TPUTCN03 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000940_H	TPUTCN04 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000944_H	TPUTCN05 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000948_H	TPUTCN06 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
$00094C_H$	TPUTCN07 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000950_H	TPUTCN10 [R/W] B,H,W ---00000	—	—	—	
000954_H	TPUTCN11 [R/W] B,H,W ---00000	—	—	—	
000958_H	TPUTCN12 [R/W] B,H,W ---00000	—	—	—	
$00095C_H$	TPUTCN13 [R/W] B,H,W ---00000	—	—	—	
000960_H	TPUTCN14 [R/W] B,H,W ---00000	—	—	—	
000964_H	TPUTCN15 [R/W] B,H,W ---00000	—	—	—	
000968_H	TPUTCN16 [R/W] B,H,W ---00000	—	—	—	
$00096C_H$	TPUTCN17 [R/W] B,H,W ---00000	—	—	—	
000970_H	TPUTCC0 [R] B,H,W -------- 00000000 00000000 00000000				
000974_H	TPUTCC1 [R] B,H,W -------- 00000000 00000000 00000000				
000978_H	TPUTCC2 [R] B,H,W -------- 00000000 00000000 00000000				
$00097C_H$	TPUTCC3 [R] B,H,W -------- 00000000 00000000 00000000				
000980_H	TPUTCC4 [R] B,H,W -------- 00000000 00000000 00000000				
000984_H	TPUTCC5 [R] B,H,W -------- 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000988_H	TPUTCC6 [R] B,H,W -------- 00000000 00000000 00000000				Time Protection Unit [S]
$00098C_H$	TPUTCC7 [R] B,H,W -------- 00000000 00000000 00000000				
000990_H to $0009FC_H$	—	—	—	—	
$000A00_H$ to $000BEC_H$	—	—	—	—	Reserved
$000BF0_H$	HSCFR [R/W] B,H,W -------- ------00 00000000 00000000				OCDU
$000BF4_H$	—	—	—	—	
$000BF8_H$	—	—	MBR [R/W] B,H,W 00------ XXXXXXXX		
$000BFC_H$	—	—	UER [W] B,H,W -------- -------X		
$000C00_H$	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000C04_H$	DCSR0 [R/W] H 0------- -----000		DTCR0 [R/W] H 00000000 00000000		
$000C08_H$	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C0C_H$	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C14_H$	DCSR1 [R/W] H 0------- -----000		DTCR1 [R/W] H 00000000 00000000		
$000C18_H$	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C1C_H$	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C20_H$	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C24_H$	DCSR2 [R/W] H 0------- -----000		DTCR2 [R/W] H 00000000 00000000		
$000C28_H$	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C2C_H$	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C30_H$	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3 [R/W] H 0------- -----000		DTCR3 [R/W] H 00000000 00000000		
$000C38_H$	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C40_H$	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000C44_H$	DCSR4 [R/W] H 0------- -----000		DTCR4 [R/W] H 00000000 00000000		DMA Controller [S]
$000C48_H$	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C4C_H$	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C50_H$	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C54_H$	DCSR5 [R/W] H 0------- -----000		DTCR5 [R/W] H 00000000 00000000		
$000C58_H$	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6 [R/W] H 0------- -----000		DTCR6 [R/W] H 00000000 00000000		
$000C68_H$	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7 [R/W] H 0------- -----000		DTCR7 [R/W] H 00000000 00000000		
$000C78_H$	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$	DCCR8 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C84_H$	DCSR8 [R/W] H 0------- -----000		DTCR8 [R/W] H 00000000 00000000		
$000C88_H$	DSAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C8C_H$	DDAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C90_H$	DCCR9 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C94_H$	DCSR9 [R/W] H 0------- -----000		DTCR9 [R/W] H 00000000 00000000		
$000C98_H$	DSAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C9C_H$	DDAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CA0_H$	DCCR10 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CA4_H$	DCSR10 [R/W] H 0------- -----000		DTCR10 [R/W] H 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000CA8_H$	DSAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA Controller [S]
$000CAC_H$	DDAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CB0_H$	DCCR11 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CB4_H$	DCSR11 [R/W] H 0------- -----000		DTCR11 [R/W] H 00000000 00000000		
$000CB8_H$	DSAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CBC_H$	DDAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CC0_H$	DCCR12 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CC4_H$	DCSR12 [R/W] H 0------- -----000		DTCR12 [R/W] H 00000000 00000000		
$000CC8_H$	DSAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CCC_H$	DDAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CD0_H$	DCCR13 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CD4_H$	DCSR13 [R/W] H 0------- -----000		DTCR13 [R/W] H 00000000 00000000		
$000CD8_H$	DSAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CDC_H$	DDAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CE0_H$	DCCR14 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CE4_H$	DCSR14 [R/W] H 0------- -----000		DTCR14 [R/W] H 00000000 00000000		
$000CE8_H$	DSAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CEC_H$	DDAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CF0_H$	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				
$000CF4_H$	DCSR15 [R/W] H 0------- -----000		DTCR15 [R/W] H 00000000 00000000		
$000CF8_H$	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CFC_H$	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000D00_H$ to $000DF0_H$	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000DF4$_H$	—	—	DNMIR [R/W] B 0------0	DILVR [R/W] B ---11111	DMA Controller [S]
000DF8$_H$	DMACR[R/W] W 0------- -------- 0------- --------				
000DFC$_H$	—	—	—	—	Reserved [S]
000E00$_H$	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
000E04$_H$	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	
000E08$_H$	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	
000E0C$_H$	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -000--00	DDR14 [R/W] B,H,W --------	DDR15 [R/W] B,H,W --000000	
000E10$_H$	DDR20 [R/W] B,H,W 00000000	DDR21 [R/W] B,H,W 00000000	DDR22 [R/W] B,H,W 000--000	DDR23 [R/W] B,H,W 00000000	
000E14$_H$	DDR24 [R/W] B,H,W --000000	DDR25 [R/W] B,H,W -0000000	DDR26 [R/W] B,H,W 000000--	DDR27 [R/W] B,H,W 000-0000	
000E18$_H$	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
000E1C$_H$	DDR28 [R/W] B,H,W 00000000	DDR29 [R/W] B,H,W 00000000	—	—	
000E20$_H$	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
000E24$_H$	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
000E28$_H$	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
000E2C$_H$	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -000--00	PFR14 [R/W] B,H,W --------	PFR15 [R/W] B,H,W --000000	
000E30$_H$	PFR20 [R/W] B,H,W 00000000	PFR21 [R/W] B,H,W 00000000	PFR22 [R/W] B,H,W 000--000	PFR23 [R/W] B,H,W 00000000	
000E34$_H$	PFR24 [R/W] B,H,W --000000	PFR25 [R/W] B,H,W -0000000	PFR26 [R/W] B,H,W 000000--	PFR27 [R/W] B,H,W 000-0000	
000E38$_H$	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	
000E3C$_H$	PFR28 [R/W] B,H,W 00000000	PFR29 [R/W] B,H,W 00000000	—	—	
000E40$_H$	PDDR00 [R] B,H,W XXXXXXXX	PDDR01 [R] B,H,W XXXXXXXX	PDDR02 [R] B,H,W XXXXXXXX	PDDR03 [R] B,H,W XXXXXXXX	Port Direct Read Register
000E44$_H$	PDDR04 [R] B,H,W XXXXXXXX	PDDR05 [R] B,H,W XXXXXXXX	PDDR06 [R] B,H,W XXXXXXXX	PDDR07 [R] B,H,W XXXXXXXX	
000E48$_H$	PDDR08 [R] B,H,W XXXXXXXX	PDDR09 [R] B,H,W XXXXXXXX	PDDR10 [R] B,H,W XXXXXXXX	PDDR11 [R] B,H,W XXXXXXXX	
000E4C$_H$	PDDR12 [R] B,H,W XXXXXXXX	PDDR13 [R] B,H,W -XXX--XX	PDDR14 [R] B,H,W --------	PDDR15 [R] B,H,W --XXXXXX	
000E50$_H$	PDDR20 [R] B,H,W XXXXXXXX	PDDR21 [R] B,H,W XXXXXXXX	PDDR22 [R] B,H,W XXX--XXX	PDDR23 [R] B,H,W XXXXXXXX	
000E54$_H$	PDDR24 [R] B,H,W --XXXXXX	PDDR25 [R] B,H,W -XXXXXXX	PDDR26 [R] B,H,W XXXXXX--	PDDR27 [R] B,H,W XXX-XXXX	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000E58_H$	PDDR16 [R] B,H,W XXXXXXXX	PDDR17 [R] B,H,W XXXXXXXX	PDDR18 [R] B,H,W XXXXXXXX	PDDR19 [R] B,H,W XXXXXXXX	Port Direct Read Register
$000E5C_H$	PDDR28 [R] B,H,W XXXXXXXX	PDDR29 [R] B,H,W XXXXXXXX	—	—	
$000E60_H$	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ----0000	EPFR03 [R/W] B,H,W ---000-0	Extended Port Function Register
$000E64_H$	EPFR04 [R/W] B,H,W ----00-0	EPFR05 [R/W] B,H,W ----0000	EPFR06 [R/W] B,H,W ----000-	EPFR07 [R/W] B,H,W ---00000	
$000E68_H$	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W -----00-	EPFR10 [R/W] B,H,W ----0000	EPFR11 [R/W] B,H,W ----0000	
$000E6C_H$	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W ------00	EPFR14 [R/W] B,H,W ------00	EPFR15 [R/W] B,H,W -----000	
$000E70_H$	—	—	—	—	
$000E74_H$	—	—	—	—	
$000E78_H$	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W ---0----	
$000E7C_H$	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
$000E80_H$	—	EPFR33 [R/W] B,H,W -----00-	EPFR34 [R/W] B,H,W -----00-	EPFR35 [R/W] B,H,W ---00000	
$000E84_H$	EPFR36 [R/W] B,H,W ----0-0-	—	—	—	
$000E88_H$	—	—	EPFR42 [R/W] B,H,W ------00	EPFR43 [R/W] B,H,W 0--0000-	
$000E8C_H$	EPFR44 [R/W] B,H,W -00---0-	EPFR45 [R/W] B,H,W -0000000	—	—	
$000E90_H$	EPFR48 [R/W] B,H,W -----0-0	EPFR49 [R/W] B,H,W -----000	EPFR50 [R/W] B,H,W ------00	EPFR51 [R/W] B,H,W ---00000	
$000E94_H$	—	—	—	—	
$000E98_H$	EPFR56 [R/W] B,H,W -----0-0	EPFR57 [R/W] B,H,W -----0-0	EPFR58 [R/W] B,H,W ----00-0	EPFR59 [R/W] B,H,W ----00-0	
$000E9C_H$	EPFR60 [R/W] B,H,W ----00--	EPFR61 [R/W] B,H,W -----00-	EPFR62 [R/W] B,H,W -----00-	EPFR63 [R/W] B,H,W ---0-0--	
$000EA0_H$ to $000EB0_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000EB4$_H$	CPCLR9 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 9 32-bit FRT
000EB8$_H$	TCDT9 [R/W] W 00000000 00000000 00000000 00000000				
000EBC$_H$	TCCSH9 [R/W] B,H,W 0-----00	TCCSL9 [R/W] B,H,W -1-00000	—	—	Free-run Timer 9 32-bit FRT
000EC0$_H$	PPER00 [R/W] B,H,W 00000000	PPER01 [R/W] B,H,W 00000000	PPER02 [R/W] B,H,W 00000000	PPER03 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
000EC4$_H$	PPER04 [R/W] B,H,W 00000000	PPER05 [R/W] B,H,W 00000000	PPER06 [R/W] B,H,W 00000000	PPER07 [R/W] B,H,W 00000000	
000EC8$_H$	PPER08 [R/W] B,H,W 00000000	PPER09 [R/W] B,H,W 00000000	PPER10 [R/W] B,H,W 00000000	PPER11 [R/W] B,H,W 00000000	
000ECC$_H$	PPER12 [R/W] B,H,W 00000000	PPER13 [R/W] B,H,W -000--00	PPER14 [R/W] B,H,W --------	PPER15 [R/W] B,H,W --000000	
000ED0$_H$	PPER20 [R/W] B,H,W 00000000	PPER21 [R/W] B,H,W 00000000	PPER22 [R/W] B,H,W 000--000	PPER23 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
000ED4$_H$	PPER24 [R/W] B,H,W --000000	PPER25 [R/W] B,H,W -0000000	PPER26 [R/W] B,H,W 000000--	PPER27 [R/W] B,H,W 000-0000	
000ED8$_H$	PPER16 [R/W] B,H,W 00000000	PPER17 [R/W] B,H,W 00000000	PPER18 [R/W] B,H,W 00000000	PPER19 [R/W] B,H,W 00000000	
000EDC$_H$	PPER28 [R/W] B,H,W 00000000	PPER29 [R/W] B,H,W 00000000	—	—	
000EE0$_H$	PILR00[R/W] B,H,W 11-1--1-	PILR01[R/W] B,H,W 11111111	—	—	Port Input Level Register
000EE4$_H$	—	PILR05[R/W] B,H,W -----1--	—	—	
000EE8$_H$	—	—	—	PILR11[R/W] B,H,W ---1----	
000EEC$_H$	PILR12[R/W] B,H,W ----1--1	—	—	PILR15[R/W] B,H,W --1-----	
000EF0$_H$	CPCLR10 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 10 32-bit FRT
000EF4$_H$	TCDT10 [R/W] W 00000000 00000000 00000000 00000000				
000EF8$_H$	TCCSH10 [R/W] B,H,W 0-----00	TCCSL10 [R/W] B,H,W -1-00000	—	—	
000EFC$_H$ to 000F0C$_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000F10_H$	RCRH2 [R/W] H,W XXXXXXXX	RCRL2 [R/W] B,H,W XXXXXXXX	UDCRH2 [R/W] H,W 00000000	UDCRL2 [R/W] B,H,W 00000000	UpDown Counter 2
$000F14_H$	CCR2 [R/W] B,H 00000000 -0001000		—	CSR2 [R/W] B 00000000	
$000F18_H$	RCRH3 [R/W] H,W XXXXXXXX	RCRL3 [R/W] B,H,W XXXXXXXX	UDCRH3 [R/W] H,W 00000000	UDCRL3 [R/W] B,H,W 00000000	UpDown Counter 3
$000F1C_H$	CCR3 [R/W] B,H 00000000 -0001000		—	CSR3 [R/W] B 00000000	
$000F20_H$ to $000F30_H$	—	—	—	—	Reserved
$000F34_H$, $000F38_H$	—	—	—	—	Reserved
$000F3C_H$	—	—	—	OCLS1213 [R/W] B,H,W ----0000	OCU12,13 Output level control register
$000F40_H$	PORTEN [R/W] B,H,W -------0	—	—	—	Port Enable Register
$000F44_H$	KEYCDR [R/W] H 00000000 00000000		—	—	KeyCodeRegister
$000F48_H$ to $000F64_H$	—	—	—	—	Reserved
$000F68_H$	MSCY6 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 Cycle measurement data register 67
$000F6C_H$	MSCY7 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000F70_H$	RCRH0 [W] H,W XXXXXXXX	RCRL0 [W] B,H,W XXXXXXXX	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	UpDown Counter 0
$000F74_H$	CCR0 [R/W] B,H 00000000 -0001000		—	CSR0 [R/W] B 00000000	
$000F78_H$, $000F7C_H$	—	—	—	—	Reserved
$000F80_H$	RCRH1 [W] H,W XXXXXXXX	RCRL1 [W] B,H,W XXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	UpDown Counter 1
$000F84_H$	CCR1 [R/W] B,H 00000000 -0001000		—	CSR1 [R/W] B 00000000	
$000F88_H$	—	—	MSCH45 [R] B,H,W 00000000	MSCL45 [R/W] B,H,W ------00	Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45
$000F8C_H$	—	—	MSCH67 [R] B,H,W 00000000	MSCL67 [R/W] B,H,W ------00	Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67
$000F90_H$	OCCP10 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000F94H	OCCP11 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU
000F98H	—	—	OCSH1011 [R/W] B,H,W ---0--00	OCSL1011 [R/W] B,H,W 0000--00	
000F9CH	—	—	—	OCLS1011 [R/W] B,H,W ----0000	OCU10,11 Output level control register
000FA0H	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 5 32-bit FRT
000FA4H	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
000FA8H	TCCSH5 [R/W]B,H,W 0-----00	TCCSL5 [R/W]B,H,W -1-00000	—	—	
000FACH	CPCLR6 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 6 32-bit FRT
000FB0H	TCDT6 [R/W] W 00000000 00000000 00000000 00000000				
000FB4H	TCCSH6 [R/W]B,H,W 0-----00	TCCSL6 [R/W]B,H,W -1-00000	—	—	
000FB8H	CPCLR7 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 7 32-bit FRT
000FBCH	TCDT7 [R/W] W 00000000 00000000 00000000 00000000				
000FC0H	TCCSH7 [R/W]B,H,W 0-----00	TCCSL7 [R/W]B,H,W -1-00000	—	—	
000FC4H	CPCLR8 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 8 32-bit FRT
000FC8H	TCDT8 [R/W] W 00000000 00000000 00000000 00000000				
000FCCH	TCCSH8 [R/W]B,H,W 0-----00	TCCSL8 [R/W]B,H,W -1-00000	—	—	
000FD0H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 32-bit ICU
000FD4H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FD8H	—	LSYNS2 [R/W] B,H,W --000000	LSYNS1 [R/W] B,H,W 00000000	ICS45 [R/W] B,H,W 00000000	
000FDCH	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 32-bit ICU
000FE0H	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FE4H	—	—	—	ICS67 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000FE8_H$	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU
$000FEC_H$	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FF0_H$	—	—	—	ICS89 [R/W] B,H,W 00000000	
$000FF4_H$	MSCY8 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU
$000FF8_H$	MSCY9 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000FFC_H$	—	—	MSCH89 [R] B,H,W 00000000	MSCL89 [R/W] B,H,W ------00	
001000_H	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Clock Control
001004_H to $00112C_H$	—	—	—	—	Reserved
001130_H	—	—	—	CRCCR [R/W] B,H,W -0000000	CRC calculation unit
001134_H	CRCINIT [R/W] B,H,W 11111111 11111111 11111111 11111111				
001138_H	CRCIN [R/W] B,H,W 00000000 00000000 00000000 00000000				
$00113C_H$	CRCR [R] B,H,W 11111111 11111111 11111111 11111111				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001140_H	SCR16/(IBCR16) [R/W] B,H,W 0--00000	SMR16 [R/W] B,H,W 000-00-0	SSR16 [R/W] B,H,W 0-000011	ESCR16/(IBSR16) [R/W] B,H,W 00000000	Multi-UART16 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001144_H	— /(RDR116/(TDR116))[R/W] B,H,W -------- --------*3		RDR016/(TDR016)[R/W] B,H,W -------0 00000000*1		
001148_H	SACSR16[R/W] B,H,W 0----000 00000000		STMR16[R] B,H,W 00000000 00000000		
$00114C_H$	STMCR16[R/W] B,H,W 00000000 00000000		— /(SCSCR16/SFUR16)[R/W] B,H,W -------- --------*3 *4		
001150_H	— /(SCSTR316)/(LAMSR16) [R/W] B,H,W --------*3	— /(SCSTR216)/(LAMCR16) [R/W] B,H,W --------*3	— /(SCSTR116)/(SFLR116) [R/W] B,H,W --------*3	— /(SCSTR016)/(SFLR016) [R/W] B,H,W --------*3	
001154_H	—	— /(SCSFR216) [R/W] B,H,W --------*3	— /(SCSFR116) [R/W] B,H,W --------*3	— /(SCSFR016) [R/W] B,H,W --------*3	
001158_H	—/(TBYTE316)/(LAMESR16) [R/W] B,H,W --------*3	—/(TBYTE216)/(LAMERT16) [R/W] B,H,W --------*3	—/(TBYTE116)/(LAMIER16) [R/W] B,H,W --------*3	TBYTE016/(LAMRID16)/(LAMTID16) [R/W] B,H,W 00000000	
$00115C_H$	BGR16[R/W] H,W 00000000 00000000		— /(ISMK16) [R/W] B,H,W --------*2	— /(ISBA16) [R/W] B,H,W --------*2	
001160_H	FCR116 [R/W] B,H,W ---00100	FCR016 [R/W] B,H,W -0000000	FBYTE16[R/W] B,H,W 00000000 00000000		
001164_H	FTICR16[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001168_H	SCR17/(IBCR17) [R/W] B,H,W 0--00000	SMR17 [R/W] B,H,W 000-00-0	SSR17 [R/W] B,H,W 0-000011	ESCR17/(IBSR17) [R/W] B,H,W 00000000	Multi-UART17 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00116C_H$	— /(RDR117/(TDR117))[R/W] B,H,W -------- --------*3		RDR017/(TDR017)[R/W] B,H,W -------0 00000000*1		
001170_H	SACSR17[R/W] B,H,W 0----000 00000000		STMR17[R] B,H,W 00000000 00000000		
001174_H	STMCR17[R/W] B,H,W 00000000 00000000		— /(SCSCR17/SFUR17)[R/W] B,H,W -------- --------*3 *4		
001178_H	— /(SCSTR317)/ (LAMSR17) [R/W] B,H,W --------*3	— /(SCSTR217)/ (LAMCR17) [R/W] B,H,W --------*3	— /(SCSTR117)/(SFLR117) [R/W] B,H,W --------*3	— /(SCSTR017)/(SFLR017) [R/W] B,H,W --------*3	
$00117C_H$	—	— /(SCSFR217) [R/W] B,H,W --------*3	— /(SCSFR117) [R/W] B,H,W --------*3	— /(SCSFR017) [R/W] B,H,W --------*3	
001180_H	—/(TBYTE317)/ (LAMESR17) [R/W] B,H,W --------*3	—/(TBYTE217)/ (LAMERT17) [R/W] B,H,W --------*3	—/(TBYTE117)/ (LAMIER17) [R/W] B,H,W --------*3	TBYTE017/(LAMRID17)/(LAMTID17) [R/W] B,H,W 00000000	
001184_H	BGR17[R/W] H,W 00000000 00000000		— /(ISMK17) [R/W] B,H,W --------*2	— /(ISBA17) [R/W] B,H,W --------*2	
001188_H	FCR117 [R/W] B,H,W ---00100	FCR017 [R/W] B,H,W -0000000	FBYTE17[R/W] B,H,W 00000000 00000000		
$00118C_H$	FTICR17[R/W] B,H,W 00000000 00000000		—	—	
001190_H	SCR18/(IBCR18) [R/W] B,H,W 0--00000	SMR18 [R/W] B,H,W 000-00-0	SSR18 [R/W] B,H,W 0-000011	ESCR18/(IBSR18) [R/W] B,H,W 00000000	Multi-UART18 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001194_H	— /(RDR118/(TDR118))[R/W] B,H,W -------- --------*3		RDR018/(TDR018)[R/W] B,H,W -------0 00000000*1		
001198_H	SACSR18[R/W] B,H,W 0----000 00000000		STMR18[R] B,H,W 00000000 00000000		
$00119C_H$	STMCR18[R/W] B,H,W 00000000 00000000		— /(SCSCR18/SFUR18)[R/W] B,H,W -------- --------*3 *4		
$0011A0_H$	— /(SCSTR318)/ (LAMSR18) [R/W] B,H,W --------*3	— /(SCSTR218)/ (LAMCR18) [R/W] B,H,W --------*3	— /(SCSTR118)/(SFLR118) [R/W] B,H,W --------*3	— /(SCSTR018)/(SFLR018) [R/W] B,H,W --------*3	
$0011A4_H$	—	— /(SCSFR218) [R/W] B,H,W --------*3	— /(SCSFR118) [R/W] B,H,W --------*3	— /(SCSFR018) [R/W] B,H,W --------*3	
$0011A8_H$	—/(TBYTE318)/ (LAMESR18) [R/W] B,H,W --------*3	—/(TBYTE218)/ (LAMERT18) [R/W] B,H,W --------*3	—/(TBYTE118)/ (LAMIER18) [R/W] B,H,W --------*3	TBYTE018/(LAMRID18)/(LAMTID18) [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0011AC$_H$	BGR18[R/W] H,W 00000000 00000000		— /(ISMK18) [R/W] B,H,W --------*2	— /(ISBA18) [R/W] B,H,W --------*2	Multi-UART18
0011B0$_H$	FCR118 [R/W] B,H,W ---00100	FCR018 [R/W] B,H,W -0000000	FBYTE18[R/W] B,H,W 00000000 00000000		
0011B4$_H$	FTICR18[R/W] B,H,W 00000000 00000000		—	—	
0011B8$_H$	SCR19/(IBCR19) [R/W] B,H,W 0--00000	SMR19 [R/W] B,H,W 000-00-0	SSR19 [R/W] B,H,W 0-000011	ESCR19/(IBSR19) [R/W] B,H,W 00000000	Multi-UART19 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0011BC$_H$	— /(RDR119/(TDR119))[R/W] B,H,W -------- --------*3		RDR019/(TDR019)[R/W] B,H,W -------0 00000000*1		
0011C0$_H$	SACSR19[R/W] B,H,W 0----000 00000000		STMR19[R] B,H,W 00000000 00000000		
0011C4$_H$	STMCR19[R/W] B,H,W 00000000 00000000		— /(SCSCR19/SFUR19)[R/W] B,H,W -------- --------*3 *4		
0011C8$_H$	— /(SCSTR319)/ (LAMSR19) [R/W] B,H,W --------*3	— /(SCSTR219)/ (LAMCR19) [R/W] B,H,W --------*3	— /(SCSTR119)/(SFLR119) [R/W] B,H,W --------*3	— /(SCSTR019)/(SFLR019) [R/W] B,H,W --------*3	
0011CC$_H$	—	— /(SCSFR219) [R/W] B,H,W --------*3	— /(SCSFR119) [R/W] B,H,W --------*3	— /(SCSFR019) [R/W] B,H,W --------*3	
0011D0$_H$	—/(TBYTE319)/ (LAMESR19) [R/W] B,H,W --------*3	—/(TBYTE219)/ (LAMERT19) [R/W] B,H,W --------*3	—/(TBYTE119)/ (LAMIER19) [R/W] B,H,W --------*3	TBYTE019/(LAMRID19)/(LAMTID19) [R/W] B,H,W 00000000	
0011D4$_H$	BGR19[R/W] H,W 00000000 00000000		— /(ISMK19) [R/W] B,H,W --------*2	— /(ISBA19) [R/W] B,H,W --------*2	
0011D8$_H$	FCR119 [R/W] B,H,W ---00100	FCR019 [R/W] B,H,W -0000000	FBYTE19[R/W] B,H,W 00000000 00000000		
0011DC$_H$	FTICR19[R/W] B,H,W 00000000 00000000		—	—	
0011E0$_H$ to 0011FC$_H$	—	—	—	—	Reserved
001200$_H$	TCGS [R/W] B,H,W ------00	—	—	TCGSE [R/W] B,H,W -----000	16-bit Free-run timer synchronous activation
001204$_H$	CPCLRB0/CPCLR0 [W] H,W 11111111 11111111		TCDT0 [R/W] H,W 00000000 00000000		16-bit Free-run timer 0
001208$_H$	TCCS0 [R/W] B,H,W 00000000 01000000 ----0000 --------				
00120C$_H$	CPCLRB1/CPCLR1 [W] H,W 11111111 11111111		TCDT1 [R/W] H,W 00000000 00000000		16-bit Free-run timer 1
001210$_H$	TCCS1 [R/W] B,H,W 00000000 01000000 ----0000 --------				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001214_H	CPCLRB2/CPCLR2 [W] H,W 11111111 11111111		TCDT2 [R/W] H,W 00000000 00000000		16-bit Free-run timer 2
001218_H	TCCS2 [R/W] B,H,W 00000000 01000000 ----0000 --------				
$00121C_H$ to 001230_H	—	—	—	—	Reserved
001234_H	FRS0 [R/W] B,H,W -------- --00--00 --00--00 --00--00				16-bit Free-run timer selection
001238_H	—		FRS1 [R/W] B,H,W --00--00 --00--00		
$00123C_H$	FRS2 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001240_H	FRS3 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001244_H	FRS4 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001248_H	—	—	—	—	Reserved
$00124C_H$	OCCPB0/OCCP0 [R/W] H,W 00000000 00000000		OCCPB1/OCCP1 [R/W] H,W 00000000 00000000		16-bit Output compare 0/1
001250_H	OCS01 [R/W] B,H,W -110--00 00001100		—	OCMOD01 [R/W] B,H,W ------00	
001254_H	OCCPB2/OCCP2 [R/W] H,W 00000000 00000000		OCCPB3/OCCP3 [R/W] H,W 00000000 00000000		16-bit Output compare 2/3
001258_H	OCS23 [R/W] B,H,W -110--00 00001100		—	OCMOD23 [R/W] B,H,W ------00	
$00125C_H$	OCCPB4/OCCP4 [R/W] H,W 00000000 00000000		OCCPB5/OCCP5 [R/W] H,W 00000000 00000000		16-bit Output compare 4/5
001260_H	OCS45 [R/W] B,H,W -110--00 00001100		—	OCMOD45 [R/W] B,H,W ------00	
001264_H to 001278_H	—	—	—	—	Reserved
$00127C_H$	IPCP0 [R] H,W 00000000 00000000		IPCP1 [R] H,W 00000000 00000000		16-bit Input capture 0/1
001280_H	ICS01 [R/W] B,H,W ------00 00000000		—	LSYNS [R/W] B,H,W ----0000	
001284_H	IPCP2 [R] H,W 00000000 00000000		IPCP3 [R] H,W 00000000 00000000		16-bit Input capture 2/3
001288_H	ICS23 [R/W] B,H,W ------00 00000000		—	—	
$00128C_H$ to 001298_H	—	—	—	—	Reserved
$00129C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0012A0_H$	TMRR0 [R/W] H,W 00000000 00000001		TMRR1 [R/W] H,W 00000000 00000001		Waveform generator 0/1/2
$0012A4_H$	TMRR2 [R/W] H,W 00000000 00000001		—	—	
$0012A8_H$	DTSCR0 [R/W] B,H,W 00000000	DTSCR1 [R/W] B,H,W 00000000	DTSCR2 [R/W] B,H,W 00000000	—	
$0012AC_H$	—	DTIR0 [R/W] B,H,W 000000--	—	DTMNS0 [R/W] B,H,W 00---000	
$0012B0_H$	—	SIGCR10 [R/W] B,H,W 00000000	—	SIGCR20 [R/W] B,H,W 000000-1	
$0012B4_H$	PICS0 [R/W] B,H,W 000000-- -------- -------- --------				
$0012B8_H$ to $0012CC_H$	—	—	—	—	Reserved
$0012D0_H$	FRS5 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare
$0012D4_H$	FRS6 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
$0012D8_H$	FRS7 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
$0012DC_H$	FRS10 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
$0012E0_H$	FRS11 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
$0012E4_H$ to $0012FC_H$	—	—	—	—	Reserved
001300_H	—				Reserved
001304_H	ADTSS0[R/W] B,H,W -------0	—	—	—	12-bit A/D converter 1/2 unit
001308_H	ADTSE0[R/W] B,H,W 00000000 00000000 00000000 00000000				
$00130C_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		
001310_H	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
001314_H	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
001318_H	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
$00131C_H$	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
001320_H	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001324_H	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		12-bit A/D converter 1/2 unit
001328_H	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000		
$00132C_H$	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001330_H	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
001334_H	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001338_H	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
$00133C_H$	ADCOMP24/ADCOMPB24[R/W] H,W 00000000 00000000		ADCOMP25/ADCOMPB25[R/W] H,W 00000000 00000000		
001340_H	ADCOMP26/ADCOMPB26[R/W] H,W 00000000 00000000		ADCOMP27/ADCOMPB27[R/W] H,W 00000000 00000000		
001344_H	ADCOMP28/ADCOMPB28[R/W] H,W 00000000 00000000		ADCOMP29/ADCOMPB29[R/W] H,W 00000000 00000000		
001348_H	ADCOMP30/ADCOMPB30[R/W] H,W 00000000 00000000		ADCOMP31/ADCOMPB31[R/W] H,W 00000000 00000000		
$00134C_H$	ADTCS0[R/W] B,H,W 00000000 0010----		ADTCS1[R/W] B,H,W 00000000 0010----		
001350_H	ADTCS2[R/W] B,H,W 00000000 0010----		ADTCS3[R/W] B,H,W 00000000 0010----		
001354_H	ADTCS4[R/W] B,H,W 00000000 0010----		ADTCS5[R/W] B,H,W 00000000 0010----		
001358_H	ADTCS6[R/W] B,H,W 00000000 0010----		ADTCS7[R/W] B,H,W 00000000 0010----		
$00135C_H$	ADTCS8[R/W] B,H,W 00000000 0010----		ADTCS9[R/W] B,H,W 00000000 0010----		
001360_H	ADTCS10[R/W] B,H,W 00000000 0010----		ADTCS11[R/W] B,H,W 00000000 0010----		
001364_H	ADTCS12[R/W] B,H,W 00000000 0010----		ADTCS13[R/W] B,H,W 00000000 0010----		
001368_H	ADTCS14[R/W] B,H,W 00000000 0010----		ADTCS15[R/W] B,H,W 00000000 0010----		
$00136C_H$	ADTCS16[R/W] B,H,W 00000000 0010----		ADTCS17[R/W] B,H,W 00000000 0010----		
001370_H	ADTCS18[R/W] B,H,W 00000000 0010----		ADTCS19[R/W] B,H,W 00000000 0010----		
001374_H	ADTCS20[R/W] B,H,W 00000000 0010----		ADTCS21[R/W] B,H,W 00000000 0010----		
001378_H	ADTCS22[R/W] B,H,W 00000000 0010----		ADTCS23[R/W] B,H,W 00000000 0010----		
$00137C_H$	ADTCS24[R/W] B,H,W 00000000 0010----		ADTCS25[R/W] B,H,W 00000000 0010----		
001380_H	ADTCS26[R/W] B,H,W 00000000 0010----		ADTCS27[R/W] B,H,W 00000000 0010----		
001384_H	ADTCS28[R/W] B,H,W 00000000 0010----		ADTCS29[R/W] B,H,W 00000000 0010----		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001388_H	ADTCS30[R/W] B,H,W 00000000 0010----		ADTCS31[R/W] B,H,W 00000000 0010----		12-bit A/D converter 1/2 unit
$00138C_H$	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001390_H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
001394_H	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001398_H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
$00139C_H$	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
$0013A0_H$	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
$0013A4_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
$0013A8_H$	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
$0013AC_H$	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
$0013B0_H$	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
$0013B4_H$	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
$0013B8_H$	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
$0013BC_H$	ADTCD24[R] B,H,W 10--0000 00000000		ADTCD25[R] B,H,W 10--0000 00000000		
$0013C0_H$	ADTCD26[R] B,H,W 10--0000 00000000		ADTCD27[R] B,H,W 10--0000 00000000		
$0013C4_H$	ADTCD28[R] B,H,W 10--0000 00000000		ADTCD29[R] B,H,W 10--0000 00000000		
$0013C8_H$	ADTCD30[R] B,H,W 10--0000 00000000		ADTCD31[R] B,H,W 10--0000 00000000		
$0013CC_H$	ADTECS0[R/W] B,H,W -------0 ---00000		ADTECS1[R/W] B,H,W -------0 ---00000		
$0013D0_H$	ADTECS2[R/W] B,H,W -------0 ---00000		ADTECS3[R/W] B,H,W -------0 ---00000		
$0013D4_H$	ADTECS4[R/W] B,H,W -------0 ---00000		ADTECS5[R/W] B,H,W -------0 ---00000		
$0013D8_H$	ADTECS6[R/W] B,H,W -------0 ---00000		ADTECS7[R/W] B,H,W -------0 ---00000		
$0013DC_H$	ADTECS8[R/W] B,H,W -------0 ---00000		ADTECS9[R/W] B,H,W -------0 ---00000		
$0013E0_H$	ADTECS10[R/W] B,H,W -------0 ---00000		ADTECS11[R/W] B,H,W -------0 ---00000		
$0013E4_H$	ADTECS12[R/W] B,H,W -------0 ---00000		ADTECS13[R/W] B,H,W -------0 ---00000		
$0013E8_H$	ADTECS14[R/W] B,H,W -------0 ---00000		ADTECS15[R/W] B,H,W -------0 ---00000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0013EC_H$	ADTECS16[R/W] B,H,W -------0 ---00000		ADTECS17[R/W] B,H,W -------0 ---00000		12-bit A/D converter 1/2 unit
$0013F0_H$	ADTECS18[R/W] B,H,W -------0 ---00000		ADTECS19[R/W] B,H,W -------0 ---00000		
$0013F4_H$	ADTECS20[R/W] B,H,W -------0 ---00000		ADTECS21[R/W] B,H,W -------0 ---00000		
$0013F8_H$	ADTECS22[R/W] B,H,W -------0 ---00000		ADTECS23[R/W] B,H,W -------0 ---00000		
$0013FC_H$	ADTECS24[R/W] B,H,W -------0 ---00000		ADTECS25[R/W] B,H,W -------0 ---00000		
001400_H	ADTECS26[R/W] B,H,W -------0 ---00000		ADTECS27[R/W] B,H,W -------0 ---00000		
001404_H	ADTECS28[R/W] B,H,W -------0 ---00000		ADTECS29[R/W] B,H,W -------0 ---00000		
001408_H	ADTECS30[R/W] B,H,W -------0 ---00000		ADTECS31[R/W] B,H,W -------0 ---00000		
$00140C_H$	ADRCUT0[R/W] B,H,W ----0000 00000000		ADRCLT0[R/W] B,H,W ----0000 00000000		
001410_H	ADRCUT1[R/W] B,H,W ----0000 00000000		ADRCLT1[R/W] B,H,W ----0000 00000000		
001414_H	ADRCUT2[R/W] B,H,W ----0000 00000000		ADRCLT2[R/W] B,H,W ----0000 00000000		
001418_H	ADRCUT3[R/W] B,H,W ----0000 00000000		ADRCLT3[R/W] B,H,W ----0000 00000000		
$00141C_H$	ADRCCS0[R/W] B,H,W 00000000	ADRCCS1[R/W] B,H,W 00000000	ADRCCS2[R/W] B,H,W 00000000	ADRCCS3[R/W] B,H,W 00000000	
001420_H	ADRCCS4[R/W] B,H,W 00000000	ADRCCS5[R/W] B,H,W 00000000	ADRCCS6[R/W] B,H,W 00000000	ADRCCS7[R/W] B,H,W 00000000	
001424_H	ADRCCS8[R/W] B,H,W 00000000	ADRCCS9[R/W] B,H,W 00000000	ADRCCS10[R/W] B,H,W 00000000	ADRCCS11[R/W] B,H,W 00000000	
001428_H	ADRCCS12[R/W] B,H,W 00000000	ADRCCS13[R/W] B,H,W 00000000	ADRCCS14[R/W] B,H,W 00000000	ADRCCS15[R/W] B,H,W 00000000	
$00142C_H$	ADRCCS16[R/W] B,H,W 00000000	ADRCCS17[R/W] B,H,W 00000000	ADRCCS18[R/W] B,H,W 00000000	ADRCCS19[R/W] B,H,W 00000000	
001430_H	ADRCCS20[R/W] B,H,W 00000000	ADRCCS21[R/W] B,H,W 00000000	ADRCCS22[R/W] B,H,W 00000000	ADRCCS23[R/W] B,H,W 00000000	
001434_H	ADRCCS24[R/W] B,H,W 00000000	ADRCCS25[R/W] B,H,W 00000000	ADRCCS26[R/W] B,H,W 00000000	ADRCCS27[R/W] B,H,W 00000000	
001438_H	ADRCCS28[R/W] B,H,W 00000000	ADRCCS29[R/W] B,H,W 00000000	ADRCCS30[R/W] B,H,W 00000000	ADRCCS31[R/W] B,H,W 00000000	
$00143C_H$	ADRCOT0[R] B,H,W 00000000 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001440_H	ADRCIF0[R,W] B,H,W 00000000 00000000 00000000 00000000				12-bit A/D converter 1/2 unit
001444_H	ADSCANS0[R/W] B,H,W 000-----	—	—	—	
001448_H	ADNCS0[R/W] B,H,W 0-000-00	ADNCS1[R/W] B,H,W 0-000-00	ADNCS2[R/W] B,H,W 0-000-00	ADNCS3[R/W] B,H,W 0-000-00	
$00144C_H$	ADNCS4[R/W] B,H,W 0-000-00	ADNCS5[R/W] B,H,W 0-000-00	ADNCS6[R/W] B,H,W 0-000-00	ADNCS7[R/W] B,H,W 0-000-00	
001450_H	ADNCS8[R/W] B,H,W 0-000-00	ADNCS9[R/W] B,H,W 0-000-00	ADNCS10[R/W] B,H,W 0-000-00	ADNCS11[R/W] B,H,W 0-000-00	
001454_H	ADNCS12[R/W] B,H,W 0-000-00	ADNCS13[R/W] B,H,W 0-000-00	ADNCS14[R/W] B,H,W 0-000-00	ADNCS15[R/W] B,H,W 0-000-00	
001458_H	ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000				
$00145C_H$	ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111				
001460_H	ADCS0[R] B,H,W 0------- --------		ADCH0[R] B,H,W ---00000	ADMD0[R/W] B,H,W 0---0000	
001464_H	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	ADSTPCS2[R/W] B,H,W 00000000	ADSTPCS3[R/W] B,H,W 00000000	
001468_H	ADSTPCS4[R/W] B,H,W 00000000	ADSTPCS5[R/W] B,H,W 00000000	ADSTPCS6[R/W] B,H,W 00000000	ADSTPCS7[R/W] B,H,W 00000000	
$00146C_H$	—				
001470_H	ADTSS1[R/W] B,H,W -------0	—	—	—	12-bit A/D converter 2/2 unit
001474_H	ADTSE1[R/W] B,H,W 00000000 00000000 00000000 00000000				
001478_H	ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000		ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000		
$00147C_H$	ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000		ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000		
001480_H	ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000		ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000		
001484_H	ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000		ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000		
001488_H	ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000		ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000		
$00148C_H$	ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000		ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000		
001490_H	ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000		ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001494_H	ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000		ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000		12-bit A/D converter 2/2 unit
001498_H	ADCOMP48/ADCOMPB48[R/W] H,W 00000000 00000000		ADCOMP49/ADCOMPB49[R/W] H,W 00000000 00000000		
$00149C_H$	ADCOMP50/ADCOMPB50[R/W] H,W 00000000 00000000		ADCOMP51/ADCOMPB51[R/W] H,W 00000000 00000000		
$0014A0_H$	ADCOMP52/ADCOMPB52[R/W] H,W 00000000 00000000		ADCOMP53/ADCOMPB53[R/W] H,W 00000000 00000000		
$0014A4_H$	ADCOMP54/ADCOMPB54[R/W] H,W 00000000 00000000		ADCOMP55/ADCOMPB55[R/W] H,W 00000000 00000000		
$0014A8_H$	ADCOMP56/ADCOMPB56[R/W] H,W 00000000 00000000		ADCOMP57/ADCOMPB57[R/W] H,W 00000000 00000000		
$0014AC_H$	ADCOMP58/ADCOMPB58[R/W] H,W 00000000 00000000		ADCOMP59/ADCOMPB59[R/W] H,W 00000000 00000000		
$0014B0_H$	ADCOMP60/ADCOMPB60[R/W] H,W 00000000 00000000		ADCOMP61/ADCOMPB61[R/W] H,W 00000000 00000000		
$0014B4_H$	ADCOMP62/ADCOMPB62[R/W] H,W 00000000 00000000		ADCOMP63/ADCOMPB63[R/W] H,W 00000000 00000000		
$0014B8_H$	ADTCS32[R/W] B,H,W 00000000 0010----		ADTCS33[R/W] B,H,W 00000000 0010----		
$0014BC_H$	ADTCS34[R/W] B,H,W 00000000 0010----		ADTCS35[R/W] B,H,W 00000000 0010----		
$0014C0_H$	ADTCS36[R/W] B,H,W 00000000 0010----		ADTCS37[R/W] B,H,W 00000000 0010----		
$0014C4_H$	ADTCS38[R/W] B,H,W 00000000 0010----		ADTCS39[R/W] B,H,W 00000000 0010----		
$0014C8_H$	ADTCS40[R/W] B,H,W 00000000 0010----		ADTCS41[R/W] B,H,W 00000000 0010----		
$0014CC_H$	ADTCS42[R/W] B,H,W 00000000 0010----		ADTCS43[R/W] B,H,W 00000000 0010----		
$0014D0_H$	ADTCS44[R/W] B,H,W 00000000 0010----		ADTCS45[R/W] B,H,W 00000000 0010----		
$0014D4_H$	ADTCS46[R/W] B,H,W 00000000 0010----		ADTCS47[R/W] B,H,W 00000000 0010----		
$0014D8_H$	ADTCS48[R/W] B,H,W 00000000 0010----		ADTCS49[R/W] B,H,W 00000000 0010----		
$0014DC_H$	ADTCS50[R/W] B,H,W 00000000 0010----		ADTCS51[R/W] B,H,W 00000000 0010----		
$0014E0_H$	ADTCS52[R/W] B,H,W 00000000 0010----		ADTCS53[R/W] B,H,W 00000000 0010----		
$0014E4_H$	ADTCS54[R/W] B,H,W 00000000 0010----		ADTCS55[R/W] B,H,W 00000000 0010----		
$0014E8_H$	ADTCS56[R/W] B,H,W 00000000 0010----		ADTCS57[R/W] B,H,W 00000000 0010----		
$0014EC_H$	ADTCS58[R/W] B,H,W 00000000 0010----		ADTCS59[R/W] B,H,W 00000000 0010----		
$0014F0_H$	ADTCS60[R/W] B,H,W 00000000 0010----		ADTCS61[R/W] B,H,W 00000000 0010----		
$0014F4_H$	ADTCS62[R/W] B,H,W 00000000 0010----		ADTCS63[R/W] B,H,W 00000000 0010----		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0014F8_H$	ADTCD32[R] B,H,W 10--0000 00000000		ADTCD33[R] B,H,W 10--0000 00000000		12-bit A/D converter 2/2 unit
$0014FC_H$	ADTCD34[R] B,H,W 10--0000 00000000		ADTCD35[R] B,H,W 10--0000 00000000		
001500_H	ADTCD36[R] B,H,W 10--0000 00000000		ADTCD37[R] B,H,W 10--0000 00000000		
001504_H	ADTCD38[R] B,H,W 10--0000 00000000		ADTCD39[R] B,H,W 10--0000 00000000		
001508_H	ADTCD40[R] B,H,W 10--0000 00000000		ADTCD41[R] B,H,W 10--0000 00000000		
$00150C_H$	ADTCD42[R] B,H,W 10--0000 00000000		ADTCD43[R] B,H,W 10--0000 00000000		
001510_H	ADTCD44[R] B,H,W 10--0000 00000000		ADTCD45[R] B,H,W 10--0000 00000000		
001514_H	ADTCD46[R] B,H,W 10--0000 00000000		ADTCD47[R] B,H,W 10--0000 00000000		
001518_H	ADTCD48[R] B,H,W 10--0000 00000000		ADTCD49[R] B,H,W 10--0000 00000000		
$00151C_H$	ADTCD50[R] B,H,W 10--0000 00000000		ADTCD51[R] B,H,W 10--0000 00000000		
001520_H	ADTCD52[R] B,H,W 10--0000 00000000		ADTCD53[R] B,H,W 10--0000 00000000		
001524_H	ADTCD54[R] B,H,W 10--0000 00000000		ADTCD55[R] B,H,W 10--0000 00000000		
001528_H	ADTCD56[R] B,H,W 10--0000 00000000		ADTCD57[R] B,H,W 10--0000 00000000		
$00152C_H$	ADTCD58[R] B,H,W 10--0000 00000000		ADTCD59[R] B,H,W 10--0000 00000000		
001530_H	ADTCD60[R] B,H,W 10--0000 00000000		ADTCD61[R] B,H,W 10--0000 00000000		
001534_H	ADTCD62[R] B,H,W 10--0000 00000000		ADTCD63[R] B,H,W 10--0000 00000000		
001538_H	ADTECS32[R/W] B,H,W -------0 ---00000		ADTECS33[R/W] B,H,W -------0 ---00000		
$00153C_H$	ADTECS34[R/W] B,H,W -------0 ---00000		ADTECS35[R/W] B,H,W -------0 ---00000		
001540_H	ADTECS36[R/W] B,H,W -------0 ---00000		ADTECS37[R/W] B,H,W -------0 ---00000		
001544_H	ADTECS38[R/W] B,H,W -------0 ---00000		ADTECS39[R/W] B,H,W -------0 ---00000		
001548_H	ADTECS40[R/W] B,H,W -------0 ---00000		ADTECS41[R/W] B,H,W -------0 ---00000		
$00154C_H$	ADTECS42[R/W] B,H,W -------0 ---00000		ADTECS43[R/W] B,H,W -------0 ---00000		
001550_H	ADTECS44[R/W] B,H,W -------0 ---00000		ADTECS45[R/W] B,H,W -------0 ---00000		
001554_H	ADTECS46[R/W] B,H,W -------0 ---00000		ADTECS47[R/W] B,H,W -------0 ---00000		
001558_H	ADTECS48[R/W] B,H,W -------0 ---00000		ADTECS49[R/W] B,H,W -------0 ---00000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00155C_H$	ADTECS50[R/W] B,H,W -------0 ---00000		ADTECS51[R/W] B,H,W -------0 ---00000		12-bit A/D converter 2/2 unit
001560_H	ADTECS52[R/W] B,H,W -------0 ---00000		ADTECS53[R/W] B,H,W -------0 ---00000		
001564_H	ADTECS54[R/W] B,H,W -------0 ---00000		ADTECS55[R/W] B,H,W -------0 ---00000		
001568_H	ADTECS56[R/W] B,H,W -------0 ---00000		ADTECS57[R/W] B,H,W -------0 ---00000		
$00156C_H$	ADTECS58[R/W] B,H,W -------0 ---00000		ADTECS59[R/W] B,H,W -------0 ---00000		
001570_H	ADTECS60[R/W] B,H,W -------0 ---00000		ADTECS61[R/W] B,H,W -------0 ---00000		
001574_H	ADTECS62[R/W] B,H,W -------0 ---00000		ADTECS63[R/W] B,H,W -------0 ---00000		
001578_H	ADRCUT4[R/W] B,H,W ----0000 00000000		ADRCLT4[R/W] B,H,W ----0000 00000000		
$00157C_H$	ADRCUT5[R/W] B,H,W ----0000 00000000		ADRCLT5[R/W] B,H,W ----0000 00000000		
001580_H	ADRCUT6[R/W] B,H,W ----0000 00000000		ADRCLT6[R/W] B,H,W ----0000 00000000		
001584_H	ADRCUT7[R/W] B,H,W ----0000 00000000		ADRCLT7[R/W] B,H,W ----0000 00000000		
001588_H	ADRCCS32[R/W] B,H,W 00000000	ADRCCS33[R/W] B,H,W 00000000	ADRCCS34[R/W] B,H,W 00000000	ADRCCS35[R/W] B,H,W 00000000	
$00158C_H$	ADRCCS36[R/W] B,H,W 00000000	ADRCCS37[R/W] B,H,W 00000000	ADRCCS38[R/W] B,H,W 00000000	ADRCCS39[R/W] B,H,W 00000000	
001590_H	ADRCCS40[R/W] B,H,W 00000000	ADRCCS41[R/W] B,H,W 00000000	ADRCCS42[R/W] B,H,W 00000000	ADRCCS43[R/W] B,H,W 00000000	
001594_H	ADRCCS44[R/W] B,H,W 00000000	ADRCCS45[R/W] B,H,W 00000000	ADRCCS46[R/W] B,H,W 00000000	ADRCCS47[R/W] B,H,W 00000000	
001598_H	ADRCCS48[R/W] B,H,W 00000000	ADRCCS49[R/W] B,H,W 00000000	ADRCCS50[R/W] B,H,W 00000000	ADRCCS51[R/W] B,H,W 00000000	
$00159C_H$	ADRCCS52[R/W] B,H,W 00000000	ADRCCS53[R/W] B,H,W 00000000	ADRCCS54[R/W] B,H,W 00000000	ADRCCS55[R/W] B,H,W 00000000	
$0015A0_H$	ADRCCS56[R/W] B,H,W 00000000	ADRCCS57[R/W] B,H,W 00000000	ADRCCS58[R/W] B,H,W 00000000	ADRCCS59[R/W] B,H,W 00000000	
$0015A4_H$	ADRCCS60[R/W] B,H,W 00000000	ADRCCS61[R/W] B,H,W 00000000	ADRCCS62[R/W] B,H,W 00000000	ADRCCS63[R/W] B,H,W 00000000	
$0015A8_H$	ADRCOT1 [R] B,H,W 00000000 00000000 00000000 00000000				
$0015AC_H$	ADRCIF1 [R,W] B,H,W 00000000 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0015B0$_H$	ADSCANS1 [R/W] B,H,W 000-----	—	—	—	12-bit A/D converter 2/2 unit
0015B4$_H$	ADNCS16 [R/W] B,H,W 0-000-00	ADNCS17 [R/W] B,H,W 0-000-00	ADNCS18 [R/W] B,H,W 0-000-00	ADNCS19 [R/W] B,H,W 0-000-00	
0015B8$_H$	ADNCS20 [R/W] B,H,W 0-000-00	ADNCS21 [R/W] B,H,W 0-000-00	ADNCS22 [R/W] B,H,W 0-000-00	ADNCS23 [R/W] B,H,W 0-000-00	
0015BC$_H$	ADNCS24 [R/W] B,H,W 0-000-00	ADNCS25 [R/W] B,H,W 0-000-00	ADNCS26 [R/W] B,H,W 0-000-00	ADNCS27 [R/W] B,H,W 0-000-00	
0015C0$_H$	ADNCS28 [R/W] B,H,W 0-000-00	ADNCS29 [R/W] B,H,W 0-000-00	ADNCS30 [R/W] B,H,W 0-000-00	ADNCS31 [R/W] B,H,W 0-000-00	
0015C4$_H$	ADPRTF1 [R] B,H,W 00000000 00000000 00000000 00000000				
0015C8$_H$	ADEOCF1 [R] B,H,W 11111111 11111111 11111111 11111111				
0015CC$_H$	ADCS1 [R] B,H,W 0------- --------		ADCH1 [R] B,H,W ---00000	ADMD1 [R/W] B,H,W 0---0000	
0015D0$_H$	ADSTPCS8 [R/W] B,H,W 00000000	ADSTPCS9 [R/W] B,H,W 00000000	ADSTPCS10 [R/W] B,H,W 00000000	ADSTPCS11 [R/W] B,H,W 00000000	
0015D4$_H$	ADSTPCS12[R/W] B,H,W 00000000	ADSTPCS13[R/W] B,H,W 00000000	ADSTPCS14[R/W] B,H,W 00000000	ADSTPCS15[R/W] B,H,W 00000000	
0015D8$_H$ to 00174C$_H$	—	—	—	—	Reserved
001750$_H$	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754$_H$	— /(RDR10/(TDR10))[R/W] B,H,W -------- --------*3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000*1		
001758$_H$	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175C$_H$	STMCR0[R/W] B,H,W 00000000 00000000		— /(SCSCR0/SFUR0)[R/W] B,H,W --------*3 --------*4		
001760$_H$	— /(SCSTR30)/ (LAMSR0) [R/W] B,H,W --------*3	— /(SCSTR20)/ (LAMCR0) [R/W] B,H,W --------*3	— /(SCSTR10) /(SFLR10) [R/W] B,H,W --------*3	— /(SCSTR00)/ (SFLR00) [R/W] B,H,W --------*3	
001764$_H$	—	— /(SCSFR20) [R/W] B,H,W --------*3	— /(SCSFR10) [R/W] B,H,W --------*3	— /(SCSFR00) [R/W] B,H,W --------*3	
001768$_H$	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W --------*3	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W --------*3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W --------*3	TBYTE00/(LAMRID0) /(LAMTID0) [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00176C_H$	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W --------*2	— /(ISBA0) [R/W] B,H,W --------*2	Multi-UART0 *2: Reserved because I^2C mode is not set immediately after reset.
001770_H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774_H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	
001778_H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W] B,H,W 00000000	Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00177C_H$	— /(RDR11/(TDR11))[R/W] B,H,W -------- --------*3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000*1		
001780_H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001784_H	STMCR1[R/W] B,H,W 00000000 00000000		— /(SCSCR1/SFUR1)[R/W] B,H,W -------- --------*3 *4		
001788_H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W --------*3	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W --------*3	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W --------*3	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W --------*3	
$00178C_H$	—	— /(SCSFR21)[R/W] B,H,W --------*3	— /(SCSFR11) [R/W] B,H,W --------*3	— /(SCSFR01) [R/W] B,H,W --------*3	
001790_H	—/(TBYTE31)/ (LAMESR1) [R/W] B,H,W --------*3	—/(TBYTE21)/ (LAMERT1) [R/W] B,H,W --------*3	—/(TBYTE11)/ (LAMIER1) [R/W] B,H,W --------*3	TBYTE01/(LAMRID1) /(LAMTID1) [R/W] B,H,W 00000000	
001794_H	BGR1[R/W] H,W 00000000 00000000		— /(ISMK1)[R/W] B,H,W --------*2	— /(ISBA1)[R/W] B,H,W --------*2	
001798_H	FCR11[R/W] B,H,W ---00100	FCR01[R/W] B,H,W -0000000	FBYTE1[R/W] B,H,W 00000000 00000000		
$00179C_H$	FTICR1[R/W] B,H,W 00000000 00000000		—	—	
$0017A0_H$	SCR2/(IBCR2)[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000-00-0	SSR2[R/W] B,H,W 0-000011	ESCR2/(IBSR2)[R/W] B,H,W 00000000	Multi-UART2 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset.
$0017A4_H$	— /(RDR12/(TDR12))[R/W] B,H,W -------- --------*3		RDR02/(TDR02)[R/W] B,H,W -------0 00000000*1		
$0017A8_H$	SACSR2[R/W] B,H,W 0----000 00000000		STMR2[R] B,H,W 00000000 00000000		
$0017AC_H$	STMCR2[R/W] B,H,W 00000000 00000000		— /(SCSCR2/SFUR2)[R/W] B,H,W -------- --------*3 *4		
$0017B0_H$	— /(SCSTR32)/ (LAMSR2) [R/W] B,H,W --------*3	— /(SCSTR22)/ (LAMCR2) [R/W] B,H,W --------*3	— /(SCSTR12)/ (SFLR12) [R/W] B,H,W --------*3	— /(SCSTR02)/ (SFLR02) [R/W] B,H,W --------*3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017B4H	—	— /(SCSFR22) [R/W] B,H,W --------*3	— /(SCSFR12) [R/W] B,H,W --------*3	— /(SCSFR02) [R/W] B,H,W --------*3	Multi-UART2 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017B8H	—/(TBYTE32)/ (LAMESR2) [R/W] B,H,W --------*3	—/(TBYTE22)/ (LAMERT2) [R/W] B,H,W --------*3	—/(TBYTE12)/ (LAMIER2) [R/W] B,H,W --------*3	TBYTE02/(LAMRID2) /(LAMTID2) [R/W] B,H,W 00000000	
0017BCH	BGR2[R/W] H, W 00000000 00000000		— /(ISMK2)[R/W] B,H,W --------*2	— /(ISBA2)[R/W] B,H,W --------*2	
0017C0H	FCR12[R/W] B,H,W ---00100	FCR02[R/W] B,H,W -0000000	FBYTE2[R/W] B,H,W 00000000 00000000		
0017C4H	FTICR2[R/W] B,H,W 00000000 00000000		—	—	
0017C8H	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000-00-0	SSR3[R/W] B,H,W 0-000011	ESCR3/(IBSR3)[R/W] B,H,W 00000000	Multi-UART3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017CCH	— /(RDR13/(TDR13))[R/W] B,H,W -------- --------*3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000*1		
0017D0H	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
0017D4H	STMCR3[R/W] B,H,W 00000000 00000000		— /(SCSCR3/SFUR3)[R/W] B,H,W -------- --------*3 *4		
0017D8H	— /(SCSTR33)/ (LAMSR3) [R/W] B,H,W --------*3	— /(SCSTR23)/ (LAMCR3) [R/W] B,H,W --------*3	— /(SCSTR13)/ (SFLR13) [R/W] B,H,W --------*3	— /(SCSTR03)/ (SFLR03) [R/W] B,H,W --------*3	
0017DCH	—	— /(SCSFR23) [R/W] B,H,W --------*3	— /(SCSFR13) [R/W] B,H,W --------*3	— /(SCSFR03) [R/W] B,H,W --------*3	
0017E0H	—/(TBYTE33)/ (LAMESR3) [R/W] B,H,W --------*3	—/(TBYTE23)/ (LAMERT3) [R/W] B,H,W --------*3	—/(TBYTE13)/ (LAMIER3) [R/W] B,H,W --------*3	TBYTE03/(LAMRID3) /(LAMTID3) [R/W] B,H,W 00000000	
0017E4H	BGR3[R/W] H, W 00000000 00000000		— /(ISMK3)[R/W] B,H,W --------*2	— /(ISBA3)[R/W] B,H,W --------*2	
0017E8H	FCR13[R/W] B,H,W ---00100	FCR03[R/W] B,H,W -0000000	FBYTE3[R/W] B,H,W 00000000 00000000		
0017ECH	FTICR3[R/W] B,H,W 00000000 00000000		—	—	
0017F0H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000-00-0	SSR4[R/W] B,H,W 0-000011	ESCR4/(IBSR4)[R/W] B,H,W 00000000	Multi-UART4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset.
0017F4H	— /(RDR14/(TDR14))[R/W] B,H,W -------- --------*3		RDR04/(TDR04)[R/W] B,H,W -------0 00000000*1		
0017F8H	SACSR4[R/W] B,H,W 0----000 00000000		STMR4[R] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017FC$_H$	STMCR4[R/W] B,H,W 00000000 00000000		— /(SCSCR4/SFUR4)[R/W] B,H,W -------- --------*3 *4		Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001800$_H$	— /(SCSTR34)/ (LAMSR4) [R/W] B,H,W --------*3	— /(SCSTR24)/ (LAMCR4) [R/W] B,H,W --------*3	— /(SCSTR14)/ (SFLR14) [R/W] B,H,W --------*3	— /(SCSTR04)/ (SFLR04) [R/W] B,H,W --------*3	
001804$_H$	—	— /(SCSFR24) [R/W] B,H,W --------*3	— /(SCSFR14) [R/W] B,H,W --------*3	— /(SCSFR04) [R/W] B,H,W --------*3	
001808$_H$	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W --------*3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W --------*3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W --------*3	TBYTE04/(LAMRID4) /(LAMTID4) [R/W] B,H,W 00000000	
00180C$_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W --------*2	— /(ISBA4)[R/W] B,H,W --------*2	
001810$_H$	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814$_H$	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818$_H$	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
00181C$_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- --------*3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000*1		
001820$_H$	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824$_H$	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- --------*3 *4		
001828$_H$	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W --------*3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W --------*3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W --------*3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W --------*3	
00182C$_H$	—	— /(SCSFR25) [R/W] B,H,W --------*3	— /(SCSFR15) [R/W] B,H,W --------*3	— /(SCSFR05) [R/W] B,H,W --------*3	
001830$_H$	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W --------*3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W --------*3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W --------*3	TBYTE05/(LAMRID5) /(LAMTID5) [R/W] B,H,W 00000000	
001834$_H$	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W --------*2	— /(ISBA5)[R/W] B,H,W --------*2	
001838$_H$	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
00183C$_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001840_H	SCR6/(IBCR6) [R/W] B,H,W 0--00000	SMR6[R/W] B,H,W 000-00-0	SSR6[R/W] B,H,W 0-000011	ESCR6/(IBSR6)[R/W] B,H,W 00000000	Multi-UART6 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001844_H	— /(RDR16/(TDR16))[R/W] B,H,W -------- --------*3		RDR06/(TDR06)[R/W] B,H,W -------0 00000000*1		
001848_H	SACSR6[R/W] B,H,W 0----000 00000000		STMR6[R] B,H,W 00000000 00000000		
$00184C_H$	STMCR6[R/W] B,H,W 00000000 00000000		— /(SCSCR6/SFUR6)[R/W] B,H,W -------- --------*3 *4		
001850_H	— /(SCSTR36)/ (LAMSR6) [R/W] B,H,W --------*3	— /(SCSTR26)/ (LAMCR6) [R/W] B,H,W --------*3	— /(SCSTR16)/ (SFLR16) [R/W] B,H,W --------*3	— /(SCSTR06)/ (SFLR06) [R/W] B,H,W --------*3	
001854_H	—	— /(SCSFR26) [R/W] B,H,W --------*3	— /(SCSFR16) [R/W] B,H,W --------*3	— /(SCSFR06) [R/W] B,H,W --------*3	
001858_H	—/(TBYTE36)/ (LAMESR6) [R/W] B,H,W --------*3	—/(TBYTE26)/ (LAMERT6) [R/W] B,H,W --------*3	—/(TBYTE16)/ (LAMIER6) [R/W] B,H,W --------*3	TBYTE06/(LAMRID6) /(LAMTID6) [R/W] B,H,W 00000000	
$00185C_H$	BGR6[R/W] H, W 00000000 00000000		— /(ISMK6)[R/W] B,H,W --------*2	— /(ISBA6)[R/W] B,H,W --------*2	
001860_H	FCR16[R/W] B,H,W ---00100	FCR06[R/W] B,H,W -0000000	FBYTE6[R/W] B,H,W 00000000 00000000		
001864_H	FTICR6[R/W] B,H,W 00000000 00000000		—	—	
001868_H	SCR7/(IBCR7) [R/W] B,H,W 0--00000	SMR7[R/W] B,H,W 000-00-0	SSR7[R/W] B,H,W 0-000011	ESCR7/(IBSR7)[R/W] B,H,W 00000000	Multi-UART7 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00186C_H$	— /(RDR17/(TDR17))[R/W] B,H,W -------- --------*3		RDR07/(TDR07)[R/W] B,H,W -------0 00000000*1		
001870_H	SACSR7[R/W] B,H,W 0----000 00000000		STMR7[R] B,H,W 00000000 00000000		
001874_H	STMCR7[R/W] B,H,W 00000000 00000000		— /(SCSCR7/SFUR7)[R/W] B,H,W -------- --------*3 *4		
001878_H	— /(SCSTR37)/ (LAMSR7) [R/W] B,H,W --------*3	— /(SCSTR27)/ (LAMCR7) [R/W] B,H,W --------*3	— /(SCSTR17)/ (SFLR17) [R/W] B,H,W --------*3	— /(SCSTR07)/ (SFLR07) [R/W] B,H,W --------*3	
$00187C_H$	—	— /(SCSFR27) [R/W] B,H,W --------*3	— /(SCSFR17) [R/W] B,H,W --------*3	— /(SCSFR07) [R/W] B,H,W --------*3	
001880_H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W --------*3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W --------*3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W --------*3	TBYTE07/(LAMRID7) /(LAMTID7) [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001884$_H$	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W --------*2	— /(ISBA7)[R/W] B,H,W --------*2	
001888$_H$	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		Multi-UART7
00188C$_H$	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890$_H$	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894$_H$	— /(RDR18/(TDR18))[R/W] B,H,W -------- --------*3		RDR08/(TDR08)[R/W] B,H,W -------0 00000000*1		
001898$_H$	SACSR8[R/W] B,H,W 0----000 00000000		STMR8[R] B,H,W 00000000 00000000		
00189C$_H$	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -------- --------*3 *4		
0018A0$_H$	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W --------*3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W --------*3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W --------*3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W --------*3	
0018A4$_H$	—	— /(SCSFR28) [R/W] B,H,W --------*3	— /(SCSFR18) [R/W] B,H,W --------*3	— /(SCSFR08) [R/W] B,H,W --------*3	
0018A8$_H$	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W --------*3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W --------*3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W --------*3	TBYTE08/(LAMRID8) /(LAMTID8) [R/W] B,H,W 00000000	
0018AC$_H$	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W --------*2	— /(ISBA8)[R/W] B,H,W --------*2	
0018B0$_H$	FCR18[R/W] B,H,W ---00100	FCR08[R/W] B,H,W -0000000	FBYTE8[R/W] B,H,W 00000000 00000000		
0018B4$_H$	FTICR8[R/W] B,H,W 00000000 00000000		—	—	
0018B8$_H$	SCR9/(IBCR9) [R/W] B,H,W 0--00000	SMR9[R/W] B,H,W 000-00-0	SSR9[R/W] B,H,W 0-000011	ESCR9/(IBSR9)[R/W] B,H,W 00000000	Multi-UART9 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset.
0018BC$_H$	— /(RDR19/(TDR19))[R/W] B,H,W -------- --------*3		RDR09/(TDR09)[R/W] B,H,W -------0 00000000*1		
0018C0$_H$	SACSR9[R/W] B,H,W 0----000 00000000		STMR9[R] B,H,W 00000000 00000000		
0018C4$_H$	STMCR9[R/W] B,H,W 00000000 00000000		— /(SCSCR9/SFUR9)[R/W] B,H,W -------- --------*3 *4		
0018C8$_H$	— /(SCSTR39)/ (LAMSR9) [R/W] B,H,W --------*3	— /(SCSTR29)/ (LAMCR9) [R/W] B,H,W --------*3	— /(SCSTR19)/ (SFLR19) [R/W] B,H,W --------*3	— /(SCSTR09)/ (SFLR09) [R/W] B,H,W --------*3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0018CC$_H$	—	— /(SCSFR29) [R/W] B,H,W --------*3	— /(SCSFR19) [R/W] B,H,W --------*3	— /(SCSFR09) [R/W] B,H,W --------*3	
0018D0$_H$	—/(TBYTE39)/ (LAMESR9) [R/W] B,H,W --------*3	—/(TBYTE29)/ (LAMERT9) [R/W] B,H,W --------*3	—/(TBYTE19)/ (LAMIER9) [R/W] B,H,W --------*3	TBYTE09/(LAMRID9) /(LAMTID9) [R/W] B,H,W 00000000	Multi-UART9 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0018D4$_H$	BGR9[R/W] H, W 00000000 00000000		— /(ISMK9)[R/W] B,H,W --------*2	— /(ISBA9)[R/W] B,H,W --------*2	
0018D8$_H$	FCR19[R/W] B,H,W ---00100	FCR09[R/W] B,H,W -0000000	FBYTE9[R/W] B,H,W 00000000 00000000		
0018DC$_H$	FTICR9[R/W] B,H,W 00000000 00000000		—	—	
0018E0$_H$	SCR10/(IBCR10) [R/W] B,H,W 0--00000	SMR10[R/W] B,H,W 000-00-0	SSR10[R/W] B,H,W 0-000011	ESCR10/(IBSR10) [R/W] B,H,W 00000000	Multi-UART10 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0018E4$_H$	— /(RDR110/(TDR110))[R/W] B,H,W -------- --------*3		RDR010/(TDR010)[R/W] B,H,W -------0 00000000*1		
0018E8$_H$	SACSR10[R/W] B,H,W 0----000 00000000		STMR10[R] B,H,W 00000000 00000000		
0018EC$_H$	STMCR10[R/W] B,H,W 00000000 00000000		— /(SCSCR10/SFUR10)[R/W] B,H,W -------- --------*3 *4		
0018F0$_H$	— /(SCSTR310)/ (LAMSR10) [R/W] B,H,W --------*3	— /(SCSTR210)/ (LAMCR10) [R/W] B,H,W --------*3	— /(SCSTR110)/ (SFLR110)[R/W] B,H,W --------*3	— /(SCSTR010)/ (SFLR010)[R/W] B,H,W --------*3	
0018F4$_H$	—	— /(SCSFR210) [R/W] B,H,W --------*3	— /(SCSFR110) [R/W] B,H,W --------*3	— /(SCSFR010) [R/W] B,H,W --------*3	
0018F8$_H$	—/(TBYTE310)/ (LAMESR10) [R/W] B,H,W --------*3	—/(TBYTE210)/ (LAMERT10) [R/W] B,H,W --------*3	—/(TBYTE110)/ (LAMIER10) [R/W] B,H,W --------*3	TBYTE010/(LAMRID 10)/(LAMTID10) [R/W] B,H,W 00000000	
0018FC$_H$	BGR10[R/W] H, W 00000000 00000000		— /(ISMK10)[R/W] B,H,W --------*2	— /(ISBA10)[R/W] B,H,W --------*2	
001900$_H$	FCR110[R/W] B,H,W ---00100	FCR010[R/W] B,H,W -0000000	FBYTE10[R/W] B,H,W 00000000 00000000		
001904$_H$	FTICR10[R/W] B,H,W 00000000 00000000		—	—	
001908$_H$	SCR11/(IBCR11) [R/W] B,H,W 0--00000	SMR11[R/W] B,H,W 000-00-0	SSR11[R/W] B,H,W 0-000011	ESCR11/(IBSR11) [R/W] B,H,W 00000000	Multi-UART11 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset.
00190C$_H$	— /(RDR111/(TDR111))[R/W] B,H,W -------- --------*3		RDR011/(TDR011)[R/W] B,H,W -------0 00000000*1		
001910$_H$	SACSR11[R/W] B,H,W 0----000 00000000		STMR11[R] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001914_H	STMCR11[R/W] B,H,W 00000000 00000000		— /(SCSCR11/SFUR11)[R/W] B,H,W -------- --------*3 *4		
001918_H	— /(SCSTR311)/ (LAMSR11) [R/W] B,H,W --------*3	— /(SCSTR211)/ (LAMCR11) [R/W] B,H,W --------*3	— /(SCSTR111)/ (SFLR111)[R/W] B,H,W --------*3	— /(SCSTR011)/ (SFLR011)[R/W] B,H,W --------*3	Multi-UART11 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00191C_H$	—	— /(SCSFR211) [R/W] B,H,W --------*3	— /(SCSFR111) [R/W] B,H,W --------*3	— /(SCSFR011) [R/W] B,H,W --------*3	
001920_H	—/(TBYTE311)/ (LAMESR11) [R/W] B,H,W --------*3	—/(TBYTE211)/ (LAMERT11) [R/W] B,H,W --------*3	—/(TBYTE111)/ (LAMIER11) [R/W] B,H,W --------*3	TBYTE011/(LAMRID 11)/(LAMTID11) [R/W] B,H,W 00000000	
001924_H	BGR11[R/W] H, W 00000000 00000000		— /(ISMK11)[R/W] B,H,W --------*2	— /(ISBA11)[R/W] B,H,W --------*2	
001928_H	FCR111[R/W] B,H,W ---00100	FCR011[R/W] B,H,W -0000000	FBYTE11[R/W] B,H,W 00000000 00000000		
$00192C_H$	FTICR11[R/W] B,H,W 00000000 00000000		—	—	
001930_H	SCR12/(IBCR12) [R/W] B,H,W 0--00000	SMR12 [R/W] B,H,W 000-00-0	SSR12 [R/W] B,H,W 0-000011	ESCR12/(IBSR12) [R/W] B,H,W 00000000	Multi-UART12 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001934_H	— /(RDR112/(TDR112))[R/W] B,H,W -------- --------*3		RDR012/(TDR012)[R/W] B,H,W -------0 00000000*1		
001938_H	SACSR12[R/W] B,H,W 0----000 00000000		STMR12[R] B,H,W 00000000 00000000		
$00193C_H$	STMCR12[R/W] B,H,W 00000000 00000000		— /(SCSCR12/SFUR12)[R/W] B,H,W -------- --------*3 *4		
001940_H	— /(SCSTR312)/ (LAMSR12) [R/W] B,H,W --------*3	— /(SCSTR212)/ (LAMCR12) [R/W] B,H,W --------*3	— /(SCSTR112)/(SFLR1 12) [R/W] B,H,W --------*3	— /(SCSTR012)/(SFLR 012) [R/W] B,H,W --------*3	
001944_H	—	— /(SCSFR212) [R/W] B,H,W --------*3	— /(SCSFR112) [R/W] B,H,W --------*3	— /(SCSFR012) [R/W] B,H,W --------*3	
001948_H	—/(TBYTE312)/ (LAMESR12) [R/W] B,H,W --------*3	—/(TBYTE212)/ (LAMERT12) [R/W] B,H,W --------*3	—/(TBYTE112)/ (LAMIER12) [R/W] B,H,W --------*3	TBYTE012/(LAMRID 12)/(LAMTID12) [R/W] B,H,W 00000000	
$00194C_H$	BGR12[R/W] H,W 00000000 00000000		— /(ISMK12) [R/W] B,H,W --------*2	— /(ISBA12) [R/W] B,H,W --------*2	
001950_H	FCR112 [R/W] B,H,W ---00100	FCR012 [R/W] B,H,W -0000000	FBYTE12[R/W] B,H,W 00000000 00000000		
001954_H	FTICR12[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001958_H	SCR13/(IBCR13) [R/W] B,H,W 0--00000	SMR13 [R/W] B,H,W 000-00-0	SSR13 [R/W] B,H,W 0-000011	ESCR13/(IBSR13) [R/W] B,H,W 00000000	Multi-UART13 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00195C_H$	— /(RDR113/(TDR113))[R/W] B,H,W -------- --------*3		RDR013/(TDR013)[R/W] B,H,W -------0 00000000*1		
001960_H	SACSR13[R/W] B,H,W 0----000 00000000		STMR13[R] B,H,W 00000000 00000000		
001964_H	STMCR13[R/W] B,H,W 00000000 00000000		— /(SCSCR13/SFUR13)[R/W] B,H,W -------- --------*3 *4		
001968_H	— /(SCSTR313)/ (LAMSR13) [R/W] B,H,W --------*3	— /(SCSTR213)/ (LAMCR13) [R/W] B,H,W --------*3	— /(SCSTR113)/(SFLR113) [R/W] B,H,W --------*3	— /(SCSTR013)/(SFLR013) [R/W] B,H,W --------*3	
$00196C_H$	—	— /(SCSFR213) [R/W] B,H,W --------*3	— /(SCSFR113) [R/W] B,H,W --------*3	— /(SCSFR013) [R/W] B,H,W --------*3	
001970_H	—/(TBYTE313)/ (LAMESR13) [R/W] B,H,W --------*3	—/(TBYTE213)/ (LAMERT13) [R/W] B,H,W --------*3	—/(TBYTE113)/ (LAMIER13) [R/W] B,H,W --------*3	TBYTE013/(LAMRID13)/(LAMTID13) [R/W] B,H,W 00000000	
001974_H	BGR13[R/W] H,W 00000000 00000000		— /(ISMK13) [R/W] B,H,W --------*2	— /(ISBA13) [R/W] B,H,W --------*2	
001978_H	FCR113 [R/W] B,H,W ---00100	FCR013 [R/W] B,H,W -0000000	FBYTE13[R/W] B,H,W 00000000 00000000		
$00197C_H$	FTICR13[R/W] B,H,W 00000000 00000000		—	—	
001980_H	SCR14/(IBCR14) [R/W] B,H,W 0--00000	SMR14 [R/W] B,H,W 000-00-0	SSR14 [R/W] B,H,W 0-000011	ESCR14/(IBSR14) [R/W] B,H,W 00000000	Multi-UART14 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001984_H	— /(RDR114/(TDR114))[R/W] B,H,W -------- --------*3		RDR014/(TDR014)[R/W] B,H,W -------0 00000000*1		
001988_H	SACSR14[R/W] B,H,W 0----000 00000000		STMR14[R] B,H,W 00000000 00000000		
$00198C_H$	STMCR14[R/W] B,H,W 00000000 00000000		— /(SCSCR14/SFUR14)[R/W] B,H,W -------- --------*3 *4		
001990_H	— /(SCSTR314)/ (LAMSR14) [R/W] B,H,W --------*3	— /(SCSTR214)/ (LAMCR14) [R/W] B,H,W --------*3	— /(SCSTR114)/(SFLR114) [R/W] B,H,W --------*3	— /(SCSTR014)/(SFLR014) [R/W] B,H,W --------*3	
001994_H	—	— /(SCSFR214) [R/W] B,H,W --------*3	— /(SCSFR114) [R/W] B,H,W --------*3	— /(SCSFR014) [R/W] B,H,W --------*3	
001998_H	—/(TBYTE314)/ (LAMESR14) [R/W] B,H,W --------*3	—/(TBYTE214)/ (LAMERT14) [R/W] B,H,W --------*3	—/(TBYTE114)/ (LAMIER14) [R/W] B,H,W --------*3	TBYTE014/(LAMRID14)/(LAMTID14) [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00199C$_H$	BGR14[R/W] H,W 00000000 00000000		— /(ISMK14) [R/W] B,H,W --------*2	— /(ISBA14) [R/W] B,H,W --------*2	Multi-UART14
0019A0$_H$	FCR114 [R/W] B,H,W ---00100	FCR014 [R/W] B,H,W -0000000	FBYTE14[R/W] B,H,W 00000000 00000000		
0019A4$_H$	FTICR14[R/W] B,H,W 00000000 00000000		—	—	
0019A8$_H$	SCR15/(IBCR15) [R/W] B,H,W 0--00000	SMR15 [R/W] B,H,W 000-00-0	SSR15 [R/W] B,H,W 0-000011	ESCR15/(IBSR15) [R/W] B,H,W 00000000	Multi-UART15 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0019AC$_H$	— /(RDR115/(TDR115))[R/W] B,H,W -------- --------*3		RDR015/(TDR015)[R/W] B,H,W -------0 00000000*1		
0019B0$_H$	SACSR15[R/W] B,H,W 0----000 00000000		STMR15[R] B,H,W 00000000 00000000		
0019B4$_H$	STMCR15[R/W] B,H,W 00000000 00000000		— /(SCSCR15/SFUR15)[R/W] B,H,W -------- --------*3 *4		
0019B8$_H$	— /(SCSTR315)/ (LAMSR15) [R/W] B,H,W --------*3	— /(SCSTR215)/ (LAMCR15) [R/W] B,H,W --------*3	— /(SCSTR115)/(SFLR115) [R/W] B,H,W --------*3	— /(SCSTR015)/(SFLR015) [R/W] B,H,W --------*3	
0019BC$_H$	—	— /(SCSFR215) [R/W] B,H,W --------*3	— /(SCSFR115) [R/W] B,H,W --------*3	— /(SCSFR015) [R/W] B,H,W --------*3	
0019C0$_H$	—/(TBYTE315)/ (LAMESR15) [R/W] B,H,W --------*3	—/(TBYTE215)/ (LAMERT15) [R/W] B,H,W --------*3	—/(TBYTE115)/ (LAMIER15) [R/W] B,H,W --------*3	TBYTE015/(LAMRID15)/(LAMTID15) [R/W] B,H,W 00000000	
0019C4$_H$	BGR15[R/W] H,W 00000000 00000000		— /(ISMK15) [R/W] B,H,W --------*2	— /(ISBA15) [R/W] B,H,W --------*2	
0019C8$_H$	FCR115 [R/W] B,H,W ---00100	FCR015 [R/W] B,H,W -0000000	FBYTE15[R/W] B,H,W 00000000 00000000		
0019CC$_H$	FTICR15[R/W] B,H,W 00000000 00000000		—	—	
0019D0$_H$	GTRS40 [R/W] B,H,W -0000000 -0000000		GTRS41 [R/W] B,H,W -0000000 -0000000		PPG controller
0019D4$_H$	GTRS42 [R/W] B,H,W -0000000 -0000000		GTRS43 [R/W] B,H,W -0000000 -0000000		
0019D8$_H$	GTREN4 [R/W] H,W 00000000 00000000		GTREN5 [R/W] H,W -------- 00000000		
0019DC$_H$	—	GATEC0 [R/W] B,H,W ------00	—	GATEC2 [R/W] B,H,W ------00	PPG GATE control
0019E0$_H$	—	GATEC4 [R/W] B,H,W ------00	—	—	
0019E4$_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0019E8_H$	GTRS0 [R/W] B,H,W -0000000 -0000000		GTRS1 [R/W] B,H,W -0000000 -0000000		PPG controller
$0019EC_H$	GTRS2 [R/W] B,H,W -0000000 -0000000		GTRS3 [R/W] B,H,W -0000000 -0000000		
$0019F0_H$	GTRS4 [R/W] B,H,W -0000000 -0000000		GTRS5 [R/W] B,H,W -0000000 -0000000		
$0019F4_H$	GTRS6 [R/W] B,H,W -0000000 -0000000		GTRS7 [R/W] B,H,W -0000000 -0000000		
$0019F8_H$	GTRS8 [R/W] B,H,W -0000000 -0000000		GTRS9 [R/W] B,H,W -0000000 -0000000		
$0019FC_H$	GTRS10 [R/W] B,H,W -0000000 -0000000		GTRS11 [R/W] B,H,W -0000000 -0000000		
$001A00_H$	GTRS12 [R/W] B,H,W -0000000 -0000000		GTRS13 [R/W] B,H,W -0000000 -0000000		
$001A04_H$	GTRS14 [R/W] B,H,W -0000000 -0000000		GTRS15 [R/W] B,H,W -0000000 -0000000		
$001A08_H$	GTRS16 [R/W] B,H,W -0000000 -0000000		GTRS17 [R/W] B,H,W -0000000 -0000000		
$001A0C_H$	GTRS18 [R/W] B,H,W -0000000 -0000000		GTRS19 [R/W] B,H,W -0000000 -0000000		
$001A10_H$	GTRS20 [R/W] B,H,W -0000000 -0000000		GTRS21 [R/W] B,H,W -0000000 -0000000		
$001A14_H$	GTRS22 [R/W] B,H,W -0000000 -0000000		GTRS23 [R/W] B,H,W -0000000 -0000000		
$001A18_H$	GTRS24 [R/W] B,H,W -0000000 -0000000		GTRS25 [R/W] B,H,W -0000000 -0000000		
$001A1C_H$	GTRS26 [R/W] B,H,W -0000000 -0000000		GTRS27 [R/W] B,H,W -0000000 -0000000		
$001A20_H$	GTRS28 [R/W] B,H,W -0000000 -0000000		GTRS29 [R/W] B,H,W -0000000 -0000000		
$001A24_H$	GTRS30 [R/W] B,H,W -0000000 -0000000		GTRS31 [R/W] B,H,W -0000000 -0000000		
$001A28_H$	GTRS32 [R/W] B,H,W -0000000 -0000000		GTRS33 [R/W] B,H,W -0000000 -0000000		
$001A2C_H$	GTRS34 [R/W] B,H,W -0000000 -0000000		GTRS35 [R/W] B,H,W -0000000 -0000000		
$001A30_H$	GTRS36 [R/W] B,H,W -0000000 -0000000		GTRS37 [R/W] B,H,W -0000000 -0000000		
$001A34_H$	GTRS38 [R/W] B,H,W -0000000 -0000000		GTRS39 [R/W] B,H,W -0000000 -0000000		
$001A38_H$	GTREN0 [R/W] H,W 00000000 00000000		GTREN1 [R/W] H,W 00000000 00000000		PPG controller
$001A3C_H$	GTREN2 [R/W] H,W 00000000 00000000		GTREN3 [R/W] H,W 00000000 00000000		
$001A40_H$	PCN0 [R/W] B,H,W 00000000 000000-0		PCSR0 [W] H,W XXXXXXXX XXXXXXXX		PPG0 (Note) for communication
$001A44_H$	PDUT0 [W] H,W XXXXXXXX XXXXXXXX		PTMR0 [R] H,W 11111111 11111111		
$001A48_H$	PCN200 [R/W] B,H,W --000000 -----110		PSDR0 [R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001A4C$_H$	PTPC0 [R/W] H,W 00000000 00000000		PCMDWD0 [R/W] B,H,W -------- ----0000		PPG0 (Note) for communication
001A50$_H$	PHCSR0 [W] H,W XXXXXXXX XXXXXXXX		PLCSR0 [W] H,W XXXXXXXX XXXXXXXX		
001A54$_H$	PHDUT0 [W] H,W XXXXXXXX XXXXXXXX		PLDUT0 [W] H,W XXXXXXXX XXXXXXXX		
001A58$_H$	PCMDDT0 [R/W] H,W 00000000 00000000		—	—	
001A5C$_H$	PCN1 [R/W] B,H,W 00000000 000000-0		PCSR1 [W] H,W XXXXXXXX XXXXXXXX		PPG1 (Note) for communication
001A60$_H$	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PTMR1 [R] H,W 11111111 11111111		
001A64$_H$	PCN201 [R/W] B,H,W --000000 -----110		PSDR1 [R/W] H,W 00000000 00000000		
001A68$_H$	PTPC1 [R/W] H,W 00000000 00000000		PCMDWD1 [R/W] B,H,W -------- ----0000		
001A6C$_H$	PHCSR1 [W] H,W XXXXXXXX XXXXXXXX		PLCSR1 [W] H,W XXXXXXXX XXXXXXXX		
001A70$_H$	PHDUT1 [W] H,W XXXXXXXX XXXXXXXX		PLDUT1 [W] H,W XXXXXXXX XXXXXXXX		
001A74$_H$	PCMDDT1 [R/W] H,W 00000000 00000000		—	—	
001A78$_H$	PCN2 [R/W] B,H,W 00000000 000000-0		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2 (Note) for communication
001A7C$_H$	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PTMR2 [R] H,W 11111111 11111111		
001A80$_H$	PCN202 [R/W] B,H,W --000000 -----110		PSDR2 [R/W] H,W 00000000 00000000		
001A84$_H$	PTPC2 [R/W] H,W 00000000 00000000		PCMDWD2 [R/W] B,H,W -------- ----0000		
001A88$_H$	PHCSR2 [W] H,W XXXXXXXX XXXXXXXX		PLCSR2 [W] H,W XXXXXXXX XXXXXXXX		
001A8C$_H$	PHDUT2 [W] H,W XXXXXXXX XXXXXXXX		PLDUT2 [W] H,W XXXXXXXX XXXXXXXX		
001A90$_H$	PCMDDT2 [R/W] H,W 00000000 00000000		—	—	
001A94$_H$	PCN3 [R/W] B,H,W 00000000 000000-0		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3 (Note) for communication
001A98$_H$	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PTMR3 [R] H,W 11111111 11111111		
001A9C$_H$	PCN203 [R/W] B,H,W --000000 -----110		PSDR3 [R/W] H,W 00000000 00000000		
001AA0$_H$	PTPC3 [R/W] H,W 00000000 00000000		PCMDWD3 [R/W] B,H,W -------- ----0000		
001AA4$_H$	PHCSR3 [W] H,W XXXXXXXX XXXXXXXX		PLCSR3 [W] H,W XXXXXXXX XXXXXXXX		
001AA8$_H$	PHDUT3 [W] H,W XXXXXXXX XXXXXXXX		PLDUT3 [W] H,W XXXXXXXX XXXXXXXX		
001AAC$_H$	PCMDDT3 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001AB0_H$	PCN4 [R/W] B,H,W 00000000 000000-0		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		PPG4
$001AB4_H$	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PTMR4 [R] H,W 11111111 11111111		
$001AB8_H$	PCN204 [R/W] B,H,W --000000 -----110		PSDR4 [R/W] H,W 00000000 00000000		
$001ABC_H$	PTPC4 [R/W] H,W 00000000 00000000		—	—	
$001AC0_H$	PCN5 [R/W] B,H,W 00000000 000000-0		PCSR5 [W] H,W XXXXXXXX XXXXXXXX		PPG5
$001AC4_H$	PDUT5 [W] H,W XXXXXXXX XXXXXXXX		PTMR5 [R] H,W 11111111 11111111		
$001AC8_H$	PCN205 [R/W] B,H,W --000000 -----110		PSDR5 [R/W] H,W 00000000 00000000		
$001ACC_H$	PTPC5 [R/W] H,W 00000000 00000000		—	—	
$001AD0_H$	PCN6 [R/W] B,H,W 00000000 000000-0		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
$001AD4_H$	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PTMR6 [R] H,W 11111111 11111111		
$001AD8_H$	PCN206 [R/W] B,H,W --000000 -----110		PSDR6 [R/W] H,W 00000000 00000000		
$001ADC_H$	PTPC6 [R/W] H,W 00000000 00000000		—	—	
$001AE0_H$	PCN7 [R/W] B,H,W 00000000 000000-0		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
$001AE4_H$	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PTMR7 [R] H,W 11111111 11111111		
$001AE8_H$	PCN207 [R/W] B,H,W --000000 -----110		PSDR7 [R/W] H,W 00000000 00000000		
$001AEC_H$	PTPC7 [R/W] H,W 00000000 00000000		—	—	
$001AF0_H$	PCN8 [R/W] B,H,W 00000000 000000-0		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
$001AF4_H$	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PTMR8 [R] H,W 11111111 11111111		
$001AF8_H$	PCN208 [R/W] B,H,W --000000 -----110		PSDR8 [R/W] H,W 00000000 00000000		
$001AFC_H$	PTPC8 [R/W] H,W 00000000 00000000		—	—	
$001B00_H$	PCN9 [R/W] B,H,W 00000000 000000-0		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
$001B04_H$	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PTMR9 [R] H,W 11111111 11111111		
$001B08_H$	PCN209 [R/W] B,H,W --000000 -----110		PSDR9 [R/W] H,W 00000000 00000000		
$001B0C_H$	PTPC9 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001B10_H$	PCN10 [R/W] B,H,W 00000000 000000-0		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
$001B14_H$	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PTMR10 [R] H,W 11111111 11111111		
$001B18_H$	PCN210 [R/W] B,H,W --000000 -----110		PSDR10 [R/W] H,W 00000000 00000000		
$001B1C_H$	PTPC10 [R/W] H,W 00000000 00000000		—	—	
$001B20_H$	PCN11 [R/W] B,H,W 00000000 000000-0		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11
$001B24_H$	PDUT11 [W] H,W XXXXXXXX XXXXXXXX		PTMR11 [R] H,W 11111111 11111111		
$001B28_H$	PCN211 [R/W] B,H,W --000000 -----110		PSDR11 [R/W] H,W 00000000 00000000		
$001B2C_H$	PTPC11 [R/W] H,W 00000000 00000000		—	—	
$001B30_H$	PCN12 [R/W] B,H,W 00000000 000000-0		PCSR12 [W] H,W XXXXXXXX XXXXXXXX		PPG12
$001B34_H$	PDUT12 [W] H,W XXXXXXXX XXXXXXXX		PTMR12 [R] H,W 11111111 11111111		
$001B38_H$	PCN212 [R/W] B,H,W --000000 -----110		PSDR12 [R/W] H,W 00000000 00000000		
$001B3C_H$	PTPC12 [R/W] H,W 00000000 00000000		—	—	
$001B40_H$	PCN13 [R/W] B,H,W 00000000 000000-0		PCSR13 [W] H,W XXXXXXXX XXXXXXXX		PPG13
$001B44_H$	PDUT13 [W] H,W XXXXXXXX XXXXXXXX		PTMR13 [R] H,W 11111111 11111111		
$001B48_H$	PCN213 [R/W] B,H,W --000000 -----110		PSDR13 [R/W] H,W 00000000 00000000		
$001B4C_H$	PTPC13 [R/W] H,W 00000000 00000000		—	—	
$001B50_H$	PCN14 [R/W] B,H,W 00000000 000000-0		PCSR14 [W] H,W XXXXXXXX XXXXXXXX		PPG14
$001B54_H$	PDUT14 [W] H,W XXXXXXXX XXXXXXXX		PTMR14 [R] H,W 11111111 11111111		
$001B58_H$	PCN214 [R/W] B,H,W --000000 -----110		PSDR14 [R/W] H,W 00000000 00000000		
$001B5C_H$	PTPC14 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001B60_H$	PCN15 [R/W] B,H,W 00000000 000000-0		PCSR15 [W] H,W XXXXXXXX XXXXXXXX		PPG15
$001B64_H$	PDUT15 [W] H,W XXXXXXXX XXXXXXXX		PTMR15 [R] H,W 11111111 11111111		
$001B68_H$	PCN215 [R/W] B,H,W --000000 -----110		PSDR15 [R/W] H,W 00000000 00000000		
$001B6C_H$	PTPC15 [R/W] H,W 00000000 00000000		—	—	
$001B70_H$	PCN16 [R/W] B,H,W 00000000 000000-0		PCSR16 [W] H,W XXXXXXXX XXXXXXXX		PPG16
$001B74_H$	PDUT16 [W] H,W XXXXXXXX XXXXXXXX		PTMR16 [R] H,W 11111111 11111111		
$001B78_H$	PCN216 [R/W] B,H,W --000000 -----110		PSDR16 [R/W] H,W 00000000 00000000		
$001B7C_H$	PTPC16 [R/W] H,W 00000000 00000000		—	—	
$001B80_H$	PCN17 [R/W] B,H,W 00000000 000000-0		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
$001B84_H$	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PTMR17 [R] H,W 11111111 11111111		
$001B88_H$	PCN217 [R/W] B,H,W --000000 -----110		PSDR17 [R/W] H,W 00000000 00000000		
$001B8C_H$	PTPC17 [R/W] H,W 00000000 00000000		—	—	
$001B90_H$	PCN18 [R/W] B,H,W 00000000 000000-0		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
$001B94_H$	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PTMR18 [R] H,W 11111111 11111111		
$001B98_H$	PCN218 [R/W] B,H,W --000000 -----110		PSDR18 [R/W] H,W 00000000 00000000		
$001B9C_H$	PTPC18 [R/W] H,W 00000000 00000000		—	—	
$001BA0_H$	PCN19 [R/W] B,H,W 00000000 000000-0		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
$001BA4_H$	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PTMR19 [R] H,W 11111111 11111111		
$001BA8_H$	PCN219 [R/W] B,H,W --000000 -----110		PSDR19 [R/W] H,W 00000000 00000000		
$001BAC_H$	PTPC19 [R/W] H,W 00000000 00000000		—	—	
$001BB0_H$	PCN20 [R/W] B,H,W 00000000 000000-0		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
$001BB4_H$	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PTMR20 [R] H,W 11111111 11111111		
$001BB8_H$	PCN220 [R/W] B,H,W --000000 -----110		PSDR20 [R/W] H,W 00000000 00000000		
$001BBC_H$	PTPC20 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001BC0_H$	PCN21 [R/W] B,H,W 00000000 000000-0		PCSR21 [W] H,W XXXXXXXX XXXXXXXX		PPG21
$001BC4_H$	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PTMR21 [R] H,W 11111111 11111111		
$001BC8_H$	PCN221 [R/W] B,H,W --000000 -----110		PSDR21 [R/W] H,W 00000000 00000000		
$001BCC_H$	PTPC21 [R/W] H,W 00000000 00000000		—	—	
$001BD0_H$	PCN22 [R/W] B,H,W 00000000 000000-0		PCSR22 [W] H,W XXXXXXXX XXXXXXXX		PPG22
$001BD4_H$	PDUT22 [W] H,W XXXXXXXX XXXXXXXX		PTMR22 [R] H,W 11111111 11111111		
$001BD8_H$	PCN222 [R/W] B,H,W --000000 -----110		PSDR22 [R/W] H,W 00000000 00000000		
$001BDC_H$	PTPC22 [R/W] H,W 00000000 00000000		—	—	
$001BE0_H$	PCN23 [R/W] B,H,W 00000000 000000-0		PCSR23 [W] H,W XXXXXXXX XXXXXXXX		PPG23
$001BE4_H$	PDUT23 [W] H,W XXXXXXXX XXXXXXXX		PTMR23 [R] H,W 11111111 11111111		
$001BE8_H$	PCN223 [R/W] B,H,W --000000 -----110		PSDR23 [R/W] H,W 00000000 00000000		
$001BEC_H$	PTPC23 [R/W] H,W 00000000 00000000		—	—	
$001BF0_H$	PCN24 [R/W] B,H,W 00000000 000000-0		PCSR24 [W] H,W XXXXXXXX XXXXXXXX		PPG24
$001BF4_H$	PDUT24 [W] H,W XXXXXXXX XXXXXXXX		PTMR24 [R] H,W 11111111 11111111		
$001BF8_H$	PCN224 [R/W] B,H,W --000000 -----110		PSDR24 [R/W] H,W 00000000 00000000		
$001BFC_H$	PTPC24 [R/W] H,W 00000000 00000000		—	—	
$001C00_H$	PCN25 [R/W] B,H,W 00000000 000000-0		PCSR25 [W] H,W XXXXXXXX XXXXXXXX		PPG25
$001C04_H$	PDUT25 [W] H,W XXXXXXXX XXXXXXXX		PTMR25 [R] H,W 11111111 11111111		
$001C08_H$	PCN225 [R/W] B,H,W --000000 -----110		PSDR25 [R/W] H,W 00000000 00000000		
$001C0C_H$	PTPC25 [R/W] H,W 00000000 00000000		—	—	
$001C10_H$	PCN26 [R/W] B,H,W 00000000 000000-0		PCSR26 [W] H,W XXXXXXXX XXXXXXXX		PPG26
$001C14_H$	PDUT26 [W] H,W XXXXXXXX XXXXXXXX		PTMR26 [R] H,W 11111111 11111111		
$001C18_H$	PCN226 [R/W] B,H,W --000000 -----110		PSDR26 [R/W] H,W 00000000 00000000		
$001C1C_H$	PTPC26 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001C20_H$	PCN27 [R/W] B,H,W 00000000 000000-0		PCSR27 [W] H,W XXXXXXXX XXXXXXXX		PPG27
$001C24_H$	PDUT27 [W] H,W XXXXXXXX XXXXXXXX		PTMR27 [R] H,W 11111111 11111111		
$001C28_H$	PCN227 [R/W] B,H,W --000000 -----110		PSDR27 [R/W] H,W 00000000 00000000		
$001C2C_H$	PTPC27 [R/W] H,W 00000000 00000000		—	—	
$001C30_H$	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXX XXXXXXXX		PPG28
$001C34_H$	PDUT28 [W] H,W XXXXXXXX XXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
$001C38_H$	PCN228 [R/W] B,H,W --000000 -----110		PSDR28 [R/W] H,W 00000000 00000000		
$001C3C_H$	PTPC28 [R/W] H,W 00000000 00000000		—	—	
$001C40_H$	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXX XXXXXXXX		PPG29
$001C44_H$	PDUT29 [W] H,W XXXXXXXX XXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
$001C48_H$	PCN229 [R/W] B,H,W --000000 -----110		PSDR29 [R/W] H,W 00000000 00000000		
$001C4C_H$	PTPC29 [R/W] H,W 00000000 00000000		—	—	
$001C50_H$	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXX XXXXXXXX		PPG30
$001C54_H$	PDUT30 [W] H,W XXXXXXXX XXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
$001C58_H$	PCN230 [R/W] B,H,W --000000 -----110		PSDR30 [R/W] H,W 00000000 00000000		
$001C5C_H$	PTPC30 [R/W] H,W 00000000 00000000		—	—	
$001C60_H$	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXX XXXXXXXX		PPG31
$001C64_H$	PDUT31 [W] H,W XXXXXXXX XXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
$001C68_H$	PCN231 [R/W] B,H,W --000000 -----110		PSDR31 [R/W] H,W 00000000 00000000		
$001C6C_H$	PTPC31 [R/W] H,W 00000000 00000000		—	—	
$001C70_H$	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXX XXXXXXXX		PPG32
$001C74_H$	PDUT32 [W] H,W XXXXXXXX XXXXXXXX		PTMR32 [R] H,W 11111111 11111111		
$001C78_H$	PCN232 [R/W] B,H,W --000000 -----110		PSDR32 [R/W] H,W 00000000 00000000		
$001C7C_H$	PTPC32 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001C80_H$	PCN33 [R/W] B,H,W 00000000 000000-0		PCSR33 [W] H,W XXXXXXXX XXXXXXXX		PPG33
$001C84_H$	PDUT33 [W] H,W XXXXXXXX XXXXXXXX		PTMR33 [R] H,W 11111111 11111111		
$001C88_H$	PCN233 [R/W] B,H,W --000000 -----110		PSDR33 [R/W] H,W 00000000 00000000		
$001C8C_H$	PTPC33 [R/W] H,W 00000000 00000000		—	—	
$001C90_H$	PCN34 [R/W] B,H,W 00000000 000000-0		PCSR34 [W] H,W XXXXXXXX XXXXXXXX		PPG34
$001C94_H$	PDUT34 [W] H,W XXXXXXXX XXXXXXXX		PTMR34 [R] H,W 11111111 11111111		
$001C98_H$	PCN234 [R/W] B,H,W --000000 -----110		PSDR34 [R/W] H,W 00000000 00000000		
$001C9C_H$	PTPC34 [R/W] H,W 00000000 00000000		—	—	
$001CA0_H$	PCN35 [R/W] B,H,W 00000000 000000-0		PCSR35 [W] H,W XXXXXXXX XXXXXXXX		PPG35
$001CA4_H$	PDUT35 [W] H,W XXXXXXXX XXXXXXXX		PTMR35 [R] H,W 11111111 11111111		
$001CA8_H$	PCN235 [R/W] B,H,W --000000 -----110		PSDR35 [R/W] H,W 00000000 00000000		
$001CAC_H$	PTPC35 [R/W] H,W 00000000 00000000		—	—	
$001CB0_H$	PCN36 [R/W] B,H,W 00000000 000000-0		PCSR36 [W] H,W XXXXXXXX XXXXXXXX		PPG36
$001CB4_H$	PDUT36 [W] H,W XXXXXXXX XXXXXXXX		PTMR36 [R] H,W 11111111 11111111		
$001CB8_H$	PCN236 [R/W] B,H,W --000000 -----110		PSDR36 [R/W] H,W 00000000 00000000		
$001CBC_H$	PTPC36 [R/W] H,W 00000000 00000000		—	—	
$001CC0_H$	PCN37 [R/W] B,H,W 00000000 000000-0		PCSR37 [W] H,W XXXXXXXX XXXXXXXX		PPG37
$001CC4_H$	PDUT37 [W] H,W XXXXXXXX XXXXXXXX		PTMR37 [R] H,W 11111111 11111111		
$001CC8_H$	PCN237 [R/W] B,H,W --000000 -----110		PSDR37 [R/W] H,W 00000000 00000000		
$001CCC_H$	PTPC37 [R/W] H,W 00000000 00000000		—	—	
$001CD0_H$	PCN38 [R/W] B,H,W 00000000 000000-0		PCSR38 [W] H,W XXXXXXXX XXXXXXXX		PPG38
$001CD4_H$	PDUT38 [W] H,W XXXXXXXX XXXXXXXX		PTMR38 [R] H,W 11111111 11111111		
$001CD8_H$	PCN238 [R/W] B,H,W --000000 -----110		PSDR38 [R/W] H,W 00000000 00000000		
$001CDC_H$	PTPC38 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001CE0$_H$	PCN39 [R/W] B,H,W 00000000 000000-0		PCSR39 [W] H,W XXXXXXXX XXXXXXXX		PPG39
001CE4$_H$	PDUT39 [W] H,W XXXXXXXX XXXXXXXX		PTMR39 [R] H,W 11111111 11111111		
001CE8$_H$	PCN239 [R/W] B,H,W --000000 -----110		PSDR39 [R/W] H,W 00000000 00000000		
001CEC$_H$	PTPC39 [R/W] H,W 00000000 00000000		—	—	
001CF0$_H$	PCN40 [R/W] B,H,W 00000000 000000-0		PCSR40 [W] H,W XXXXXXXX XXXXXXXX		PPG40
001CF4$_H$	PDUT40 [W] H,W XXXXXXXX XXXXXXXX		PTMR40 [R] H,W 11111111 11111111		
001CF8$_H$	PCN240 [R/W] B,H,W --000000 -----110		PSDR40 [R/W] H,W 00000000 00000000		
001CFC$_H$	PTPC40 [R/W] H,W 00000000 00000000		—	—	
001D00$_H$	PCN41 [R/W] B,H,W 00000000 000000-0		PCSR41 [W] H,W XXXXXXXX XXXXXXXX		PPG41
001D04$_H$	PDUT41 [W] H,W XXXXXXXX XXXXXXXX		PTMR41 [R] H,W 11111111 11111111		
001D08$_H$	PCN241 [R/W] B,H,W --000000 -----110		PSDR41 [R/W] H,W 00000000 00000000		
001D0C$_H$	PTPC41 [R/W] H,W 00000000 00000000		—	—	
001D10$_H$	PCN42 [R/W] B,H,W 00000000 000000-0		PCSR42 [W] H,W XXXXXXXX XXXXXXXX		PPG42
001D14$_H$	PDUT42 [W] H,W XXXXXXXX XXXXXXXX		PTMR42 [R] H,W 11111111 11111111		
001D18$_H$	PCN242 [R/W] B,H,W --000000 -----110		PSDR42 [R/W] H,W 00000000 00000000		
001D1C$_H$	PTPC42 [R/W] H,W 00000000 00000000		—	—	
001D20$_H$	PCN43 [R/W] B,H,W 00000000 000000-0		PCSR43 [W] H,W XXXXXXXX XXXXXXXX		PPG43
001D24$_H$	PDUT43 [W] H,W XXXXXXXX XXXXXXXX		PTMR43 [R] H,W 11111111 11111111		
001D28$_H$	PCN243 [R/W] B,H,W --000000 -----110		PSDR43 [R/W] H,W 00000000 00000000		
001D2C$_H$	PTPC43 [R/W] H,W 00000000 00000000		—	—	
001D30$_H$	PCN44 [R/W] B,H,W 00000000 000000-0		PCSR44 [W] H,W XXXXXXXX XXXXXXXX		PPG44
001D34$_H$	PDUT44 [W] H,W XXXXXXXX XXXXXXXX		PTMR44 [R] H,W 11111111 11111111		
001D38$_H$	PCN244 [R/W] B,H,W --000000 -----110		PSDR44 [R/W] H,W 00000000 00000000		
001D3C$_H$	PTPC44 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001D40$_H$	PCN45 [R/W] B,H,W 00000000 000000-0		PCSR45 [W] H,W XXXXXXXX XXXXXXXX		PPG45
001D44$_H$	PDUT45 [W] H,W XXXXXXXX XXXXXXXX		PTMR45 [R] H,W 11111111 11111111		
001D48$_H$	PCN245 [R/W] B,H,W --000000 -----110		PSDR45 [R/W] H,W 00000000 00000000		
001D4C$_H$	PTPC45 [R/W] H,W 00000000 00000000		—	—	
001D50$_H$	PCN46 [R/W] B,H,W 00000000 000000-0		PCSR46 [W] H,W XXXXXXXX XXXXXXXX		PPG46
001D54$_H$	PDUT46 [W] H,W XXXXXXXX XXXXXXXX		PTMR46 [R] H,W 11111111 11111111		
001D58$_H$	PCN246 [R/W] B,H,W --000000 -----110		PSDR46 [R/W] H,W 00000000 00000000		
001D5C$_H$	PTPC46 [R/W] H,W 00000000 00000000		—	—	
001D60$_H$	PCN47 [R/W] B,H,W 00000000 000000-0		PCSR47 [W] H,W XXXXXXXX XXXXXXXX		PPG47
001D64$_H$	PDUT47 [W] H,W XXXXXXXX XXXXXXXX		PTMR47 [R] H,W 11111111 11111111		
001D68$_H$	PCN247 [R/W] B,H,W --000000 -----110		PSDR47 [R/W] H,W 00000000 00000000		
001D6C$_H$	PTPC47 [R/W] H,W 00000000 00000000		—	—	
001D70$_H$	PCN48 [R/W] B,H,W 00000000 000000-0		PCSR48 [W] H,W XXXXXXXX XXXXXXXX		PPG48
001D74$_H$	PDUT48 [W] H,W XXXXXXXX XXXXXXXX		PTMR48 [R] H,W 11111111 11111111		
001D78$_H$	PCN248 [R/W] B,H,W --000000 -----110		PSDR48 [R/W] H,W 00000000 00000000		
001D7C$_H$	PTPC48 [R/W] H,W 00000000 00000000		—	—	
001D80$_H$	PCN49 [R/W] B,H,W 00000000 000000-0		PCSR49 [W] H,W XXXXXXXX XXXXXXXX		PPG49
001D84$_H$	PDUT49 [W] H,W XXXXXXXX XXXXXXXX		PTMR49 [R] H,W 11111111 11111111		
001D88$_H$	PCN249 [R/W] B,H,W --000000 -----110		PSDR49 [R/W] H,W 00000000 00000000		
001D8C$_H$	PTPC49 [R/W] H,W 00000000 00000000		—	—	
001D90$_H$	PCN50 [R/W] B,H,W 00000000 000000-0		PCSR50 [W] H,W XXXXXXXX XXXXXXXX		PPG50
001D94$_H$	PDUT50 [W] H,W XXXXXXXX XXXXXXXX		PTMR50 [R] H,W 11111111 11111111		
001D98$_H$	PCN250 [R/W] B,H,W --000000 -----110		PSDR50 [R/W] H,W 00000000 00000000		
001D9C$_H$	PTPC50 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001DA0$_H$	PCN51 [R/W] B,H,W 00000000 000000-0		PCSR51 [W] H,W XXXXXXXX XXXXXXXX		PPG51
001DA4$_H$	PDUT51 [W] H,W XXXXXXXX XXXXXXXX		PTMR51 [R] H,W 11111111 11111111		
001DA8$_H$	PCN251 [R/W] B,H,W --000000 -----110		PSDR51 [R/W] H,W 00000000 00000000		
001DAC$_H$	PTPC51 [R/W] H,W 00000000 00000000		—	—	
001DB0$_H$	PCN52 [R/W] B,H,W 00000000 000000-0		PCSR52 [W] H,W XXXXXXXX XXXXXXXX		PPG52
001DB4$_H$	PDUT52 [W] H,W XXXXXXXX XXXXXXXX		PTMR52 [R] H,W 11111111 11111111		
001DB8$_H$	PCN252 [R/W] B,H,W --000000 -----110		PSDR52 [R/W] H,W 00000000 00000000		
001DBC$_H$	PTPC52 [R/W] H,W 00000000 00000000		—	—	
001DC0$_H$	PCN53 [R/W] B,H,W 00000000 000000-0		PCSR53 [W] H,W XXXXXXXX XXXXXXXX		PPG53
001DC4$_H$	PDUT53 [W] H,W XXXXXXXX XXXXXXXX		PTMR53 [R] H,W 11111111 11111111		
001DC8$_H$	PCN253 [R/W] B,H,W --000000 -----110		PSDR53 [R/W] H,W 00000000 00000000		
001DCC$_H$	PTPC53 [R/W] H,W 00000000 00000000		—	—	
001DD0$_H$	PCN54 [R/W] B,H,W 00000000 000000-0		PCSR54 [W] H,W XXXXXXXX XXXXXXXX		PPG54
001DD4$_H$	PDUT54 [W] H,W XXXXXXXX XXXXXXXX		PTMR54 [R] H,W 11111111 11111111		
001DD8$_H$	PCN254 [R/W] B,H,W --000000 -----110		PSDR54 [R/W] H,W 00000000 00000000		
001DDC$_H$	PTPC54 [R/W] H,W 00000000 00000000		—	—	
001DE0$_H$	PCN55 [R/W] B,H,W 00000000 000000-0		PCSR55 [W] H,W XXXXXXXX XXXXXXXX		PPG55
001DE4$_H$	PDUT55 [W] H,W XXXXXXXX XXXXXXXX		PTMR55 [R] H,W 11111111 11111111		
001DE8$_H$	PCN255 [R/W] B,H,W --000000 -----110		PSDR55 [R/W] H,W 00000000 00000000		
001DEC$_H$	PTPC55 [R/W] H,W 00000000 00000000		—	—	
001DF0$_H$	PCN56 [R/W] B,H,W 00000000 000000-0		PCSR56 [W] H,W XXXXXXXX XXXXXXXX		PPG56
001DF4$_H$	PDUT56 [W] H,W XXXXXXXX XXXXXXXX		PTMR56 [R] H,W 11111111 11111111		
001DF8$_H$	PCN256 [R/W] B,H,W --000000 -----110		PSDR56 [R/W] H,W 00000000 00000000		
001DFC$_H$	PTPC56 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001E00_H$	PCN57 [R/W] B,H,W 00000000 000000-0		PCSR57 [W] H,W XXXXXXXX XXXXXXXX		PPG57
$001E04_H$	PDUT57 [W] H,W XXXXXXXX XXXXXXXX		PTMR57 [R] H,W 11111111 11111111		
$001E08_H$	PCN257 [R/W] B,H,W --000000 -----110		PSDR57 [R/W] H,W 00000000 00000000		
$001E0C_H$	PTPC57 [R/W] H,W 00000000 00000000		—	—	
$001E10_H$	PCN58 [R/W] B,H,W 00000000 000000-0		PCSR58 [W] H,W XXXXXXXX XXXXXXXX		PPG58
$001E14_H$	PDUT58 [W] H,W XXXXXXXX XXXXXXXX		PTMR58 [R] H,W 11111111 11111111		
$001E18_H$	PCN258 [R/W] B,H,W --000000 -----110		PSDR58 [R/W] H,W 00000000 00000000		
$001E1C_H$	PTPC58 [R/W] H,W 00000000 00000000		—	—	
$001E20_H$	PCN59 [R/W] B,H,W 00000000 000000-0		PCSR59 [W] H,W XXXXXXXX XXXXXXXX		PPG59
$001E24_H$	PDUT59 [W] H,W XXXXXXXX XXXXXXXX		PTMR59 [R] H,W 11111111 11111111		
$001E28_H$	PCN259 [R/W] B,H,W --000000 -----110		PSDR59 [R/W] H,W 00000000 00000000		
$001E2C_H$	PTPC59 [R/W] H,W 00000000 00000000		—	—	
$001E30_H$	PCN60 [R/W] B,H,W 00000000 000000-0		PCSR60 [W] H,W XXXXXXXX XXXXXXXX		PPG60
$001E34_H$	PDUT60 [W] H,W XXXXXXXX XXXXXXXX		PTMR60 [R] H,W 11111111 11111111		
$001E38_H$	PCN260 [R/W] B,H,W --000000 -----110		PSDR60 [R/W] H,W 00000000 00000000		
$001E3C_H$	PTPC60 [R/W] H,W 00000000 00000000		—	—	
$001E40_H$	PCN61 [R/W] B,H,W 00000000 000000-0		PCSR61 [W] H,W XXXXXXXX XXXXXXXX		PPG61
$001E44_H$	PDUT61 [W] H,W XXXXXXXX XXXXXXXX		PTMR61 [R] H,W 11111111 11111111		
$001E48_H$	PCN261 [R/W] B,H,W --000000 -----110		PSDR61 [R/W] H,W 00000000 00000000		
$001E4C_H$	PTPC61 [R/W] H,W 00000000 00000000		—	—	
$001E50_H$	PCN62 [R/W] B,H,W 00000000 000000-0		PCSR62 [W] H,W XXXXXXXX XXXXXXXX		PPG62
$001E54_H$	PDUT62 [W] H,W XXXXXXXX XXXXXXXX		PTMR62 [R] H,W 11111111 11111111		
$001E58_H$	PCN262 [R/W] B,H,W --000000 -----110		PSDR62 [R/W] H,W 00000000 00000000		
$001E5C_H$	PTPC62 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001E60_H$	PCN63 [R/W] B,H,W 00000000 000000-0		PCSR63 [W] H,W XXXXXXXX XXXXXXXX		PPG63
$001E64_H$	PDUT63 [W] H,W XXXXXXXX XXXXXXXX		PTMR63 [R] H,W 11111111 11111111		
$001E68_H$	PCN263 [R/W] B,H,W --000000 -----110		PSDR63 [R/W] H,W 00000000 00000000		
$001E6C_H$	PTPC63 [R/W] H,W 00000000 00000000		—	—	
$001E70_H$	PCN64 [R/W] B,H,W 00000000 000000-0		PCSR64 [W] H,W XXXXXXXX XXXXXXXX		PPG64
$001E74_H$	PDUT64 [W] H,W XXXXXXXX XXXXXXXX		PTMR64 [R] H,W 11111111 11111111		
$001E78_H$	PCN264 [R/W] B,H,W --000000 -----110		PSDR64 [R/W] H,W 00000000 00000000		
$001E7C_H$	PTPC64 [R/W] H,W 00000000 00000000		—	—	
$001E80_H$	PCN65 [R/W] B,H,W 00000000 000000-0		PCSR65 [W] H,W XXXXXXXX XXXXXXXX		PPG65
$001E84_H$	PDUT65 [W] H,W XXXXXXXX XXXXXXXX		PTMR65 [R] H,W 11111111 11111111		
$001E88_H$	PCN265 [R/W] B,H,W --000000 -----110		PSDR65 [R/W] H,W 00000000 00000000		
$001E8C_H$	PTPC65 [R/W] H,W 00000000 00000000		—	—	
$001E90_H$	PCN66 [R/W] B,H,W 00000000 000000-0		PCSR66 [W] H,W XXXXXXXX XXXXXXXX		PPG66
$001E94_H$	PDUT66 [W] H,W XXXXXXXX XXXXXXXX		PTMR66 [R] H,W 11111111 11111111		
$001E98_H$	PCN266 [R/W] B,H,W --000000 -----110		PSDR66 [R/W] H,W 00000000 00000000		
$001E9C_H$	PTPC66 [R/W] H,W 00000000 00000000		—	—	
$001EA0_H$	PCN67 [R/W] B,H,W 00000000 000000-0		PCSR67 [W] H,W XXXXXXXX XXXXXXXX		PPG67
$001EA4_H$	PDUT67 [W] H,W XXXXXXXX XXXXXXXX		PTMR67 [R] H,W 11111111 11111111		
$001EA8_H$	PCN267 [R/W] B,H,W --000000 -----110		PSDR67 [R/W] H,W 00000000 00000000		
$001EAC_H$	PTPC67 [R/W] H,W 00000000 00000000		—	—	
$001EB0_H$	PCN68 [R/W] B,H,W 00000000 000000-0		PCSR68 [W] H,W XXXXXXXX XXXXXXXX		PPG68
$001EB4_H$	PDUT68 [W] H,W XXXXXXXX XXXXXXXX		PTMR68 [R] H,W 11111111 11111111		
$001EB8_H$	PCN268 [R/W] B,H,W --000000 -----110		PSDR68 [R/W] H,W 00000000 00000000		
$001EBC_H$	PTPC68 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001EC0_H$	PCN69 [R/W] B,H,W 00000000 000000-0		PCSR69 [W] H,W XXXXXXXX XXXXXXXX		PPG69
$001EC4_H$	PDUT69 [W] H,W XXXXXXXX XXXXXXXX		PTMR69 [R] H,W 11111111 11111111		
$001EC8_H$	PCN269 [R/W] B,H,W --000000 -----110		PSDR69 [R/W] H,W 00000000 00000000		
$001ECC_H$	PTPC69 [R/W] H,W 00000000 00000000		—	—	
$001ED0_H$	PCN70 [R/W] B,H,W 00000000 000000-0		PCSR70 [W] H,W XXXXXXXX XXXXXXXX		PPG70
$001ED4_H$	PDUT70 [W] H,W XXXXXXXX XXXXXXXX		PTMR70 [R] H,W 11111111 11111111		
$001ED8_H$	PCN270 [R/W] B,H,W --000000 -----110		PSDR70 [R/W] H,W 00000000 00000000		
$001EDC_H$	PTPC70 [R/W] H,W 00000000 00000000		—	—	
$001EE0_H$	PCN71 [R/W] B,H,W 00000000 000000-0		PCSR71 [W] H,W XXXXXXXX XXXXXXXX		PPG71
$001EE4_H$	PDUT71 [W] H,W XXXXXXXX XXXXXXXX		PTMR71 [R] H,W 11111111 11111111		
$001EE8_H$	PCN271 [R/W] B,H,W --000000 -----110		PSDR71 [R/W] H,W 00000000 00000000		
$001EEC_H$	PTPC71 [R/W] H,W 00000000 00000000		—	—	
$001EF0_H$	PCN72 [R/W] B,H,W 00000000 000000-0		PCSR72 [W] H,W XXXXXXXX XXXXXXXX		PPG72
$001EF4_H$	PDUT72 [W] H,W XXXXXXXX XXXXXXXX		PTMR72 [R] H,W 11111111 11111111		
$001EF8_H$	PCN272 [R/W] B,H,W --000000 -----110		PSDR72 [R/W] H,W 00000000 00000000		
$001EFC_H$	PTPC72 [R/W] H,W 00000000 00000000		—	—	
$001F00_H$	PCN73 [R/W] B,H,W 00000000 000000-0		PCSR73 [W] H,W XXXXXXXX XXXXXXXX		PPG73
$001F04_H$	PDUT73 [W] H,W XXXXXXXX XXXXXXXX		PTMR73 [R] H,W 11111111 11111111		
$001F08_H$	PCN273 [R/W] B,H,W --000000 -----110		PSDR73 [R/W] H,W 00000000 00000000		
$001F0C_H$	PTPC73 [R/W] H,W 00000000 00000000		—	—	
$001F10_H$	PCN74 [R/W] B,H,W 00000000 000000-0		PCSR74 [W] H,W XXXXXXXX XXXXXXXX		PPG74
$001F14_H$	PDUT74 [W] H,W XXXXXXXX XXXXXXXX		PTMR74 [R] H,W 11111111 11111111		
$001F18_H$	PCN274 [R/W] B,H,W --000000 -----110		PSDR74 [R/W] H,W 00000000 00000000		
$001F1C_H$	PTPC74 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001F20_H$	PCN75 [R/W] B,H,W 00000000 000000-0		PCSR75 [W] H,W XXXXXXXX XXXXXXXX		PPG75
$001F24_H$	PDUT75 [W] H,W XXXXXXXX XXXXXXXX		PTMR75 [R] H,W 11111111 11111111		
$001F28_H$	PCN275 [R/W] B,H,W --000000 -----110		PSDR75 [R/W] H,W 00000000 00000000		
$001F2C_H$	PTPC75 [R/W] H,W 00000000 00000000		—	—	
$001F30_H$	PCN76 [R/W] B,H,W 00000000 000000-0		PCSR76 [W] H,W XXXXXXXX XXXXXXXX		PPG76
$001F34_H$	PDUT76 [W] H,W XXXXXXXX XXXXXXXX		PTMR76 [R] H,W 11111111 11111111		
$001F38_H$	PCN276 [R/W] B,H,W --000000 -----110		PSDR76 [R/W] H,W 00000000 00000000		
$001F3C_H$	PTPC76 [R/W] H,W 00000000 00000000		—	—	
$001F40_H$	PCN77 [R/W] B,H,W 00000000 000000-0		PCSR77 [W] H,W XXXXXXXX XXXXXXXX		PPG77
$001F44_H$	PDUT77 [W] H,W XXXXXXXX XXXXXXXX		PTMR77 [R] H,W 11111111 11111111		
$001F48_H$	PCN277 [R/W] B,H,W --000000 -----110		PSDR77 [R/W] H,W 00000000 00000000		
$001F4C_H$	PTPC77 [R/W] H,W 00000000 00000000		—	—	
$001F50_H$	PCN78 [R/W] B,H,W 00000000 000000-0		PCSR78 [W] H,W XXXXXXXX XXXXXXXX		PPG78
$001F54_H$	PDUT78 [W] H,W XXXXXXXX XXXXXXXX		PTMR78 [R] H,W 11111111 11111111		
$001F58_H$	PCN278 [R/W] B,H,W --000000 -----110		PSDR78 [R/W] H,W 00000000 00000000		
$001F5C_H$	PTPC78 [R/W] H,W 00000000 00000000		—	—	
$001F60_H$	PCN79 [R/W] B,H,W 00000000 000000-0		PCSR79 [W] H,W XXXXXXXX XXXXXXXX		PPG79
$001F64_H$	PDUT79 [W] H,W XXXXXXXX XXXXXXXX		PTMR79 [R] H,W 11111111 11111111		
$001F68_H$	PCN279 [R/W] B,H,W --000000 -----110		PSDR79 [R/W] H,W 00000000 00000000		
$001F6C_H$	PTPC79 [R/W] H,W 00000000 00000000		—	—	
$001F70_H$	PCN80 [R/W] B,H,W 00000000 000000-0		PCSR80 [W] H,W XXXXXXXX XXXXXXXX		PPG80
$001F74_H$	PDUT80 [W] H,W XXXXXXXX XXXXXXXX		PTMR80 [R] H,W 11111111 11111111		
$001F78_H$	PCN280 [R/W] B,H,W --000000 -----110		PSDR80 [R/W] H,W 00000000 00000000		
$001F7C_H$	PTPC80 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001F80_H$	PCN81 [R/W] B,H,W 00000000 000000-0		PCSR81 [W] H,W XXXXXXXX XXXXXXXX		PPG81
$001F84_H$	PDUT81 [W] H,W XXXXXXXX XXXXXXXX		PTMR81 [R] H,W 11111111 11111111		
$001F88_H$	PCN281 [R/W] B,H,W --000000 -----110		PSDR81 [R/W] H,W 00000000 00000000		
$001F8C_H$	PTPC81 [R/W] H,W 00000000 00000000		—	—	
$001F90_H$	PCN82 [R/W] B,H,W 00000000 000000-0		PCSR82 [W] H,W XXXXXXXX XXXXXXXX		PPG82
$001F94_H$	PDUT82 [W] H,W XXXXXXXX XXXXXXXX		PTMR82 [R] H,W 11111111 11111111		
$001F98_H$	PCN282 [R/W] B,H,W --000000 -----110		PSDR82 [R/W] H,W 00000000 00000000		
$001F9C_H$	PTPC82 [R/W] H,W 00000000 00000000		—	—	
$001FA0_H$	PCN83 [R/W] B,H,W 00000000 000000-0		PCSR83 [W] H,W XXXXXXXX XXXXXXXX		PPG83
$001FA4_H$	PDUT83 [W] H,W XXXXXXXX XXXXXXXX		PTMR83 [R] H,W 11111111 11111111		
$001FA8_H$	PCN283 [R/W] B,H,W --000000 -----110		PSDR83 [R/W] H,W 00000000 00000000		
$001FAC_H$	PTPC83 [R/W] H,W 00000000 00000000		—	—	
$001FB0_H$	PCN84 [R/W] B,H,W 00000000 000000-0		PCSR84 [W] H,W XXXXXXXX XXXXXXXX		PPG84
$001FB4_H$	PDUT84 [W] H,W XXXXXXXX XXXXXXXX		PTMR84 [R] H,W 11111111 11111111		
$001FB8_H$	PCN284 [R/W] B,H,W --000000 -----110		PSDR84 [R/W] H,W 00000000 00000000		
$001FBC_H$	PTPC84 [R/W] H,W 00000000 00000000		—	—	
$001FC0_H$	PCN85 [R/W] B,H,W 00000000 000000-0		PCSR85 [W] H,W XXXXXXXX XXXXXXXX		PPG85
$001FC4_H$	PDUT85 [W] H,W XXXXXXXX XXXXXXXX		PTMR85 [R] H,W 11111111 11111111		
$001FC8_H$	PCN285 [R/W] B,H,W --000000 -----110		PSDR85 [R/W] H,W 00000000 00000000		
$001FCC_H$	PTPC85 [R/W] H,W 00000000 00000000		—	—	
$001FD0_H$	PCN86 [R/W] B,H,W 00000000 000000-0		PCSR86 [W] H,W XXXXXXXX XXXXXXXX		PPG86
$001FD4_H$	PDUT86 [W] H,W XXXXXXXX XXXXXXXX		PTMR86 [R] H,W 11111111 11111111		
$001FD8_H$	PCN286 [R/W] B,H,W --000000 -----110		PSDR86 [R/W] H,W 00000000 00000000		
$001FDC_H$	PTPC86 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001FE0_H$	PCN87 [R/W] B,H,W 00000000 000000-0		PCSR87 [W] H,W XXXXXXXX XXXXXXXX		PPG87
$001FE4_H$	PDUT87 [W] H,W XXXXXXXX XXXXXXXX		PTMR87 [R] H,W 11111111 11111111		
$001FE8_H$	PCN287 [R/W] B,H,W --000000 -----110		PSDR87 [R/W] H,W 00000000 00000000		
$001FEC_H$	PTPC87 [R/W] H,W 00000000 00000000		—	—	
$001FF0_H$ to $001FFC_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002000_H	CTRLR0 [R/W] B,H,W -------- 000-0001		STATR0 [R/W] B,H,W -------- 00000000		CAN0 (128msb)
002004_H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0 [R/W] B,H,W -0100011 00000001		
002008_H	INTR0 [R] B,H,W 00000000 00000000		TESTR0 [R/W] B,H,W -------- X00000--		
$00200C_H$	BRPER0 [R/W] B,H,W -------- ----0000		—	—	
002010_H	IF1CREQ0 [R/W] B,H,W 0------- 00000001		IF1CMSK0 [R/W] B,H,W -------- 00000000		
002014_H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018_H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
$00201C_H$	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002020_H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20 [R/W] B,H,W 00000000 00000000		
002024_H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028_H	—	—	—	—	
$00202C_H$	—	—	—	—	
002030_H, 002034_H	Reserved (IF1 data mirror)				
002038_H	—	—	—	—	
$00203C_H$	—	—	—	—	
002040_H	IF2CREQ0 [R/W] B,H,W 0------- 00000001		IF2CMSK0 [R/W] B,H,W -------- 00000000		
002044_H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048_H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
$00204C_H$	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002050_H	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		
002054_H	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
002058_H	—	—	—	—	
$00205C_H$	—	—	—	—	
002060_H, 002064_H	Reserved (IF2 data mirror)				
002068_H to $00207C_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002080_H	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		CAN0 (128msb)
002084_H	TREQR40 [R] B,H,W 00000000 00000000		TREQR30 [R] B,H,W 00000000 00000000		
002088_H	TREQR60 [R] B,H,W 00000000 00000000		TREQR50 [R] B,H,W 00000000 00000000		
$00208C_H$	TREQR80 [R] B,H,W 00000000 00000000		TREQR70 [R] B,H,W 00000000 00000000		
002090_H	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
002094_H	NEWDT40 [R] B,H,W 00000000 00000000		NEWDT30 [R] B,H,W 00000000 00000000		
002098_H	NEWDT60 [R] B,H,W 00000000 00000000		NEWDT50 [R] B,H,W 00000000 00000000		
$00209C_H$	NEWDT80 [R] B,H,W 00000000 00000000		NEWDT70 [R] B,H,W 00000000 00000000		
$0020A0_H$	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		
$0020A4_H$	INTPND40 [R] B,H,W 00000000 00000000		INTPND30 [R] B,H,W 00000000 00000000		
$0020A8_H$	INTPND60 [R] B,H,W 00000000 00000000		INTPND50 [R] B,H,W 00000000 00000000		
$0020AC_H$	INTPND80 [R] B,H,W 00000000 00000000		INTPND70 [R] B,H,W 00000000 00000000		
$0020B0_H$	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
$0020B4_H$	MSGVAL40 [R] B,H,W 00000000 00000000		MSGVAL30 [R] B,H,W 00000000 00000000		
$0020B8_H$	MSGVAL60 [R] B,H,W 00000000 00000000		MSGVAL50 [R] B,H,W 00000000 00000000		
$0020BC_H$	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		
$0020C0_H$ to $0020FC_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002100_H	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN1 (128msb)
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108_H	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110_H	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114_H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118_H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120_H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128_H	—	—	—	—	
$00212C_H$	—	—	—	—	
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H	—	—	—	—	
$00213C_H$	—	—	—	—	
002140_H	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144_H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
$00214C_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002150_H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		
002154_H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158_H	—	—	—	—	
$00215C_H$	—	—	—	—	
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H to $00217C_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002180_H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		CAN1 (128msb)
002184_H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000		
002188_H	TREQR61 [R] B,H,W 00000000 00000000		TREQR51 [R] B,H,W 00000000 00000000		
$00218C_H$	TREQR81 [R] B,H,W 00000000 00000000		TREQR71 [R] B,H,W 00000000 00000000		
002190_H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194_H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000		
002198_H	NEWDT61 [R] B,H,W 00000000 00000000		NEWDT51 [R] B,H,W 00000000 00000000		
$00219C_H$	NEWDT81 [R] B,H,W 00000000 00000000		NEWDT71 [R] B,H,W 00000000 00000000		
$0021A0_H$	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000		
$0021A8_H$	INTPND61 [R] B,H,W 00000000 00000000		INTPND51 [R] B,H,W 00000000 00000000		
$0021AC_H$	INTPND81 [R] B,H,W 00000000 00000000		INTPND71 [R] B,H,W 00000000 00000000		
$0021B0_H$	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
$0021B4_H$	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000		
$0021B8_H$	MSGVAL61 [R] B,H,W 00000000 00000000		MSGVAL51 [R] B,H,W 00000000 00000000		
$0021BC_H$	MSGVAL81 [R] B,H,W 00000000 00000000		MSGVAL71 [R] B,H,W 00000000 00000000		
$0021C0_H$ to $0021FC_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002200_H	CTRLR2 [R/W] B,H,W -------- 000-0001		STATR2 [R/W] B,H,W -------- 00000000		CAN2 (128msb)
002204_H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2 [R/W] B,H,W -0100011 00000001		
002208_H	INTR2 [R] B,H,W 00000000 00000000		TESTR2 [R/W] B,H,W -------- X00000--		
$00220C_H$	BRPER2 [R/W] B,H,W -------- ----0000		—		
002210_H	IF1CREQ2 [R/W] B,H,W 0------- 00000001		IF1CMSK2 [R/W] B,H,W -------- 00000000		
002214_H	IF1MSK22 [R/W] B,H,W 11-11111 11111111		IF1MSK12 [R/W] B,H,W 11111111 11111111		
002218_H	IF1ARB22 [R/W] B,H,W 00000000 00000000		IF1ARB12 [R/W] B,H,W 00000000 00000000		
$00221C_H$	IF1MCTR2 [R/W] B,H,W 00000000 0---0000		—		
002220_H	IF1DTA12 [R/W] B,H,W 00000000 00000000		IF1DTA22 [R/W] B,H,W 00000000 00000000		
002224_H	IF1DTB12 [R/W] B,H,W 00000000 00000000		IF1DTB22 [R/W] B,H,W 00000000 00000000		
002228_H	—	—	—	—	
$00222C_H$	—	—	—	—	
002230_H, 002234_H	Reserved (IF1 data mirror)				
002238_H	—	—	—	—	
$00223C_H$	—	—	—	—	
002240_H	IF2CREQ2 [R/W] B,H,W 0------- 00000001		IF2CMSK2 [R/W] B,H,W -------- 00000000		
002244_H	IF2MSK22 [R/W] B,H,W 11-11111 11111111		IF2MSK12 [R/W] B,H,W 11111111 11111111		
002248_H	IF2ARB22 [R/W] B,H,W 00000000 00000000		IF2ARB12 [R/W] B,H,W 00000000 00000000		
$00224C_H$	IF2MCTR2 [R/W] B,H,W 00000000 0---0000		—		
002250_H	IF2DTA12 [R/W] B,H,W 00000000 00000000		IF2DTA22 [R/W] B,H,W 00000000 00000000		
002254_H	IF2DTB12 [R/W] B,H,W 00000000 00000000		IF2DTB22 [R/W] B,H,W 00000000 00000000		
002258_H	—	—	—	—	
$00225C_H$	—	—	—	—	
002260_H, 002264_H	Reserved (IF2 data mirror)				
002268_H to $00227C_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002280_H	TREQR22 [R] B,H,W 00000000 00000000		TREQR12 [R] B,H,W 00000000 00000000		CAN2 (128msb)
002284_H	TREQR42 [R] B,H,W 00000000 00000000		TREQR32 [R] B,H,W 00000000 00000000		
002288_H	TREQR62 [R] B,H,W 00000000 00000000		TREQR52 [R] B,H,W 00000000 00000000		
$00228C_H$	TREQR82 [R] B,H,W 00000000 00000000		TREQR72 [R] B,H,W 00000000 00000000		
002290_H	NEWDT22 [R] B,H,W 00000000 00000000		NEWDT12 [R] B,H,W 00000000 00000000		
002294_H	NEWDT42 [R] B,H,W 00000000 00000000		NEWDT32 [R] B,H,W 00000000 00000000		
002298_H	NEWDT62 [R] B,H,W 00000000 00000000		NEWDT52 [R] B,H,W 00000000 00000000		
$00229C_H$	NEWDT82 [R] B,H,W 00000000 00000000		NEWDT72 [R] B,H,W 00000000 00000000		
$0022A0_H$	INTPND22 [R] B,H,W 00000000 00000000		INTPND12 [R] B,H,W 00000000 00000000		
$0022A4_H$	INTPND42 [R] B,H,W 00000000 00000000		INTPND32 [R] B,H,W 00000000 00000000		
$0022A8_H$	INTPND62 [R] B,H,W 00000000 00000000		INTPND52 [R] B,H,W 00000000 00000000		
$0022AC_H$	INTPND82 [R] B,H,W 00000000 00000000		INTPND72 [R] B,H,W 00000000 00000000		
$0022B0_H$	MSGVAL22 [R] B,H,W 00000000 00000000		MSGVAL12 [R] B,H,W 00000000 00000000		
$0022B4_H$	MSGVAL42 [R] B,H,W 00000000 00000000		MSGVAL32 [R] B,H,W 00000000 00000000		
$0022B8_H$	MSGVAL62 [R] B,H,W 00000000 00000000		MSGVAL52 [R] B,H,W 00000000 00000000		
$0022BC_H$	MSGVAL82 [R] B,H,W 00000000 00000000		MSGVAL72 [R] B,H,W 00000000 00000000		
$0022C0_H$ to $0022FC_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002300_H	DFCTLR [R/W] B,H,W -0------ --------		—	DFSTR [R/W] B,H,W -----001	WorkFlash
002304_H	—	—	—	—	
002308_H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W --------	FLIFFER2 [R/W] B,H,W --------	Flash / WorkFlash
$00230C_H$	—				Reserved
002310_H	TRCR [R/W] B,H,W 00000000	TRAR [R/W] B,H,W 00000000	—		TuningRAM
002314_H to $0023FC_H$	—				Reserved
002400_H	SEEARX [R] B,H,W 00000000 00000000		DEEARX [R] B,H,W 00000000 00000000		XBS RAM ECC control
002404_H	EECSRX [R/W] B,H,W ----00--	—	EFEARX [R/W] B,H,W 00000000 00000000		
002408_H	—	EFECRX [R/W] B,H,W -------0 00000000 00000000			
$00240C_H$ to $0024FC_H$	—				Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002500_H	CTRLR3 [R/W] B,H,W -------- 000-0001		STATR3 [R/W] B,H,W -------- 00000000		CAN3 (128msb)
002504_H	ERRCNT3 [R] B,H,W 00000000 00000000		BTR3 [R/W] B,H,W -0100011 00000001		
002508_H	INTR3 [R] B,H,W 00000000 00000000		TESTR3 [R/W] B,H,W -------- X00000--		
$00250C_H$	BRPER3 [R/W] B,H,W -------- ----0000		—	—	
002510_H	IF1CREQ3 [R/W] B,H,W 0------- 00000001		IF1CMSK3 [R/W] B,H,W -------- 00000000		
002514_H	IF1MSK23 [R/W] B,H,W 11-11111 11111111		IF1MSK13 [R/W] B,H,W 11111111 11111111		
002518_H	IF1ARB23 [R/W] B,H,W 00000000 00000000		IF1ARB13 [R/W] B,H,W 00000000 00000000		
$00251C_H$	IF1MCTR3 [R/W] B,H,W 00000000 0---0000		—	—	
002520_H	IF1DTA13 [R/W] B,H,W 00000000 00000000		IF1DTA23 [R/W] B,H,W 00000000 00000000		
002524_H	IF1DTB13 [R/W] B,H,W 00000000 00000000		IF1DTB23 [R/W] B,H,W 00000000 00000000		
002528_H	—	—	—	—	
$00252C_H$	—	—	—	—	
002530_H, 002534_H	Reserved (IF1 data mirror)				
002538_H	—	—	—	—	
$00253C_H$	—	—	—	—	
002540_H	IF2CREQ3 [R/W] B,H,W 0------- 00000001		IF2CMSK3 [R/W] B,H,W -------- 00000000		
002544_H	IF2MSK23 [R/W] B,H,W 11-11111 11111111		IF2MSK13 [R/W] B,H,W 11111111 11111111		
002548_H	IF2ARB23 [R/W] B,H,W 00000000 00000000		IF2ARB13 [R/W] B,H,W 00000000 00000000		
$00254C_H$	IF2MCTR3 [R/W] B,H,W 00000000 0---0000		—	—	
002550_H	IF2DTA13 [R/W] B,H,W 00000000 00000000		IF2DTA23 [R/W] B,H,W 00000000 00000000		
002554_H	IF2DTB13 [R/W] B,H,W 00000000 00000000		IF2DTB23 [R/W] B,H,W 00000000 00000000		
002558_H	—	—	—	—	
$00255C_H$	—	—	—	—	
002560_H, 002564_H	Reserved (IF2 data mirror)				
002568_H	—	—	—	—	
$00256C_H$	—	—	—	—	
002570_H to $00257C_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002580_H	TREQR23 [R] B,H,W 00000000 00000000		TREQR13 [R] B,H,W 00000000 00000000		CAN3 (128msb)
002584_H	TREQR43 [R] B,H,W 00000000 00000000		TREQR33 [R] B,H,W 00000000 00000000		
002588_H	TREQR63 [R] B,H,W 00000000 00000000		TREQR53 [R] B,H,W 00000000 00000000		
$00258C_H$	TREQR83 [R] B,H,W 00000000 00000000		TREQR73 [R] B,H,W 00000000 00000000		
002590_H	NEWDT23 [R] B,H,W 00000000 00000000		NEWDT13 [R] B,H,W 00000000 00000000		
002594_H	NEWDT43 [R] B,H,W 00000000 00000000		NEWDT33 [R] B,H,W 00000000 00000000		
002598_H	NEWDT63 [R] B,H,W 00000000 00000000		NEWDT53 [R] B,H,W 00000000 00000000		
$00259C_H$	NEWDT83 [R] B,H,W 00000000 00000000		NEWDT73 [R] B,H,W 00000000 00000000		
$0025A0_H$	INTPND23 [R] B,H,W 00000000 00000000		INTPND13 [R] B,H,W 00000000 00000000		
$0025A4_H$	INTPND43 [R] B,H,W 00000000 00000000		INTPND33 [R] B,H,W 00000000 00000000		
$0025A8_H$	INTPND63 [R] B,H,W 00000000 00000000		INTPND53 [R] B,H,W 00000000 00000000		
$0025AC_H$	INTPND83 [R] B,H,W 00000000 00000000		INTPND73 [R] B,H,W 00000000 00000000		
$0025B0_H$	MSGVAL23 [R] B,H,W 00000000 00000000		MSGVAL13 [R] B,H,W 00000000 00000000		
$0025B4_H$	MSGVAL43 [R] B,H,W 00000000 00000000		MSGVAL33 [R] B,H,W 00000000 00000000		
$0025B8_H$	MSGVAL63 [R] B,H,W 00000000 00000000		MSGVAL53 [R] B,H,W 00000000 00000000		
$0025BC_H$	MSGVAL83 [R] B,H,W 00000000 00000000		MSGVAL73 [R] B,H,W 00000000 00000000		
$0025C0_H$ to $0025FC_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002600_H	CTRLR4 [R/W] B,H,W -------- 000-0001		STATR4 [R/W] B,H,W -------- 00000000		CAN4 (128msb)
002604_H	ERRCNT4 [R] B,H,W 00000000 00000000		BTR4 [R/W] B,H,W -0100011 00000001		
002608_H	INTR4 [R] B,H,W 00000000 00000000		TESTR4 [R/W] B,H,W -------- X00000--		
$00260C_H$	BRPER4 [R/W] B,H,W -------- ----0000		—	—	
002610_H	IF1CREQ4 [R/W] B,H,W 0------- 00000001		IF1CMSK4 [R/W] B,H,W -------- 00000000		
002614_H	IF1MSK24 [R/W] B,H,W 11-11111 11111111		IF1MSK14 [R/W] B,H,W 11111111 11111111		
002618_H	IF1ARB24 [R/W] B,H,W 00000000 00000000		IF1ARB14 [R/W] B,H,W 00000000 00000000		
$00261C_H$	IF1MCTR4 [R/W] B,H,W 00000000 0---0000		—	—	
002620_H	IF1DTA14 [R/W] B,H,W 00000000 00000000		IF1DTA24 [R/W] B,H,W 00000000 00000000		
002624_H	IF1DTB14 [R/W] B,H,W 00000000 00000000		IF1DTB24 [R/W] B,H,W 00000000 00000000		
002628_H	—	—	—	—	
$00262C_H$	—	—	—	—	
002630_H, 002634_H	Reserved (IF1 data mirror)				
002638_H	—	—	—	—	
$00263C_H$	—	—	—	—	
002640_H	IF2CREQ4 [R/W] B,H,W 0------- 00000001		IF2CMSK4 [R/W] B,H,W -------- 00000000		
002644_H	IF2MSK24 [R/W] B,H,W 11-11111 11111111		IF2MSK14 [R/W] B,H,W 11111111 11111111		
002648_H	IF2ARB24 [R/W] B,H,W 00000000 00000000		IF2ARB14 [R/W] B,H,W 00000000 00000000		
$00264C_H$	IF2MCTR4 [R/W] B,H,W 00000000 0---0000		—	—	
002650_H	IF2DTA14 [R/W] B,H,W 00000000 00000000		IF2DTA24 [R/W] B,H,W 00000000 00000000		
002654_H	IF2DTB14 [R/W] B,H,W 00000000 00000000		IF2DTB24 [R/W] B,H,W 00000000 00000000		
002658_H	—	—	—	—	
$00265C_H$	—	—	—	—	
002660_H, 002664_H	Reserved (IF2 data mirror)				
002668_H	—	—	—	—	
$00266C_H$	—	—	—	—	
002670_H to $00267C_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002680_H	TREQR24 [R] B,H,W 00000000 00000000		TREQR14 [R] B,H,W 00000000 00000000		CAN4 (128msb)
002684_H	TREQR44 [R] B,H,W 00000000 00000000		TREQR34 [R] B,H,W 00000000 00000000		
002688_H	TREQR64 [R] B,H,W 00000000 00000000		TREQR54 [R] B,H,W 00000000 00000000		
$00268C_H$	TREQR84 [R] B,H,W 00000000 00000000		TREQR74 [R] B,H,W 00000000 00000000		
002690_H	NEWDT24 [R] B,H,W 00000000 00000000		NEWDT14 [R] B,H,W 00000000 00000000		
002694_H	NEWDT44 [R] B,H,W 00000000 00000000		NEWDT34 [R] B,H,W 00000000 00000000		
002698_H	NEWDT64 [R] B,H,W 00000000 00000000		NEWDT54 [R] B,H,W 00000000 00000000		
$00269C_H$	NEWDT84 [R] B,H,W 00000000 00000000		NEWDT74 [R] B,H,W 00000000 00000000		
$0026A0_H$	INTPND24 [R] B,H,W 00000000 00000000		INTPND14 [R] B,H,W 00000000 00000000		
$0026A4_H$	INTPND44 [R] B,H,W 00000000 00000000		INTPND34 [R] B,H,W 00000000 00000000		
$0026A8_H$	INTPND64 [R] B,H,W 00000000 00000000		INTPND54 [R] B,H,W 00000000 00000000		
$0026AC_H$	INTPND84 [R] B,H,W 00000000 00000000		INTPND74 [R] B,H,W 00000000 00000000		
$0026B0_H$	MSGVAL24 [R] B,H,W 00000000 00000000		MSGVAL14 [R] B,H,W 00000000 00000000		
$0026B4_H$	MSGVAL44 [R] B,H,W 00000000 00000000		MSGVAL34 [R] B,H,W 00000000 00000000		
$0026B8_H$	MSGVAL64 [R] B,H,W 00000000 00000000		MSGVAL54 [R] B,H,W 00000000 00000000		
$0026BC_H$	MSGVAL84 [R] B,H,W 00000000 00000000		MSGVAL74 [R] B,H,W 00000000 00000000		
$0026C0_H$ to $0026FC_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002700_H	CTRLR5 [R/W] B,H,W -------- 000-0001		STATR5 [R/W] B,H,W -------- 00000000		CAN5 (128msb)
002704_H	ERRCNT5 [R] B,H,W 00000000 00000000		BTR5 [R/W] B,H,W -0100011 00000001		
002708_H	INTR5 [R] B,H,W 00000000 00000000		TESTR5 [R/W] B,H,W -------- X00000--		
$00270C_H$	BRPER5 [R/W] B,H,W -------- ----0000		—	—	
002710_H	IF1CREQ5 [R/W] B,H,W 0------- 00000001		IF1CMSK5 [R/W] B,H,W -------- 00000000		
002714_H	IF1MSK25 [R/W] B,H,W 11-11111 11111111		IF1MSK15 [R/W] B,H,W 11111111 11111111		
002718_H	IF1ARB25 [R/W] B,H,W 00000000 00000000		IF1ARB15 [R/W] B,H,W 00000000 00000000		
$00271C_H$	IF1MCTR5 [R/W] B,H,W 00000000 0---0000		—	—	
002720_H	IF1DTA15 [R/W] B,H,W 00000000 00000000		IF1DTA25 [R/W] B,H,W 00000000 00000000		
002724_H	IF1DTB15 [R/W] B,H,W 00000000 00000000		IF1DTB25 [R/W] B,H,W 00000000 00000000		
002728_H	—	—	—	—	
$00272C_H$	—	—	—	—	
002730_H, 002734_H	Reserved (IF1 data mirror)				
002738_H	—	—	—	—	
$00273C_H$	—	—	—	—	
002740_H	IF2CREQ5 [R/W] B,H,W 0------- 00000001		IF2CMSK5 [R/W] B,H,W -------- 00000000		
002744_H	IF2MSK25 [R/W] B,H,W 11-11111 11111111		IF2MSK15 [R/W] B,H,W 11111111 11111111		
002748_H	IF2ARB25 [R/W] B,H,W 00000000 00000000		IF2ARB15 [R/W] B,H,W 00000000 00000000		
$00274C_H$	IF2MCTR5 [R/W] B,H,W 00000000 0---0000		—	—	
002750_H	IF2DTA15 [R/W] B,H,W 00000000 00000000		IF2DTA25 [R/W] B,H,W 00000000 00000000		
002754_H	IF2DTB15 [R/W] B,H,W 00000000 00000000		IF2DTB25 [R/W] B,H,W 00000000 00000000		
002758_H	—	—	—	—	
$00275C_H$	—	—	—	—	
002760_H, 002764_H	Reserved (IF2 data mirror)				
002768_H	—	—	—	—	
$00276C_H$	—	—	—	—	
002770_H to $00277C_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002780_H	TREQR25 [R] B,H,W 00000000 00000000		TREQR15 [R] B,H,W 00000000 00000000		CAN5 (128msb)
002784_H	TREQR45 [R] B,H,W 00000000 00000000		TREQR35 [R] B,H,W 00000000 00000000		
002788_H	TREQR65 [R] B,H,W 00000000 00000000		TREQR55 [R] B,H,W 00000000 00000000		
$00278C_H$	TREQR85 [R] B,H,W 00000000 00000000		TREQR75 [R] B,H,W 00000000 00000000		
002790_H	NEWDT25 [R] B,H,W 00000000 00000000		NEWDT15 [R] B,H,W 00000000 00000000		
002794_H	NEWDT45 [R] B,H,W 00000000 00000000		NEWDT35 [R] B,H,W 00000000 00000000		
002798_H	NEWDT65 [R] B,H,W 00000000 00000000		NEWDT55 [R] B,H,W 00000000 00000000		
$00279C_H$	NEWDT85 [R] B,H,W 00000000 00000000		NEWDT75 [R] B,H,W 00000000 00000000		
$0027A0_H$	INTPND25 [R] B,H,W 00000000 00000000		INTPND15 [R] B,H,W 00000000 00000000		
$0027A4_H$	INTPND45 [R] B,H,W 00000000 00000000		INTPND35 [R] B,H,W 00000000 00000000		
$0027A8_H$	INTPND65 [R] B,H,W 00000000 00000000		INTPND55 [R] B,H,W 00000000 00000000		
$0027AC_H$	INTPND85 [R] B,H,W 00000000 00000000		INTPND75 [R] B,H,W 00000000 00000000		
$0027B0_H$	MSGVAL25 [R] B,H,W 00000000 00000000		MSGVAL15 [R] B,H,W 00000000 00000000		
$0027B4_H$	MSGVAL45 [R] B,H,W 00000000 00000000		MSGVAL35 [R] B,H,W 00000000 00000000		
$0027B8_H$	MSGVAL65 [R] B,H,W 00000000 00000000		MSGVAL55 [R] B,H,W 00000000 00000000		
$0027BC_H$	MSGVAL85 [R] B,H,W 00000000 00000000		MSGVAL75 [R] B,H,W 00000000 00000000		
$0027C0_H$ to $002FFC_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003000_H	SEEARA [R] B,H,W ----0000 00000000		DEEARA [R] B,H,W ----0000 00000000		Backup RAM ECC control
003004_H	EECSRA [R/W] B,H,W ----00--	—	EFEARA [R/W] B,H,W ----0000 00000000		
003008_H	—	EFECRA [R/W] B,H,W -------0 00000000 00000000			
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- 00000000 00000000				RAM/diagnosis XBS RAM
003010_H	TEAR1X[R] B,H,W 000----- -------- 00000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- 00000000 00000000				
003018_H	TAEARX [R/W] B,H,W 10111111 11111111		TASARX [R/W] B,H,W 00000000 00000000		
$00301C_H$	TFECRX [R/W] B,H,W ----0000	TICRX [R/W] B,H,W ----0000	TTCRX [R/W] B,H,W ------00 00001100		
003020_H	TSRCRX [W] B,H,W 0-------	—	—	TKCCRX [R/W] B,H,W 00----00	
003024_H to $00302C_H$	—				Reserved
003030_H	TEAR0A[R] B,H,W 000----- -------- ----0000 00000000				RAM/diagnosis Backup RAM
003034_H	TEAR1A[R] B,H,W 000----- -------- ----0000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- ----0000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W ----1111 11111111		TASARA[R/W] B,H,W ----0000 00000000		
003040_H	TFECRA [R/W] B,H,W ----0000	TICRA [R/W] B,H,W ----0000	TTCRA [R/W] B,H,W ------00 00001100		
003044_H	TSRCRA [W] B,H,W 0-------	—	—	TKCCRA [R/W] B,H,W 00----00	
003048_H, $00304C_H$	—				Reserved
003050_H	SEEARH [R] B,H,W --000000 00000000		DEEARH [R] B,H,W --000000 00000000		AHB RAM ECC control
003054_H	EECSRH [R/W] B,H,W ----00--	—	EFEARH [R/W] B,H,W --000000 00000000		
003058_H	—	EFECRH [R/W] B,H,W -------0 00000000 00000000			
$00305C_H$	—				Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003060_H	TEAR0H[R] B,H,W 000----- -------- --000000 00000000				RAM/diagnosis AHB RAM
003064_H	TEAR1H[R] B,H,W 000----- -------- --000000 00000000				
003068_H	TEAR2H[R] B,H,W 000----- -------- --000000 00000000				
$00306C_H$	TAEARH[R/W] B,H,W --111111 11111111		TASARH[R/W] B,H,W --000000 00000000		
003070_H	TFECRH [R/W] B,H,W ----0000	TICRH [R/W] B,H,W ----0000	TTCRH [R/W] B,H,W ------00 00001100		
003074_H	TSRCRH [W] B,H,W 0-------	—	—	TKCCRH [R/W] B,H,W 00----00	
003078_H to $0030FC_H$	—				Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		BUS diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114_H	—	—	BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
$00311C_H$	—	—	—	—	
003120_H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128_H to $003FFC_H$	—				Reserved
004000_H to $007FFC_H$	Backup-RAM				Backup RAM area
008000_H to $00CFFC_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00D000_H$	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF
$00D004_H$	CIF1[R/W] W 00000000 -------0 -0000000 --------				
$00D008_H$ to $00D018_H$	—	—	—	—	Reserved
$00D01C_H$	LCK[R/W] W -------- -------- -------- 00000000				FlexRay GIF
$00D020_H$	EIR[R/W] W -----000 -----000 ----0000 00000000				FlexRay INT
$00D024_H$	SIR[R/W] W ------00 ------00 00000000 00000000				
$00D028_H$	EILS[R/W] W -----000 -----000 ----0000 00000000				
$00D02C_H$	SILS[R/W] W ------11 ------11 11111111 11111111				
$00D030_H$	EIES[R/W] W -----000 -----000 ----0000 00000000				
$00D034_H$	EIER[R/W] W -----000 -----000 ----0000 00000000				
$00D038_H$	SIES[R/W] W ------00 ------00 00000000 00000000				
$00D03C_H$	SIER[R/W] W ------00 ------00 00000000 00000000				
$00D040_H$	ILE[R/W] W -------- -------- -------- ------00				
$00D044_H$	T0C[R/W] W --000000 00000000 -0000000 ------00				
$00D048_H$	T1C[R/W] W --000000 00000010 -------- ------00				
$00D04C_H$	STPW1[R/W] W --000000 00000000 --000000 -0000000				
$00D050_H$	STPW2[R] W -----000 00000000 -----000 00000000				
$00D054_H$ to $00D07C_H$	—	—	—	—	Reserved
$00D080_H$	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC
$00D084_H$	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
$00D088_H$	SUCC3[R/W] W -------- -------- -------- 00010001				
$00D08C_H$	NEMC[R/W] W -------- -------- -------- ----0000				FlexRay NEM
$00D090_H$	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT
$00D094_H$	PRTC2[R/W] W --001111 00101101 --001010 —001110				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00D098_H$	MHDC[R/W] W ---00000 00000000 -------- -0000000				FlexRay MHD
$00D09C_H$	—				Reserved
$00D0A0_H$	GTUC1[R/W] W -------- ----0000 00000010 10000000				FlexRay GTU
$00D0A4_H$	GTUC2[R/W] W -------- ----0010 --000000 00001010				
$00D0A8_H$	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
$00D0AC_H$	GTUC4[R/W] W --000000 00001000 --000000 00000111				
$00D0B0_H$	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
$00D0B4_H$	GTUC6[R/W] W -----000 00000010 -----000 00000000				
$00D0B8_H$	GTUC7[R/W] W ------00 00000010 ------00 00000100				
$00D0BC_H$	GTUC8[R/W] W ---00000 00000000 -------- --000010				
$00D0C0_H$	GTUC9[R/W] W -------- ------00 ---00001 —000001				
$00D0C4_H$	GTUC10[R/W] W -----000 00000010 --000000 00000101				
$00D0C8_H$	GTUC11[R/W] W -----000 -----000 ------00 ------00				
$00D0CC_H$ to $00D0FC_H$	—	—	—	—	Reserved
$00D100_H$	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC
$00D104_H$	CCEV[R] W -------- -------- ---00000 00--0000				
$00D108_H$	—				Reserved
$00D10C_H$	—				
$00D110_H$	SCV[R] W -----000 00000000 -----000 00000000				FlexRay GTU
$00D114_H$	MTCCV[R] W -------- --000000 --000000 00000000				
$00D118_H$	RCV[R] W -------- -------- ----0000 00000000				
$00D11C_H$	OCV[R] W -------- -----000 00000000 00000000				
$00D120_H$	SFS[R] W -------- ----0000 00000000 00000000				
$00D124_H$	SWNIT[R] W -------- -------- ----0000 00000000				
$00D128_H$	ACS[R/W] W -------- -------- ---00000 ---00000				
$00D12C_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00D130_H$	ESID1[R] W -------- -------- 00----00 00000000				FlexRay GTU
$00D134_H$	ESID2[R] W -------- -------- 00----00 00000000				
$00D138_H$	ESID3[R] W -------- -------- 00----00 00000000				
$00D13C_H$	ESID4[R] W -------- -------- 00----00 00000000				
$00D140_H$	ESID5[R] W -------- -------- 00----00 00000000				
$00D144_H$	ESID6[R] W -------- -------- 00----00 00000000				
$00D148_H$	ESID7[R] W -------- -------- 00----00 00000000				
$00D14C_H$	ESID8[R] W -------- -------- 00----00 00000000				
$00D150_H$	ESID9[R] W -------- -------- 00----00 00000000				
$00D154_H$	ESID10[R] W -------- -------- 00----00 00000000				
$00D158_H$	ESID11[R] W -------- -------- 00----00 00000000				
$00D15C_H$	ESID12[R] W -------- -------- 00----00 00000000				
$00D160_H$	ESID13[R] W -------- -------- 00----00 00000000				
$00D164_H$	ESID14[R] W -------- -------- 00----00 00000000				
$00D168_H$	ESID15[R] W -------- -------- 00----00 00000000				
$00D16C_H$	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00D170_H$	OSID1[R] W -------- -------- 00----00 00000000				FlexRay GTU
$00D174_H$	OSID2[R] W -------- -------- 00----00 00000000				
$00D178_H$	OSID3[R] W -------- -------- 00----00 00000000				
$00D17C_H$	OSID4[R] W -------- -------- 00----00 00000000				
$00D180_H$	OSID5[R] W -------- -------- 00----00 00000000				
$00D184_H$	OSID6[R] W -------- -------- 00----00 00000000				
$00D188_H$	OSID7[R] W -------- -------- 00----00 00000000				
$00D18C_H$	OSID8[R] W -------- -------- 00----00 00000000				
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				
$00D198_H$	OSID11[R] W -------- -------- 00----00 00000000				
$00D19C_H$	OSID12[R] W -------- -------- 00----00 00000000				
$00D1A0_H$	OSID13[R] W -------- -------- 00----00 00000000				
$00D1A4_H$	OSID14[R] W -------- -------- 00----00 00000000				
$00D1A8_H$	OSID15[R] W -------- -------- 00----00 00000000				
$00D1AC_H$	—				Reserved
$00D1B0_H$	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM
$00D1B4_H$	NMV2[R] W 00000000 00000000 00000000 00000000				
$00D1B8_H$	NMV3[R] W 00000000 00000000 00000000 00000000				
$00D1BC_H$ to $00D2FC_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00D300_H$	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD
$00D304_H$	FRF[R/W] W -------1 10000000 ---00000 00000000				
$00D308_H$	FRFM[R/W] W -------- -------- ---00000 000000--				
$00D30C_H$	FCL[R/W] W -------- -------- -------- 10000000				
$00D310_H$	MHDS[R/W] W -0000000 -0000000 -0000000 10000000				
$00D314_H$	LDTS[R] W -----000 00000000 -----000 00000000				
$00D318_H$	FSR[R] W -------- -------- 00000000 -----000				
$00D31C_H$	MHDF[R/W] W -------- -------- -------0 00000000				
$00D320_H$	TXRQ1[R] W 00000000 00000000 00000000 00000000				
$00D324_H$	TXRQ2[R] W 00000000 00000000 00000000 00000000				
$00D328_H$	TXRQ3[R] W 00000000 00000000 00000000 00000000				
$00D32C_H$	TXRQ4[R] W 00000000 00000000 00000000 00000000				
$00D330_H$	NDAT1[R] W 00000000 00000000 00000000 00000000				
$00D334_H$	NDAT2[R] W 00000000 00000000 00000000 00000000				
$00D338_H$	NDAT3[R] W 00000000 00000000 00000000 00000000				
$00D33C_H$	NDAT4[R] W 00000000 00000000 00000000 00000000				
$00D340_H$	MBSC1[R] W 00000000 00000000 00000000 00000000				
$00D344_H$	MBSC2[R] W 00000000 00000000 00000000 00000000				
$00D348_H$	MBSC3[R] W 00000000 00000000 00000000 00000000				
$00D34C_H$	MBSC4[R] W 00000000 00000000 00000000 00000000				
$00D350_H$ to $00D3EC_H$	—	—	—	—	Reserved
$00D3F0_H$	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF
$00D3F4_H$	ENDN[R] W 10000111 01100101 01000011 00100001				
$00D3F8_H$, $00D3FC_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00D400_H$ to $00D4FC_H$	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF
$00D500_H$	WRHS1[R/W] W --000000 -0000000 -----000 00000000				
$00D504_H$	WRHS2[R/W] W -------- -0000000 -----000 00000000				
$00D508_H$	WRHS3[R/W] W -------- -------- -----000 00000000				
$00D50C_H$	—				
$00D510_H$	IBCM[R/W] W -------- -----000 -------- -----000				
$00D514_H$	IBCR[R/W] W 0------- -0000000 0------- -0000000				
$00D518_H$ to $00D5FC_H$	—	—	—	—	Reserved
$00D600_H$ to $00D6FC_H$	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF
$00D700_H$	RDHS1[R] W --000000 -0000000 -----000 00000000				
$00D704_H$	RDHS2[R] W -0000000 -0000000 -----000 00000000				
$00D708_H$	RDHS3[R] W --000000 --000000 -----000 00000000				
$00D70C_H$	MBS[R] W --000000 --000000 00-00000 00000000				
$00D710_H$	OBCM[R/W] W -------- ------00 -------- ------00				
$00D714_H$	OBCR[R/W] W -------- -0000000 0-----00 -0000000				
$00D718_H$ to $00D7FC_H$	—	—	—	—	Reserved
$00D800_H$ to $00EFFC_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$00F000_H$ to $00FEFC_H$	—	—	—	—	Reserved [S]
$00FF00_H$	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
$00FF04_H$ to $00FF0C_H$	—				Reserved [S]
$00FF10_H$	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF18_H$ to $00FFF4_H$	—				Reserved [S]
$00FFF8_H$	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]:It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

Interrupt vector
MB91F52xR (144pin)

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of illegal instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation at internal bus diagnosis XBS RAM double-bit error detection Backup RAM double-bit error detection AHB RAM double-bit error detection TPU violation	15	0F	$15(F_H)$ Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt -	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*[6]
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*[2]
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*[2]
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*[1]
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*[1]
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*[1]
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*[1]

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*[1]
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*[1]
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*[1]
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed) Multi-function serial interface ch.4 (status)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed) Multi-function serial interface ch.5 (status)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (transmission completed) FlexRay0	31	1F	ICR15	380_H	$000FFF80_H$	15*[7]
Multi-function serial interface ch.6 (reception completed) Multi-function serial interface ch.6 (status) FlexRay1	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (transmission completed) FlexRay timer 0	33	21	ICR17	378_H	$000FFF78_H$	17*[8]
CAN0 CAN3 FlexRay timer 1	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1 RAM diagnosis completed RAM initialization completed Error generation at RAM diagnosis Backup RAM diagnosis completed Backup RAM initialization completed Error generation at Backup RAM diagnosis AHB RAM diagnosis completed AHB RAM initialization completed Error generation at AHB RAM diagnosis CAN4	35	23	ICR19	370_H	$000FFF70_H$	-

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
CAN2 Up/down counter 0 Up/down counter 1 CAN5 FlexRay PLL gear/FlexRay PLL alarm	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed) Multi-function serial interface ch.7 (status)	38	26	ICR22	364_H	$000FFF64_H$	22*1
16-bit free-run timer 0 ("0" detection) / (compare clear) Multi-function serial interface ch.7 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG0/1/10/11/20/21/30/31/40/41 16-bit free-run timer 1 ("0" detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
PPG2/3/12/13/22/23/32/33/43 16-bit free-run timer 2 ("0" detection) / (compare clear)	41	29	ICR25	358_H	$000FFF58_H$	25*3
PPG4/5/14/15/24/25/34/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG6/7/16/17/26/27/36/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (Sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1 *4
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
32-bit ICU6 (fetching /measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching /measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37
32-bit ICU8 (fetching /measurement) Multi-function serial interface ch.11 (reception completed) Multi-function serial interface ch.11 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching /measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4 (fetching /measurement) Multi-function serial interface ch.11 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5 (fetching /measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 Base timer 0 IRQ1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45*5
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delayed interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS™*9)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

*: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.
*1: The status of the multi-function serial interface does not support the DMA transfer by the I2C reception and FlexRay.
*2: The reload timer ch.4 to ch.7 does not support the DMA transfer by the interrupt.
*3: The PPG ch.24 to ch.87 does not support the DMA transfer by the interrupt.

*4: The clock calibration unit does not support the DMA transfer by the interrupt.
*5: The 32-bit free-run timer ch.3 to ch.10 does not support the DMA transfer by the interrupt.
*6: It does not support the DMA transfer by the external low-voltage detection interrupt.
*7: It does not support the DMA transfer by the FlexRay interrupt.
*8: It does not support the DMA transfer by the FlexRay timer interrupt.
*9: REALOS is a trademark of Cypress.

MB91F52xU (176pin)

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of illegal instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation at internal bus diagnosis XBS RAM double-bit error detection Backup RAM double-bit error detection AHB RAM double-bit error detection TPU violation	15	0F	$15(F_H)$ Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt -	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*6
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*[1]
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394_H	$000FFF94_H$	10*[1]
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15*[7]
FlexRay0						
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6 (status)						
FlexRay1						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17*[8]
FlexRay timer 0						
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN3						
FlexRay timer 1						
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis completed						
RAM initialization completed						
Error generation at RAM diagnosis						
Backup RAM diagnosis completed						
Backup RAM initialization completed						
Error generation at Backup RAM diagnosis						
AHB RAM diagnosis completed						
AHB RAM initialization completed						
Error generation at AHB RAM diagnosis						
CAN4						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
CAN5						
FlexRay PLL gear/FlexRay PLL alarm						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.7 (reception completed) Multi-function serial interface ch.7 (status)	38	26	ICR22	364_H	$000FFF64_H$	22*1
16-bit free-run timer 0 ("0" detection) / (compare clear) Multi-function serial interface ch.7 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG0/1/10/11/20/21/30/31/40/41 16-bit free-run timer 1 ("0" detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
PPG2/3/12/13/22/23/32/33/42/43 16-bit free-run timer 2 ("0" detection) / (compare clear)	41	29	ICR25	358_H	$000FFF58_H$	25*3
PPG4/5/14/15/24/25/34/35/44/45	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG6/7/16/17/26/27/36/37/46/47	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG8/9/18/19/28/29/38/39	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3
Multi-function serial interface ch.8 (reception completed) Multi-function serial interface ch.8 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (Sub oscillation) Multi-function serial interface ch.9 (reception completed) Multi-function serial interface ch.9 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1 *4
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit free-run timer 4 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit free-run timer 3/5 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU6 (fetching /measurement) Multi-function serial interface ch.10 (reception completed) Multi-function serial interface ch.10 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching /measurement) Multi-function serial interface ch.10 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
32-bit ICU8 (fetching /measurement)	54	36	ICR38	324_H	$000FFF24_H$	38*1
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching /measurement)	55	37	ICR39	320_H	$000FFF20_H$	39
WG dead timer underflow 0 / 1/ 2						
WG dead timer reload 0 / 1/ 2						
WG DTTI 0						
32-bit ICU4 (fetching /measurement)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
Multi-function serial interface ch.11 (transmission completed)						
32-bit ICU5 (fetching /measurement)	57	39	ICR41	318_H	$000FFF18_H$	41
A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47						
32-bit OCU6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 0 IRQ1						
Base timer 1 IRQ0	61	3D	ICR45	308_H	$000FFF08_H$	45*5
Base timer 1 IRQ1						
-						
-						
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delayed interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

*: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.
*1: The status of the multi-function serial interface does not support the DMA transfer by the I^2C reception and FlexRay.
*2: The reload timer ch.4 to ch.7 does not support the DMA transfer by the interrupt.
*3: The PPG ch.24 to ch.87 does not support the DMA transfer by the interrupt.
*4: The clock calibration unit does not support the DMA transfer by the interrupt.
*5: The 32-bit free-run timer ch.3 to ch.10 does not support the DMA transfer by the interrupt.
*6: It does not support the DMA transfer by the external low-voltage detection interrupt.
*7: It does not support the DMA transfer by the FlexRay interrupt.
*8: It does not support the DMA transfer by the FlexRay timer interrupt.

MB91F52xM (208pin)

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of illegal instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation at internal bus diagnosis XBS RAM double-bit error detection Backup RAM double-bit error detection AHB RAM double-bit error detection TPU violation	15	0F	$15(F_H)$ Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt External interrupt 16-23	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*[6]
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*[2]
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*[2]
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*[1]
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*[1]
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*[1]
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*[1]
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*[1]

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*[1]
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394_H	$000FFF94_H$	10*[1]
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4/ ch.12 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4/ ch.12 (status)						
Multi-function serial interface ch.4/ ch.12 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5/ ch.13 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5/ ch.13 (status)						
Multi-function serial interface ch.5/ ch.13 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15*[7]
FlexRay0						
Multi-function serial interface ch.6/ ch.14 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6/ ch.14 (status)						
FlexRay1						
Multi-function serial interface ch.6/ ch.14 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17*[8]
FlexRay timer 0						
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN3						
FlexRay timer 1						
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis completed						
RAM initialization completed						
Error generation at RAM diagnosis						
Backup RAM diagnosis completed						
Backup RAM initialization completed						
Error generation at Backup RAM diagnosis						
AHB RAM diagnosis completed						
AHB RAM initialization completed						
Error generation at AHB RAM diagnosis						
CAN4						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0/2						
Up/down counter 1/3						
CAN5						
FlexRay PLL gear/FlexRay PLL alarm						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.7/ ch.15 (reception completed) Multi-function serial interface ch.7/ ch.15 (status)	38	26	ICR22	364_H	$000FFF64_H$	22*1
16-bit free-run timer 0 ("0" detection) / (compare clear) Multi-function serial interface ch.7/ ch.15 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG0/1/10/11/20/21/30/31/40/41/50/51/60/61 16-bit free-run timer 1 ("0" detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
PPG2/3/12/13/22/23/32/33/42/43/52/53/62/63 16-bit free-run timer 2 ("0" detection) / (compare clear)	41	29	ICR25	358_H	$000FFF58_H$	25*3
PPG4/5/14/15/24/25/34/35/44/45/54/55	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG6/7/16/17/26/27/36/37/46/47/56/57	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG8/9/18/19/28/29/38/39/48/49/58/59	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3
Multi-function serial interface ch.8/ ch.16 (reception completed) Multi-function serial interface ch.8/ ch.16 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*1
Main timer Sub timer PLL timer Multi-function serial interface ch.8/ ch.16 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (Sub oscillation) Multi-function serial interface ch.9/ ch.17 (reception completed) Multi-function serial interface ch.9/ ch.17 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*1 *4
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9/ ch.17 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit free-run timer 4/6/8/10 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*5
32-bit free-run timer 3/5/7/9 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*5
32-bit ICU6 (fetching /measurement) Multi-function serial interface ch.10/ ch.18 (reception completed) Multi-function serial interface ch.10/ ch.18 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*1
32-bit ICU7 (fetching /measurement) Multi-function serial interface ch.10/ ch.18 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
32-bit ICU8 (fetching /measurement) Multi-function serial interface ch.11/ ch.19 (reception completed) Multi-function serial interface ch.11/ ch.19 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching /measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4/10 (fetching /measurement) Multi-function serial interface ch.11/ ch.19 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5/11 (fetching /measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 48/49/50/51/52/53/54/55/56/57/58/59/60/61/62/63	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9/12/13 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 Base timer 0 IRQ1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45*5
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delayed interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

*: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.
*1: The status of the multi-function serial interface does not support the DMA transfer by the I^2C reception and FlexRay.
*2: The reload timer ch.4 to ch.7 does not support the DMA transfer by the interrupt.
*3: The PPG ch.24 to ch.87 does not support the DMA transfer by the interrupt.
*4: The clock calibration unit does not support the DMA transfer by the interrupt.
*5: The 32-bit free-run timer ch.3 to ch.10 does not support the DMA transfer by the interrupt.
*6: It does not support the DMA transfer by the external low-voltage detection interrupt.
*7: It does not support the DMA transfer by the FlexRay interrupt.
*8: It does not support the DMA transfer by the FlexRay timer interrupt.

MB91F52xY (416pin)

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of illegal instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation at internal bus diagnosis XBS RAM double-bit error detection Backup RAM double-bit error detection AHB RAM double-bit error detection TPU violation	15	0F	$15(F_H)$ Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt External interrupt 16-23	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*6
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*[1]
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394_H	$000FFF94_H$	10*[1]
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4/ ch.12 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*[1]
Multi-function serial interface ch.4/ ch.12 (status)						
Multi-function serial interface ch.4/ ch.12 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5/ ch.13 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*[1]
Multi-function serial interface ch.5/ ch.13 (status)						
Multi-function serial interface ch.5/ ch.13 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15*[7]
FlexRay0						
Multi-function serial interface ch.6/ ch.14 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*[1]
Multi-function serial interface ch.6/ ch.14 (status)						
FlexRay1						
Multi-function serial interface ch.6/ ch.14 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17*[8]
FlexRay timer 0						
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN3						
FlexRay timer 1						
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis completed						
RAM initialization completed						
Error generation at RAM diagnosis						
Backup RAM diagnosis completed						
Backup RAM initialization completed						
Error generation at Backup RAM diagnosis						
AHB RAM diagnosis completed						
AHB RAM initialization completed						
Error generation at AHB RAM diagnosis						
CAN4						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0/2						
Up/down counter 1/3						
CAN5						
FlexRay PLL gear/FlexRay PLL alarm						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.7/ ch.15 (reception completed) Multi-function serial interface ch.7/ ch.15 (status)	38	26	ICR22	364_H	$000FFF64_H$	22*[1]
16-bit free-run timer 0 ("0" detection) / (compare clear) Multi-function serial interface ch.7/ ch.15 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 0/1/10/11/20/21/30/31/40/41/50/51/60/61/70/71/80/81 16-bit free-run timer 1 ("0" detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*[3]
PPG 2/3/12/13/22/23/32/33/42/43/52/53/62/63/72/73/82/83 16-bit free-run timer 2 ("0" detection) / (compare clear)	41	29	ICR25	358_H	$000FFF58_H$	25*[3]
PPG 4/5/14/15/24/25/34/35/44/45/54/55/64/65/74/75/84/85	42	2A	ICR26	354_H	$000FFF54_H$	26*[3]
PPG 6/7/16/17/26/27/36/37/46/47/56/57/66/67/76/77/86/87	43	2B	ICR27	350_H	$000FFF50_H$	27*[3]
PPG 8/9/18/19/28/29/38/39/48/49/58/59/68/69/78/79	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*[3]
Multi-function serial interface ch.8/ ch.16 (reception completed) Multi-function serial interface ch.8/ ch.16 (status) 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)	45	2D	ICR29	348_H	$000FFF48_H$	29*[1]
Main timer Sub timer PLL timer Multi-function serial interface ch.8/ ch.16 (transmission completed) 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching)	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (Sub oscillation) Multi-function serial interface ch.9/ ch.17 (reception completed) Multi-function serial interface ch.9/ ch.17 (status)	47	2F	ICR31	340_H	$000FFF40_H$	31*[1] *[4]
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration unit (CR oscillation) Multi-function serial interface ch.9/ ch.17 (transmission completed) 16-bit OCU 0 (match) / 16-bit OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33
32-bit free-run timer 4/6/8/10 16-bit OCU 2 (match) / 16-bit OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34*[5]
32-bit free-run timer 3/5/7/9 16-bit OCU 4 (match) / 16-bit OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35*[5]
32-bit ICU6 (fetching /measurement) Multi-function serial interface ch.10/ ch.18 (reception completed) Multi-function serial interface ch.10/ ch.18 (status)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36*[1]
32-bit ICU7 (fetching /measurement) Multi-function serial interface ch.10/ ch.18 (transmission completed)	53	35	ICR37	328_H	$000FFF28_H$	37

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
32-bit ICU8 (fetching /measurement) Multi-function serial interface ch.11/ ch.19 (reception completed) Multi-function serial interface ch.11/ ch.19 (status)	54	36	ICR38	324_H	$000FFF24_H$	38*1
32-bit ICU9 (fetching /measurement) WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39
32-bit ICU4/10 (fetching /measurement) Multi-function serial interface ch.11/ ch.19 (transmission completed)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
32-bit ICU5/11 (fetching /measurement) A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 48/49/50/51/52/53/54/55/56/57/58/59/60/61/62/63	57	39	ICR41	318_H	$000FFF18_H$	41
32-bit OCU6/7/10/11 (match)	58	3A	ICR42	314_H	$000FFF14_H$	42
32-bit OCU8/9/12/13 (match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 Base timer 0 IRQ1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 Base timer 1 IRQ1 - -	61	3D	ICR45	308_H	$000FFF08_H$	45*5
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delayed interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System reserved (Used for REALOS)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System reserved (Used for REALOS)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

*: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.
*1: The status of the multi-function serial interface does not support the DMA transfer by the I^2C reception and FlexRay.
*2: The reload timer ch.4 to ch.7 does not support the DMA transfer by the interrupt.
*3: The PPG ch.24 to ch.87 does not support the DMA transfer by the interrupt.
*4: The clock calibration unit does not support the DMA transfer by the interrupt.
*5: The 32-bit free-run timer ch.3 to ch.10 does not support the DMA transfer by the interrupt.
*6: It does not support the DMA transfer by the external low-voltage detection interrupt.
*7: It does not support the DMA transfer by the FlexRay interrupt.
*8: It does not support the DMA transfer by the FlexRay timer interrupt.

11. Electrical Characteristics

Absolute Maximum Ratings

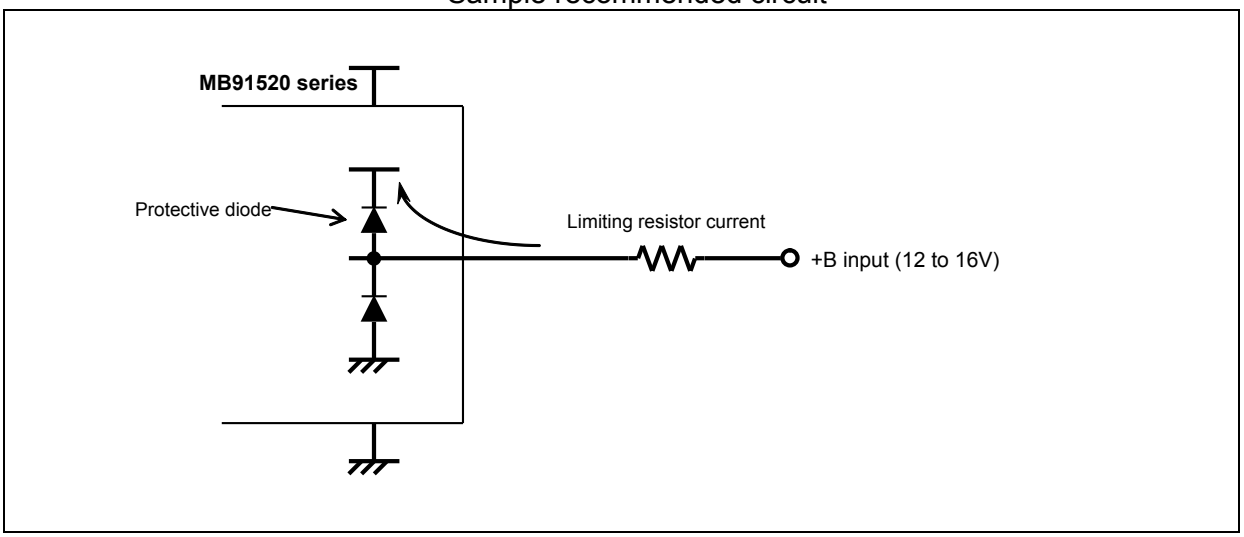
Parameter		Symbol	Rating		Unit	Remarks
			Min	Max		
Power supply voltage *1,*2		V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
		V_{CCE}	V_{SS}-0.3	V_{CC}	V	
Analog power supply voltage *1,*2		AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC} ≤ V_{CC}
Analog reference voltage *1		AVRH	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC}
Input voltage *1		V_I	V_{SS}-0.3	V_{CC}+0.3	V	When VCCE pin is a power supply *9
			V_{SS}-0.3	V_{CCE}+0.3		
Analog pin input voltage *1		V_{IA5}	V_{SS}-0.3	V_{CC}+0.3	V	
			V_{SS}-0.3	V_{CCE}+0.3	V	When VCCE pin is a power supply *9
Output voltage *1		V_o	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current		I_{CLAMP}	-	4.0	mA	*6
Total maximum clamp current		$\Sigma\|I_{CLAMP}\|$	-	20	mA	*6
"L" level maximum output current *3		I_{OL1}	-	15	mA	
		I_{OL2}	-	30	mA	
"L" level average output current *4		I_{OLAV1}	-	4	mA	*13
		I_{OLAV2}	-	12	mA	*14
"L" level total output current *5		ΣI_{OL1}	-	100	mA	
		ΣI_{OL2}	-	120	mA	
"H" level maximum output current*3		I_{OH1}	-	-15	mA	
		I_{OH2}	-	-30	mA	
"H" level average output current*4		I_{OHAV1}	-	-4	mA	*13
		I_{OHAV2}	-	-12	mA	*14
"H" level total output current *5		ΣI_{OH1}	-	-100	mA	
		ΣI_{OH2}	-	-120	mA	
Power consumption	T_A: -40°C to +105°C	P_D	-	990	mW	*8
	T_A: -40°C to +125°C		-	990	mW	*8, *10
			-	780	mW	*8, *12
				755	mW	*8, *11
Operating temperature		T_A	-40	+105	°C	
			-40	+125	°C	*7
Storage temperature		Tstg	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0V
*2: Caution must be taken that AV_{CC}, AVRH and V_{CCE} do not exceed V_{CC} upon power-on and under other circumstances.
*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.
*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Corresponding pins: all general-purpose ports except P035, 041, 093, 122, P222, P227, P232 and P236.
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

*7: When it is used under this condition, contact your sales representative.
*8: It is a standard when four-layer substrate is used.
*9: Please see to the item of "Product lineup" for details.
*10: It is a condition that can be used by limiting the product type of LES144, LEP176, LER208, and PAB416.
*11: It is a condition that can be used by the package limitation of LQS144 and LQP176.
*12: It is a condition that can be used by limiting the package of LQR208.
*13: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.
*14: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.

Sample recommended circuit



<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

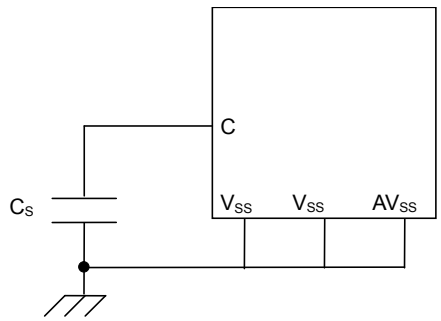
12. Recommended Operating Conditions

(V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} V_{CCE} AV_{CC}	4.5	5.5	V	Recommended operation guarantee range (When 5.0V is used)
		3.0	3.6	V	Recommended operation guarantee range (When 3.3V is used)
		2.7	5.5	V	Operation guarantee range *1
Smoothing capacitor *2	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*3

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative.
The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).
This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
*2: See the following diagram for details on the connection of smoothing capacitor C_S.
*3: When it is used under this condition, contact your sales representative.

·C Pin Connection Diagram



<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

13. DC Characteristics

(T_A: -40°C to +105°C, V_{CC}= AVcc=5.0V±10%/ V_{CC}= AVcc=3.3V±0.3V ,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=128MHz, Fcpp=32MHz, *3 at normal operation		-	85	122	mA	
			Operating frequency F_{CP}=128MHz, Fcpp=32MHz, *3 at Flash write *2		-	95	135	mA	
			Operating frequency F_{CP}=128MHz, Fcpp=32MHz, *3 at Flash erase *2		-	95	135	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	80	117	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write *2		-	90	130	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase *2		-	90	130	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	73	110	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write *2		-	83	123	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase *2		-	83	123	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	53	100	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write *2		-	63	113	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase *2		-	63	113	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	57	94	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	39	79	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*1	-	2000	3600	µA	
				When using built-in CR clock 50kHz, T_A=+25°C*1	-	640	2440		
				When using sub clock 32kHz, T_A=+25°C*1	-	660	2460		
	$I_{CCH}5$		Stop mode	T_A=+25°C*1	-	640	2440	µA	

Parameter	Symbol	Pin name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	$I_{CCT}52$	VCC	Watch mode (power off)	When using crystal 4MHz T_A=+25°C*1	-	1400	1600	µA	LVD/ RTC operation, Backup RAM 16KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*1	-	63	203		
				When using sub clock 32kHz T_A=+25°C*1	-	80	220		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*1	-	60	200	µA	Backup RAM 16KB retention

(T_A: -40°C to +125°C, V_{CC}= AVcc=5.5V±10%/ V_{CC}= AVcc=3.3V±0.3V ,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	$I_{CC}5$	VCC	Operating frequency F_{CP}=128MHz, Fcpp=32MHz, *3 at normal operation		-	85	122	mA	
			Operating frequency F_{CP}=128MHz, Fcpp=32MHz, *3 at Flash write *2		-	95	135	mA	
			Operating frequency F_{CP}=128MHz, Fcpp=32MHz, *3 at Flash erase *2		-	95	135	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at normal operation		-	80	117	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash write *2		-	90	130	mA	
			Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at Flash erase *2		-	90	130	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at normal operation		-	73	110	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash write *2		-	83	123	mA	
			Operating frequency F_{CP}=64MHz, Fcpp=32MHz, at Flash erase *2		-	83	123	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at normal operation		-	53	100	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash write *2		-	63	113	mA	
			Operating frequency F_{CP}=48MHz, Fcpp=24MHz, at Flash erase *2		-	63	113	mA	
	$I_{CCS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at CPU sleep mode		-	57	94	mA	
	$I_{CCBS}5$		Operating frequency F_{CP}=80MHz, Fcpp=40MHz, at bus sleep mode		-	39	79	mA	
	$I_{CCT}5$		Watch mode	When using crystal 4MHz T_A=+25°C*1	-	2000	3600	μA	
				When using built-in CR clock 50kHz T_A=+25°C*1	-	640	2440		
				When using sub clock 32kHz T_A=+25°C*1	-	660	2460		
	$I_{CCH}5$		Stop mode	T_A=+25°C*1	-	640	2440	μA	

Parameter	Symbol	Pin name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	$I_{CCT}52$	VCC	Watch mode (power off)	When using crystal 4MHz T_A=+25°C*1	-	1400	1600	µA	LVD/ RTC operation, Backup RAM 16KB retention
				When using built-in CR clock 50kHz , T_A=+25°C*1	-	63	203		
				When using sub clock 32kHz T_A=+25°C*1	-	80	220		
	$I_{CCH}52$		Stop mode (power off)	T_A=+25°C*1	-	60	200	µA	Backup RAM 16KB retention

*1: It is a standard in BRAMSC (Backup RAM sleep control bit)=1(Enter the state of the sleep at the standby mode) condition.
*2: It is a prohibition two flash or more writing/erasing the flash and the WorkFlash for the internally stored program at the same time.
*3: There is a frequency limitation by the product type. Please see "4. AC Characteristics" for details.

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/Vcc=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	All input pins	V_{CC}=AV_{CC}=5.5V V_{SS}<V_I<V_{CC}	-5	-	5	µA	
Input capacitance 1	C_{IN1}	Other than VCC,VCCE, VSS, AVCC, AVSS, C	-	-	5	15	pF	
Pull-up resistance	R_{UP1}	RSTX, NMIX	V_{CC}=5.0V±10 %	25	-	100	kΩ	
			Vcc=3.3V±0.3 V	45	-	140		
	R_{UP2}	P073,074,077	V_{CC}=5.0V±10 %	25	-	60	kΩ	
			Vcc=3.3V±0.3 V	33	-	90		
	R_{UP3}	Port pin other than P035,041,073,074,077, 093, 122,222,227, 232,236	V_{CC}=5.0V±10 %	25	-	100	kΩ	
			Vcc=3.3V±0.3 V	45	-	140		
"H" level output voltage[*1]	V_{OH1}	Normal output pin	Vcc=4.5V I_{OH}=-4.0mA	V_{CC} -0.5	-	V_{CC}	V	
			Vcc=3.0V I_{OH}=-2.0mA					
		P076,200,201, 204,205,210, 211,214,215, 220,221,225, 226,230,231, 234,235	Vcc=4.5V I_{OH}=-4.0mA	V_{CC} -0.5	-	V_{CC}	V	When I^2C function is non-selected
			Vcc=3.0V I_{OH}=-2.0mA					
	V_{OH2}	P073,074,077	Vcc=4.5V I_{OH}=-3.0mA	V_{CC} -0.5	-	V_{CC}	V	I^2C pin output
		P076,200,201, 204,205,210, 211,214,215, 220,221,225, 226,230,231, 234,235	Vcc=4.5V I_{OH}=-3.0mA	V_{CC} -0.5	-	V_{CC}	V	When I^2C function is non-selected
	V_{OH3}	P103 to 106	Vcc=4.5V I_{OH}=-12.0mA	V_{CC} -0.5	-	V_{CC}	V	
			Vcc=3.0V I_{OH}=-8.0mA					

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	Normal output pin	Vcc=4.5V I_{OL}=4.0mA / Vcc=3.0V I_{OL}=2.0mA	0	-	0.4	V	
		P076,200,201, 204,205,210, 211,214,215, 220,221,225, 226,230,231, 234,235	Vcc=4.5V I_{OL}=4.0mA / Vcc=3.0V I_{OL}=2.0mA	0	-	0.4	V	When I^2C function is non-selected
	V_{OL2}	P073,074,077	Vcc=4.5V I_{OL}=3.0mA	0	-	0.4	V	I^2C pin output
		P076,200,201, 204,205,210, 211,214,215, 220,221,225, 226,230,231, 234,235	Vcc=4.5V I_{OH}=-3.0mA	0	-	0.4	V	When I^2C function is non-selected
	V_{OL3}	P103 to 106	Vcc=4.5V I_{OL}=12.0mA / Vcc=3.0V I_{OL}=8.0mA	0	-	0.4	V	
"H" level input voltage[*1]	V_{IH1}	P000,002,003, 005,020,022, 024,026,035, 041,045,055, 057,071-077, 081,082,093, 096,097, 100-102, 111,115,116, 122,126,130, 134,150,151, 153,200-202, 204-206, 210-212, 214-216, 220-222, 225-227, 230-232, 234-236, TCK, TDI, TMS, TRST	CMOS hysteresis input level	0.7× V_{CC}	-	V_{CC}	V	
	V_{IH2}	P001,004,006, 007,010-017, 052,114,120, 123,155	CMOS hysteresis input level	0.7× V_{CC}	-	V_{CC}	V	
	V_{IH3}		Automotive input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IH4}	Port other than V_{IH1},V_{IH2},V_{IH3}	Automotive input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IH5}	RSTX,NMIX,MD0,MD1	CMOS hysteresis input level	0.8× V_{CC}	-	V_{CC}	V	
	V_{IHT}	DEBUGIF	TTL input level	2	-	V_{CC}	V	

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage*1	V_{IL1}	P000,002,003, 005,020,022, 024,026,035, 041,045,055, 057,071-077, 081,082,093, 096,097, 100-102,111, 115,116,122, 126,130,134, 150,151,153, 200-202, 204-206, 210-212, 214-216, 220-222, 225-227, 230-232, 234-236, TCK, TDI, TMS, TRST	CMOS hysteresis input level	Vss	-	0.3× V_{CC}	V	
	V_{IL2}	P001,004,006, 007,010-017, 052,114,120, 123,155	CMOS hysteresis input level	Vss	-	0.3× V_{CC}	V	
	V_{IL3}		Automotive input level	Vss	-	0.5× V_{CC}	V	
	V_{IL4}	Port other than V_{IH1},V_{IH2},V_{IH3}	Automotive input level	Vss	-	0.5× V_{CC}	V	
	V_{IL5}	RSTX,NMIX,MD0,MD1	CMOS hysteresis input level	Vss	-	0.2× V_{CC}	V	
	V_{ILT}	DEBUGIF	TTL input level	Vss	-	0.8	V	

*1: It is provided by V_{CCE} for the pin corresponding to the V_{CCE} power supply instead of V_{CC}. Please see "PRODUCT LINEUP" for details.

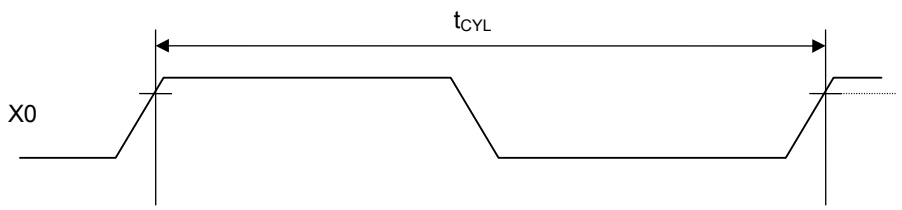
14. AC Characteristics

(1) Main Clock Timing
(T_A: -40°C to +125°C,V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS} =AV_{SS}=0.0V)

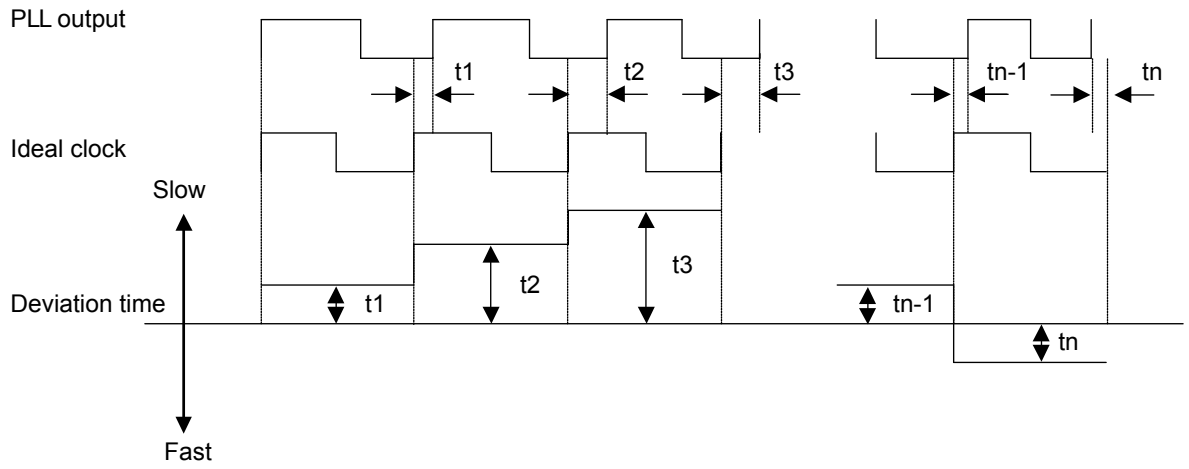
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	-	4	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		62.5	250	-	ns	
Internal operating clock frequency *1	F_{CP}	-		2	-	128	MHz	CPU clock *3
	F_{CPP}			1		40		Peripheral bus clock
	F_{CPT}			1		40		External bus clock (When V_{CC}=5.0V is used) *2
				1		32		External bus clock (When V_{CC}=3.3V is used)
Internal operating clock cycle time *1	t_{CP}	-		7.82	-	500	ns	CPU clock *4
	t_{CPP}			25		1000		Peripheral bus clock
	t_{CPT}			25		1000		External bus clock (When V_{CC}=5.0V is used)
				31.25		1000		External bus clock (When V_{CC}=3.3V is used)
CAN PLL jitter (during lock)	t_{PJ}	-		-10	-	10	ns	F_{CP}=80MHz (4MHz × Multiplied by 20)
Built-in CR oscillation frequency	F_{CCR}	-		50	100	150	kHz	

*1: The maximum / minimum value is defined when using the main clock and PLL clock.
*2: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).
*3: MB91F52xR/MB91F52xU(LQS144/LQN144/LQP176) is 80MHz or less.
MB91F52xR/MB91F52xU(LES144/LEP176) and MB91F52xM/MB91F52xY is 128MHz or less.
*4: MB91F52xR/MB91F52xU(LQS144/LQN144/LQP176) is 12.5ns or more.
MB91F52xR/MB91F52xU(LES144/LEP176) and MB91F52xM/MB91F52xY is 7.82ns or more.

·X0,X1 clock timing



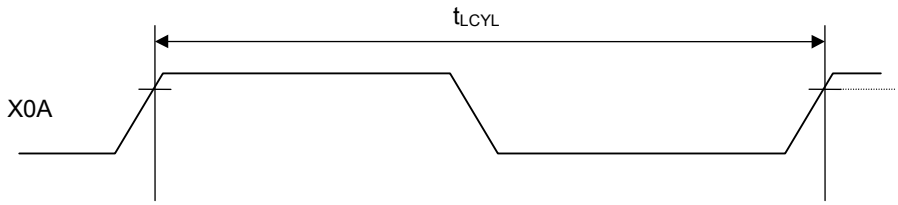
·CAN PLL jitter
Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



(1-2) Sub clock timing
(T_A: -40°C to +125°C,V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

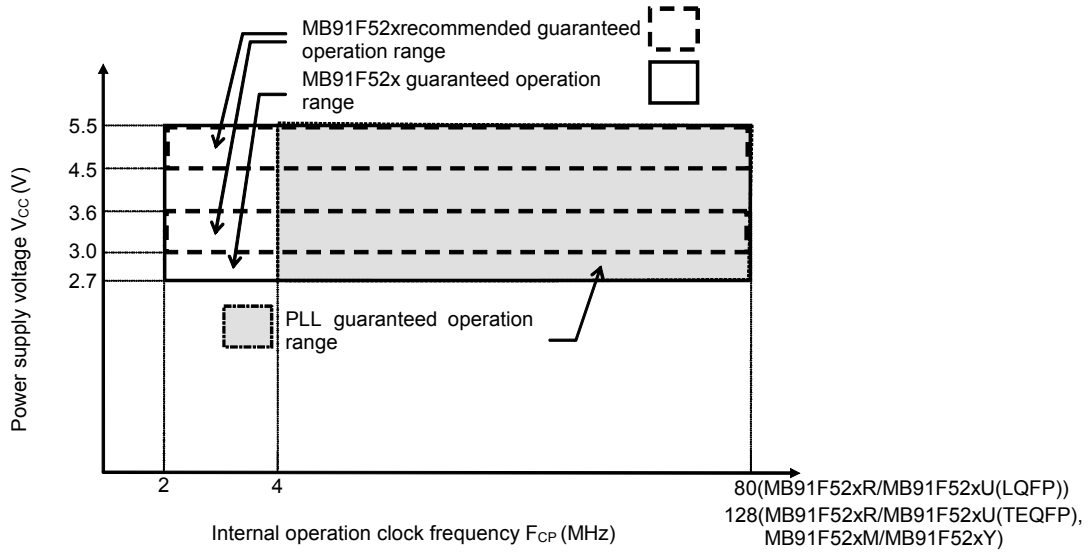
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A		-	30.52	-	µs	

·X0A,X1A clock timing



・Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

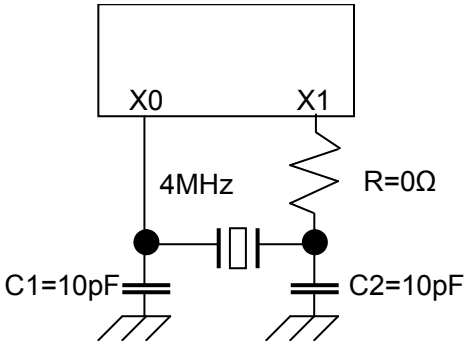


Note: The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency							
		Main Clock	PLL clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 31	Multiplied by 32
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	124MHz	128MHz

·Example of oscillation circuit



Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.

AC characteristics are specified by the following measurement reference voltage values.

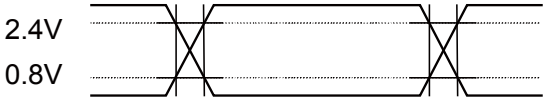
● Input Signal Waveform

Hysteresis Input Pin (Automotive)

Hysteresis Input Pin (CMOS schmitt)

● Output Signal Waveform

Output Pin



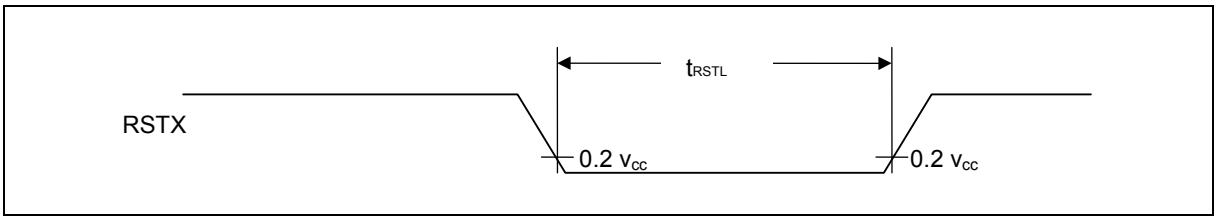
(2) Reset Input

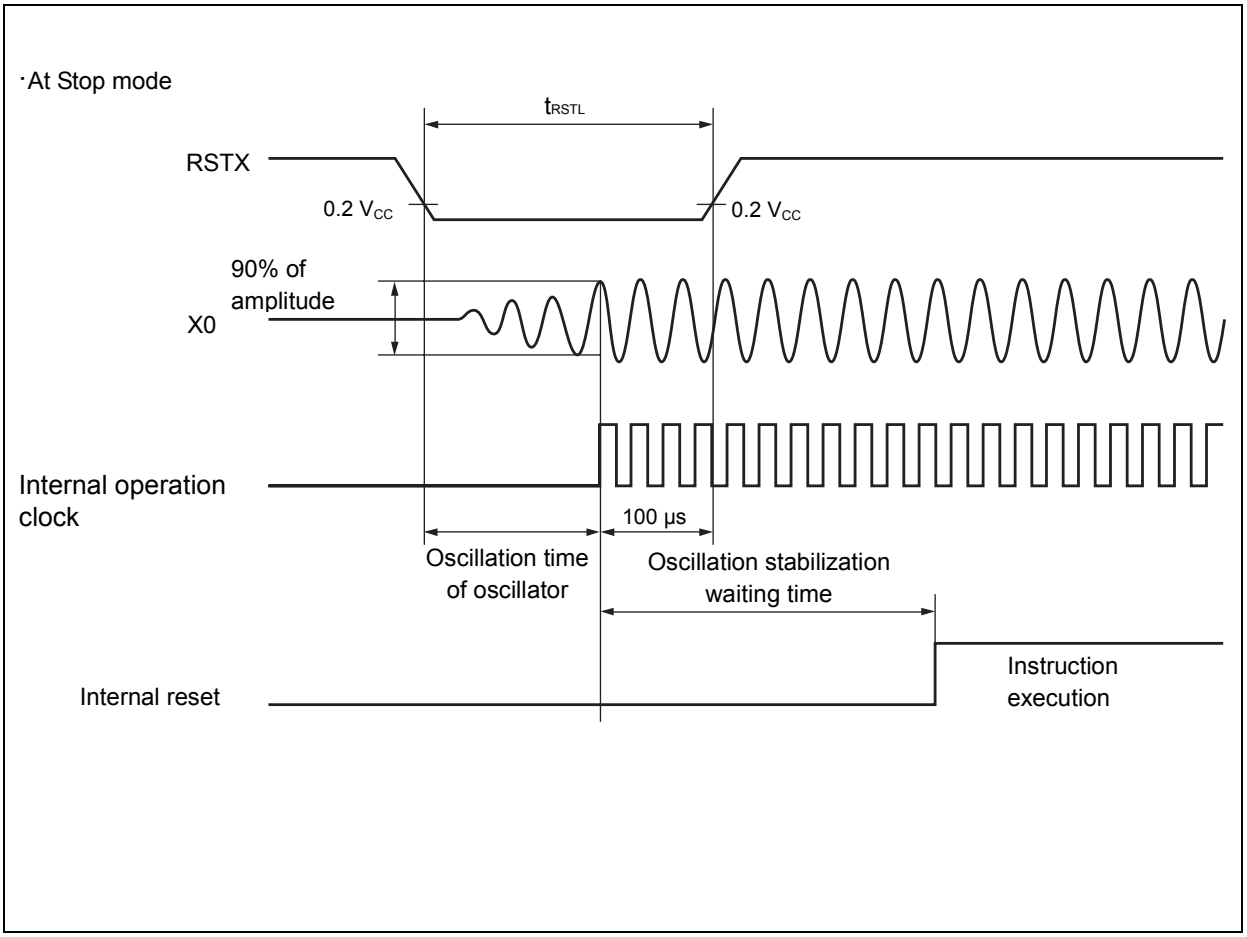
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	–	10	–	µs	When normal operation
				Oscillation time of oscillator* +100	–	µs	At Stop mode At Power-on*2
				100	–	µs	At Watch mode
Width for reset input removal				1	–	µs	

*1: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

*2: In case of using MB91F52xxxD or MB91F52xxxE and corresponding to note in (3) Power-on Conditions of next subsection, assert RSTX with power-on.





(3) Power-on Conditions

(3-1) [MB9152xxxC/MB9152xxxD]

(T_A: -40°C to +125°C , V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V_{CC}	–	2.024	2.2	2.376	V	
Level detection hysteresis width	–	V_{CC}	–	–	100	–	mV	
Level detection time	–	–	–	–	–	30	µs	*1
Power off time	t_{OFF}	V_{CC}	–	50	–	–	ms	*2
Power ramp rate	dV/dt	V_{CC}	VCC: 0.2V to 2.376V	–	–	4	mV/µs	*3
C pin voltage at Power-on	–	C	–	–	–	60	mV	*4

*1: This spec is at 4mV/µs of power ramp rate. If the power ramp rate is faster than 4mV/µs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Vcc must be held below 0.2V for a minimum period of t_{OFF}.

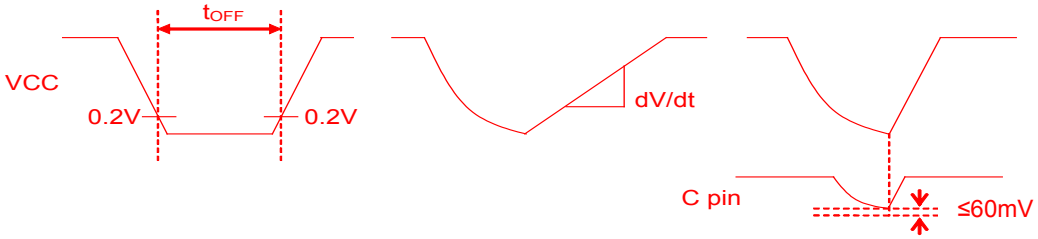
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when VCC is turned on again.

Note:

When using MB91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use MB91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

・Power off time, Power ramp rate, C pin voltage at Power-on



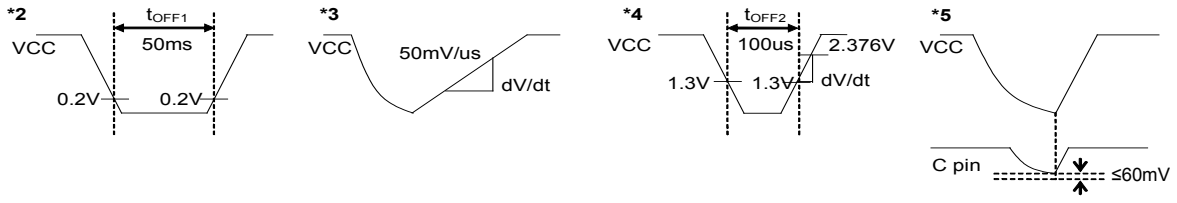
(3-2) [MB9152xxxE]
(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V_{CC}	–	2.024	2.2	2.376	V	
Level detection hysteresis width	–	V_{CC}	–	–	100	–	mV	
Level detection time	–	–	–	–	–	30	µs	*1
Power off time	t_{OFF1}	V_{CC}	Vcc ≤ 0.2V	50	–	–	ms	*2
	t_{OFF2}	V_{CC}	Vcc ≤ 1.3V	100	–	–	µs	*4
Power ramp rate	dV/dt	V_{CC}	VCC: 0.2V to 2.376V (t_{OFF1}〈50ms)	–	–	50	mV/µs	*3
	dV/dt	V_{CC}	VCC: 1.3V to 2.376V (t_{OFF2} ≥ 100µs)	–	–	1000	mV/µs	*4
C pin voltage at Power-on	–	C	–	–	–	60	mV	*5
Maximum ramp rate guaranteed to not generate power-on reset	|dV/dt|	Vcc	VCC: Between 2.4V and 4.5V	–	–	50	mV/µs	*6

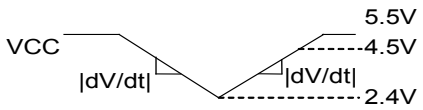
*1: The specified level detection time applies only for power ramp rate of 1000mV/µs or less.
*2: Vcc must be held below 0.2V for a minimum period of t_{OFF1}.
*3: Power-on can detect by satisfying power ramp rate when t_{OFF1} is not satisfied.
*4: Vcc must be held below 1.3V for a minimum period of t_{OFF2}.
Power ramp rate must be 1000mV/µs or less from 1.3V to 2.376V.
Power-on can detect by satisfying power ramp rate and power off time.
*5: C-pin voltage is below 60 mV when VCC is turned on again.
*6: This specification is specified the power supply fluctuation after power on detection. When VCC voltage is between 2.4V and 4.5V, the power supply fluctuation is below 50mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5V and 5.5V.

Note: When using MB91F52xxxE, either *2 or *3 or *4 or *5 must be satisfied. When neither *2 nor *3 nor *4 nor *5 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

・Power off time, Power ramp rate, C pin voltage at Power-on



・Maximum ramp rate guaranteed to not generate power-on reset



(4) Multi-function Serial

(4-1) CSIO timing

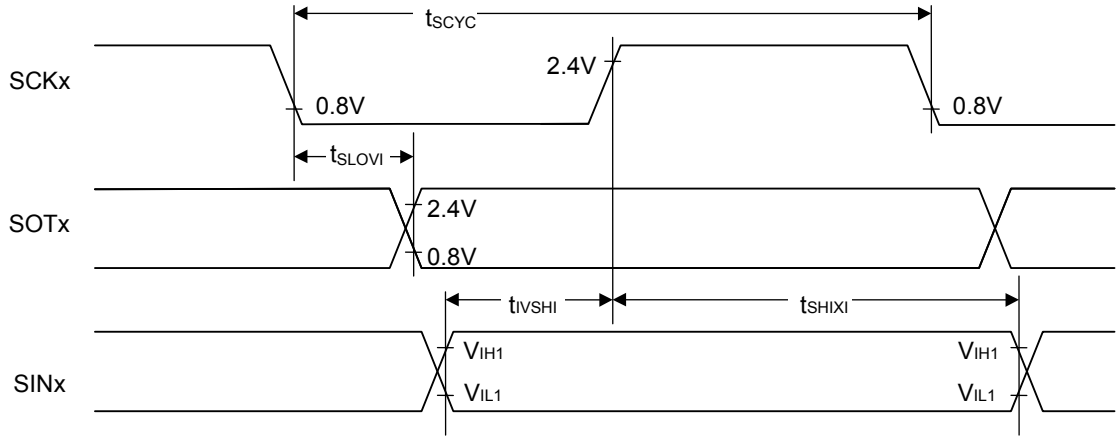
(4-1-1) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=0, SCR:SPI=0

(T_A: -40°C to +125°C , V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

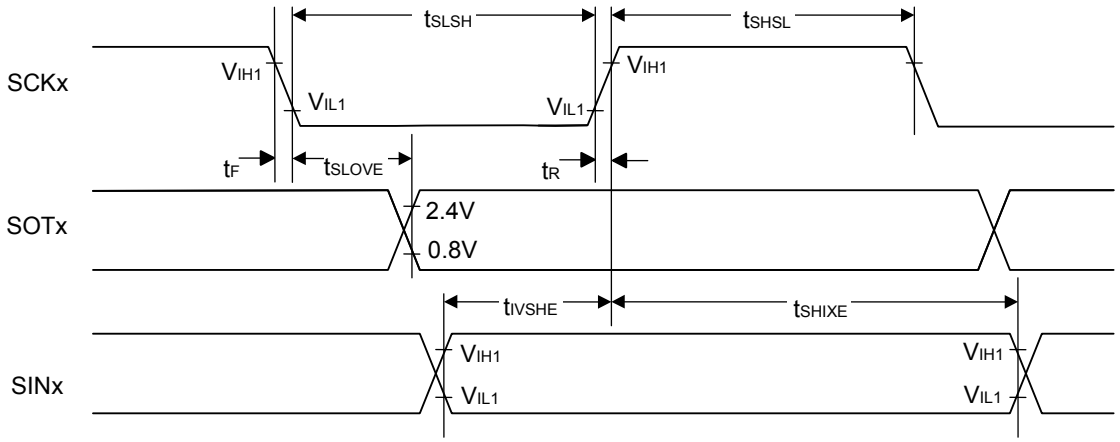
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK19	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-30	30	ns	
		SCK3, SCK4 SOT3, SOT4		-300	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK19 SIN0 to SIN2, SIN5 to SIN19		34	-	ns	
		SCK3, SCK4 SIN3, SIN4		300	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK19 SIN0 to SIN19		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK19	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-	33	ns	
		SCK3, SCK4 SOT3, SOT4		-	300	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK19 SIN0 to SIN19		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK19		-	5	ns	
SCK rise time	t_R	SCK0 to SCK19		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



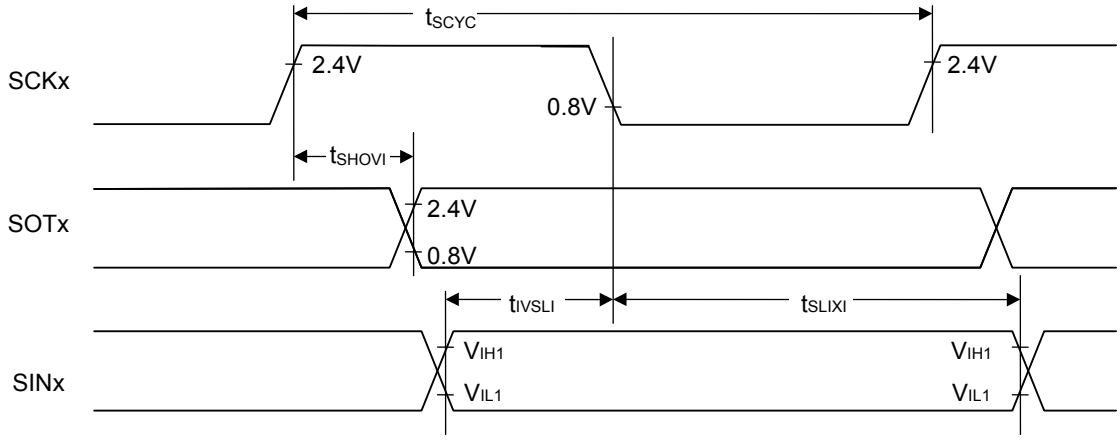
(4-1-2) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=1, SCR:SPI=0

(T_A: -40°C to +125°C , V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

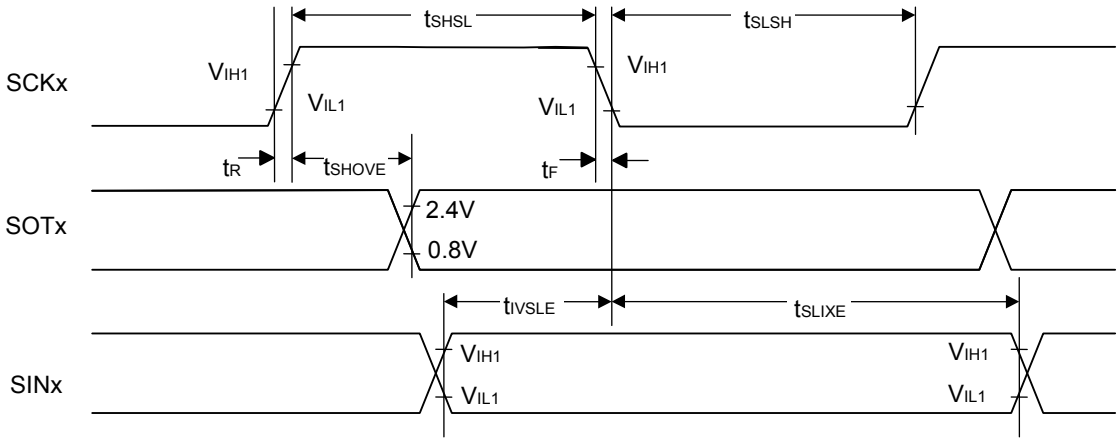
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK19	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-30	30	ns	
		SCK3, SCK4 SOT3, SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK19 SIN0 to SIN2, SIN5 to SIN19		34	-	ns	
		SCK3, SCK4 SIN3, SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK19 SIN0 to SIN19		0	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK19	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-	33	ns	
		SCK3, SCK4 SOT3, SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK19 SIN0 to SIN19		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK19		-	5	ns	
SCK rise time	t_R	SCK0 to SCK19		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode

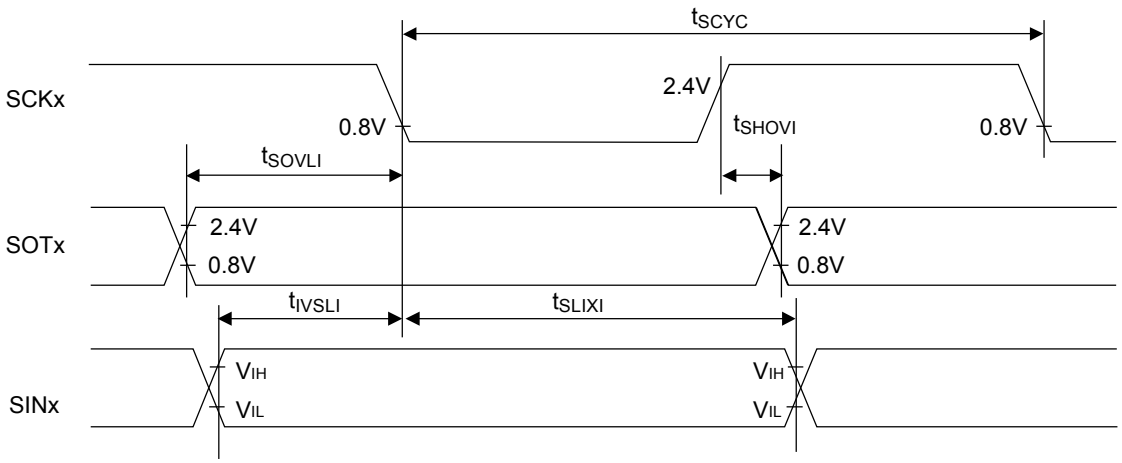


(4-1-3) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=0, SCR:SPI=1
(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

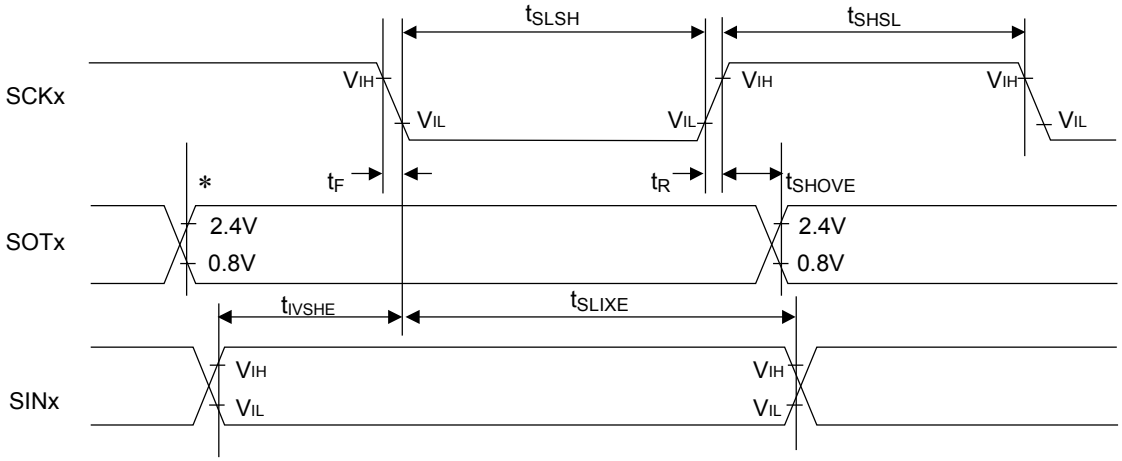
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK19	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-30	30	ns	
		SCK3, SCK4 SOT3, SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK2, SCK5 to SCK19 SIN0 to SIN2, SIN5 to SIN19		34	-	ns	
		SCK3, SCK4 SIN3, SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK19 SIN0 to SIN19		0	-	ns	
SOT→SCK↓ delay time	t_{SOVLI}	SCK0 to SCK19 SOT0 to SOT19		$2t_{CPP}$-30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK19	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-	33	ns	
		SCK3, SCK4 SOT3, SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t_{IVSHE}	SCK0 to SCK19 SIN0 to SIN19		10	-	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK19		-	5	ns	
SCK rise time	t_R	SCK0 to SCK19		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.

·Internal shift clock mode



· External shift clock mode



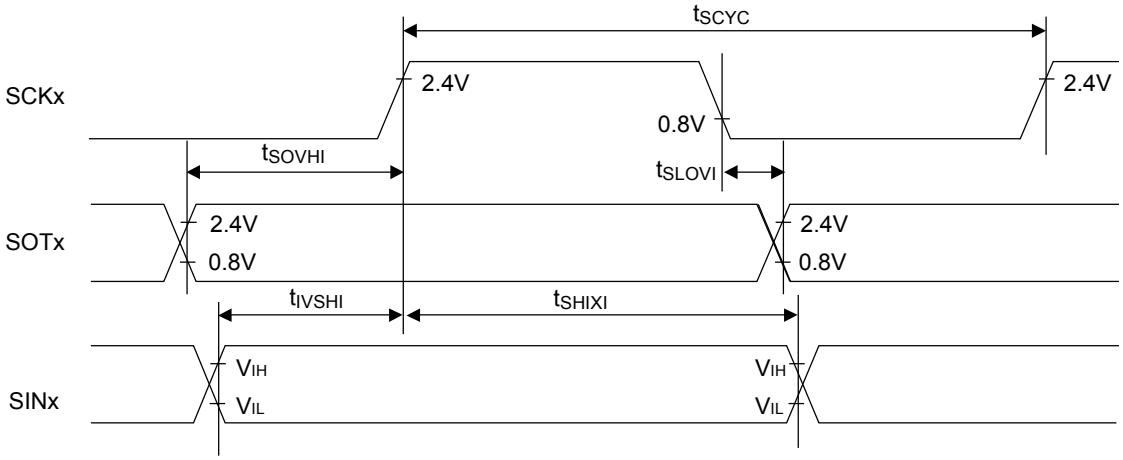
*: It writes in the TDR register and, then, it changes.

(4-1-4) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=1, SCR:SPI=1
(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

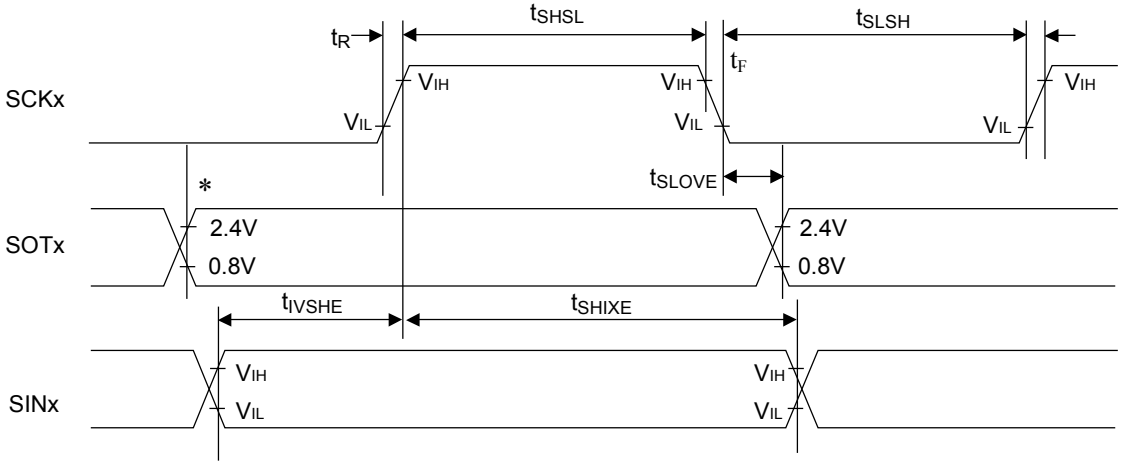
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK19	-	$4t_{CPP}$	-	ns	Internal shift clock mode output pin : C_L=50pF
SCK↓→ SOT delay time	t_{SLOVI}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-30	30	ns	
		SCK3, SCK4 SOT3, SOT4		-300	300	ns	
Valid SIN → SCK↑setup time	t_{IVSHI}	SCK0 to SCK2, SCK5 to SCK19 SIN0 to SIN2, SIN5 to SIN19		34	-	ns	
		SCK3, SCK4 SIN3, SIN4		300	-	ns	
SCK↑→ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK19 SIN0 to SIN19		0	-	ns	
SOT→SCK↑ delay time	t_{SOVHI}	SCK0 to SCK19 SOT0 to SOT19		$2t_{CPP}$-30	-	ns	
Serial clock "H"pulse width	t_{SHSL}	SCK0 to SCK19	-	t_{CPP}+10	-	ns	External shift clock mode output pin: C_L=50pF
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK↓→ SOT delay time	t_{SLOVE}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-	33	ns	
		SCK3, SCK4 SOT3, SOT4		-	300	ns	
Valid SIN → SCK↑setup time	t_{IVSHE}	SCK0 to SCK19 SIN0 to SIN19		10	-	ns	
SCK↑→ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK19		-	5	ns	
SCK rise time	t_R	SCK0 to SCK19		-	5	ns	

Notes:
AC characteristic in CLK synchronized mode.
C_L is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.
See Hardware Manual for details.

・Internal shift clock mode



・External shift clock mode



*: It writes in the TDR register and, then, it changes.

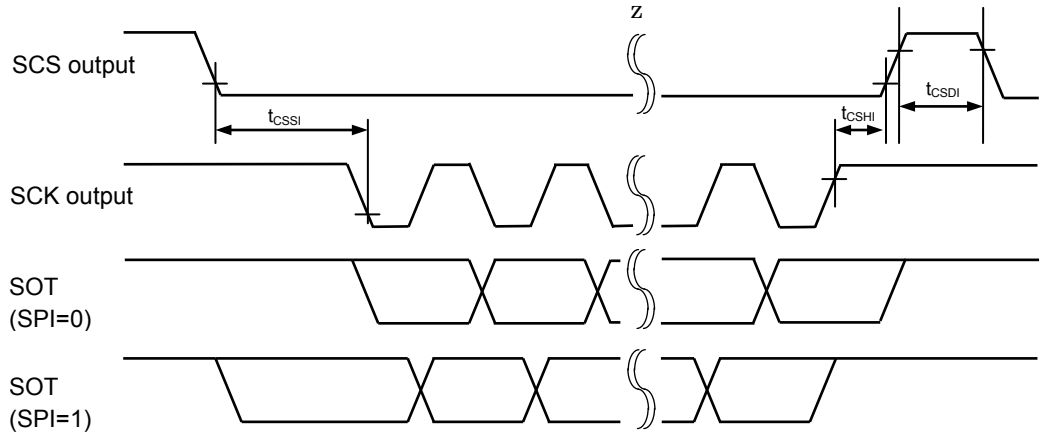
(4-1-5) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1
(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

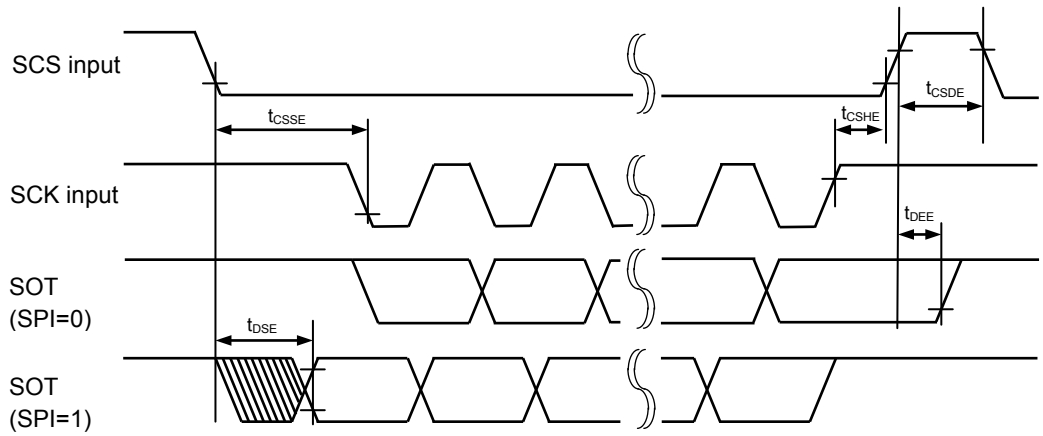
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↑→SCS↑ hold time	t_{CSHI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	
SCS↓→SCK↓ setup time	t_{CSSE}	SCK1 to SCK15, SCK18, SCK19 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑→SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		$3t_{CPP}$+30	-	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SOT delay time	t_{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1, SOT2, SOT5 to SOT15, SOT18, SOT19	-	-	40	ns	External shift clock mode output pin: C_L=50pF
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS↑→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1 to SOT15, SOT18, SOT19		+0	-	ns	
SCK↓→SCS↓ clock switch time	t_{SCC}	SCK1,SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

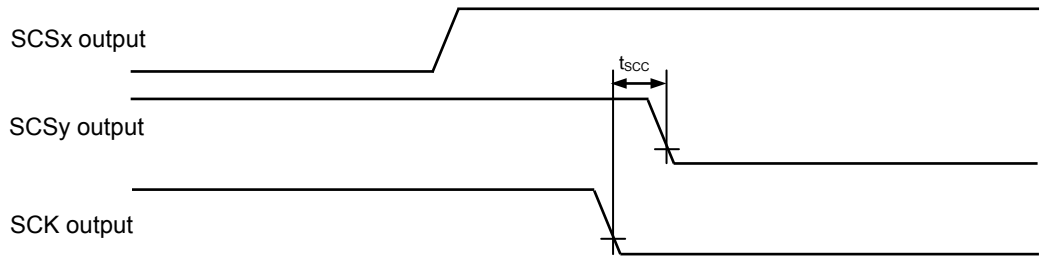
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operating clock
*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operating clock
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again.

Please see the hardware manual for details of above-mentioned *1,*2, and *3.





When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

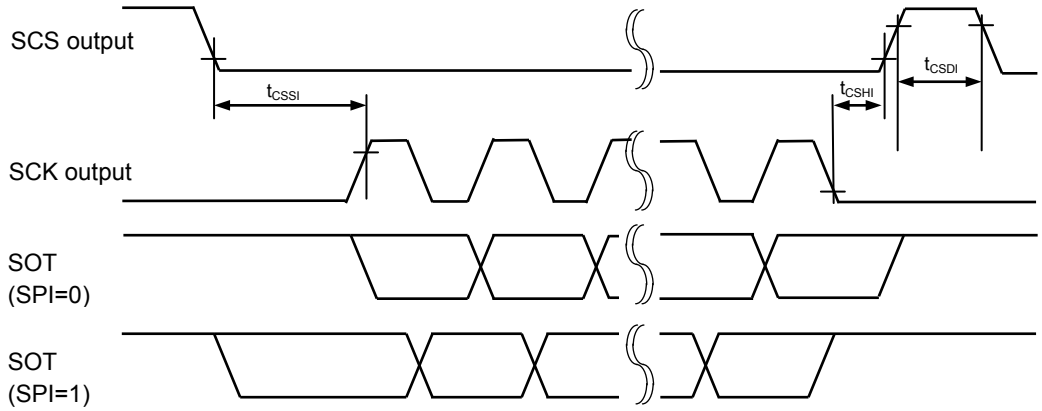
(4-1-6) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1
(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↓→SCS↑ hold time	t_{CSHI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	
SCS↓→SCK↑ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}			$3t_{CPP}$+30	-	ns	

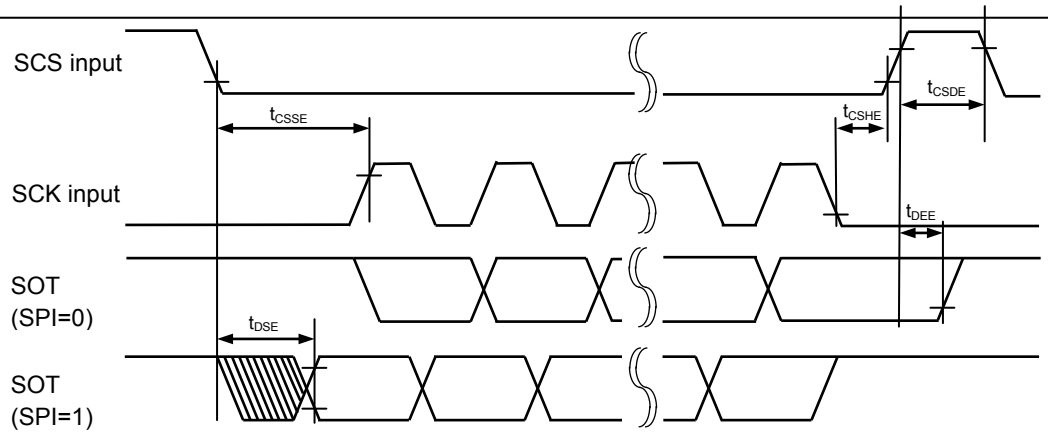
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SOT delay time	t_{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1, SOT2, SOT5 to SOT15, SOT18, SOT19	-	-	40	ns	External shift clock mode output pin: C_L=50pF
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS↑→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1 to SOT15, SOT18, SOT19		+0	-	ns	
SCK↑→SCS↓ clock switch time	t_{SCC}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operating clock
*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operating clock
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again.

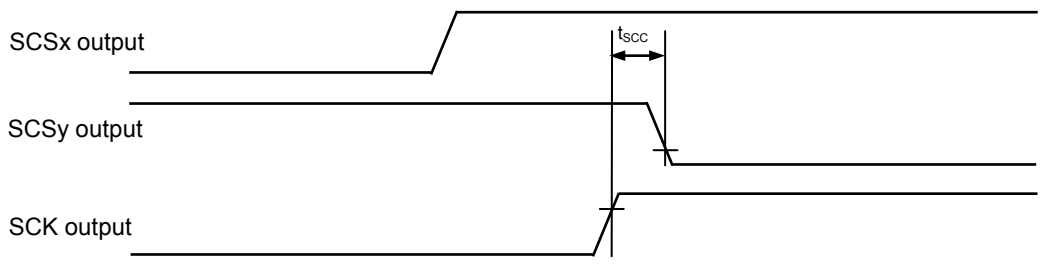
Please see the hardware manual for details of above-mentioned *1,*2, and *3



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

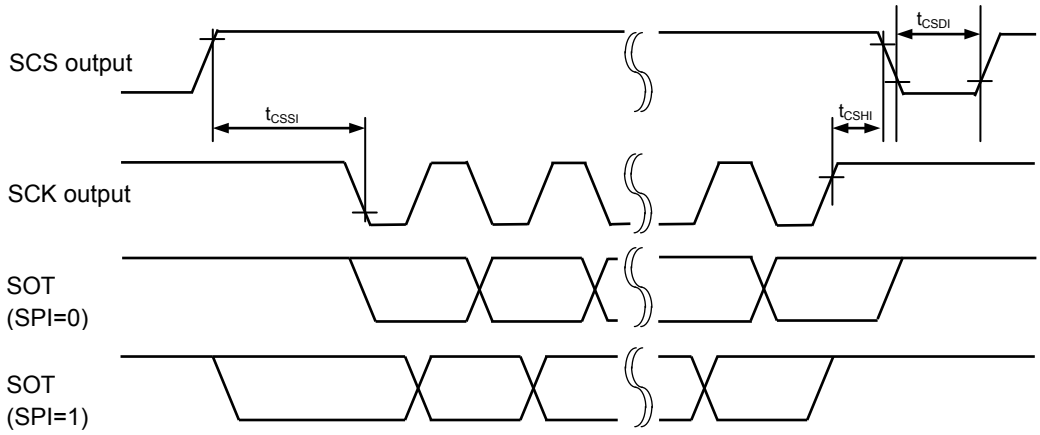
(4-1-7) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0
(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↓ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↑→SCS↓ hold time	t_{CSHI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	
SCS↑→SCK↓ setup time	t_{CSSE}	SCK1 to SCK15, SCK18, SCK19 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑→SCS↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		$3t_{CPP}$+30	-	ns	

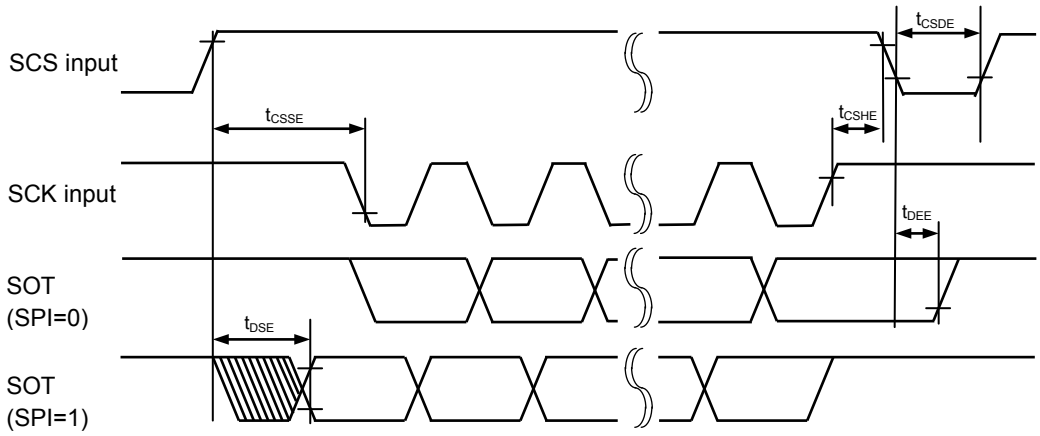
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SOT delay time	t_{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCK18, SCK19 SOT1, SOT2, SOT5 to SOT15, SOT18, SOT19	-	-	40	ns	External shift clock mode output pin: C_L=50pF
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS↓→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15 SCK18, SCK19 SOT1 to SOT15, SOT18, SOT19		+0	-	ns	
SCK↓→SCS↑ clock switch time	t_{SCC}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1,SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operating clock
*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operating clock
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again.

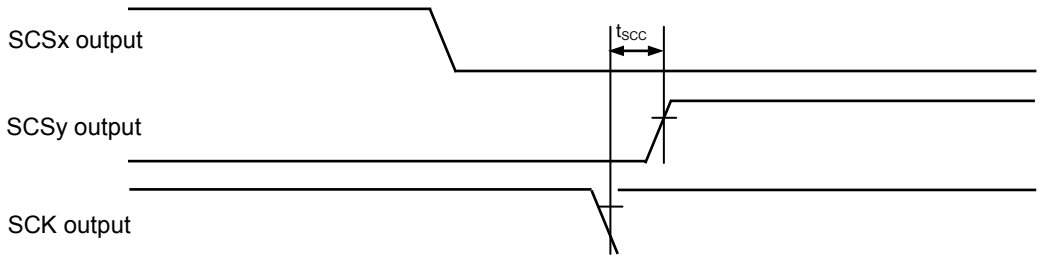
Please see the hardware manual for details of above-mentioned *1,*2, and *3.



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

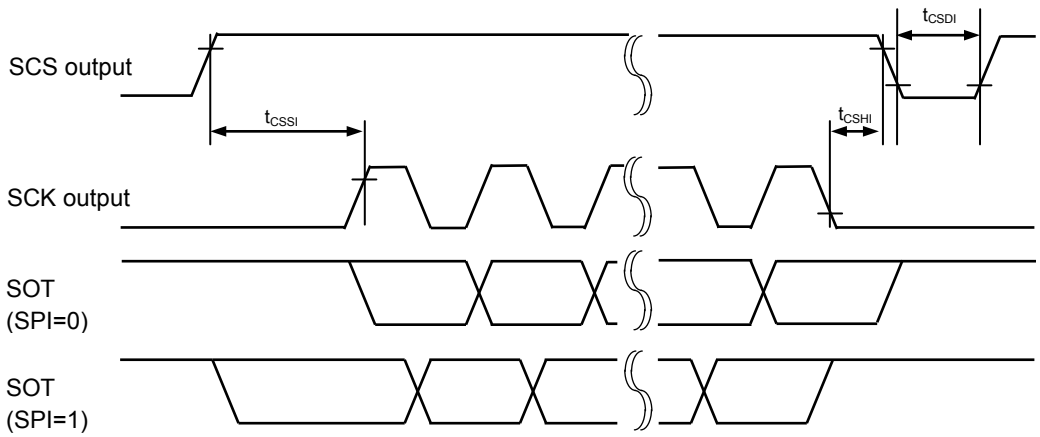
(4-1-8) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used: SCSCR:CSEN=1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0
(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11, SCS18, SCS19	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↓→SCS↓ hold time	t_{CSHI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11, SCS18, SCS19		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11, SCS18, SCS19		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	
SCS↑→SCK↑ setup time	t_{CSSE}	SCK1 to SCK15, SCK18, SCK19 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		$3t_{CPP}$+30	-	ns	

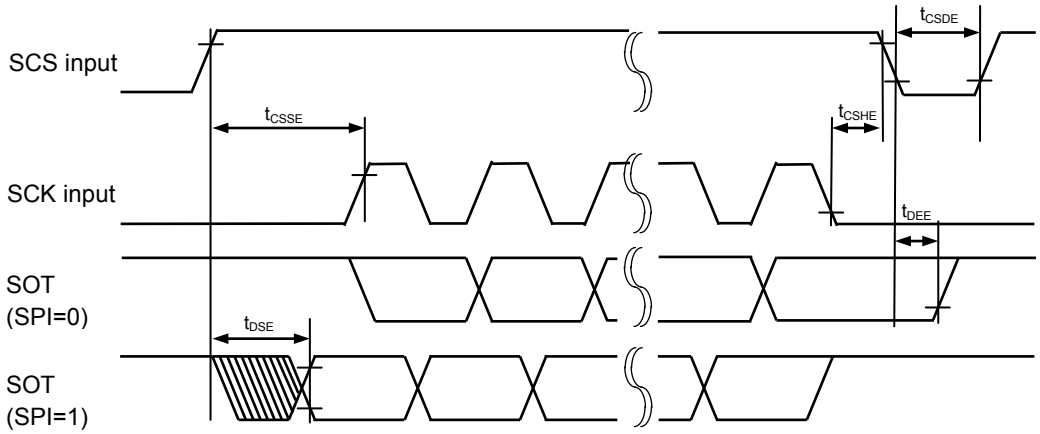
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SOT delay time	t_{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1, SOT2, SOT5 to SOT15, SOT18, SOT19	-	-	40	ns	External shift clock mode output pin: C_L=50pF
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS↓→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1 to SOT15, SOT18, SOT19		+0	-	ns	
SCK↑→SCS↑ clock switch time	t_{SCC}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operating clock
*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operating clock
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again.

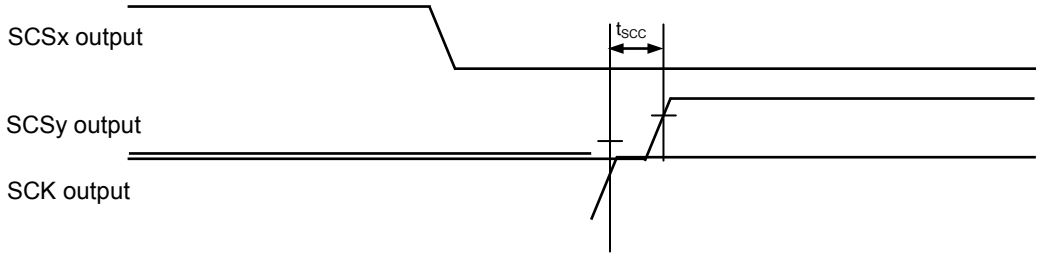
Please see the hardware manual for details of above-mentioned *1,*2, and *3.



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Slave mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

(4-2) UART (Asynchronous serial interface) timing

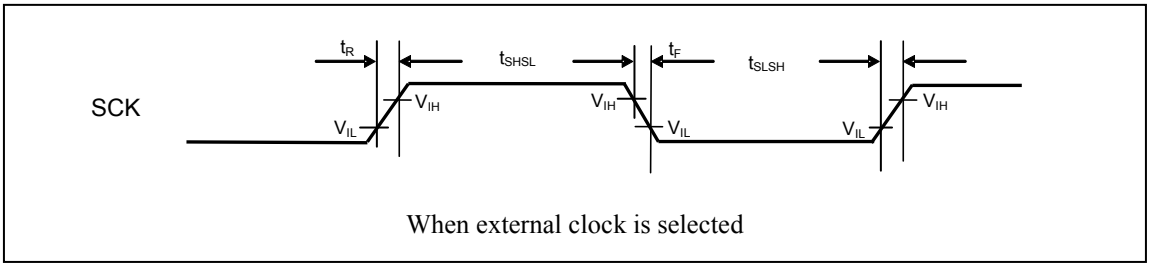
Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=0

Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=1

When external clock is selected (BGR:EXT=1)

(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

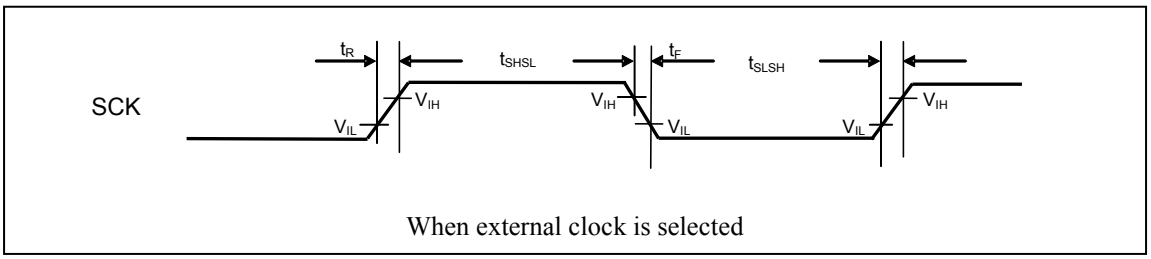
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK19	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When external clock is selected

(4-3) LIN Interface (v2.1)(Asynchronous Serial Interface for LIN (v2.1)) timing
Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=1
(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK19	-	t_{CPP} +10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP} +10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When external clock is selected

(4-4) I^2C timing

(T_A: -40°C to +125°C,V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Standard mode		Fast mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK3 to SCK8, SCK11 to SCK19	C_L=50pF R= (V_P/I_{OL}) *1	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOT3 to SOT8, SOT11 to SOT19 (SDA), SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.0	–	0.6	–	µs	
Period of "L" for SCL clock	t_{LOW}	SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.7	–	1.3	–	µs	
Period of "H" for SCL clock	t_{HIGH}	SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.0	–	0.6	–	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.7	–	0.6	–	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOT3 to SOT8, SOT11 to SOT19 (SDA) SCK3 to SCK8, SCK11 to SCK19 (SCL)		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SOT3 to SOT8, SOT11 to SOT19 (SDA) SCK3 to SCK8, SCK11 to SCK19 (SCL)		250	–	100	–	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SOT3 to SOT8, SOT11 to SOT19 (SDA) SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.0	–	0.6	–	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	–		4.7	–	1.3	–	µs	
Noise filter	t_{SP}	–	–	$2t_{CPP}$*4	–	$2t_{CPP}$*4	–	ns	

Notes: Only ch.3, ch.4 and ch.12-ch.19 are standard mode/fast mode correspondence. In ch.5-ch.8 and ch.11, only a standard mode is correspondences.

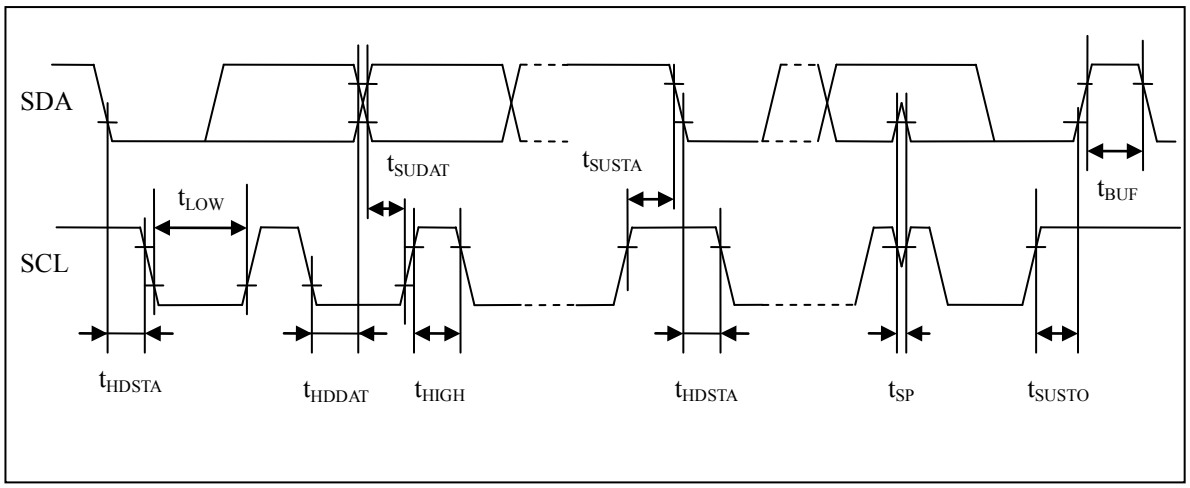
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. Vp shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A fast mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8MHz or more when use I^2C.

·I²C timing

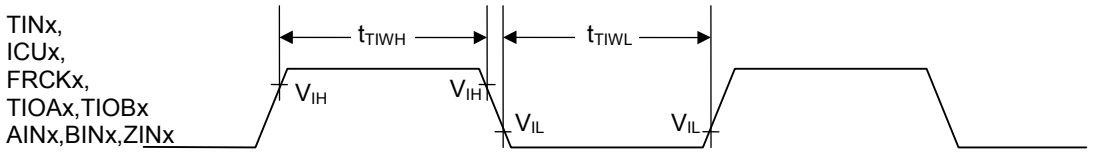


(5) Timer input timing

(T_A: -40°C to +125°C , V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0 to TIN7, ICU0 to ICU11, FRCK0 to FRCK10, TIOA0, TIOA1, TIOB0, TIOB1, AIN0 to AIN3, BIN0 to BIN3, ZIN0 to ZIN3	–	$4t_{CPP}$	–	ns	

·Timer input timing

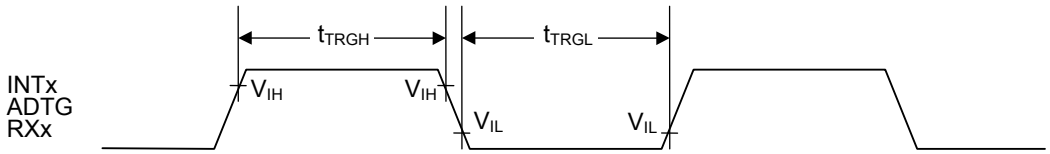


(6) Trigger input timing

(T_A: -40°C to +125°C, ,V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT23, ADTG0, ADTG1, RX0 to RX5	–	$5t_{CPP}$	–	ns	
				1	–	µs	At stop mode

·Trigger input timing

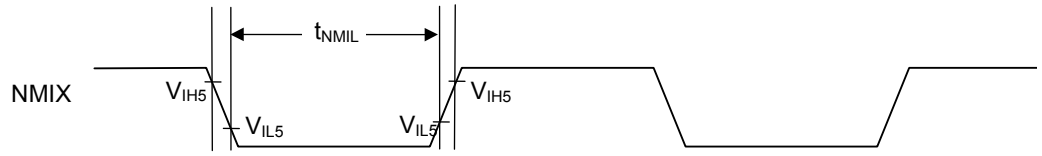


(7) NMI input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	–	$4t_{CPP}$	–	ns	

·NMIX input timing



(8) Low voltage detection (External low-voltage detection)
(T_A: -40°C to +125°C , V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC	-	2.7	-	5.5	V	
Detection voltage*3	V_{DL}		*1	-8%	LVD5F_SEL[3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.
Hysteresis width	V_{HYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	Td	-		-	-	30	µs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.
*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low voltage detection by detecting voltage (V_{DL}).
*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).
This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7V).
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(9) Low voltage detection (Internal low-voltage detection)
(T_A: -40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage*2	V_{RDL}		*1	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	-	-		-	-	30	µs	

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.
*2: The detection voltage of the internal low voltage detection is 0.9V±0.1V.
This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(10) External bus I/F (synchronous mode) timing
(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

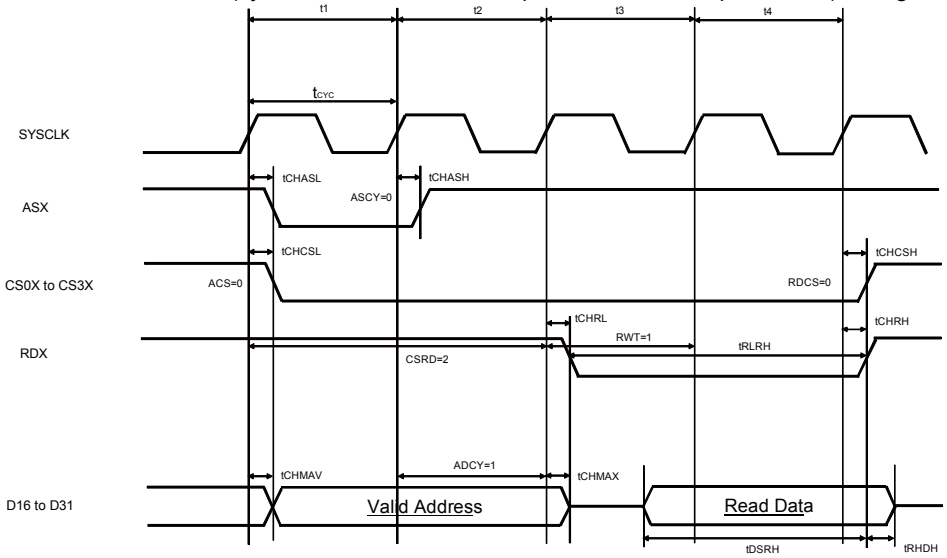
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	V_{CC}=5.0V±10% *1
			31.25			V_{CC}=3.3V±0.3V
ASX delay time	t_{CHASL}, t_{CHASH}	SYSCLK, ASX	0.5	18	ns	
CS0X to CS3X delay time	t_{CHCSL}, t_{CHCSH}	SYSCLK, CS0X to CS3X	0.5	18	ns	
A00 to A21 delay time	t_{CHAV}, t_{CHAX}	SYSCLK, A00 to A21	0.5	18	ns	
RDX delay time	t_{CHRL}, t_{CHRH}	SYSCLK, RDX	0.5	18	ns	
RDX minimum pulse	t_{RLRH}	RDX	t_{CYC}× 2 - 20	-	ns	RWT=1, set RWT to 1 or more. *2
Data setup → RDX↑time	t_{DSRH}	RDX, D16 to D31	18+t_{CYC}	-	ns	Same as above
RDX↑→ data hold	t_{RHDH}		0	-	ns	
WRnX delay time	t_{CHWL}, t_{CHWH}	SYSCLK, WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse	t_{WLWH}	WR0X, WR1X	t_{CYC} - 10	-	ns	WWT=0 *2
SYSCLK↑→ data output time	t_{CHDV}	SYSCLK, D16 to D31	0.5	18	ns	
SYSCLK↑→ data hold time	t_{CHDX}		-	18	ns	Set WRCS to 1 or more.

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
SYSCLK↑→ address output time	t_{CHMAV}	SYSCLK, D16 to D31	0.5	18	ns	
SYSCLK↑→ address hold time	t_{CHMAX}		-	18	ns	In multiplex mode, set as follows: ·Set CSWR and CSRD to 2 or more. ·ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

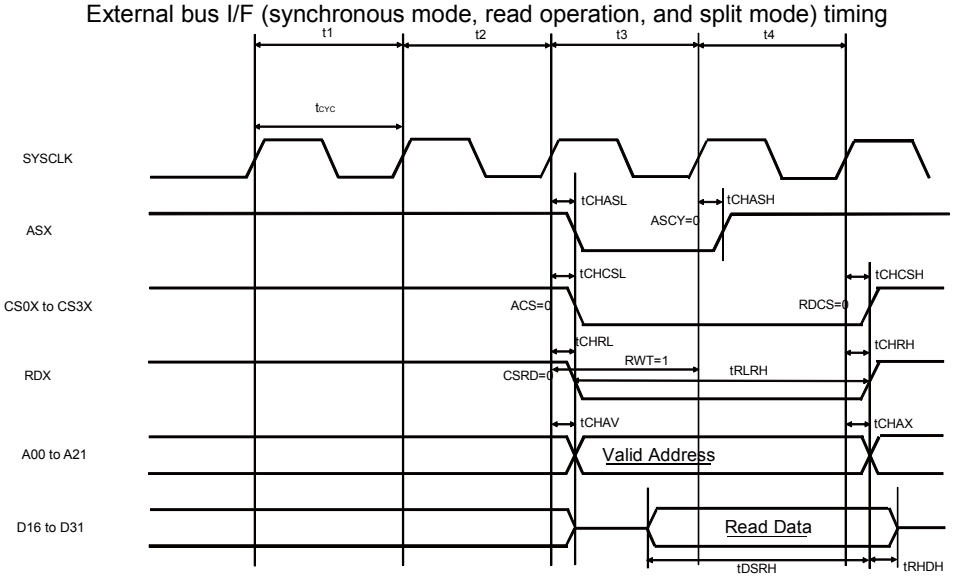
*1: Please use it with external load capacity 12pF or less for V_{CCE}=3.3V±0.3V (40MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

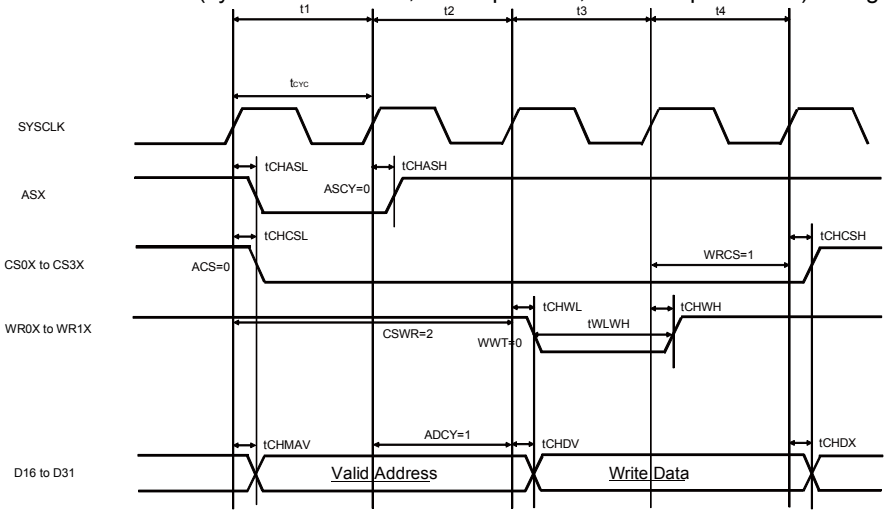
External bus I/F (synchronous mode, read operation, and multiplex mode) timing



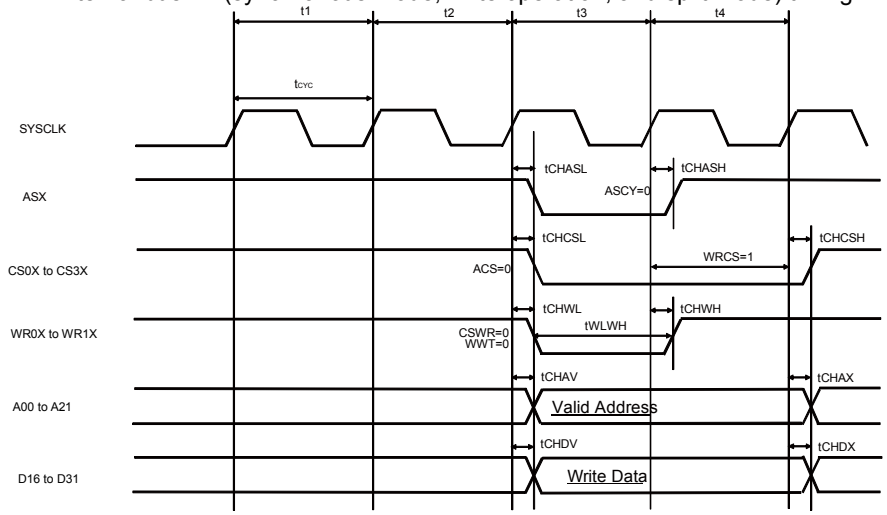
External bus I/F (synchronous mode, read operation, and split mode) timing



External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing

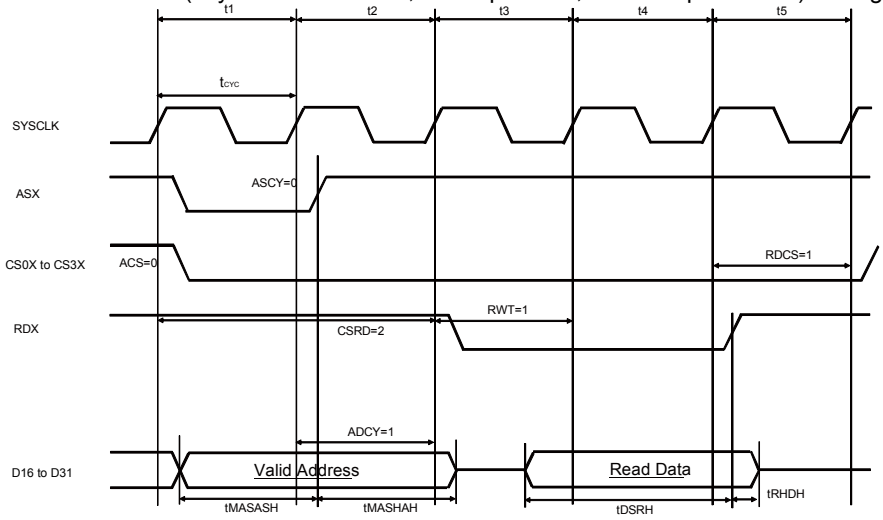


(11) External bus I/F (asynchronous mode) timing
(T_A: -40°C to +105°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

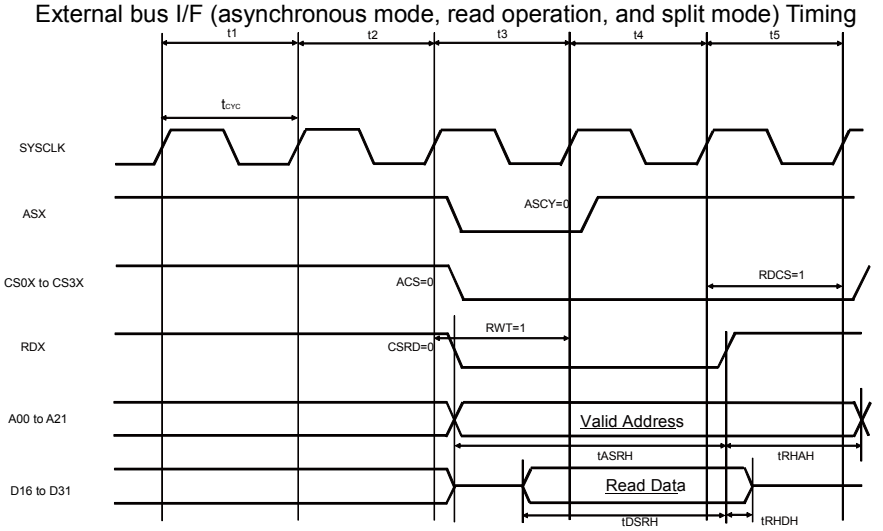
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	V_{CC}=5.0V±10% *1
			31.25			V_{CC}=3.3V±0.3V
Address setup → RDX↑time	t_{ASRH}	RDX, A00 to A21	2×t_{CYC} - 12	2×t_{CYC} + 12	ns	RWT=1, set RWT to 1 or more. *2
RDX↑→ Address hold	t_{RHAH}		t_{CYC} - 12	t_{CYC} + 12	ns	Set RDCS to 1 or more.
Data setup→ RDX↑time	t_{DSRH}	RDX, D16 to D31	18 + t_{CYC}	-	ns	RWT=1, set RWT to 1 or more.
RDX↑→ Data hold	t_{RHDH}		0	-	ns	
Address setup→ WRnX↑time	t_{ASWH}	WR0X to WR1X, A00 to A21	t_{CYC} - 12	t_{CYC} + 12	ns	WWT=0 *2
WRnX↑→ Address hold	t_{WHAH}		t_{CYC} - 12	t_{CYC} + 12	ns	Set WRCS to 1 or more.
Data setup→ WRnX↑time	t_{DSWH}	WR0X to WR1X, D16 to D31	t_{CYC} - 16	t_{CYC} + 16	ns	WWT=0 *2
WRnX↑→ Data hold	t_{WHDH}		t_{CYC} - 16	t_{CYC} + 16	ns	Set WRCS to 1 or more.
Address setup → ASX↑time	t_{MASASH}	ASX, D16 to D31	t_{CYC}-16	t_{CYC}+ 16	ns	ASCY=0
ASX↑→Address hold	t_{MASHAH}		t_{CYC}-16	t_{CYC} + 16	ns	In multiplex mode, set as follows: ☐Set CSWR and CSRD to 2 or more. ☐ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY +1 ≤ ACS + CSRD ADCY +1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

*1: Please use it with external load capacity 12pF or less for V_{CCE}=3.3V±0.3V (40MHz operation).
*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

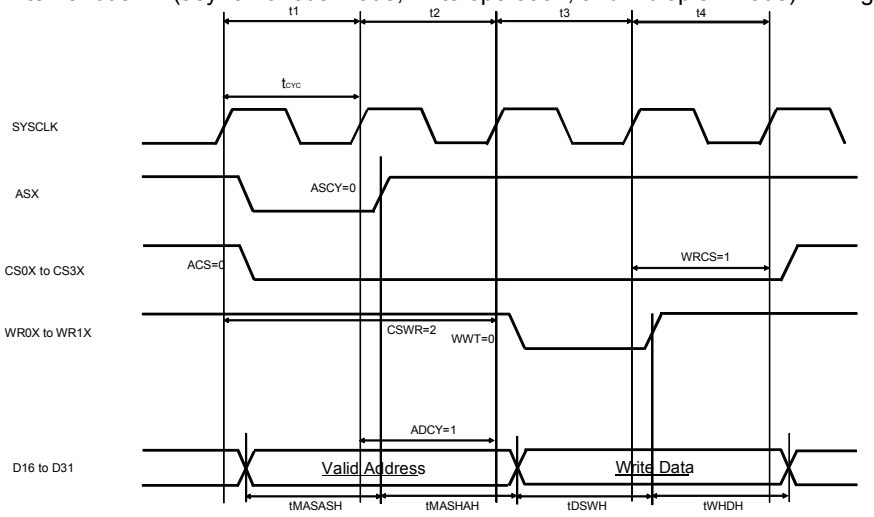
External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing



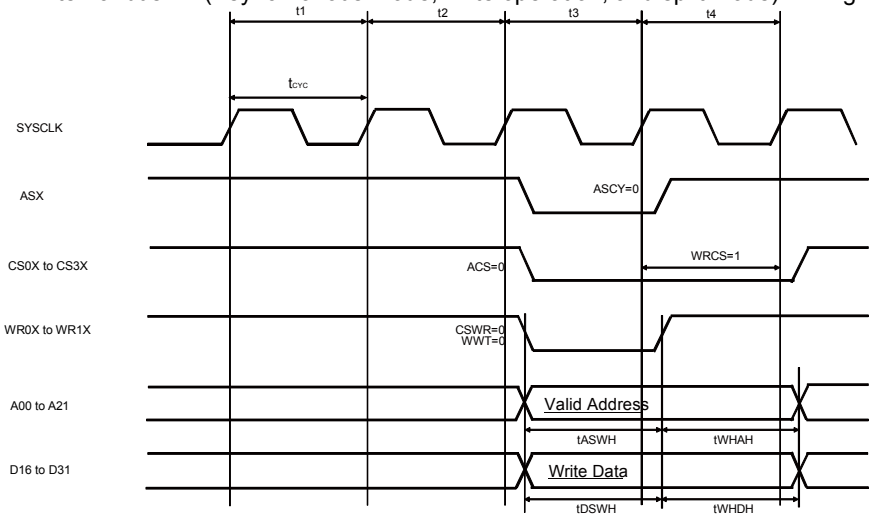
External bus I/F (asynchronous mode, read operation, and split mode) Timing



External bus I/F (asynchronous mode, write operation, and multiplex mode) Timing



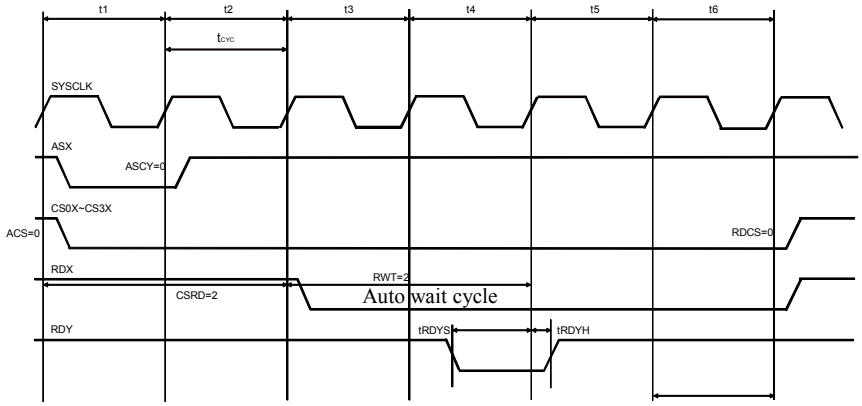
External bus I/F (Asynchronous mode, write operation, and split mode) Timing



(12) External bus I/F (ready) Timing
(T_A: -40°C to +105°C,V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)
(external load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK↑	t_{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK, RDY	0	-	ns	

External bus I/F (ready) Timing



12. A/D Converter

(1) 12-bit A/D Converter Electrical Characteristics

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±12	LSB	
Linearity error	-	-	-	-	± 4.0	LSB	
Differential linearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN63	AVRL-11.5LSB	-	AVRL+12.5LSB	V	1LSB= (V_{FST}-V_{OT})/4094
Full-scale transition voltage	V_{FST}	AN0 to AN63	AVRH-13.5LSB	-	AVRH+10.5LSB	V	
Sampling time	t_{SMP}	-	0.7	-	-	µs	*1
Compare time	t_{CMP}	-	0.7	-	-	µs	*1
A/D conversion time	t_{CNV}	-	1.4	-	-	µs	*1
Analog port input current	I_{AIN}	AN0 to AN63	-1.0	-	+1.0	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN63	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH	3.0	-	5.5	V	
	AVRL	AVSS/AVRL	-	0.0	-	V	
Power supply current	I_A	AVCC*3	-	0.47	0.63	mA	Per unit T_A: +105°C
			-	0.47	0.7	mA	Per unit T_A: +125°C
	I_{AH}		-	-	2.5	µA	*2
	I_R	AVRH	-	1	1.96	mA	Per unit
	I_{RH}		-	-	1.6	µA	*2
Variation between channels	-	AN0 to AN63	-	-	4	LSB	

*1: Time for each channel.

*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

*3: The power supply current described only current value on A/D converter.

The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.

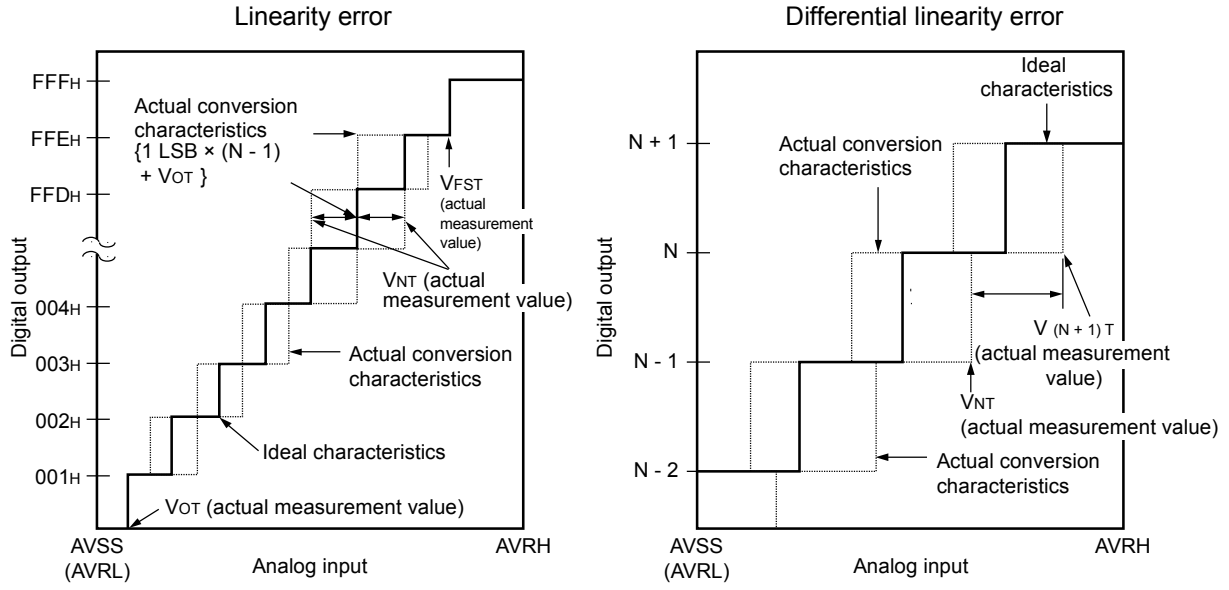
Note: Please use the clock of 0.5MHz-20MHz for the output clock of A/D converter to guarantee accuracy.

(2) Definition of A/D Converter Terms

Resolution : Analog variation that is recognized by an A/D converter.

Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"← →"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"← →"1111 1111 1111").

Differential linearity error : Deviation of the input voltage from the ideal value that is required to change the output code by LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ LSB} \quad \text{[LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \text{ [V]}$$

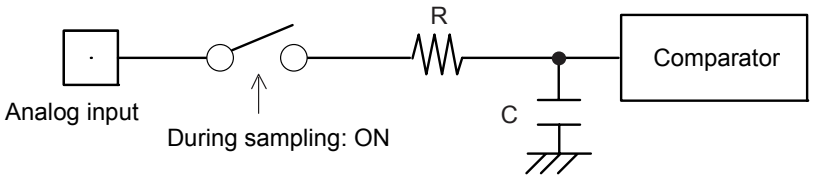
V_{OT} : Voltage at which the digital output changes from "000_H" to "001_H".
V_{FST} : Voltage at which the digital output changes from "FFE_H" to "FFF_H".

(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

· When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

☐Analog input circuit model



	R	C	
12bit A/D	1.9kΩ (Max)	8.30pF (Max)	(4.5V ≤ AV_{CC} ≤ 5.5V)
	4.3kΩ (Max)	8.30pF (Max)	(3.0V ≤ AV_{CC} ≤ 3.6V)

Note: Listed values must be considered as reference values.

15. Flash Memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbytes sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbytes sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbytes sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbytes sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T_A=+85°C*3

*1: The guaranteed value for erasure up to 100,000 cycles.
*2: Number of erase cycles for each sector.
*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes
While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.
In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc at 2.7V or more within the duration calculated by the following expression:

Td*[µs] + (period of PCLK [µs] × 257) + 50 [µs]

*: See “4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) ”

16. D/A Converter

(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

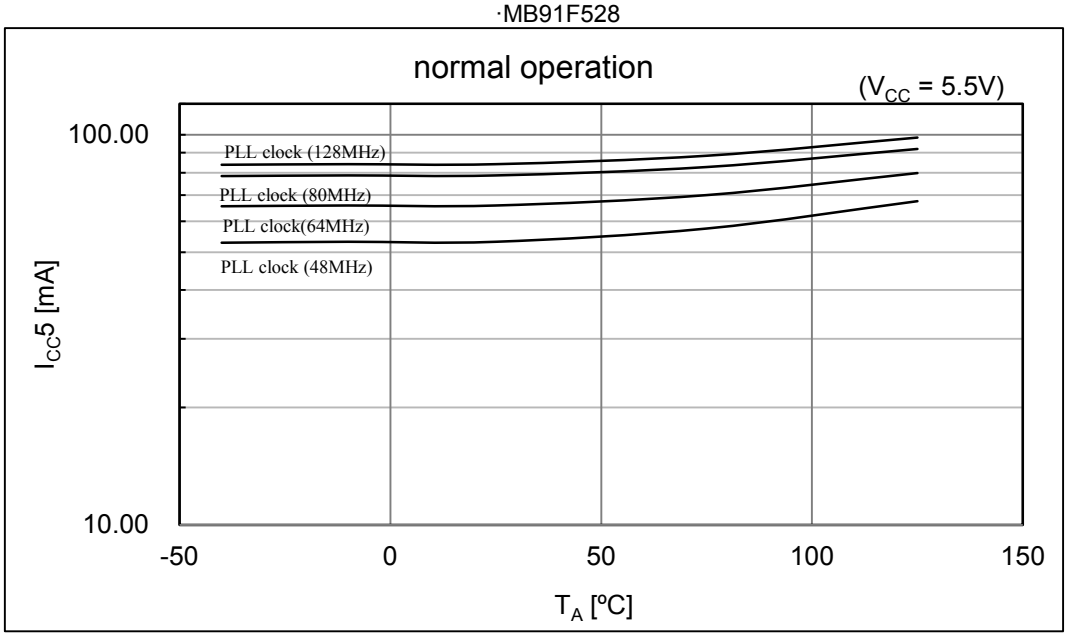
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	-	-	–	–	–	8	bit	
Differential linearity error	-	-	–	–	–	± 3.0	LSB	
Conversion time	-	-	–	0.47	0.58	0.69	µs	C_L=20
			–	2.37	2.90	3.43	µs	C_L=100
Output impedance	Ro	DA0, DA1	–	3.1	3.8	4.5	kΩ	
Power supply current *1	IA	AVCC	–	–	475	580	µA	Each channel
	IAH	AVCC	–	–	–	7.5	µA	When powerdown Each channel

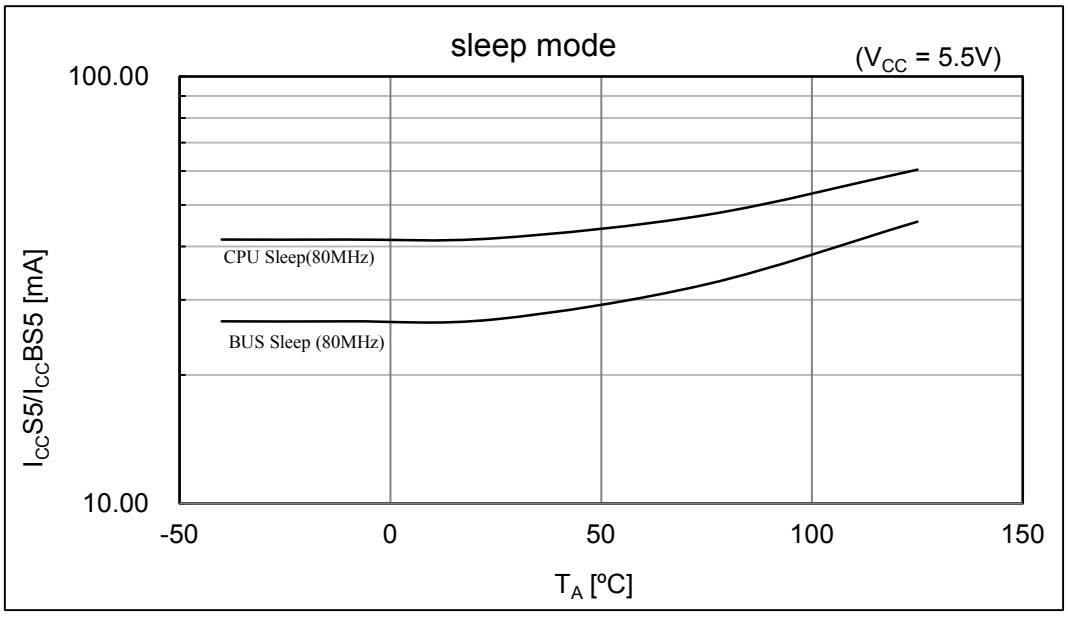
*1: The power supply current described only current value on D/A converter.
The total AVcc current value must be calculated the power supply current for D/A converter and A/D converter.

17. Example Characteristics

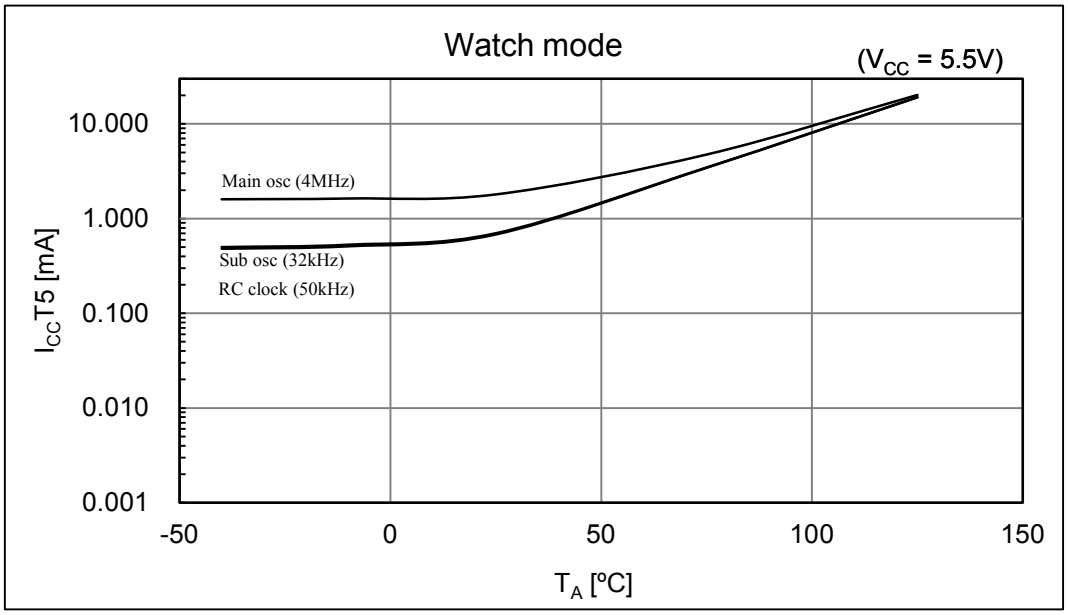
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

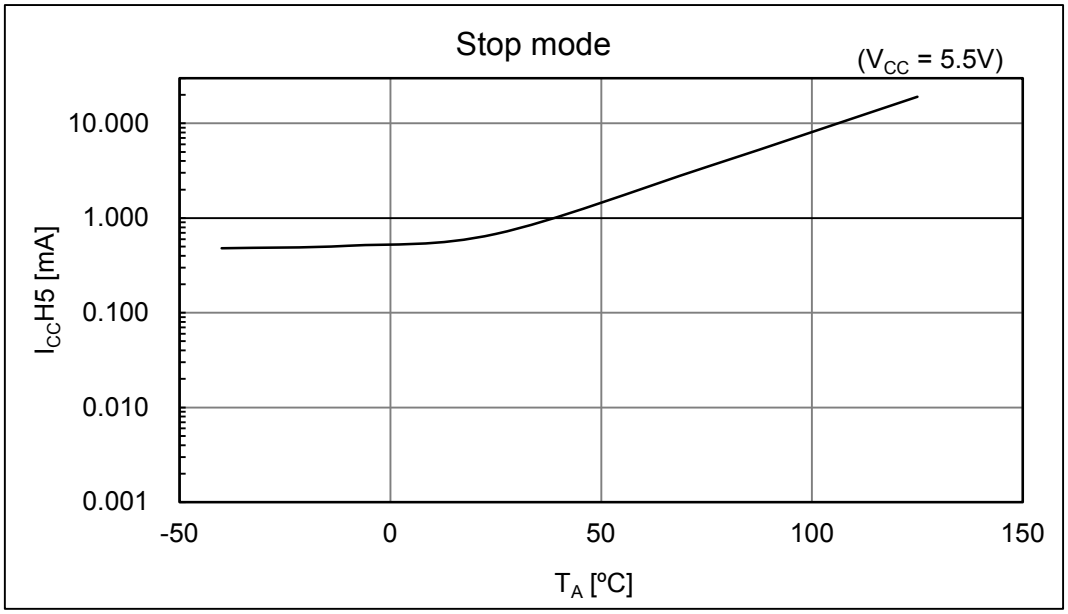
·MB91F528



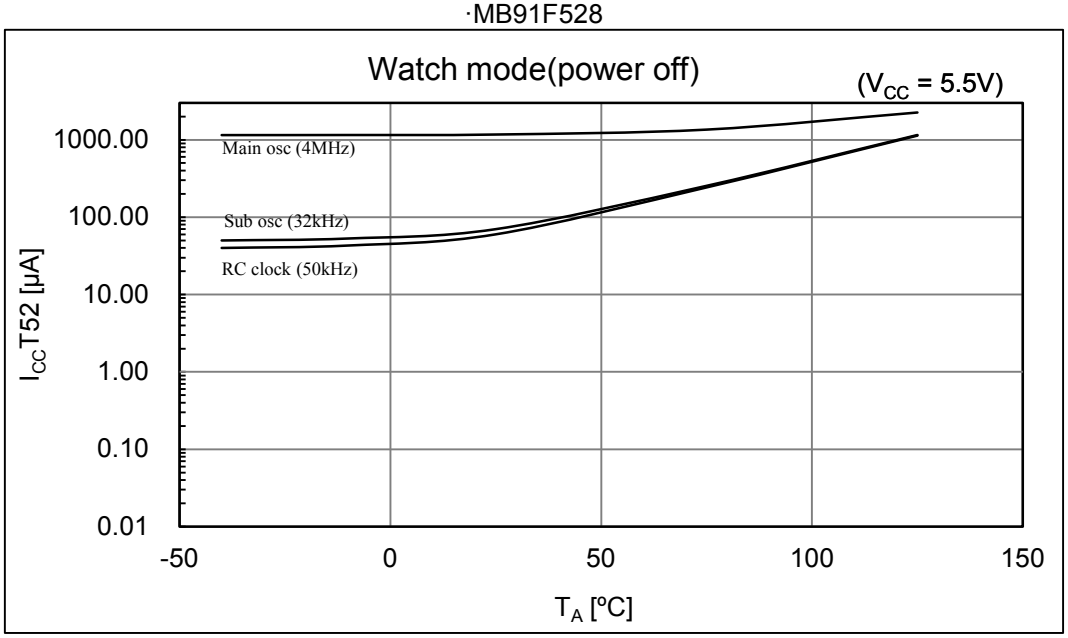


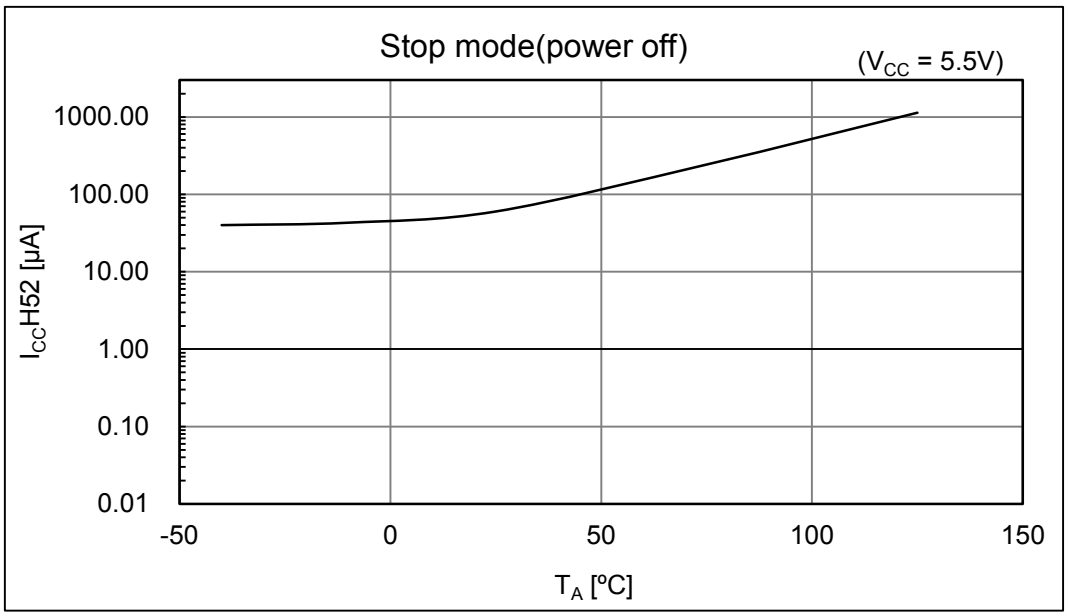
·MB91F528





·MB91F528





18. Ordering Information MB91F52xxxC[*1]

Part number	Sub clock	CSV Initial value	LVD Initial value	Package[*2]
MB91F528YWCPB	Yes	ON	ON	PAB•416 pin, Plastic
MB91F528YYCPB			OFF	
MB91F528YJCPB		OFF	ON	
MB91F528YLCPB			OFF	
MB91F527YWCPB		ON	ON	
MB91F527YYCPB			OFF	
MB91F527YJCPB		OFF	ON	
MB91F527YLCPB			OFF	
MB91F528YSCPB	None	ON	ON	
MB91F528YUCPB			OFF	
MB91F528YHCPB		OFF	ON	
MB91F528YKCPB			OFF	
MB91F527YSCPB		ON	ON	
MB91F527YUCPB			OFF	
MB91F527YHCPB		OFF	ON	
MB91F527YKCPB			OFF	
MB91F528MWCPMC	Yes	ON	ON	LQR•208 pin, Plastic
MB91F528MYCPMC			OFF	
MB91F528MJCPMC		OFF	ON	
MB91F528MLCPMC			OFF	
MB91F527MWCPMC		ON	ON	
MB91F527MYCPMC			OFF	
MB91F527MJCPMC		OFF	ON	
MB91F527MLCPMC			OFF	
MB91F528MSCPMC	None	ON	ON	
MB91F528MUCPMC			OFF	
MB91F528MHCPMC		OFF	ON	
MB91F528MKCPMC			OFF	
MB91F527MSCPMC		ON	ON	
MB91F527MUCPMC			OFF	
MB91F527MHCPMC		OFF	ON	
MB91F527MKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F528UWCPMC	Yes	ON	ON	LQP•176 pin, Plastic
MB91F528UYCPMC			OFF	
MB91F528UJCPMC		OFF	ON	
MB91F528ULCPMC			OFF	
MB91F527UWCPMC		ON	ON	
MB91F527UYCPMC			OFF	
MB91F527UJCPMC		OFF	ON	
MB91F527ULCPMC			OFF	
MB91F528USCPMC	None	ON	ON	
MB91F528UUCPMC			OFF	
MB91F528UHCPMC		OFF	ON	
MB91F528UKCPMC			OFF	
MB91F527USCPMC		ON	ON	
MB91F527UUCPMC			OFF	
MB91F527UHCPMC		OFF	ON	
MB91F527UKCPMC			OFF	
MB91F528RWCPMC	Yes	ON	ON	LQS•144 pin, (Lead pitch 0.5mm) Plastic
MB91F528RYCPMC			OFF	
MB91F528RJCPMC		OFF	ON	
MB91F528RLCPMC			OFF	
MB91F527RWCPMC		ON	ON	
MB91F527RYCPMC			OFF	
MB91F527RJCPMC		OFF	ON	
MB91F527RLCPMC			OFF	
MB91F528RSCPMC	None	ON	ON	
MB91F528RUCPMC			OFF	
MB91F528RHCPMC		OFF	ON	
MB91F528RKCPMC			OFF	
MB91F527RSCPMC		ON	ON	
MB91F527RUCPMC			OFF	
MB91F527RHCPMC		OFF	ON	
MB91F527RKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F528RWCPMC1	Yes	ON	ON	LQN•144 pin, (Lead pitch 0.4mm) Plastic
MB91F528RYCPMC1			OFF	
MB91F528RJCPMC1		OFF	ON	
MB91F528RLCPMC1			OFF	
MB91F527RWCPMC1		ON	ON	
MB91F527RYCPMC1			OFF	
MB91F527RJCPMC1		OFF	ON	
MB91F527RLCPMC1			OFF	
MB91F528RSCPMC1	None	ON	ON	
MB91F528RUCPMC1			OFF	
MB91F528RHCPMC1		OFF	ON	
MB91F528RKCPMC1			OFF	
MB91F527RSCPMC1		ON	ON	
MB91F527RUCPMC1			OFF	
MB91F527RHCPMC1		OFF	ON	
MB91F527RKCPMC1			OFF	
MB91F528MWCEQ	Yes	ON	ON	LER•208 pin, Plastic
MB91F528MYCEQ			OFF	
MB91F528MJCEQ		OFF	ON	
MB91F528MLCEQ			OFF	
MB91F527MWCEQ		ON	ON	
MB91F527MYCEQ			OFF	
MB91F527MJCEQ		OFF	ON	
MB91F527MLCEQ			OFF	
MB91F528MSCEQ	None	ON	ON	
MB91F528MUCEQ			OFF	
MB91F528MHCEQ		OFF	ON	
MB91F528MKCEQ			OFF	
MB91F527MSCEQ		ON	ON	
MB91F527MUCEQ			OFF	
MB91F527MHCEQ		OFF	ON	
MB91F527MKCEQ			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F528UWCEQ	Yes	ON	ON	LEP•176 pin, Plastic
MB91F528UYCEQ			OFF	
MB91F528UJCEQ		OFF	ON	
MB91F528ULCEQ			OFF	
MB91F527UWCEQ		ON	ON	
MB91F527UYCEQ			OFF	
MB91F527UJCEQ		OFF	ON	
MB91F527ULCEQ			OFF	
MB91F528USCEQ	None	ON	ON	
MB91F528UUCEQ			OFF	
MB91F528UHCEQ		OFF	ON	
MB91F528UKCEQ			OFF	
MB91F527USCEQ		ON	ON	
MB91F527UUCEQ			OFF	
MB91F527UHCEQ		OFF	ON	
MB91F527UKCEQ			OFF	
MB91F528RWCEQ	Yes	ON	ON	LEx•144 pin, Plastic
MB91F528RYCEQ			OFF	
MB91F528RJCEQ		OFF	ON	
MB91F528RLCEQ			OFF	
MB91F527RWCEQ		ON	ON	
MB91F527RYCEQ			OFF	
MB91F527RJCEQ		OFF	ON	
MB91F527RLCEQ			OFF	
MB91F528RSCEQ	None	ON	ON	
MB91F528RUCEQ			OFF	
MB91F528RHCEQ		OFF	ON	
MB91F528RKCEQ			OFF	
MB91F527RSCEQ		ON	ON	
MB91F527RUCEQ			OFF	
MB91F527RHCEQ		OFF	ON	
MB91F527RKCEQ			OFF	

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
*2: For details of the package, see "■ PACKAGE DIMENSIONS ".

19. Ordering Information MB91F52xxxD

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*1
MB91F528YWDPB	Yes	ON	ON	PAB・416 pin, Plastic)
MB91F528YJDPB		OFF	ON	
MB91F527YWDPB		ON	ON	
MB91F527YJDPB		OFF	ON	
MB91F528YSDPB	None	ON	ON	
MB91F528YHDPB		OFF	ON	
MB91F527YSDPB		ON	ON	
MB91F527YHDPB		OFF	ON	
MB91F528MWDPMC	Yes	ON	ON	LQR・208 pin, Plastic
MB91F528MJDPMC		OFF	ON	
MB91F527MWDPMC		ON	ON	
MB91F527MJDPMC		OFF	ON	
MB91F528MSDPMC	None	ON	ON	
MB91F528MHDPMC		OFF	ON	
MB91F527MSDPMC		ON	ON	
MB91F527MHDPMC		OFF	ON	
MB91F528UWDPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F528UJDPMC		OFF	ON	
MB91F527UWDPMC		ON	ON	
MB91F527UJDPMC		OFF	ON	
MB91F528USDPMC	None	ON	ON	
MB91F528UHDPMC		OFF	ON	
MB91F527USDPMC		ON	ON	
MB91F527UHDPMC		OFF	ON	
MB91F528RWDPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F528RJDPMC		OFF	ON	
MB91F527RWDPMC		ON	ON	
MB91F527RJDPMC		OFF	ON	
MB91F528RSDPMC	None	ON	ON	
MB91F528RHDPMC		OFF	ON	
MB91F527RSDPMC		ON	ON	
MB91F527RHDPMC		OFF	ON	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*1
MB91F528RWDPMC1	Yes	ON	ON	LQN・144 pin, (Lead pitch 0.4mm) Plastic
MB91F528RJDPMC1		OFF	ON	
MB91F527RWDPMC1		ON	ON	
MB91F527RJDPMC1		OFF	ON	
MB91F528RSDPMC1	None	ON	ON	
MB91F528RHDPMC1		OFF	ON	
MB91F527RSDPMC1		ON	ON	
MB91F527RHDPMC1		OFF	ON	
MB91F528MWDEQ	Yes	ON	ON	LER・208 pin, Plastic
MB91F528MJDEQ		OFF	ON	
MB91F527MWDEQ		ON	ON	
MB91F527MJDEQ		OFF	ON	
MB91F528MSDEQ	None	ON	ON	
MB91F528MHDEQ		OFF	ON	
MB91F527MSDEQ		ON	ON	
MB91F527MHDEQ		OFF	ON	
MB91F528UWDEQ	Yes	ON	ON	LEP・176 pin, Plastic
MB91F528UJDEQ		OFF	ON	
MB91F527UWDEQ		ON	ON	
MB91F527UJDEQ		OFF	ON	
MB91F528USDEQ	None	ON	ON	
MB91F528UHDEQ		OFF	ON	
MB91F527USDEQ		ON	ON	
MB91F527UHDEQ		OFF	ON	
MB91F528RWDEQ	Yes	ON	ON	LES・144 pin, Plastic
MB91F528RJDEQ		OFF	ON	
MB91F527RWDEQ		ON	ON	
MB91F527RJDEQ		OFF	ON	
MB91F528RSDEQ	None	ON	ON	
MB91F528RHDEQ		OFF	ON	
MB91F527RSDEQ		ON	ON	
MB91F527RHDEQ		OFF	ON	

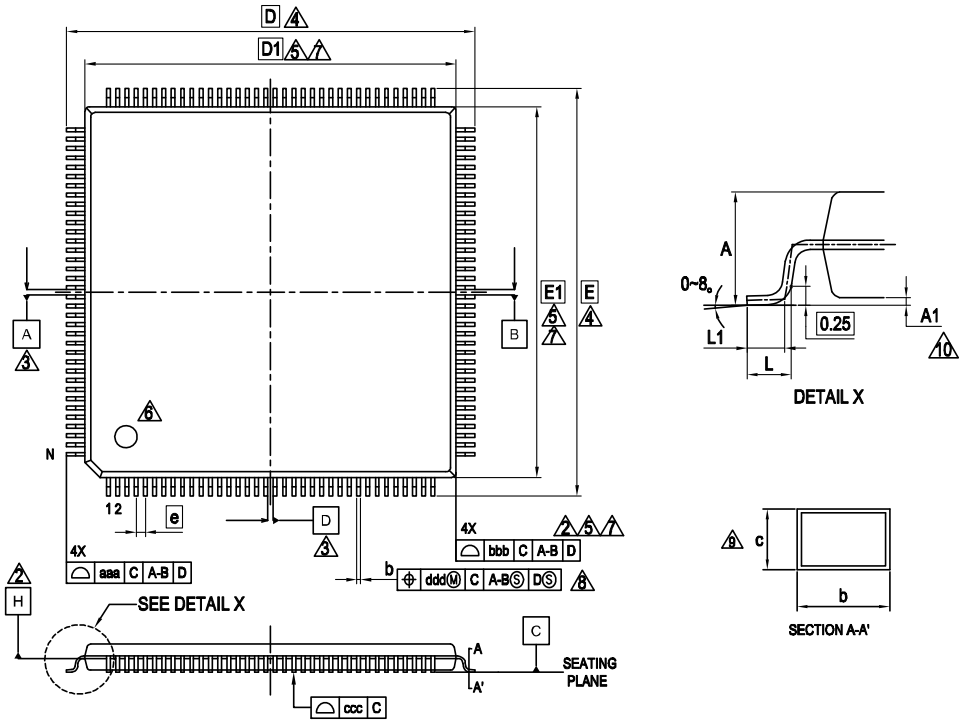
20. Ordering Information MB91F52xxxE

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*1
MB91F528YWEPB	Yes	ON	ON	PAB・416 pin, Plastic)
MB91F528YJEPB		OFF	ON	
MB91F527YWEPB		ON	ON	
MB91F527YJEPB		OFF	ON	
MB91F528YSEPB	None	ON	ON	
MB91F528YHEPB		OFF	ON	
MB91F527YSEPB		ON	ON	
MB91F527YHEPB		OFF	ON	
MB91F528MWEPMC	Yes	ON	ON	LQR・208 pin, Plastic
MB91F528MJEPMC		OFF	ON	
MB91F527MWEPMC		ON	ON	
MB91F527MJEPMC		OFF	ON	
MB91F528MSEPMC	None	ON	ON	
MB91F528MHEPMC		OFF	ON	
MB91F527MSEPMC		ON	ON	
MB91F527MHEPMC		OFF	ON	
MB91F528UWEPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F528UJEPMC		OFF	ON	
MB91F527UWEPMC		ON	ON	
MB91F527UJEPMC		OFF	ON	
MB91F528USEPMC	None	ON	ON	
MB91F528UHEPMC		OFF	ON	
MB91F527USEPMC		ON	ON	
MB91F527UHEPMC		OFF	ON	
MB91F528RWEPMC	Yes	ON	ON	LQS・144 pin, (LeaE pitch 0.5mm) Plastic
MB91F528RJEPMC		OFF	ON	
MB91F527RWEPMC		ON	ON	
MB91F527RJEPMC		OFF	ON	
MB91F528RSEPMC	None	ON	ON	
MB91F528RHEPMC		OFF	ON	
MB91F527RSEPMC		ON	ON	
MB91F527RHEPMC		OFF	ON	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*1
MB91F528RWEPMC1	Yes	ON	ON	LQN・144 pin, (LeaE pitch 0.4mm) Plastic
MB91F528RJEPMC1		OFF	ON	
MB91F527RWEPMC1		ON	ON	
MB91F527RJEPMC1		OFF	ON	
MB91F528RSEPMC1	None	ON	ON	
MB91F528RHEPMC1		OFF	ON	
MB91F527RSEPMC1		ON	ON	
MB91F527RHEPMC1		OFF	ON	
MB91F528MWEEQ	Yes	ON	ON	LER・208 pin, Plastic
MB91F528MJEEQ		OFF	ON	
MB91F527MWEEQ		ON	ON	
MB91F527MJEEQ		OFF	ON	
MB91F528MSEEQ	None	ON	ON	
MB91F528MHEEQ		OFF	ON	
MB91F527MSEEQ		ON	ON	
MB91F527MHEEQ		OFF	ON	
MB91F528UWEEQ	Yes	ON	ON	LEP・176 pin, Plastic
MB91F528UJEEQ		OFF	ON	
MB91F527UWEEQ		ON	ON	
MB91F527UJEEQ		OFF	ON	
MB91F528USEEQ	None	ON	ON	
MB91F528UHEEQ		OFF	ON	
MB91F527USEEQ		ON	ON	
MB91F527UHEEQ		OFF	ON	
MB91F528RWEEQ	Yes	ON	ON	LES・144 pin, Plastic
MB91F528RJEEQ		OFF	ON	
MB91F527RWEEQ		ON	ON	
MB91F527RJEEQ		OFF	ON	
MB91F528RSEEQ	None	ON	ON	
MB91F528RHEEQ		OFF	ON	
MB91F527RSEEQ		ON	ON	
MB91F527RHEEQ		OFF	ON	

21. Package Dimensions

LQS144 , 144 Lead Plastic Low Profile Quad Flat Package



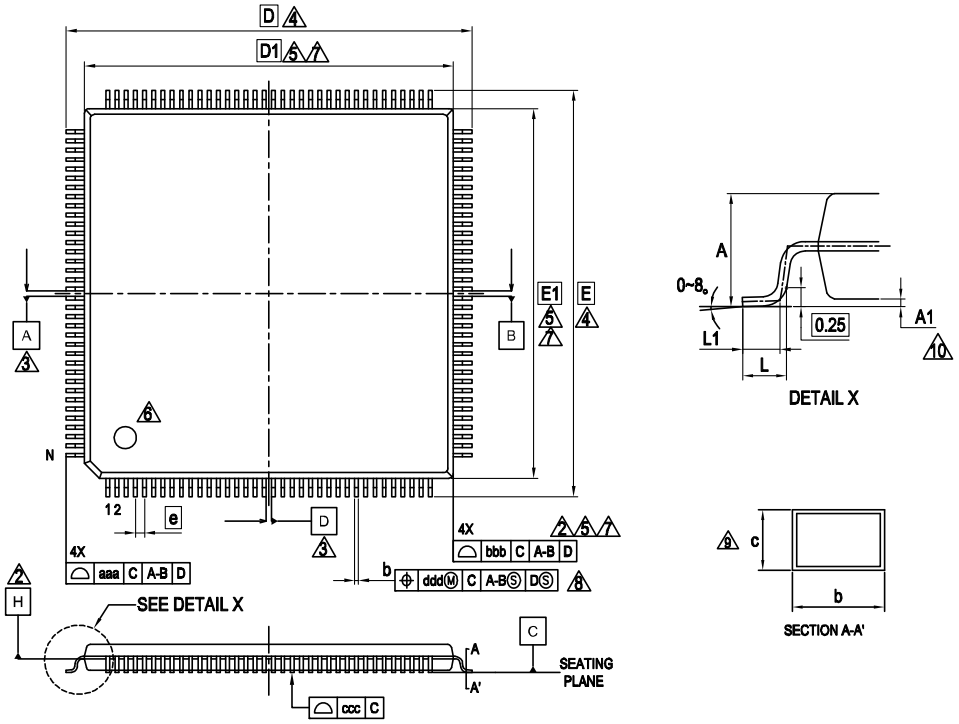
PACKAGE	LQS144		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.06	——	0.26
b	0.17	0.22	0.27
c	0.09	——	0.20
D	22.00 BSC.		
D1	20.00 BSC.		
e	0.50 BSC		
E	22.00 BSC.		
E1	20.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.08
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQN144 , 144 Lead Plastic Low Profile Quad Flat Package



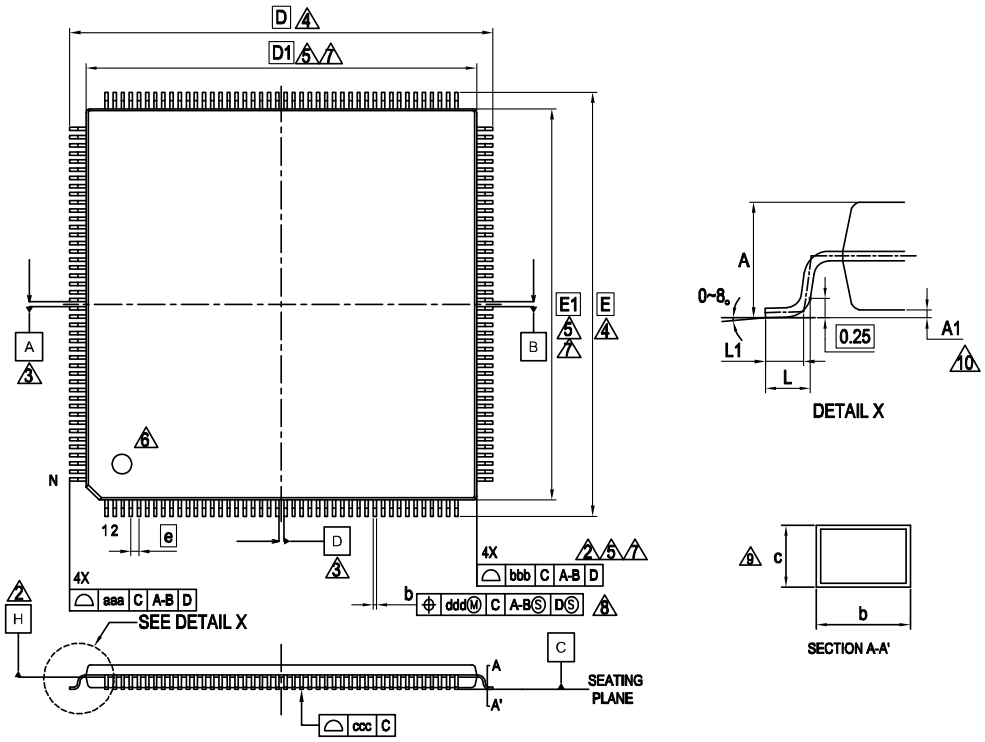
PACKAGE	LQN144		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.145	0.18	0.215
c	0.115	—	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.40 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.07
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQP176 , 176 Lead Plastic Low Profile Quad Flat Package



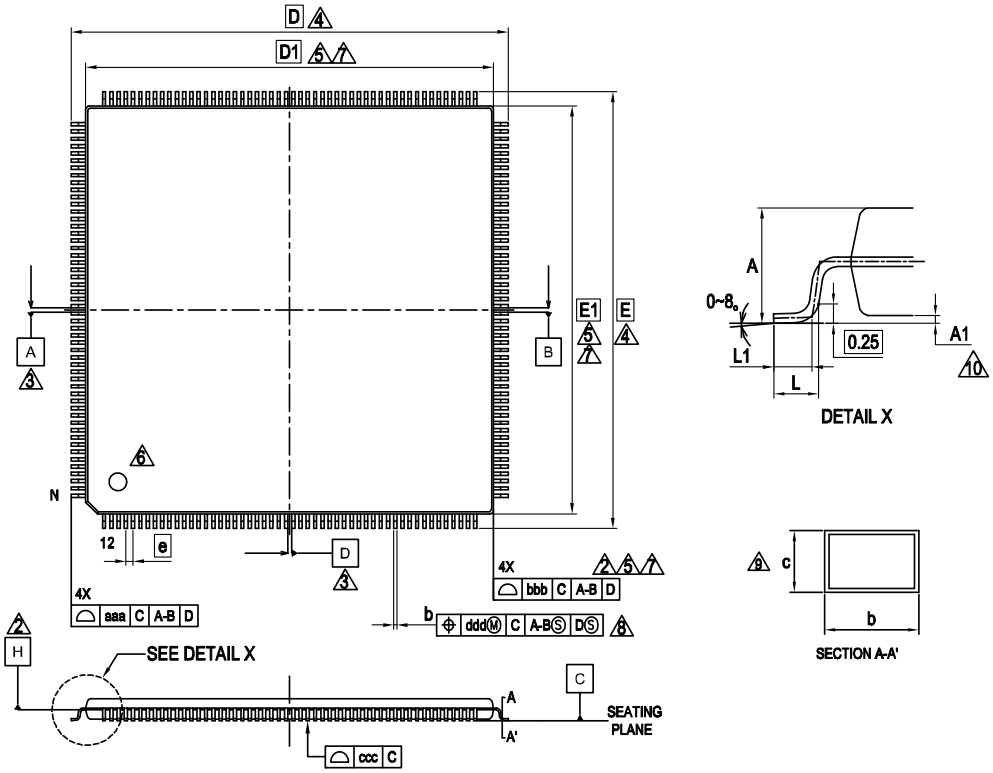
PACKAGE	LQP176		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.17	0.22	0.27
c	0.09	——	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.50 BSC		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.08
N	176		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQR208 , 208 Lead Plastic Low Profile Quad Flat Package



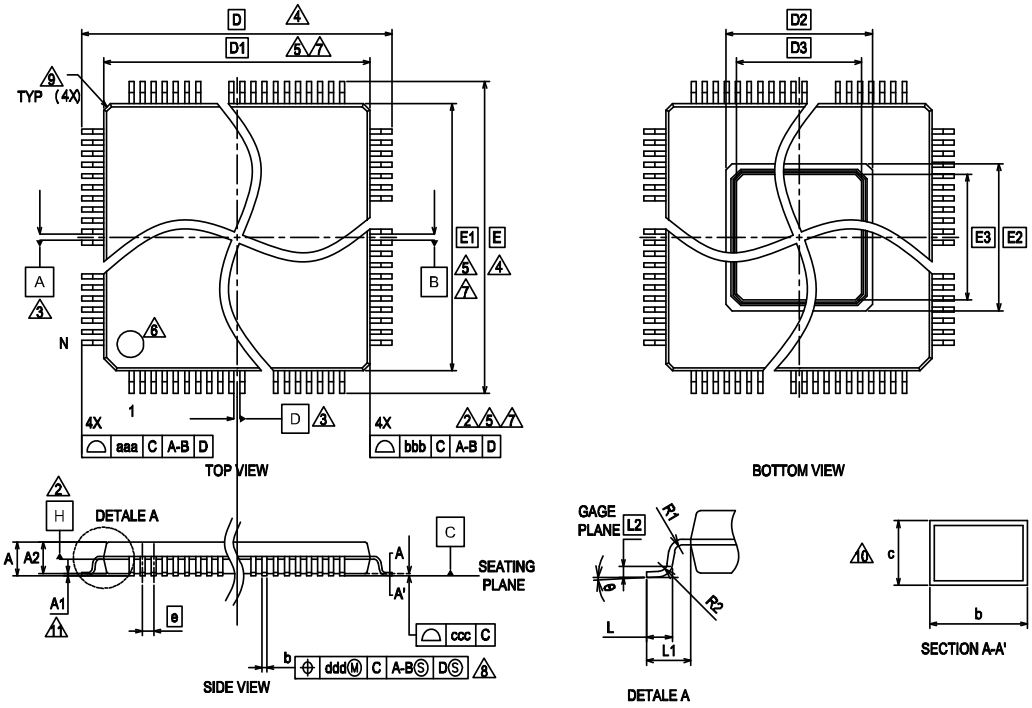
PACKAGE	LQR208		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.17	0.22	0.27
c	0.09	——	0.20
D	30.00 BSC.		
D1	28.00 BSC.		
e	0.50 BSC		
E	30.00 BSC.		
E1	28.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.08
N	208		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LES144 144PIN ExposedPAD Low Profile Quad Flat Package



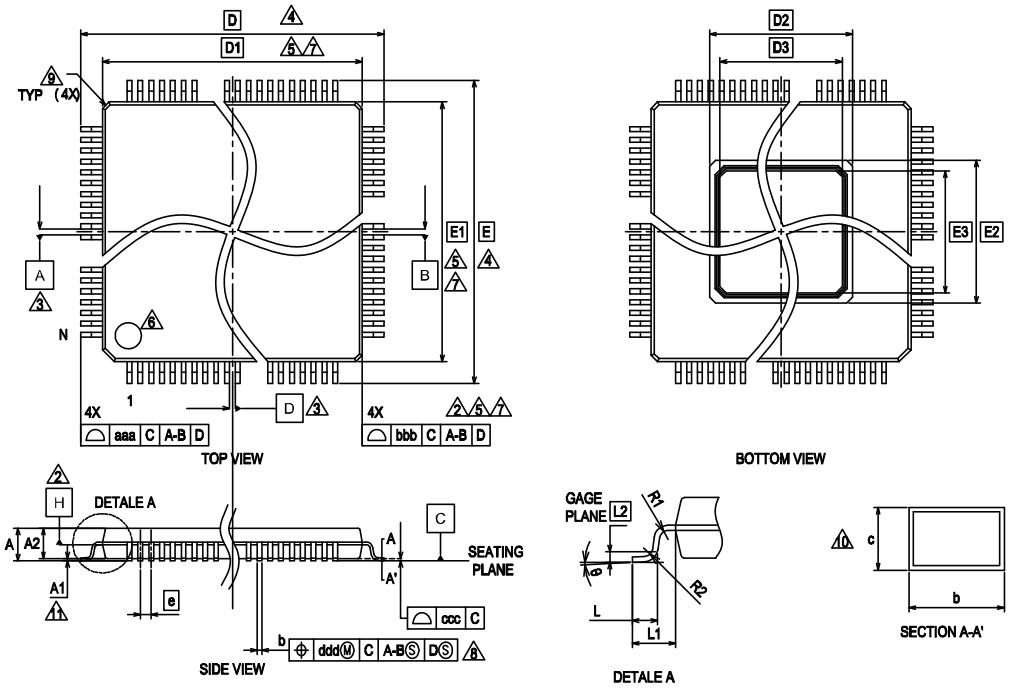
PACKAGE	LES144		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A_1	0.00	—	0.20
A_2	1.35	1.40	1.45
D	22.00 BSC.		
D_1	20.00 BSC.		
D_2	8.25 REF		
D_3	7.05 REF		
E	22.00 BSC.		
E_1	20.00 BSC.		
E_2	8.25 REF		
E_3	7.05 REF		
R_1	0.08	—	—
R_2	0.08	—	0.20
θ	0°	4°	8°
c	0.12	—	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L_1	1.00 REF		
L_2	0.25		
e	0.50 BSC.		

JEDEC	MO-108C		
SYMBOL	MIN.	NOM.	MAX.
aaa	0.20		
bbb	0.10		
ccc	0.08		
ddd	0.08		
N	144		

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. B

LEP176 176PIN ExposedPAD Low Profile Quad Flat Package



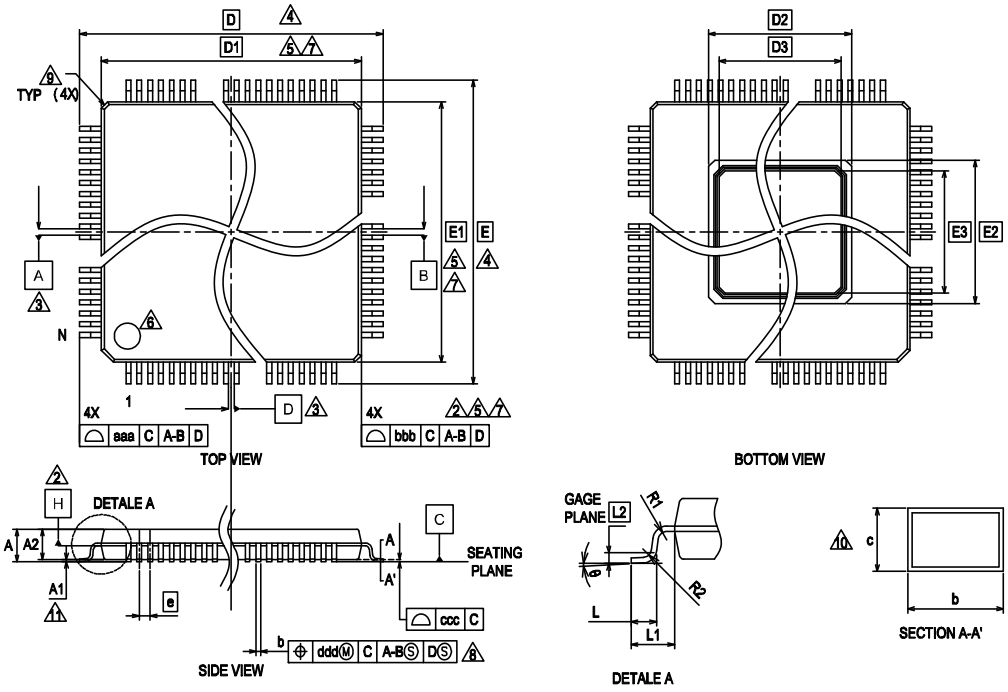
PACKAGE	LEP176		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A_1	0.00	——	0.20
A_2	1.35	1.40	1.45
D	26.00 BSC.		
D_1	24.00 BSC.		
D_2	9.26 REF		
D_3	8.06 REF		
E	26.00 BSC.		
E_1	24.00 BSC.		
E_2	9.26 REF		
E_3	8.06 REF		
R_1	0.08	——	——
R_2	0.08	——	0.20
θ	0°	4°	8°
c	0.12	——	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L_1	1.00 REF		
L_2	0.25		
e	0.50 BSC.		

JEDEC	MO-108C		
SYMBOL	MIN.	NOM.	MAX.
aaa	0.20		
bbb	0.10		
ccc	0.08		
ddd	0.08		
N	176		

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. B

LER208 208PIN ExposedPAD Low Profile Quad Flat Package



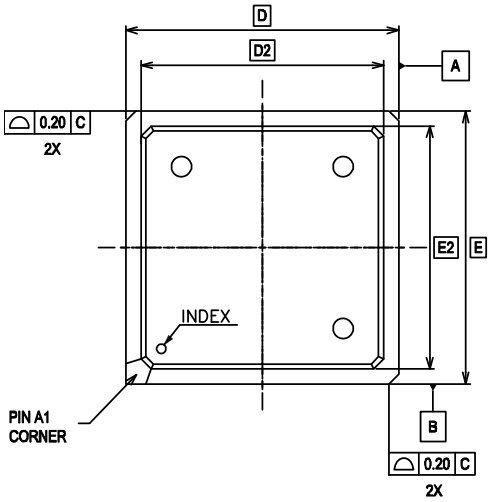
PACKAGE	LER208		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
A2	1.35	1.40	1.45
D	30.00 BSC.		
D1	28.00 BSC.		
D2	9.26 REF		
D3	8.06 REF		
E	30.00 BSC.		
E1	28.00 BSC.		
E2	9.26 REF		
E3	8.06 REF		
R1	0.08	——	——
R2	0.08	——	0.20
θ	0°	4°	8°
c	0.12	——	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25		
e	0.50 BSC.		

JEDEC	MO-108C		
SYMBOL	MIN.	NOM.	MAX.
aaa	0.20		
bbb	0.10		
ccc	0.08		
ddd	0.08		
N	208		

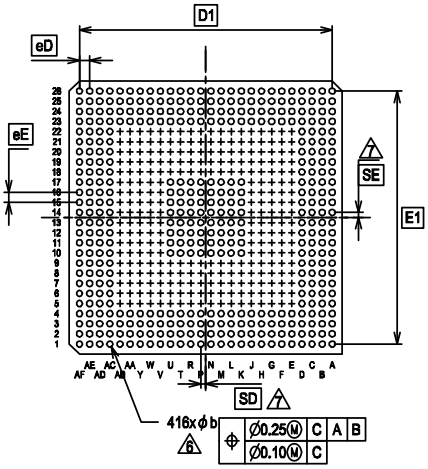
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

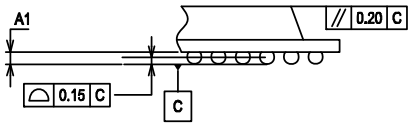
PAB416 416 BALL PLASTIC BALL GRID ARRAY PACKAGE



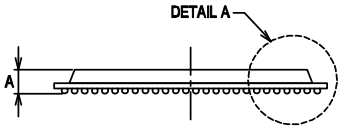
TOP VIEW



BOTTOM VIEW



DETAIL A



SIDE VIEW

PACKAGE	PAB416			NOTE
SYMBOL	MIN.	NOM.	MAX.	
A	——	——	2.37	PROFILE
A_1	0.40	0.50	0.60	TERMINAL HEIGHT
D	27.00 BSC			BODY SIZE
E	27.00 BSC			BODY SIZE
D_2	24.00 BSC			MOLD SIZE
E_2	24.00 BSC			MOLD SIZE
D_1	25.00 BSC			MATRIX FOOTPRINT
E_1	25.00 BSC			MATRIX FOOTPRINT
MD	26			MATRIX SIZE D DIRECTION
ME	26			MATRIX SIZE E DIRECTION
n	416			BALL COUNT
Φb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC			BALL PITCH
eE	1.00 BSC			BALL PITCH
SD / SE	0.50			SOLDER BALL PLACEMENT
	E5–E22, F5–F22, G5–G22, H5–H22 J5–J22, K5–K9, K18–K22, L5–L9 L18–L22, M5–M9, M18–M22, N5–N9 N18–N22, P5–P9, P18–P22, R5–R9 R18–R22, T5–T9, T18, T22, U5–U9 U18–U22, V5–V22, W5–W22, Y5–Y22 AA5–AA22, AB5–AB22			DEPOPULATED SOLDER BALL LOCATIONS

1. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

Rev. 0A

22. Errata

This section describes the errata for the MB91520 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
MB91F527R/U/M/Y, MB91F528R/U/M/Y

MB91F527/8 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available MB91520 Series devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Power-on Conditions is not enough in the Datasheet Specification	MB91F527R/U/M/Y, MB91F528R/U/M/Y	C	Will be fixed in production silicon version D, E
[2]. Limitation for Watch mode (power off)		C, D, E	-

1. Power-on Conditions is not enough in the Datasheet Specification

■ **Problem Definition**

If the Power-On Reset and Internal Low Voltage Detection are not generated, some port functions will not be available.

■ **Parameters Affected**

t_{OFF} for Power off time on Power-on Conditions

VCC Power ramp rate on Power-on Conditions

■ **Trigger Condition**

When the power supply voltage to the MCU has been turned off but has not reached 0 V when the power supply voltage is turned on again, MCU does not generate an internal power-on-reset signal (Power-On reset or Internal LVD reset). Then, some port functions will not be available.

If below condition (1) or (2) or (3) is satisfied, Power-On Reset (Initialization-Reset signal) is generated and no problem occurs.

(1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})

(2) VCC Power ramp rate less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

■ **Scope of Impact**

For the affected parts, when the Power-On Reset and Internal Low Voltage Detection are not generated, the MCU may set invalid package and sub clock option information. Therefore, the MCU may operate with an invalid pin configuration.

■ **Workaround**

For the affected parts, it is necessary to satisfy at least one of the Power-On Reset requirements for any Power-On event as given below:

(1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})

(2) VCC Power ramp rate is less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

If the customer system does not satisfy the condition above-mentioned, Cypress will releases new version D, so Cypress recommends the version D for MB91F52x. The new version prevents the limitation when an external reset signal is asserted at pin RSTX anytime the supply voltage (VCC) is turned on.

■ **Fix Status**

Will be fixed in production silicon version D, E

2. Limitation for Watch mode (power off)

■ **Problem Definition**

If the below all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

■ **Trigger Conditions**

(1) Using the watch mode (power off)

(2) Interrupt levels that are used as sources for recovering from the watch mode (power off) are ‘16’ to ‘30’, or using NMIX pin as source for recovering from the watch mode (power off)

(3) The sources for recovering from the watch mode (power off) are generated between PCLK 1 cycle and PMUCLK 3 cycles (*), after CPU state changes to the watch mode (power off)
(*): In case of PCLK = 0.5 MHz and PMUCLK = 32 kHz, it is approx. 2 µs to 100 µs

■ **Scope of Impact**

If the all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

WTCRH, WTCRM, WTCRL

CSELR.SCEN

CMONR.SCRDY

CCRTSELR.CST

CCRTSELR.CSC

■ **Workaround**

It is necessary to satisfy the below both conditions of (1) and (2).

(1) Interrupt levels that are used as sources for recovering from the watch mode (power off) are ‘31’, before CPU state changes to the watch mode (power off)

(2) Don’t use NMIX pin as source for recovering from the watch mode (power off)

■ **Fix Status**

Will not be planned

23. Major Changes

Spansion Publication Number: MB91F528_DS705-00016

Page	Section	Change Results
Revision 1.0		
–	–	Initial release
Cypress Document Number: 002-04669		
Rev *B		
1, 3	Features	Package description modified to JEDEC description.
6, 8, 10, 12	1. Product Lineup	Package description modified to JEDEC description.
53	6. Handling Devices ■During power-on	The following sentence modified as fdeleted from Interrupt (Error) To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.
146, 150, 154, 158	10. Interrupt Vector Table	The following sentence deleted from Interrupt vector table. *number up corrected. (Error) *5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.
160	11. Electrical Characteristics Absolute Maximum Ratings	*10 to *12: Package description modified to JEDEC description.
166	13. DC Characteristics Pull-up resistance	The following pin name deleted from $R_{UP3.}$ P073, P074, P077
169	14. AC Characteristics (1) Main Clock Timing	*3 and *4: Package description modified to JEDEC description.
172	14. AC Characteristics (2) Reset Input	Added the At power-on*2 condition to the remarks in Reset input time.
174	14. AC Characteristics (3) Power-on Conditions	Deleted the Slope detection undetected specification. Added the Power ramp rate and C pin voltage at Power-on. *1, *2: Changed the sentence. Added *3, *4, Note, Figure at the Power off time, Power ramp rate, C pin voltage at Power-on.
217 to 220	18. Ordering Information	Package description modified to JEDEC description.
221, 222	19. Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxD
223 to 230	20. Package Dimensions	Package description modified to JEDEC description.

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td colspan="3">Rev *C</td></tr>
<tr><td>5</td><td>Features
Peripheral Functions</td><td>The following sentence modified in I2C as following:

(Error)
< I2C >
10 channels (ch.3, ch.4, ch.12 to ch.19) Standard mode / High-speed mode supported

Standard mode (Max. 100kbps) / High-speed mode (Max. 400kbps) supported

(Correct)
< I2C >
10 channels (ch.3, ch.4, ch.12 to ch.19) Standard mode / Fast mode supported

Standard mode (Max. 100kbps) / Fast mode (Max. 400kbps) supported</td></tr>
<tr><td>5</td><td>1. Product Lineup</td><td>The following *3 added as follows:

(Error)
Multi-Function Serial | 12 channels

(Correct)
Multi-Function Serial | 12 channels *3</td></tr>
<tr><td>6</td><td>1. Product Lineup</td><td>The following *4 added as follows:

(Error)
Power supply | 2.7 V to 5.5 V

(Correct)
Power supply | 2.7 V to 5.5 V *4</td></tr>
<tr><td>6</td><td>1. Product Lineup</td><td>The following sentence added as follows:

(Correct)
*3: Only channel 3 and channel 4 support the I^{2}C (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^{2}C (standard mode).
*4: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V).
This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V).
Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector.
Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</td></tr>
</table>

Page	Section	Change Results
7	1. Product Lineup	The following *2 added as follows: (Error) Multi-Function Serial | 12 channels (Correct) Multi-Function Serial | 12 channels *2
8	1. Product Lineup	The following *3 added as follows: (Error) Power supply | 2.7 V to 5.5 V (Correct) Power supply | 2.7 V to 5.5 V *3
8	1. Product Lineup	The following sentence added as follows: (Correct) *2: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode). *3: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.
9	1. Product Lineup	The following *2 added as follows: (Error) Multi-Function Serial | 20 channels (Correct) Multi-Function Serial | 20 channels *2
10	1. Product Lineup	The following *3 added as follows: (Error) Power supply | 2.7 V to 5.5 V (Correct) Power supply | 2.7 V to 5.5 V *3

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>10</td><td>1. Product Lineup</td><td>The following sentence added as follows:

(Correct)
*2: Only channel 3, channel 4 and channel 12 to channel 19 support the I²C (high-speed mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode)
*3: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V).
This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V).
Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector.
Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</td></tr>
<tr><td>11</td><td>1. Product Lineup</td><td>The following *1 added as follows:

(Error)<table><tr><td>Multi-Function Serial</td><td>20 channels</td></tr></table>
(Correct)<table><tr><td>Multi-Function Serial</td><td>20 channels *1</td></tr></table></td></tr>
<tr><td>12</td><td>1. Product Lineup</td><td>The following *2 added as follows:

(Error)<table><tr><td>Power supply</td><td>2.7 V to 5.5 V</td></tr></table>
(Correct)<table><tr><td>Power supply</td><td>2.7 V to 5.5 V *2</td></tr></table></td></tr>
<tr><td>12</td><td>1. Product Lineup</td><td>The following sentence added as follows:

(Correct)
*1: Only channel 3, channel 4 and channel 12 to channel 19 support the I²C (high-speed mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).
*2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V).
This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V).
Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector.
Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</td></tr>
<tr><td>13</td><td>1. Product Lineup</td><td>Added silicon version E</td></tr>
</table>

Page	Section	Change Results
53	■During Power-on	The following sentence modified as following: (Error) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.
163	12. Electrical Characteristics Recommended operating conditions	The following sentence modified as following: (Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset. (Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.
178, 179	14. AC Characteristics	Added (3-2) Power-on Conditions for MB91F52xxxE

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>204</td><td>14. AC Characteristics
(4) Multi-function Serial
(4-4) I²C timing</td><td>The following sentence modified as following:

(Error)
<table>
<tr><th colspan="2">High-speed mode*3</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
</table>

Notes: Only ch.3, ch.4 and ch.12-ch.19 are standard mode/ high-speed mode correspondence.

*3: A high-speed mode I²C bus device can be used

(Correct)
<table>
<tr><th colspan="2">Fast mode*3</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
</table>

Notes: Only ch.3, ch.4 and ch.12-ch.19 are standard mode/ fast mode correspondence.

*3: A fast mode I²C bus device can be used</td></tr>
<tr><td>208</td><td>14. AC Characteristics
(8) Low voltage detection (External low-voltage detection)</td><td>The following sentence modified in the Detection voltage as following:

(Error)
<table>
<tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr>
<tr><td>-8%</td><td>2.8</td><td>+8%</td><td>V</td><td>When power-supply voltage falls and detection level is set initially</td></tr>
</table>

(Correct)
<table>
<tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr>
<tr><td>-8%</td><td>LVD5F_SEL [3:0]</td><td>+8%</td><td>V</td><td>LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.</td></tr>
</table>
</td></tr>
<tr><td>208</td><td>14. AC Characteristics
(9) Low voltage detection (RAM retention low-voltage detection)</td><td>The following sentence modified as following:

(Error)
(9) Low voltage detection (Internal low-voltage detection)

(Correct)
(9) Low voltage detection (RAM retention low-voltage detection)</td></tr>
</table>

Page	Section	Change Results
231, 232	20. Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxE
Rev *D		
2	Features	The following sentence should be modified as follows: (Error) Conversion time : 1µs (Correct) Conversion time : 1.4µs
6	1. Product Lineup	The following sentence should be modified as follows: (Error) *4: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. (Correct) *4: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Page	Section	Change Results
8, 10	1. Product Lineup	The following sentence should be modified as follows: (Error) *3: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. *3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
12	1. Product Lineup	The following sentence should be modified as follows: (Correct) *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. *2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Page	Section	Change Results
163	12. Electrical Characteristics Recommended operating conditions	The following sentence should be modified as follows: (Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. (Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
168	11. Electrical Characteristics DC Characteristics	Pin name of R_{UP3} should be modified as follows: (Error) Port pin other than P035,041,093,122,222,227,232,236 (Correct) Port pin other than P035,041,073,074,077,093,122,222,227,232,236
208	11. Electrical Characteristics (8) Low voltage detection (External low-voltage detection)	Note of Detection voltage should be added as follows: (Correct) Detection voltage *3 *3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7V). Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Page	Section	Change Results
208	11. Electrical Characteristics (9) Low voltage detection (Internal low-voltage detection)	The following sentence modified as following: (Error) (9) Low voltage detection (RAM retention low-voltage detection) (Correct) (9) Low voltage detection (Internal low-voltage detection)
		The following symbol should be modified as follows: (Error) * (Correct) *1
		Note of Detection voltage should be added as follows: (Correct) Detection voltage *2 *2: The detection voltage of the internal low voltage detection is 0.9V±0.1V. This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
241, 242	22. Errata	Limitation for Watch mode (power off) should be added in Errata.

Document History

Document Title: MB91F527R/MB91F527U/MB91F527M/MB91F527Y/MB91F528R/MB91F528U/MB91F528M/MB91F528Y 32-bit FR81S Microcontroller

Document Number: 002-04669

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	—	03/28/2014	Initial release
*A	5005210	JHMU	11/16/2015	Updated to Cypress template. Added the following note to the remarks of ""L" level average output current" and ""H" level average output current" in “Absolute Maximum Ratings” of “ELECTRICAL CHARACTERISTICS”. *13: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106. *14: Corresponding pins: General-purpose ports of P103, P104, P105 and P106. Added Errata section.
*B	5107086	KUME	01/26/2016	For details, please see the chapter 21. Major Changes.
*C	5196361	KUME	04/28/2016	For details, please see the chapter 23. Major Changes.
*D	5318662	KUME	06/22/2016	For details, please see the chapter 23. Major Changes.

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