SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND.)
V_{CC} ..... -0.3V to +4.0V
All Other Pins (Note 1) ..... -0.3V to (V_{CC} + 0.3V)
Continuous Current IN_P, IN_M, OUT_P, OUT_M ..... ±30mA
Peak Current IN_P, IN_M, OUT_P, OUT_M for 1µs .... ±100mA
Continuous Power Dissipation (T_A = +70°C)
42-Pin TQFN (derate 34.5mW/°C above +70°C) 2758mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: All I/O pins are clamped by internal diodes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_{CL} = 10nF coupling capacitor on each input and output, R_L = 50Ω on each input and output, T_A = 0°C to +70°C (MAX4986C), T_A = -40°C to +85°C (MAX4986E), unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Power-Supply Range	V_{CC}			3.0		3.6	V
Standby Current	I_{STBY}	EN = 0 or $\overline{EN}$ = 1, V_{CC} = 3.6V			2.5	4	mA
		EN = 0 or $\overline{EN}$ = 1, V_{CC} = 3.3V			1.0	2	
Supply Current	I_{CC}	OUTPE = PEA = PEB = 0, INEQ = EQA = EQB = 0			145	170	mA
		OUTPE = PEA = PEB = 1, INEQ = EQA = EQB = 1			185	230	
Input Termination, Single-Ended	R_{RX-SE}	DC		42.5		57.5	Ω
Output Termination, Single-Ended	R_{TX-SE}	DC		42.5		57.5	Ω
AC PERFORMANCE							
Input Return Loss, Differential (Note 3)	SDD11	0.1GHz < f ≤ 0.3GHz				-10	dB
		0.3GHz < f ≤ 3.0GHz				-7.9	
		3.0GHz < f ≤ 6.0GHz				0	
Input Return Loss, Common Mode (Note 3)	SCC11	0.1GHz < f ≤ 0.3GHz				-6	dB
		0.3GHz < f ≤ 3.0GHz				-5	
		3.0GHz < f ≤ 6.0GHz				0	
Output Return Loss, Differential (Note 3)	SDD22	0.1GHz < f ≤ 0.3GHz				-10	dB
		0.3GHz < f ≤ 3.0GHz				-7.9	
		3.0GHz < f ≤ 6.0GHz				0	
Output Return Loss, Common Mode (Note 3)	SCC22	0.1GHz < f ≤ 0.3GHz				-6	dB
		0.3GHz < f ≤ 3.0GHz				-5	
		3.0GHz < f ≤ 6.0GHz				0	
Differential Input Voltage	$V_{IN-DIFF}$	SAS 1.5Gbps, 3Gbps, MODE_ = 0		275		1600	mV_{P-P}
		SAS 6Gbps, MODE_ = 0		300		1600	
		SATA 1.5Gbps, 3Gbps, 6Gbps, MODE_ = 1		225		1600	
Input Equalization	EQ	f = 1.5GHz, INEQ = 1			4		dB
Differential Output Voltage	$V_{OUT-DIFF}$	f = 0.75GHz, 1.5GHz, PE_ = 0	OAMP_ = 0	700		1200	mV_{P-P}
			OAMP_ = 1	425		700	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 10nF coupling capacitor on each input and output, R_L = 50Ω on each input and output, T_A = 0°C to +70°C (MAX4986C), T_A = -40°C to +85°C (MAX4986E), unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Preemphasis	PE	f = 1.5GHz, PE_ = 1, Figure 1			3		dB
Propagation Delay	t_{PD}				300		ps
Output Transition Time	t_{TX-RF}	f < 3.0GHz, PE_ = 0 (Notes 3, 4)		40	60		ps
Differential Output Skew Same Pair	t_{SK}				10		ps
Deterministic Jitter	t_{DJ}	K28.5± pattern, PE_ = 0, EQ_ = 0 (Note 3)				20	ps_{P-P}
Random Jitter	$t_{TX-RJ-DD}$	D10.2 pattern, PE_ = 0, EQ_ = 0			1	1.5	ps_{RMS}
OOB Squelch Threshold	$V_{SQ-DIFF}$	f = 0.75GHz (Note 3)	MODE_ = 0	120		220	mV_{P-P}
			MODE_ = 1	50		150	
OOB Squelch Time	$t_{OOB,SQ}$	f = 0.75GHz (Note 3)			5	10	ns
OOB Exit Time	$t_{OOB,EX}$	f = 0.75GHz (Note 3)			5	10	ns
OOB Differential-Offset Delta	$\Delta V_{OOB,DIFF}$	Difference between OOB and active-mode output offset		-80		80	mV
OOB Common-Mode Delta	$\Delta V_{OOB,CM}$	Difference between OOB and active-mode output V_{CM}		-50		50	mV
OOB Output Disable	$V_{OOB,OUT}$	OOB-disabled output level				30	mV_{P-P}
CONTROL LOGIC							
Input Logic-High	V_{IH}			1.4			V
Input Logic-Low	V_{IL}					0.6	V
Input Logic Hysteresis	V_{HYST}				0.1		V
Pullup/Pulldown Input Resistor	$R_{UP/DOWN}$				330		kΩ

Note 2: MAX4986C devices are 100% production tested at T_A = +70°C. MAX4986E devices are 100% production tested at T_A = +85°C. Specifications for all temperature limits are guaranteed by design.

Note 3: Guaranteed by design.

Note 4: Rise and fall times are measured using 20% and 80% levels.

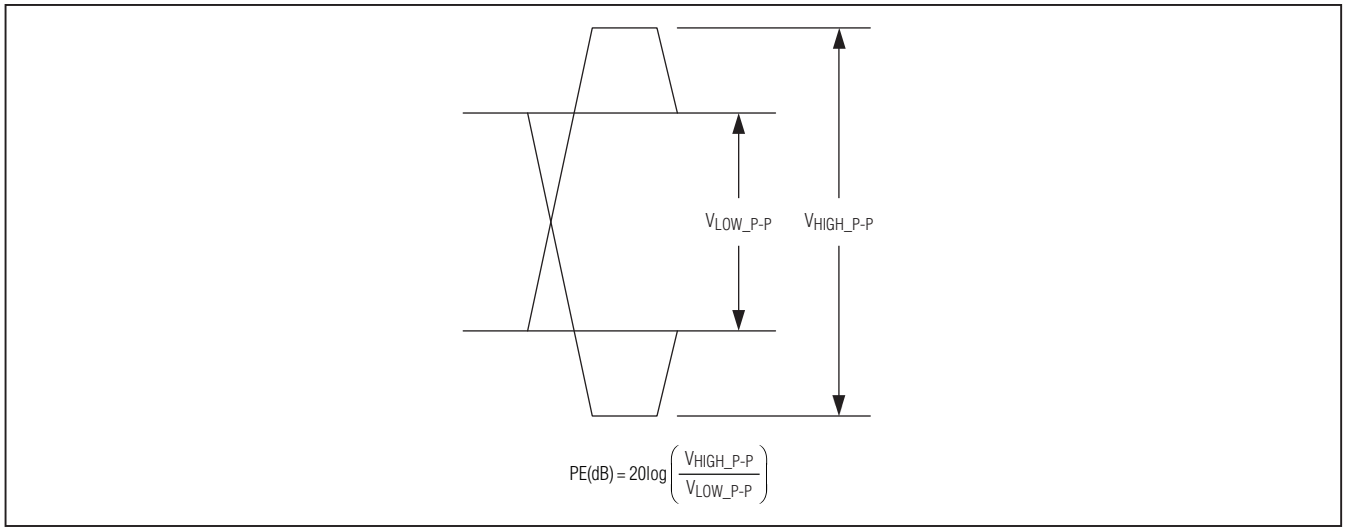


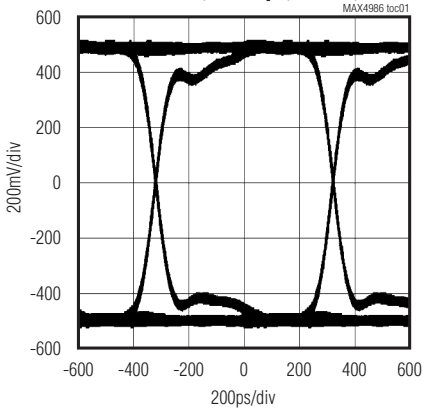
Figure 1. Output Preemphasis

SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

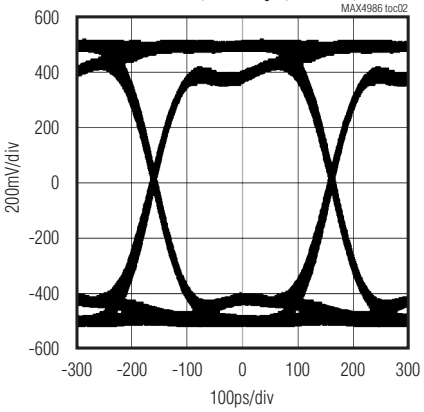
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

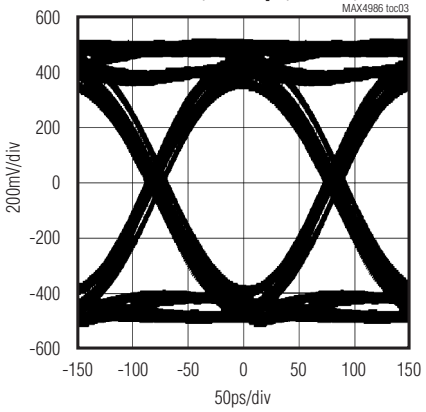
V_{IN} = 275mV$_{P-P}$, 1.5Gbps, PE = 0, EQ = 0



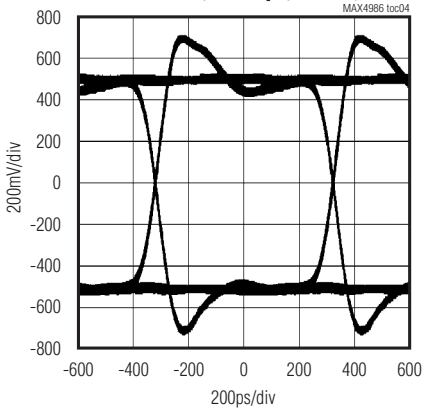
V_{IN} = 275mV$_{P-P}$, 3.0Gbps, PE = 0, EQ = 0



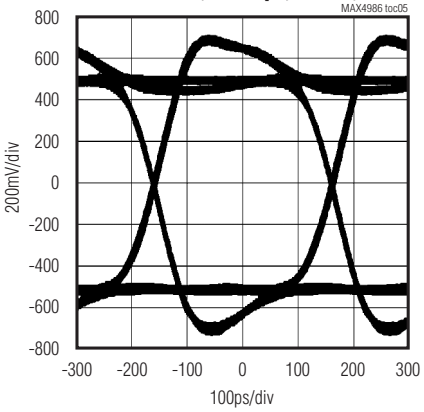
V_{IN} = 275mV$_{P-P}$, 6.0Gbps, PE = 0, EQ = 0



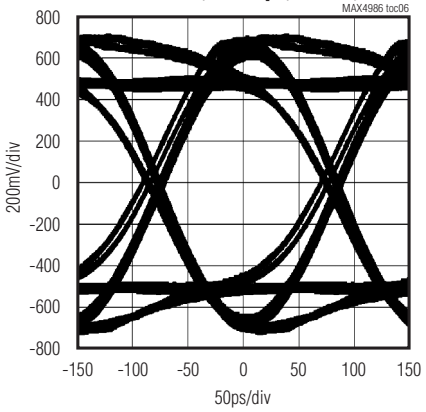
V_{IN} = 275mV$_{P-P}$, 1.5Gbps, PE = 1, EQ = 0



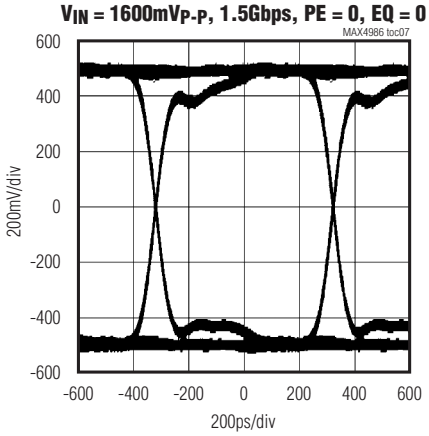
V_{IN} = 275mV$_{P-P}$, 3.0Gbps, PE = 1, EQ = 0



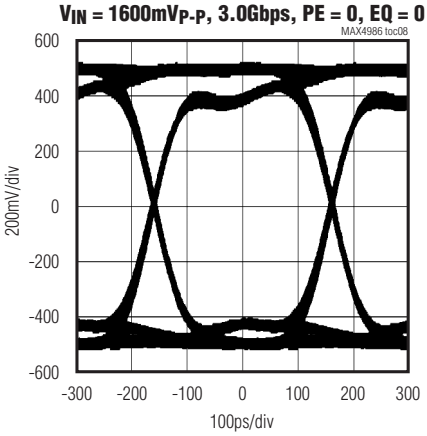
V_{IN} = 275mV$_{P-P}$, 6.0Gbps, PE = 1, EQ = 0



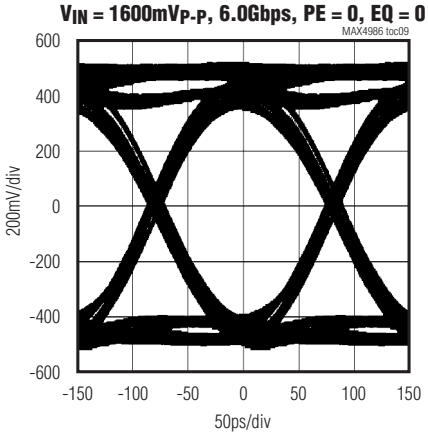
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, PE = 0, EQ = 0



V_{IN} = 1600mV$_{P-P}$, 3.0Gbps, PE = 0, EQ = 0



V_{IN} = 1600mV$_{P-P}$, 6.0Gbps, PE = 0, EQ = 0

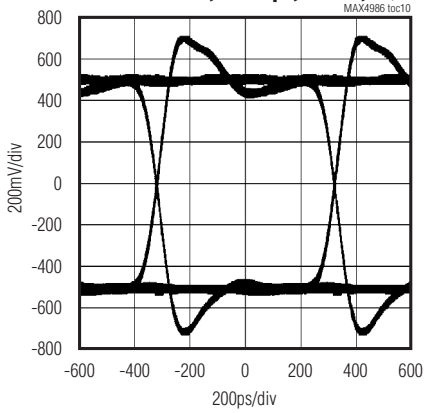


SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

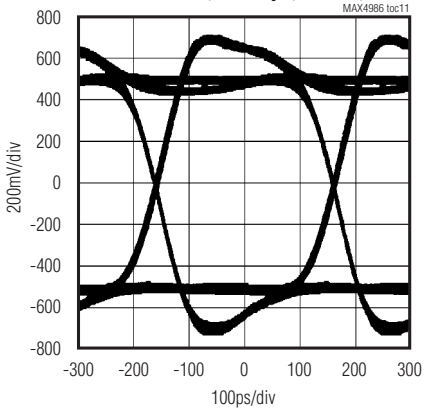
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

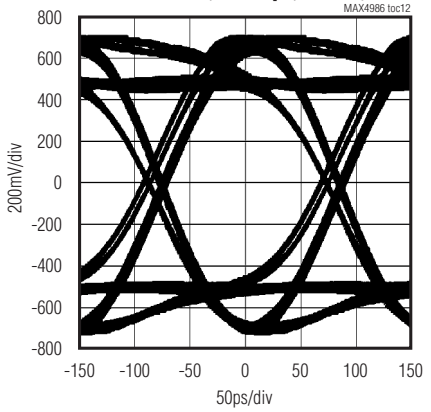
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, PE = 1, EQ = 0



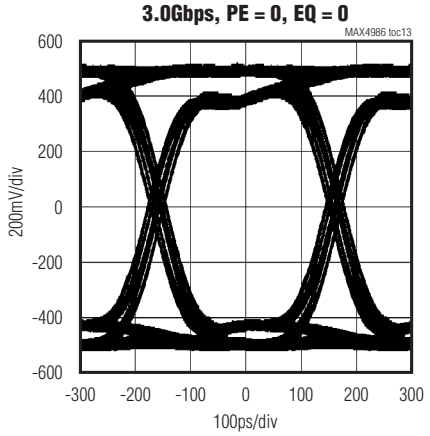
V_{IN} = 1600mV$_{P-P}$, 3.0Gbps, PE = 1, EQ = 0



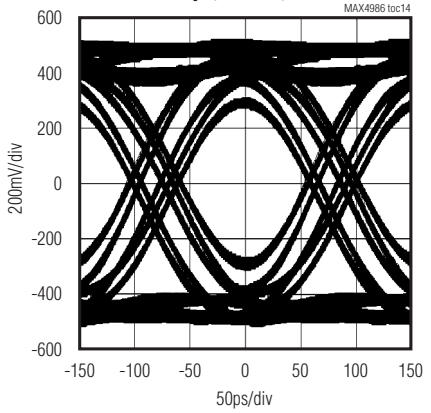
V_{IN} = 1600mV$_{P-P}$, 6.0Gbps, PE = 1, EQ = 0



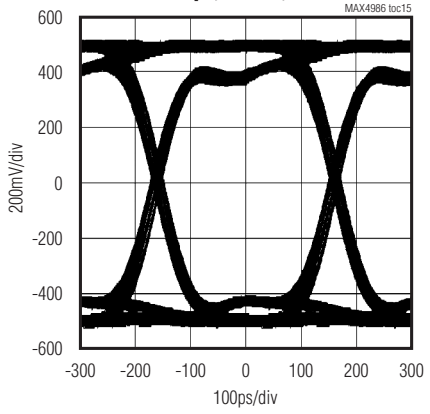
V_{IN} = 500mV$_{P-P}$ WITH 12in FR4 STRIPLINE INPUT, 3.0Gbps, PE = 0, EQ = 0



V_{IN} = 500mV$_{P-P}$ WITH 12in FR4 STRIPLINE INPUT, 6.0Gbps, PE = 0, EQ = 0



V_{IN} = 500mV$_{P-P}$ WITH 12in FR4 STRIPLINE INPUT, 3.0Gbps, PE = 0, EQ = 1

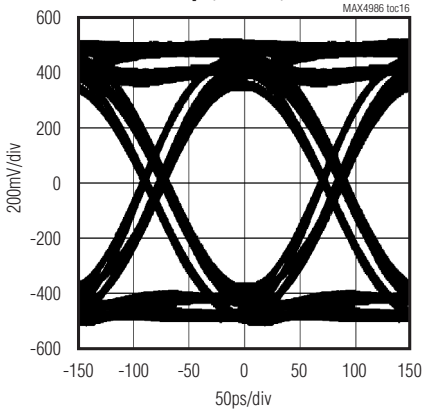


SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

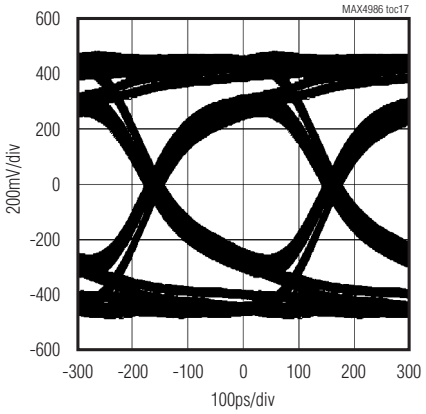
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

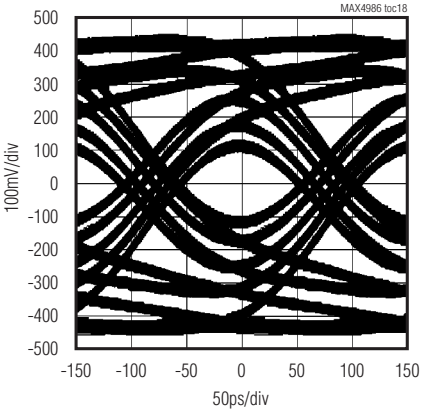
V_{IN} = 500mV$_{P-P}$ WITH 12in FR4 STRIPLINE INPUT, 6.0Gbps, PE = 0, EQ = 1



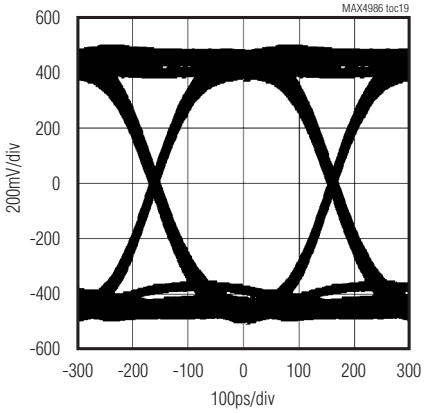
V_{IN} = 275mV$_{P-P}$, 3.0Gbps, PE = 0, EQ = 0 OUTPUT AFTER 12in FR4 STRIPLINE



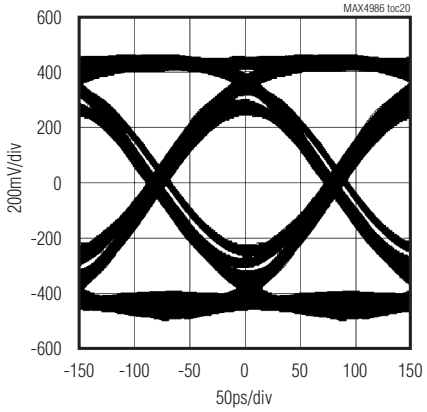
V_{IN} = 275mV$_{P-P}$, 6.0Gbps, PE = 0, EQ = 0 OUTPUT AFTER 12in FR4 STRIPLINE



V_{IN} = 275mV$_{P-P}$, 3.0Gbps, PE = 1, EQ = 0 OUTPUT AFTER 12in FR4 STRIPLINE

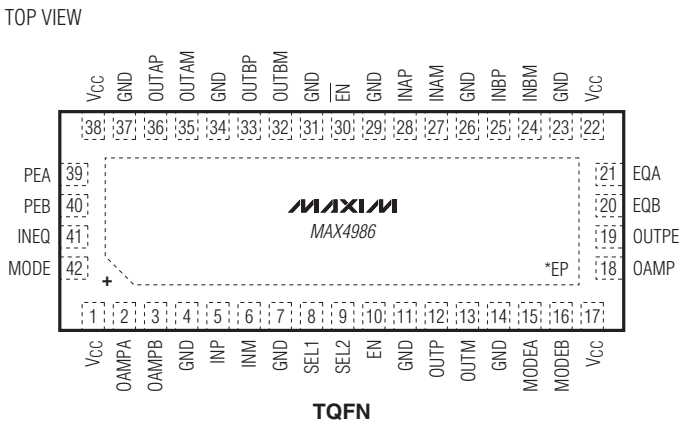


V_{IN} = 275mV$_{P-P}$, 6.0Gbps, PE = 1, EQ = 0 OUTPUT AFTER 12in FR4 STRIPLINE



SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

Pin Configuration



*CONNECT EXPOSED PAD TO GND.

Pin Description

PIN	NAME	FUNCTION
1, 17, 22, 38	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 1µF and 0.01µF capacitors in parallel as close to the device as possible; recommended for each V_{CC} pin.
2	OAMPA	OUTAP/OUTAM Output Level Selection. Drive OAMPA high for low output amplitude. Drive OAMPA low or leave unconnected for high output amplitude. See the *Electrical Characteristics* table. OAMPA is internally pulled down by a 330kΩ (typ) resistor.
3	OAMPB	OUTBP/OUTBM Output Level Selection. Drive OAMPB high for low output amplitude. Drive OAMPB low or leave unconnected for high output amplitude. See the *Electrical Characteristics* table. OAMPB is internally pulled down by a 330kΩ (typ) resistor.
4, 7, 11, 14, 23, 26, 29, 31, 34, 37	GND	Ground
5	INP	Channel 1 Noninverting Input
6	INM	Channel 1 Inverting Input
8	SEL1	Channel 1 Active-Output Selection Input. Drive SEL1 low or leave unconnected to activate A outputs. Drive SEL1 high to activate B outputs. SEL1 is internally pulled down by a 330kΩ (typ) resistor.
9	SEL2	Channel 2 Active-Input Selection Input. Drive SEL2 low or leave unconnected to activate A inputs. Drive SEL2 high to activate B inputs. SEL2 is internally pulled down by a 330kΩ (typ) resistor.
10	EN	Enable Input. Drive EN low or leave unconnected for reduced power standby mode. Drive EN high for normal operation. See Table 1. EN is internally pulled down by a 330kΩ (typ) resistor.
12	OUTP	Channel 2 Noninverting Output
13	OUTM	Channel 2 Inverting Output

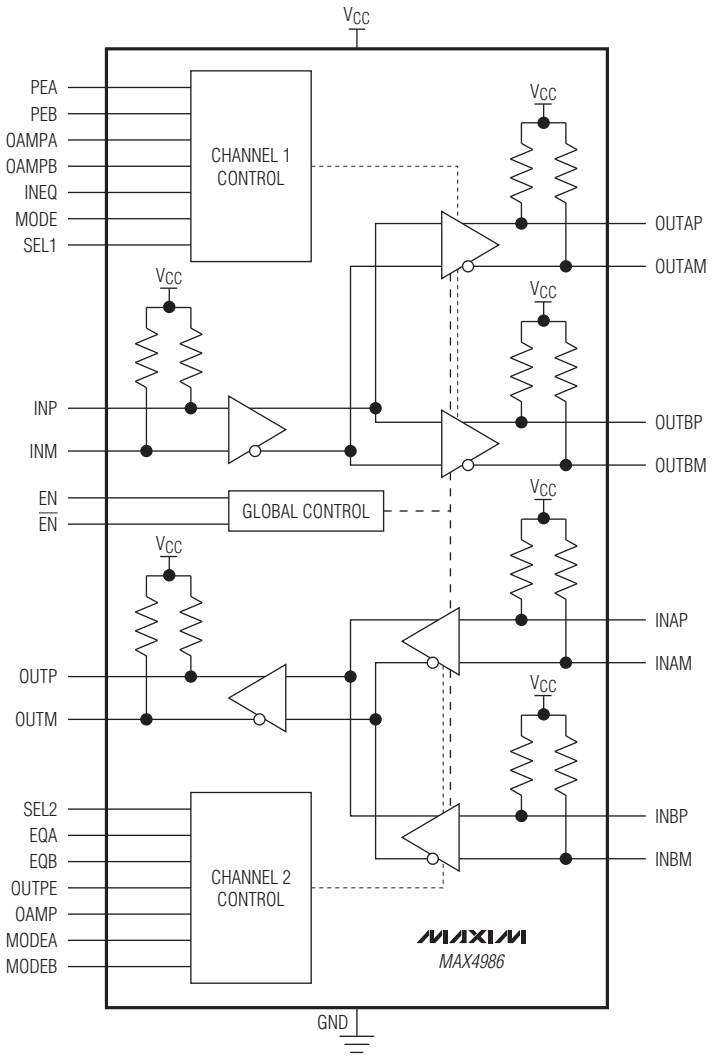
SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

Pin Description (continued)

PIN	NAME	FUNCTION
15	MODEA	INAP/INAM OOB-Mode Logic Input. Drive MODEA low or leave unconnected for SAS OOB threshold. Drive MODEA high for SATA OOB threshold. MODEA is internally pulled down by a 330kΩ (typ) resistor.
16	MODEB	INBP/INBM OOB-Mode Logic Input. Drive MODEB low or leave unconnected for SAS OOB threshold. Drive MODEB high for SATA OOB threshold. MODEB is internally pulled down by a 330kΩ (typ) resistor.
18	OAMP	OUTP/OUTM Output Level Selection. Drive OAMP high for low output amplitude. Drive OAMP low or leave unconnected for high output amplitude. See the *Electrical Characteristics* table. OAMP is internally pulled down by a 330kΩ (typ) resistor.
19	OUTPE	OUTP/OUTM Output Preemphasis Logic Input. Drive OUTPE low or leave unconnected for no output preemphasis. Drive OUTPE high for 3dB (typ) output preemphasis. OUTPE is internally pulled down by a 330kΩ (typ) resistor.
20	EQB	INBP/INBM Input Equalization Logic Input. Drive EQB low or leave unconnected for no input equalization. Drive EQB high for 4dB (typ) input equalization. EQB is internally pulled down by a 330kΩ (typ) resistor.
21	EQA	INAP/INAM Input Equalization Logic Input. Drive EQA low or leave unconnected for no input equalization. Drive EQA high for 4dB (typ) input equalization. EQA is internally pulled down by a 330kΩ (typ) resistor.
24	INBM	Channel 2 Inverting Input B
25	INBP	Channel 2 Noninverting Input B
27	INAM	Channel 2 Inverting Input A
28	INAP	Channel 2 Noninverting Input A
30	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ high or leave unconnected for reduced power standby mode. Drive $\overline{EN}$ low for normal operation. See Table 1. $\overline{EN}$ is internally pulled up by a 330kΩ (typ) resistor.
32	OUTBM	Channel 1 Inverting Output B
33	OUTBP	Channel 1 Noninverting Output B
35	OUTAM	Channel 1 Inverting Output A
36	OUTAP	Channel 1 Noninverting Output A
39	PEA	OUTAP/OUTAM Output Preemphasis Logic Input. Drive PEA low or leave unconnected for no output preemphasis. Drive PEA high for 3dB (typ) output preemphasis. PEA is internally pulled down by a 330kΩ (typ) resistor.
40	PEB	OUTBP/OUTBM Output Preemphasis Logic Input. Drive PEB low or leave unconnected for no output preemphasis. Drive PEB high for 3dB (typ) output preemphasis. PEB is internally pulled down by a 330kΩ (typ) resistor.
41	INEQ	INP/INM Input Equalization Logic Input. Drive INEQ low or leave unconnected for no input equalization. Drive INEQ high for 4dB (typ) input equalization. INEQ is internally pulled down by a 330kΩ (typ) resistor.
42	MODE	INP/INM OOB-Mode Logic Input. Drive MODE low or leave unconnected for SAS OOB threshold. Drive MODE high for SATA OOB threshold. MODE is internally pulled down by a 330kΩ (typ) resistor.
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance.

SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

Functional Diagram



SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

Detailed Description

The MAX4986 is an active 2:1/1:2 multiplexer/demultiplexer designed to equalize and redrive SAS/SATA (Enterprise Class, SATA _X) or SATA-only signals up to 6.0Gbps.

Input/Output Terminations

Inputs and outputs are internally 50Ω terminated to VCC and must be AC-coupled using low-ESR, X7R, 10nF capacitors to the SAS/SATA controller IC and SAS/SATA device for proper operation.

Enable Inputs (EN, $\overline{EN}$)

The MAX4986 features both an active-high enable input (EN) and an active-low enable input ($\overline{EN}$). EN has an internal pulldown resistor of 330kΩ (typ), and $\overline{EN}$ has an internal pullup resistor of 330kΩ (typ). When EN is driven low or left unconnected, or when $\overline{EN}$ is driven high or left unconnected, the MAX4986 enters reduced power standby mode and the redrivers are disabled. In standby mode, supply current is reduced to 350µA (typ). Drive EN high and $\overline{EN}$ low for normal operation. See Table 1. $\overline{EN}$ is useful as an automated cable-detect. See the *Typical Application Circuits*.

Active Input/Output Select (SEL1, SEL2)

SEL1 selects the active output for channel 1 and SEL2 selects the active input for channel 2. Drive SEL1 or SEL2 low or leave unconnected to activate A inputs or outputs. Drive SEL1 or SEL2 high to activate B inputs or outputs. See Table 2. SEL1 and SEL2 have internal pulldown resistors of 330kΩ (typ).

Programmable Output Preemphasis (OUTPE, PEA, PEB)

The MAX4986 features independent output preemphasis capable of providing 3dB preemphasis on each channel. When OUTPE, PEA, or PEB are driven low or left unconnected, the corresponding output has no preemphasis. When OUTPE, PEA, or PEB are driven high, the corresponding output has 3dB preemphasis. See Table 3. OUTPE, PEA, and PEB have internal pulldown resistors of 330kΩ (typ). Output preemphasis should be used when driving long traces or cables.

Programmable Input Equalization (INEQ, EQA, EQB)

The MAX4986 features independent input equalization capable of providing 4dB of high-frequency equalization on each channel. When INEQ, EQA, or EQB are driven low or left unconnected, the corresponding input has no equalization. When INEQ, EQA, or EQB are driven high, the corresponding input has 4dB equalization. See Table 4. INEQ, EQA, and EQB have internal pulldown resistors of 330kΩ (typ). Input equalization should be used for long traces or cables.

Table 1. Standby Mode

EN	$\overline{EN}$	STATUS
0	X	Reduced Power Standby
X	1	Reduced Power Standby
1	0	Active

X = Don't care.

Table 2. Active Input/Output Select

SEL1	SEL2	ACTIVE OUTPUT	ACTIVE INPUT
X	0	X	INAP/INAM
X	1	X	INBP/INBM
0	X	OUTAP/OUTAM	X
1	X	OUTBP/OUTBM	X

X = Don't care.

Table 3. Output Preemphasis

OUTPE	PEA	PEB	OUTP/OUTM	OUTAP/OUTAM	OUTBP/OUTBM
0	X	X	0dB	X	X
1	X	X	3dB	X	X
X	0	X	X	0dB	X
X	1	X	X	3dB	X
X	X	0	X	X	0dB
X	X	1	X	X	3dB

X = Don't care.

Table 4. Input Equalization

INEQ	EQA	EQB	INP/INM	INAP/INAM	INBP/INBM
0	X	X	0dB	X	X
1	X	X	4dB	X	X
X	0	X	X	0dB	X
X	1	X	X	4dB	X
X	X	0	X	X	0dB
X	X	1	X	X	4dB

X = Don't care.

Table 5. OOB Mode Select

MODE	MODEA	MODEB	INP/INM	INAP/INAM	INBP/INBM
0	X	X	SAS	X	X
1	X	X	SATA	X	X
X	0	X	X	SAS	X
X	1	X	X	SATA	X
X	X	0	X	X	SAS
X	X	1	X	X	SATA

X = Don't care.

Table 6. Output Amplitude Selection

OAMP	OAMPA	OAMPB	OUTP/OUTM	OUTAP/OUTAM	OUTBP/OUTBM
0	X	X	HIGH*	X	X
1	X	X	LOW*	X	X
X	0	X	X	HIGH*	X
X	1	X	X	LOW*	X
X	X	0	X	X	HIGH*
X	X	1	X	X	LOW*

X = Don't care.

**See the* Electrical Characteristics *table.*

SAS/SATA Mode Inputs (MODE, MODEA, MODEB)

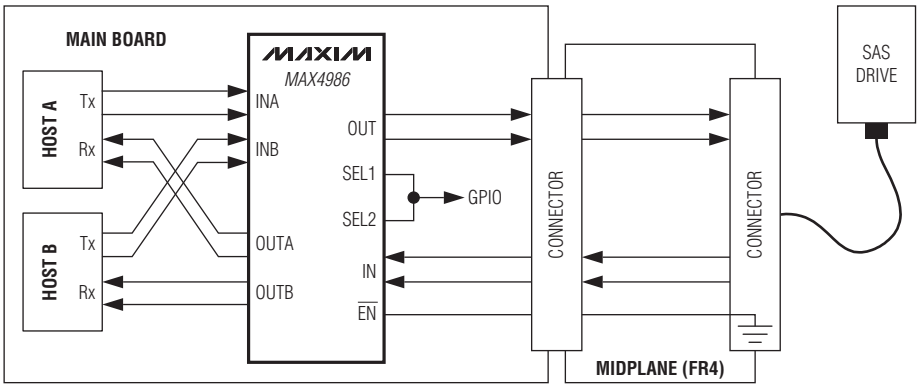
The MAX4986 supports both SAS and SATA OOB levels. When MODE, MODEA, or MODEB are driven low or left unconnected, the corresponding input's OOB threshold is 120mV$_{P-P}$ (min) (SAS mode). When MODE, MODEA, or MODEB are driven high, the corresponding input's OOB threshold is 50mV$_{P-P}$ (min) (SATA mode). Signals below the OOB threshold are squelched to prevent unwanted noise from being redriven at the output. See Table 5. MODE, MODEA, and MODEB have internal pulldown resistors of 330kΩ (typ).

Output Amplitude Selection Inputs (OAMP, OAMPA, OAMPB)

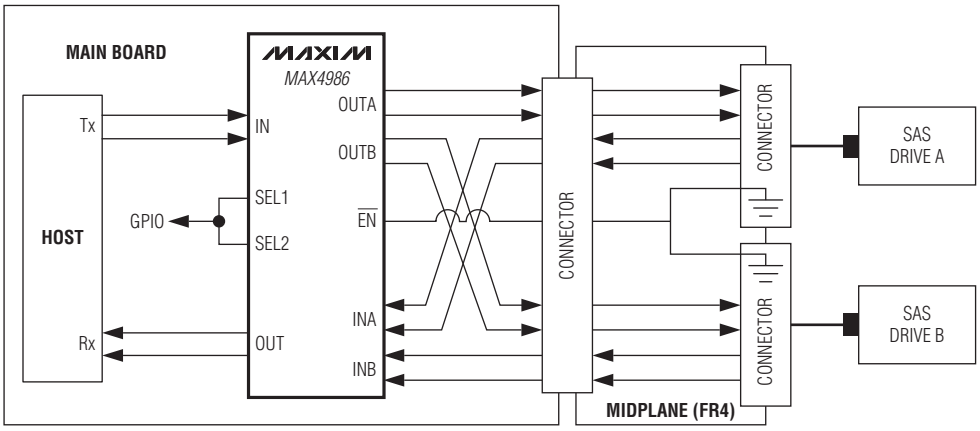
The MAX4986 features independent output amplitude selection. When OAMP, OAMPA, or OAMPB are driven high, the corresponding output amplitude is low. When OAMP, OAMPA, or OAMPB are driven low or left unconnected, the corresponding output amplitude is high. See Table 6. OAMP, OAMPA, and OAMPB have internal pulldown resistors of 330kΩ (typ).

SAS/SATA Single Lane 2:1/1:2 Multiplexer/ Demultiplexer Plus Redriver with Equalization

Typical Application Circuits



NOTE: TWO HOSTS SHARING A SINGLE SAS DRIVE WITH CABLE-DETECT.



NOTE: SINGLE HOST WITH TWO SAS DRIVES AND CABLE-DETECT.

Applications Information

Layout

Circuit board layout and design can significantly affect the performance of the MAX4986. Use good, high-frequency design techniques, including minimizing ground inductance and using controlled impedance transmission lines on data signals. It is recommended to place 1µF and 0.01µF power-supply bypass capacitors in parallel as close to V_{CC} as possible for each V_{CC} pin. Always connect V_{CC} to a power plane.

Exposed-Pad Package

The exposed-pad, 42-pin TQFN package incorporates features that provide a very low-thermal resistance path for heat removal from the IC. The exposed pad on the MAX4986 must be soldered to the circuit board ground plane for proper thermal performance. For more information on exposed-pad packages, refer to Maxim Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

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Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply GND then V_{CC} before applying signals, especially if the signal is not current-limited.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
42 TQFN-EP	T423590+1	21-0181	90-0078

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/10	Initial release	—
1	7/12	Added MAX4986ETO+ to data sheet	1, 2, 3