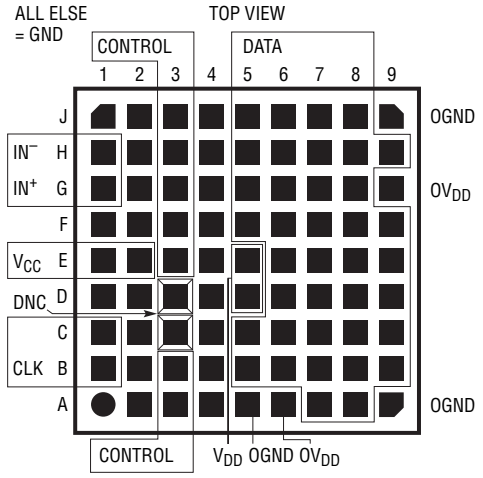
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 3.6V
Supply Voltage (V_{DD}) ..... –0.3V to 4V
Digital Output Supply Voltage (OV_{DD}) ..... –0.3V to 4V
Analog Input Current (IN^+, IN^-) ..... ±10mA
Digital Input Voltage
(Except AMPSHDN) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage
(AMPSHDN) ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)
Operating Temperature Range
LTM9001C ..... 0°C to 70°C
LTM9001I ..... –40°C to 85°C
Storage Temperature Range ..... –45°C to 125°C
Maximum Junction Temperature ..... 125°C

PIN CONFIGURATION



LGA PACKAGE
T_{JMAX} = 125°C, θ_{JA} = 15°C/W, θ_{JC} = 19°C/W
θ_{JA} DERIVED FROM 60mm × 70mm PCB WITH 4 LAYERS
WEIGHT = 0.71g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9001CV-GA#PBF	LTM9001CV-GA#PBF	LTM9001V-GA	81-Lead (11.25mm × 11.25mm × 2.3mm) LGA	0°C to 70°C
LTM9001IV-GA#PBF	LTM9001IV-GA#PBF	LTM9001V-GA	81-Lead (11.25mm × 11.25mm × 2.3mm) LGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G_{DIFF}	Gain	DC, LTM9001-GA f_{IN} = 5MHz	●	7.2	8 8	8.8	dB
G_{TEMP}	Gain Temperature Drift	V_{IN} = Maximum, (Note 3)			2		mdB/°C
V_{INCM}	Input Common Mode Voltage Range	(IN^+ + IN^-)/2			1.0–1.6		V
V_{IN}	Input Voltage Range at –1dBFS	LTM9001-GA at 5MHz			900		mV_{P-P}
R_{INDIFF}	Differential Input Impedance	LTM9001-GA			400		Ω
C_{INDIFF}	Differential Input Capacitance	Includes Parasitic			1		pF
V_{OS}	Offset Error (Note 6)	Including Amplifier and ADC (LTM9001-GA)	●	–50	–10		mV
	Offset Drift	Including Amplifier and ADC			±10		µV/°C
	Full-Scale Drift	Internal Reference External Reference			±30 ±15		ppm/°C ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio				60		dB
I_{SENSE}	SENSE Input Leakage Current	0V < SENSE < V_{DD} (Note 9)	●	–3		3	µA
I_{MODE}	MODE Pin Pull-Down Current to GND				10		µA
$I_{\overline{OE}}$	$\overline{OE}$ Pin Pull-Down Current to GND				10		µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				70		fs_{RMS}

CONVERTER CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	16			Bits
Integral Linearity Error	Differential Input LTM9001-GA (Note 5)	●		±2.4	±8	LSB
Differential Linearity Error	Differential Input	●		±0.3	±1	LSB
Transition Noise	External Reference			1		LSB_{RMS}

DYNAMIC ACCURACY

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input (PGA = 0) 5MHz Input (PGA = 1)	●	76	78 75.4		dBFS dBFS
SFDR	Spurious Free Dynamic Range, 2nd or 3rd Harmonic	5MHz Input (PGA = 0) 5MHz Input (PGA = 1)	●	76	87 89.8		dBc dBc
SFDR	Spurious Free Dynamic Range 4th or Higher	5MHz Input (PGA = 0) 5MHz Input (PGA = 1)	●	91	100 99		dBc dBc
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input (PGA = 0) 5MHz Input (PGA = 1)	●	75	77.4 74.8		dBFS dBFS
SFDR	Spurious Free Dynamic Range at –15dBFS, Dither "OFF"	5MHz Input (PGA = 0) 5MHz Input (PGA = 1)	●	91	105 107.5		dBFS dBFS
SFDR	Spurious Free Dynamic Range at –15dBFS, Dither "ON"	5MHz Input (PGA = 0) 5MHz Input (PGA = 1)	●	93	107 109		dBFS dBFS
IMD3	Third Order Intermodulation Distortion; 1MHz Tone Spacing, 2 Tones at –7dBFS	f_{IN} = 5MHz			85		dB
IIP3	Equivalent Third Order Input Intercept Point, 2 Tone	f_{IN} = 5MHz			36.5		dBm

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (DITH, PGA, ADCSHDN, RAND, CLK, $\overline{OE}$)							
V_{IH}	High Level Input Voltage	V_{DD} = 3.3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3.3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Input Capacitance	(Note 7)			1.5		pF
Logic Inputs (AMPSHDN)							
V_{IH}	High Level Input Voltage	V_{CC} = 3.3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.3V	●			0.8	V
I_{IH}	Input High Current	V_{IN} = 2V			1.3		µA
I_{IL}	Input Low Current	V_{IN} = 0.8V			0.1		µA
C_{IN}	Input Capacitance	(Note 7)			1.5		pF
Logic Outputs							
OV_{DD} = 3.3V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –10µA V_{DD} = 3.3V, I_O = –200µA	 ●	 3.1	3.299 3.29		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 10µA V_{DD} = 3.3V, I_O = 1.6mA	 ●		0.01 0.1	 0.4	V V
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3.3V			50		mA
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 1.6mA			0.1		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 1.6µA			0.1		V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	ADC Analog Supply Voltage	(Note 8)	●	3.135	3.3	3.465	V
V_{CC}	Amplifier Supply Voltage		●	2.85		3.5	V
I_{CC}	Amplifier Supply Current		●		100	136	mA
P_{SHDN}	Total Shutdown Power	AMPSHDN = ADCSHDN = 3.3V			10		mW
OV_{DD}	Output Supply Voltage	(Note 8)	●	0.5		3.6	V
I_{VDD}	Analog Supply Current	LTM9001-GA	●		66	80	mA
P_{DISS}	ADC Power Dissipation	LTM9001-GA	●		220	265	mW
$P_{DISS(TOTAL)}$	Total Power Dissipation	LTM9001-GA			550		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency (Note 8)	LTM9001-GA	●	1		25	MHz
t_L	CLK Low Time (Note 7)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	18.9 5	20 20	500 500	ns ns
t_H	CLK High Time (Note 7)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	18.9 5	20 20	500 500	ns ns
CMOS Output Mode							
t_D	CLK to DATA Delay	(Note 7)	●	1.3	3.1	4.9	ns
t_C	CLK to CLKOUT Delay	(Note 7)	●	1.3	3.1	4.9	ns
t_{SKEW}	DATA to CLKOUT Skew	(t_C – t_D) (Note 7)	●	–0.6	0	0.6	ns
	Data Latency				7		Cycles

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: Gain is measured from IN^+/IN^- through the ADC.

Note 4: V_{CC} = V_{DD} = 3.3V, f_{SAMPLE} = maximum sample frequency, input range = –1dBFS with PGA = 0 with differential drive, AC-coupled inputs, unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a "best fit straight line" to the transfer curve. The deviation is measured from the center of the quantization band.

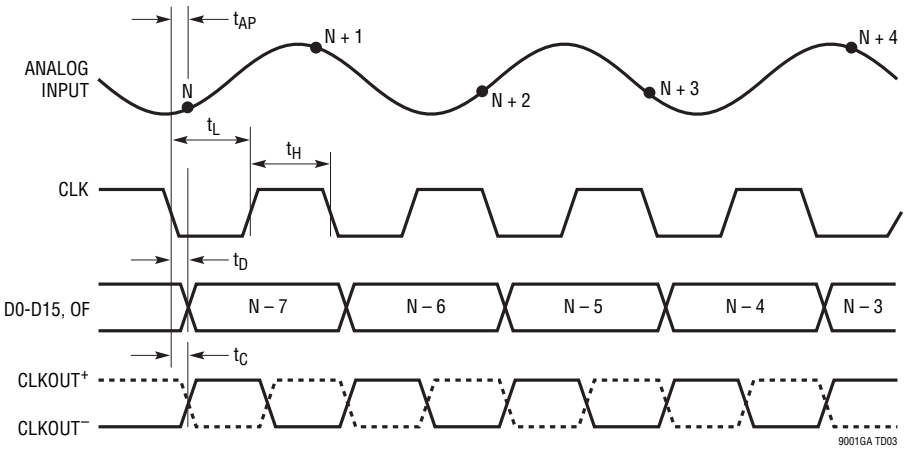
Note 6: Offset error is the voltage applied between the IN^+ and IN^- pins required to make the output code flicker between 0000 0000 0000 0000 and 1111 1111 1111 1111.

Note 7: Guaranteed by design, not subject to test.

Note 8: Recommended operating conditions.

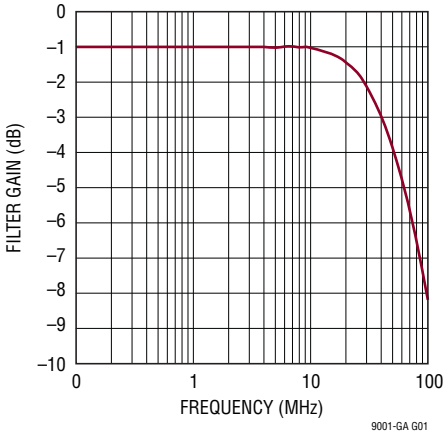
Note 9: Leakage current will experience transient at power up. Keep resistance <1kΩ.

TIMING DIAGRAM

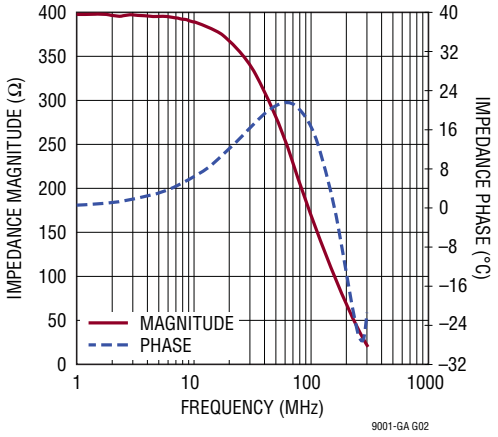


TYPICAL PERFORMANCE CHARACTERISTICS

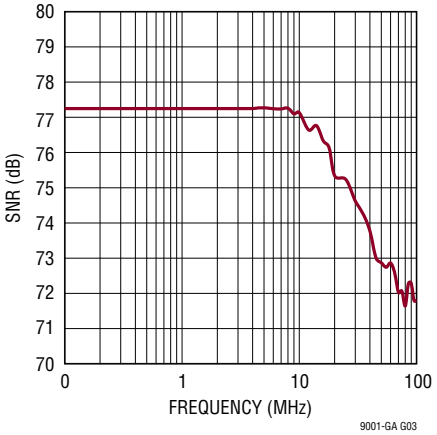
IF Frequency Response



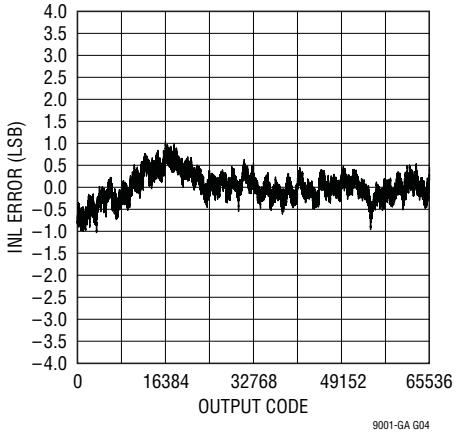
Input Impedance vs Frequency



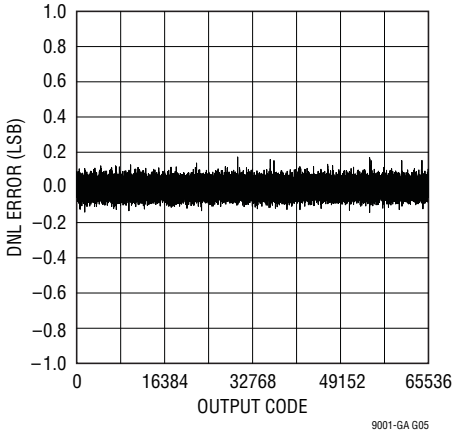
SNR vs Frequency



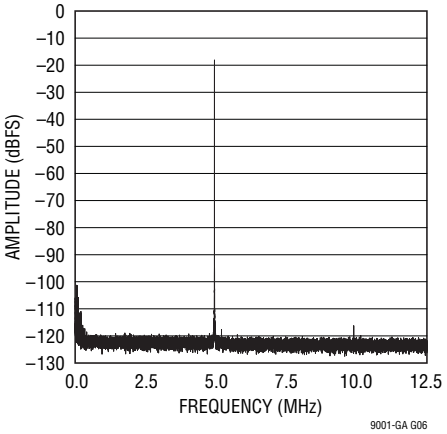
Integral Non-Linearity (INL) vs Output Code



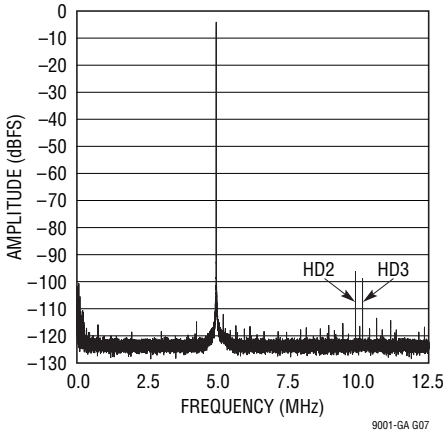
Differential Non-Linearity (DNL) vs Output Code



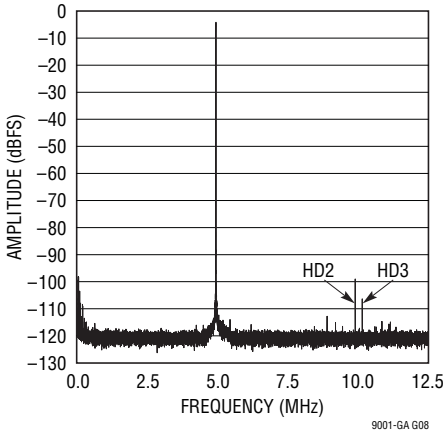
64k Point FFT, f_{IN} = 5MHz, –15dBFS, PGA = 0, RAND "On", Dither "On"



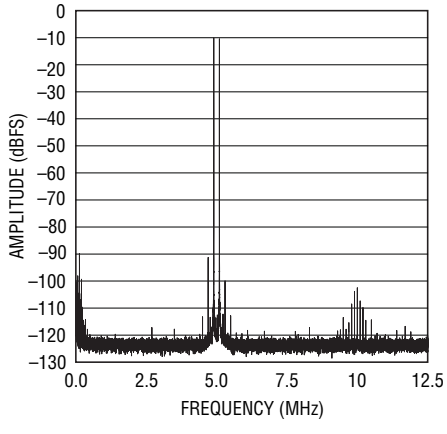
64k Point FFT, f_{IN} = 5MHz, –1dBFS, PGA = 0, RAND "Off", Dither "Off"



64k Point FFT, f_{IN} = 5MHz, –1dBFS, PGA = 1, RAND "Off", Dither "Off"



64k Point 2-Tone FFT, f_{IN} = 4.9MHz, and f_{IN} = 5.1MHz, –7dBFS Per Tone, PGA = 0, RAND "Off", Dither "Off"



PIN FUNCTIONS

Supply Pins

V_{CC} (Pins E1, E2): 3.3V Analog Supply Pin for Amplifier. The voltage on this pin provides power for the amplifier stage only and is internally bypassed to GND.

V_{DD} (Pins E5, D5): 3.3V Analog Supply Pin for ADC. This supply is internally bypassed to GND.

OV_{DD} (Pins A6, G9): Positive Supply for the ADC Output Drivers. This supply is internally bypassed to OGND.

GND (Pins A1, A2, A4, B2, B4, C2, C4, D1, D2, D4, E4, F1, F2, F4, G2, G4, H2, H4, J1, J2, J4): Analog Ground.

OGND (Pins A5, A9, G8, J9): ADC Output Driver Ground.

Analog Inputs

IN^+ (Pin G1): Positive (Noninverting) Amplifier Input.

IN^- (Pin H1): Negative (Inverting) Amplifier Input.

DNC (Pins C3, D3): Do Not Connect. These pins are used for testing and should not be connected on the PCB. They may be soldered to unconnected pads and should be well isolated. The DNC pins connect to the signal path prior to the ADC inputs; therefore, care should be taken to keep other signals away from these sensitive nodes.

NC (See Pin Configuration Table for Pin Locations): No Connect.

CLK (Pin B1): Clock Input. The sampled analog input is held on the falling edge of CLK. The output data may be latched on the rising edge of CLK.

Control Inputs

SENSE (Pin J3): Reference Mode Select and External Reference Input. Tie SENSE to V_{DD} to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set the maximum full-scale input range.

AMPSHDN (Pin H3): Power Shutdown Pin for Amplifier. This pin is a logic input referenced to analog ground. AMPSHDN = low results in normal operation. AMPSHDN = high results in powered down amplifier with typically 3mA amplifier supply current.

MODE (Pin G3): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to $1/3V_{DD}$ selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to $2/3V_{DD}$ selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to V_{DD} selects 2's complement output format and disables the clock duty cycle stabilizer.

RAND (Pin F3): Digital Output Randomization Selection Pin. RAND = low results in normal operation. RAND = high selects D1 to D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. This mode of operation reduces the effects of digital output interference.

PGA (Pin E3): Programmable Gain Amplifier Control Pin. PGA = low selects the normal (maximum) input voltage range. PGA = high selects a 3.5dB reduced input range for slightly better distortion performance at the expense of SNR.

ADCSHDN (Pin B3): Power Shutdown Pin for ADC. ADCSHDN = low results in normal operation. ADCSHDN = high results in powered down analog circuitry and the digital outputs are placed in a high impedance state.

DITH (Pin A3): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation.

$\overline{OE}$ (Pin F5): Output Enable Pin. Low enables the digital output drivers. High puts digital outputs in Hi-Z state.

Digital Outputs

D0 to D15 (See Pin Configuration Table for Pin Locations): Digital Outputs. D15 is the MSB and D0 the LSB.

$CLKOUT^+$ (Pin E7): Inverted Data Valid Output. $CLKOUT^+$ will toggle at the sample rate. Latch the data on the rising edge of $CLKOUT^+$.

$CLKOUT^-$ (Pin E6): Data Valid Output. $CLKOUT^-$ will toggle at the sample rate. Latch the data on the falling edge of $CLKOUT^-$.

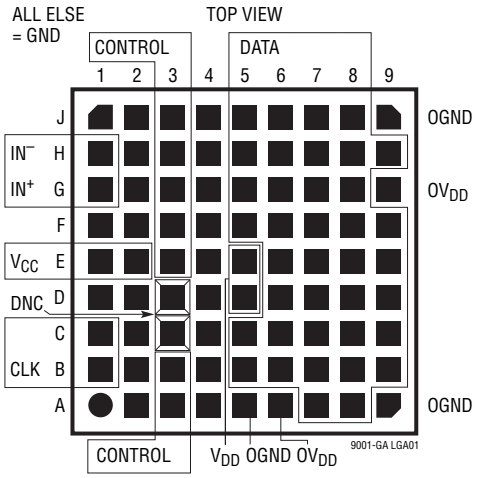
OF (Pin G5): Over/Under Flow Digital Output. OF is high when an over or under flow has occurred.

PIN FUNCTIONS

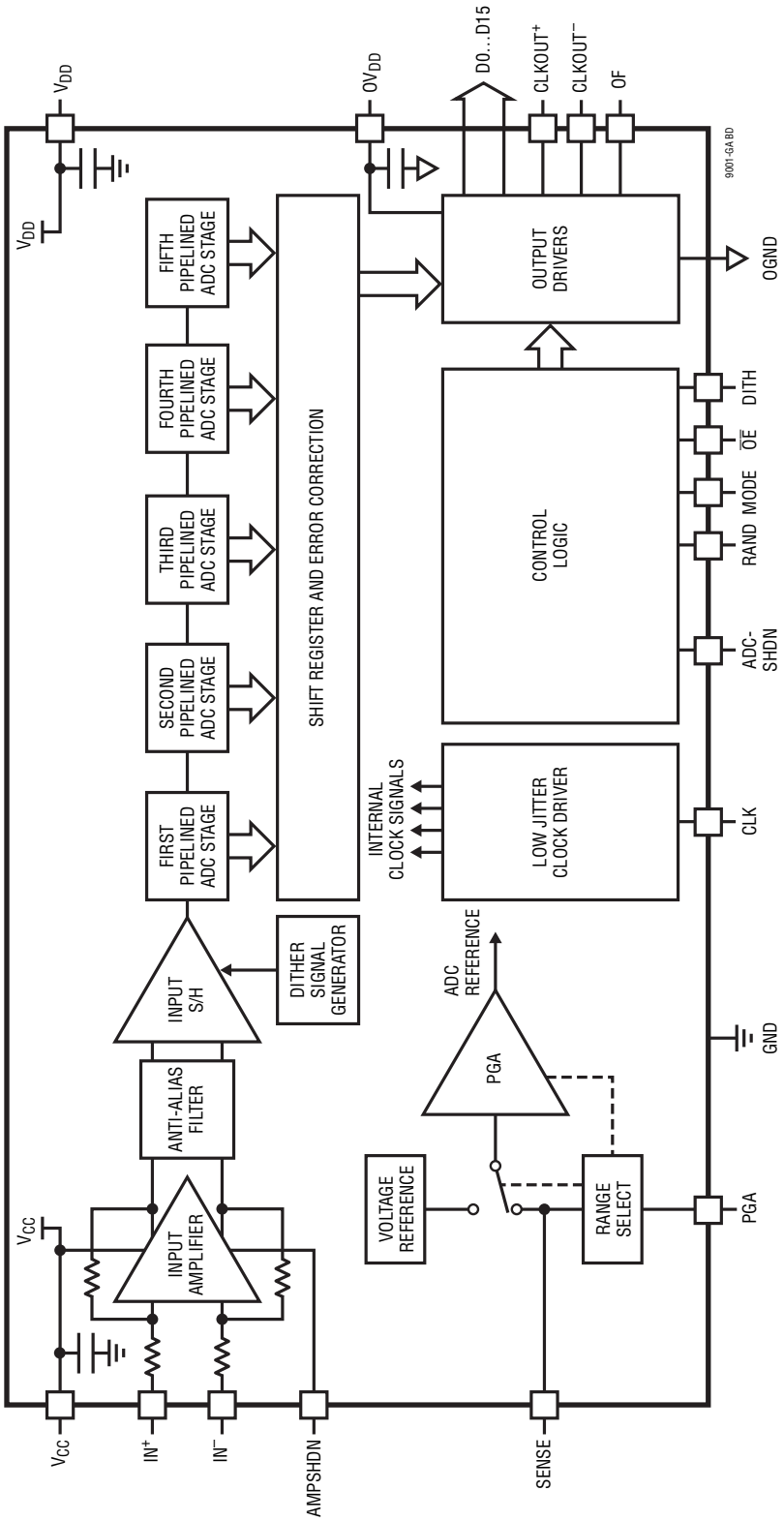
Pin Configuration

	1	2	3	4	5	6	7	8	9
J	GND	GND	SENSE	GND	D14	NC	D12	NC	OGND
H	IN^-	GND	AMPSHDN	GND	NC	NC	NC	NC	D11
G	IN^+	GND	MODE	GND	OF	D15	D13	OGND	OV_{DD}
F	GND	GND	RAND	GND	$\overline{OE}$	NC	D9	NC	D10
E	V_{CC}	V_{CC}	PGA	GND	V_{DD}	$CLKOUT^-$	CLKOUT	NC	D8
D	GND	GND	DNC	GND	V_{DD}	NC	D6	NC	D7
C	NC	GND	DNC	GND	D0	NC	D4	NC	D5
B	CLK	GND	ADCSHDN	GND	NC	NC	D1	D3	NC
A	GND	GND	DITH	GND	OGND	OV_{DD}	NC	D2	OGND

Top View of LGA Pinout (Looking Through Component)



FUNCTIONAL BLOCK DIAGRAM



OPERATION

DYNAMIC PERFORMANCE DEFINITIONS

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output.

Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = -20Log\left(\sqrt{(V2^2 + V3^2 + V4^2 + ...Vn^2)}/V1\right)$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics.

Intermodulation Distortion

If the input signal consists of more than one spectral component, the transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the input, nonlinearities in the transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc.

For example, the 3rd order IMD terms include (2fa + fb), (fa + 2fb), (2fa – fb) and (fa – 2fb). The 3rd order IMD is defined as the ration of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

Spurious Free Dynamic Range (SFDR)

The ratio of the RMS input signal amplitude to the RMS value of the peak spurious spectral component expressed in dBc. SFDR may also be calculated relative to full scale and expressed in dBFS.

Aperture Delay Time

Aperture Delay is the time from when a rising ENC^+ equals the $ENC^–$ voltage to the instant that the input signal is held by the sample and-hold circuit. Or, for single-ended CLK versions, the time from when CLK reaches 0.45 of V_{DD} to the instant that the input signal is held by the sample-and-hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20log\ (2\pi \bullet f_{IN} \bullet t_{JITTER})$$

DESCRIPTION

The LTM9001 is an integrated System in a Package (SiP) µModule® receiver that includes a high-speed, sampling 16-bit A/D converter, matching network, anti-aliasing filter and a low noise, differential amplifier with fixed gain. It is designed for digitizing high frequency, wide dynamic range signals with an intermediate frequency (IF) range up to 300MHz.

µModule is a registered trademark of Linear Technology Corporation.

OPERATION

The following sections describe in further detail the functional operation of the LTM9001. The SiP technology allows the LTM9001 to be customized and this is described in the first section. The remaining outline follows the basic functional elements as shown in Figure 1.

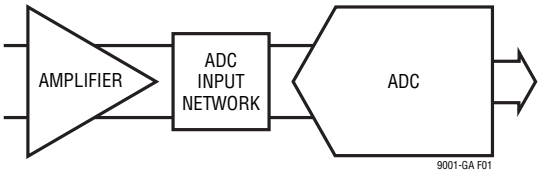


Figure 1. Basic Functional Elements

SEMI-CUSTOM OPTIONS

The µModule construction affords a new level of flexibility in application-specific standard products. Standard ADC and amplifier components can be integrated regardless of their process technology and matched with passive components to a particular application. The LTM9001-AA, on a separate data sheet, is configured with a 16-bit ADC sampling at rates up to 130Msps. The amplifier gain is 20dB with an input impedance of 200Ω and an input range of $233mV_{P-P}$. The matching network is designed to optimize the interface between the amplifier output and the ADC under these conditions. Additionally, there is a 2-pole bandpass filter designed for 162.5MHz ±25MHz.

However, other options are possible through Linear Technology's semi-custom development program. Linear Technology has in place a program to deliver other speed, resolution, IF range, gain and filter configurations for a wide range of applications. See Table 1 for the LTM9001 configuration and potential options. These semi-custom designs are based on existing ADCs and amplifiers with an appropriately modified matching network. The final subsystem is then tested to the exact parameters defined for the application. The final result is a fully integrated, accurately tested and reliable solution. For more details on the semi-custom receiver subsystem program, contact Linear Technology.

Note that not all combinations of options in Table 1 are possible at this time and specified performance may differ significantly from existing values. The higher speed options support LVDS or CMOS outputs and are available on a separate data sheet. This data sheet discusses CMOS only versions which have a different pin assignment.

AMPLIFIER INFORMATION

The amplifiers used in the LTM9001 are low noise and low distortion fully differential ADC drivers. The amplifiers are very flexible in terms of I/O coupling. They can be AC- or DC-coupled at the inputs. Users are advised to keep the input common mode voltage between 1V and 1.6V for proper operation. If the inputs are AC-coupled, the input common mode voltage is automatically biased. The input signal can be either single-ended or differential with almost no difference in distortion performance.

ADC INPUT NETWORK

The passive network between the amplifier output stage and the ADC input stage can be configured for bandpass or lowpass response with different cutoff frequencies and bandwidths. The LTM9001-GA, for example, implements a 1-pole lowpass filter with 10MHz bandwidth. Note that the filter attenuates the signal at 10MHz by 0.2dB, making the overall gain of the subsystem 7.8dB.

For production test purposes the filter is designed to allow DC inputs into the ADC.

CONVERTER INFORMATION

The analog-to-digital converter (ADC) is a CMOS pipelined multistep converter with a front-end PGA. As shown in the Functional Block Diagram, the converter has five pipelined ADC stages; a sampled analog input will result in a digitized value seven cycles later (see the Timing Diagram section). The encode input is differential for improved common mode noise immunity.

OPERATION

Table 1. Semi-Custom Options

AMPLIFIER IF RANGE	AMPLIFIER INPUT IMPEDANCE	AMPLIFIER GAIN	FILTER	ADC SAMPLE RATE	ADC RESOLUTION	OUTPUT	PART NUMBER
300MHz	200Ω	20dB	162.5MHz BPF, 50MHz BW	130Msps	16-bit	LVDS/CMOS	LTM9001-AA
300MHz	200Ω	14dB	70MHz BPF, 25MHz BW	130Msps	16-bit	LVDS/CMOS	LTM9001-AD
300MHz	400Ω	8dB	DC-300MHz LPF	160Msps	16-bit	LVDS/CMOS	LTM9001-BA
300MHz	400Ω	8dB	DC-10MHz LPF	25Msps	16-bit	CMOS	LTM9001-GA
Select Combination of Options from Columns Below							
DC-300MHz	50Ω	26dB	LPF TBD	160Msps	16-bit	LVDS/CMOS	
DC-140MHz	200Ω	20dB	BPF TBD	130Msps	14-bit	LVDS/CMOS	
DC-70MHz	200Ω	14dB		105Msps		CMOS	
DC-35MHz	400Ω	8dB		80Msps		CMOS	
	200Ω	6dB		65Msps		CMOS	
				40Msps		CMOS	
				25Msps		CMOS	
				10Msps		CMOS	

APPLICATIONS INFORMATION

INPUT SPAN

The LTM9001 is configured with a fixed input span and input impedance. With the amplifier gain and the ADC input network described above for LTM9001-GA, the full-scale input range of the driver circuit is 1000mV$_{P-P}$. The recommended ADC input span is achieved by tying the SENSE pin to V_{DD}. However, the ADC input span can be changed by applying a DC voltage to the SENSE pin.

Input Impedance and Matching

The differential input impedance of the LTM9001 can be 50Ω, 200Ω or 400Ω. In some applications the differential inputs may need to be terminated to a lower value impedance, e.g. 50Ω, in order to provide an impedance match for the source. Several choices are available.

One approach is to use a differential shunt resistor (Figure 2). Another approach is to employ a wideband transformer (Figure 3). Both methods provide a wideband match. The termination resistor or the transformer must be placed close to the input pins in order to minimize the reflection due to input mismatch.

Table 2. Differential Amplifier Input Termination Values

Z_{IN}	R_T Figure 2
400Ω	57Ω
200Ω	66.5Ω
50Ω	None

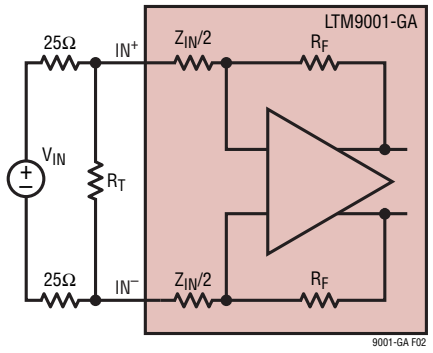


Figure 2. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor (See Table 2 for R_T Values)

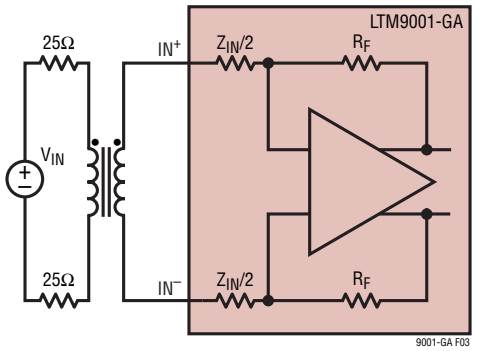


Figure 3. Input Termination for Differential 50Ω Input Impedance Using a Wideband Transformer

APPLICATIONS INFORMATION

Alternatively, one could apply a narrowband impedance match at the inputs for frequency selection and/or noise reduction.

Referring to Figure 4, amplifier inputs can be easily configured for single-ended input without a balun. The signal is fed to one of the inputs through a matching network while the other input is connected to the same impedance. In general, the single-ended input impedance and termination resistor R_T are determined by the combination of R_S, $Z_{IN}/2$ and R_F.

Table 3. Single-Ended Amplifier Input Termination Values

Z_{IN}	R_T Figure 4
400Ω	59Ω
200Ω	68.5Ω
50Ω	150Ω

The LTM9001 amplifier is stable with all source impedances. The overall differential gain is affected by the source impedance in Figure 5:

$$A_V = | V_{OUT}/V_{IN} | = (1000/(R_S + Z_{IN}/2))$$

The noise performance of the amplifier also depends upon the source impedance and termination. For example, an input 1:4 transformer in Figure 3 improves the input noise figure by adding 6dB voltage gain at the inputs.

Reference and SENSE Pin Operation

Figure 6 shows the converter reference circuitry consisting of a 2.5V bandgap reference, a programmable gain amplifier and control circuit. There are three modes of reference operation: Internal Reference, 1.25V external reference or 2.5V external reference. To use the internal reference, tie the SENSE pin to V_{DD}. To use an external reference, simply apply either a 1.25V or 2.5V reference voltage to the SENSE input pin. Both 1.25V and 2.5V applied to SENSE will result in the maximum full-scale range.

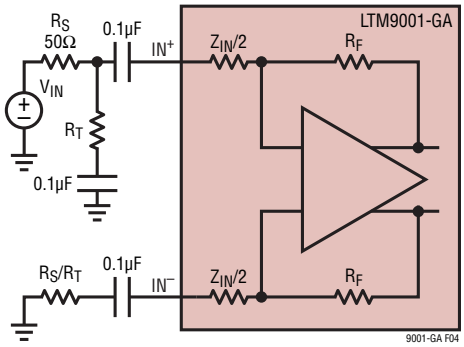


Figure 4. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor

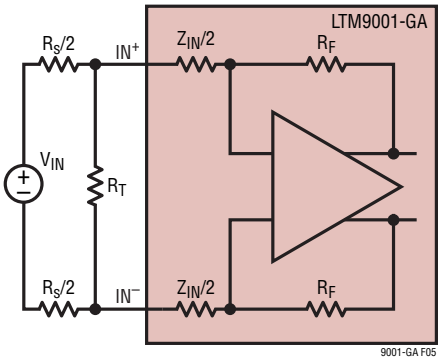


Figure 5. Calculate Differential Gain

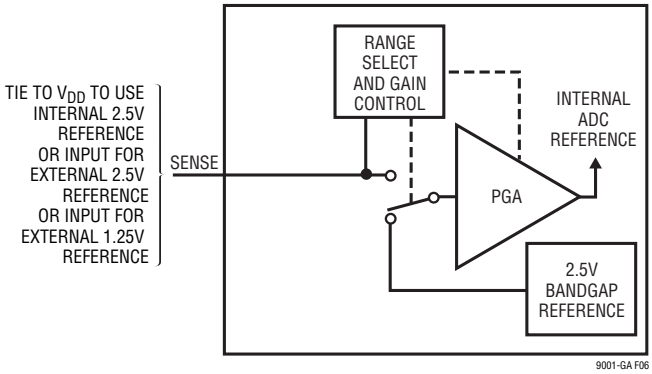


Figure 6. Reference Circuit

APPLICATIONS INFORMATION

PGA Pin

The PGA pin selects between two gain settings for the ADC front-end. PGA = low selects the maximum input span; PGA = high selects a 3.5dB lower input span. The high input range has the best SNR. For applications with high linearity requirements, the low input range will have improved distortion; however, the SNR will be 1.8dB worse. See the Typical Performance Characteristics section.

Driving the Clock or Encode Inputs

Certain versions of LTM9001 have differential encode inputs, others have a single-ended clock input.The noise performance of the converter can depend on the encode signal quality as much as the analog input. The encode inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter. In applications where jitter is critical (high input frequencies), take the following into consideration:

1. Differential drive should be used.
2. Use the largest amplitude possible. If using transformer coupling, use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a fixed frequency sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs such that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.2V to V_{DD}. Each input may be driven from ground to V_{DD} for single-ended drive.

The encode clock inputs have a differential 100Ω input impedance. For 50Ω inputs e.g. signal generators, an additional 100Ω impedance will provide an impedance match, as shown in Figure 7b.

The single-ended CLK input on LTM9001-GA can be driven directly with a CMOS or TTL level signal. A sinusoidal clock can be used along with a low-jitter squaring circuit before the CLK pin (Figure 8).

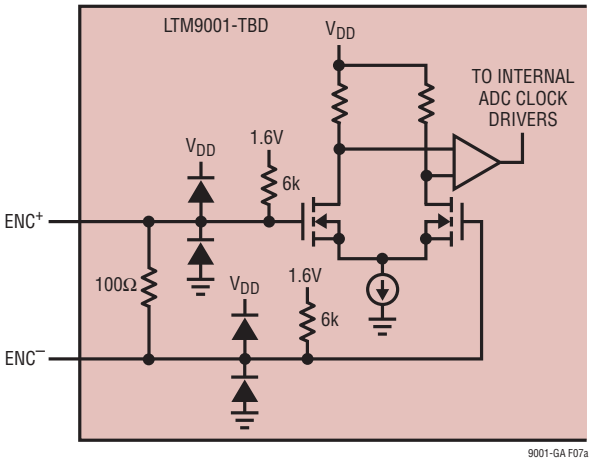
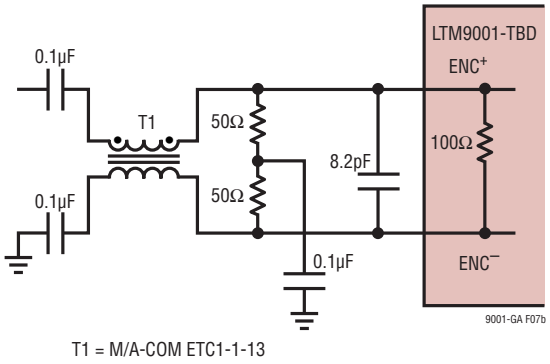


Figure 7a. Equivalent Encode Input Circuit



T1 = M/A-COM ETC1-1-13

Figure 7b. Transformer Driven Encode

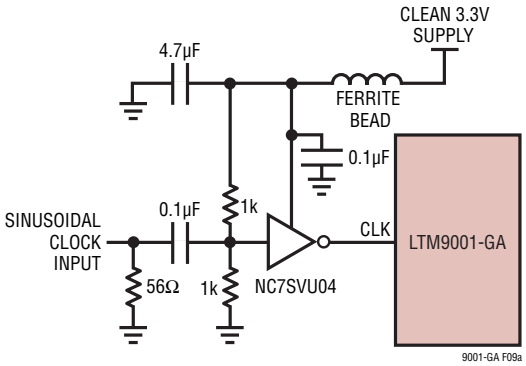


Figure 8. Sinusoidal Single-Ended CLK Drive

APPLICATIONS INFORMATION

Maximum and Minimum Encode Rates

The maximum encode rate for the LTM9001-GA is 25Msps. For the ADC to operate properly the CLK signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 18.9ns (LTM9001-GA) for the ADC internal circuitry to have enough settling time for proper operation.

An optional clock duty cycle stabilizer can be used if the input clock does not have a 50% duty cycle. This circuit uses the rising edge of CLK or ENC to sample the analog input. The falling edge of CLK or ENC is ignored and an internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 30% to 70% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin must be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the sample rate is determined by the droop of the sample and hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTM9001 is 1Msps.

DIGITAL OUTPUTS

Digital Output Buffers

Figure 9 shows an equivalent circuit for a single output buffer in CMOS mode. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and eliminates the need for external damping resistors.

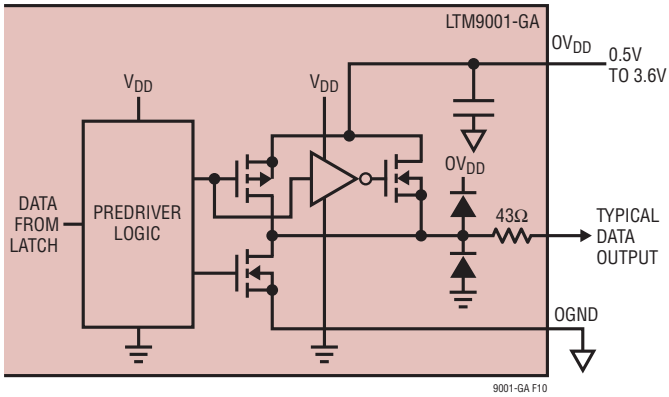


Figure 9. Equivalent Circuit for a Digital Output Buffer

APPLICATIONS INFORMATION

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTM9001 should drive a minimum capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF. A resistor in series with the output may be used but is not required since the ADC has a series resistor of 43Ω on chip.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Data Format

The LTM9001 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. This pin has a four level logic input, centered at 0, $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD}. An external resistive divider can be used to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 5 shows the logic states for the MODE pin.

Table 5. MODE Pin Function

MODE	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0V(GND)	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

An overflow output bit (OF) indicates when the converter is over-ranged or under-ranged. A logic high on the OF pin indicates an overflow or underflow.

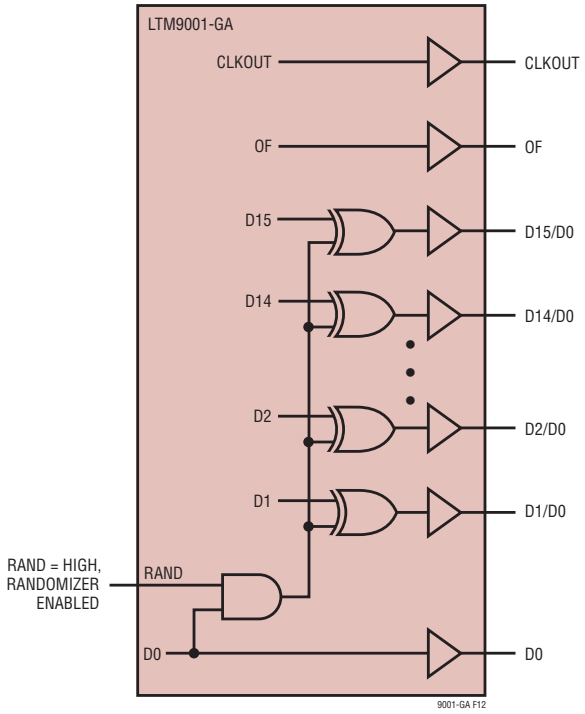


Figure 10. Functional Equivalent of Digital Output Randomizer

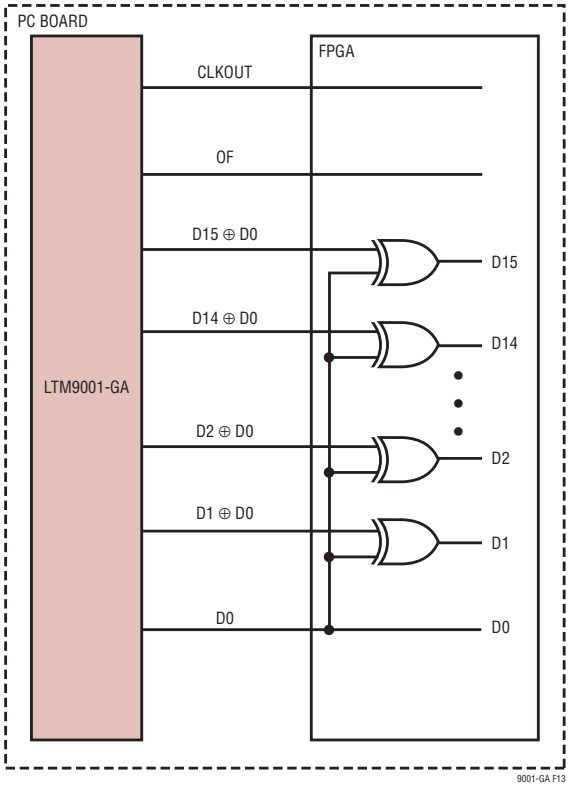


Figure 11. Derandomizing a Randomized Digital Output

APPLICATIONS INFORMATION

Output Clock

The ADC has a delayed version of the encode input available as a digital output. Both a non-inverted version, CLKOUT+, and an inverted version, CLKOUT–, are provided. The CLKOUT pins can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. Data will be updated as CLKOUT+ falls and CLKOUT– rises. Data may be latched on the rising edge of CLKOUT+ or the falling edge of CLKOUT–.

Digital Output Randomizer

Interference from the ADC digital outputs is sometimes unavoidable. Interference from the digital outputs may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can result in discernible unwanted tones in the ADC output spectrum.

By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized, trading a slight increase in the noise floor for a large reduction in unwanted tone amplitude.

The digital output is randomized by applying an exclusive-OR logic operation between the LSB and all other data output bits (see figure 10). To decode, the reverse operation is applied; that is, an exclusive-OR operation is applied between the LSB and all other bits (see figure 11). The LSB, OF and CLKOUT output are not affected. The output randomizer function is active when the RAND pin is high.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For example, if the converter is driving a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply. OV_{DD} can be powered with any logic voltage up to the 3.6V. OGND can be powered with any voltage from ground up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Internal Dither

The LTM9001 is a 16-bit receiver subsystem with a very linear transfer function; however, at low input levels even slight imperfections in the transfer function will result in unwanted tones. Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input location on the ADC transfer curve, resulting in improved SFDR for low signal levels.

APPLICATIONS INFORMATION

As shown in Figure 12, the output of the sample-and-hold amplifier is summed with the output of a dither DAC. The dither DAC is driven by a long sequence pseudo-random number generator; the random number fed to the dither DAC is also subtracted from the ADC result. If the dither DAC is precisely calibrated to the ADC, very little of the dither signal will be seen at the output. The dither signal that does leak through will appear as white noise. The dither DAC will cause a small elevation in the noise floor of the ADC, as compared to the noise floor with dither off.

For best noise performance with the dither signal on, the driving impedance connected across pins IN^+/IN^- should closely match that of the module (see Table 1). A source impedance that is resistive and matches that of the module within 10% will give the best results.

Supply Sequencing

The V_{CC} pin provides the supply to the amplifier and the V_{DD} pin provides the supply to the ADC. The amplifier and the ADC are separate integrated circuits within the LTM9001; however, there are no supply sequencing considerations beyond standard practice. It is recommended that the amplifier and ADC both use the same low noise, 3.3V supply, but the amplifier may be operated from a lower voltage level if desired. Both devices can operate from the same 3.3V linear regulator but place a ferrite bead between the V_{CC} and V_{DD} pins. Separate linear regulators can be used without additional supply sequencing circuitry if they have common input supplies.

Grounding and Bypassing

The LTM9001 requires a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTM9001 has been optimized for a flow-through layout so that the interaction between inputs and digital outputs is minimized. A continuous row of ground pads facilitate a layout that ensures that digital and analog signal lines are separated as much as possible.

The LTM9001 is internally bypassed with the amplifier (V_{CC}) and ADC (V_{DD}) supplies returning to a common ground (GND). The digital output supply ($0V_{DD}$) is returned to OGND. Additional bypass capacitance is optional and may be required if power supply noise is significant.

The differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

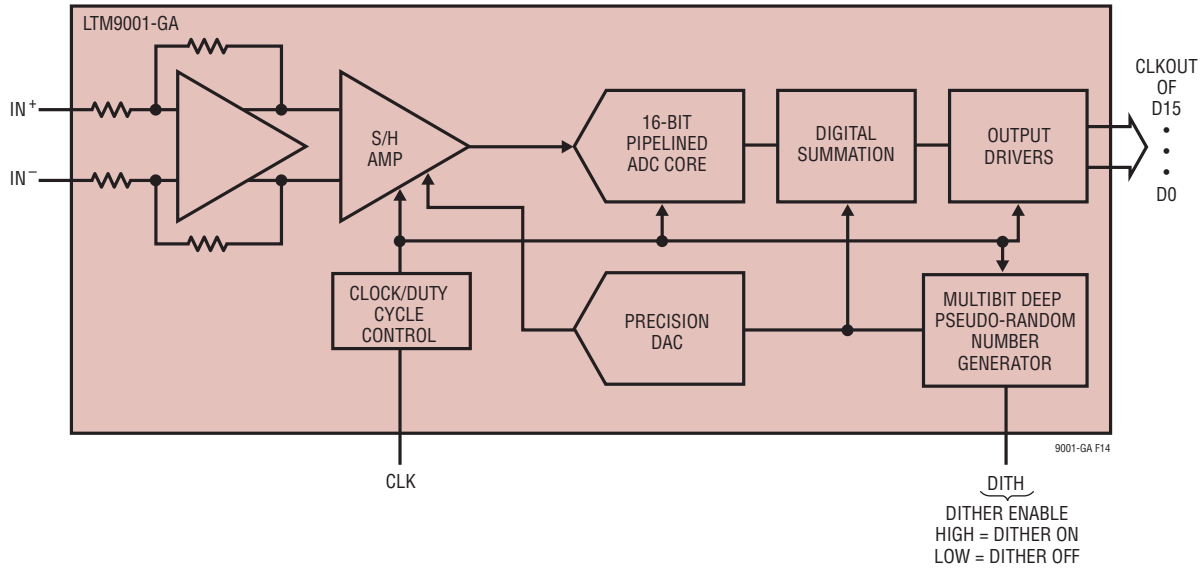


Figure 12. Functional Equivalent Block Diagram of Internal Dither Circuit

APPLICATIONS INFORMATION

Heat Transfer

Most of the heat generated by the LTM9001 is transferred through the bottom-side ground pads. For good electrical and thermal performance, it is critical that all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

Recommended Layout

The high integration of the LTM9001 makes the PC board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary, see Figures 13 to 16.

- Use large PCB copper areas for ground. This helps to dissipate heat in the package through the board and also helps to shield sensitive on-board analog signals. Common ground (GND) and output ground (OGND) are electrically isolated on the LTM9001, but can be connected on the PCB underneath the part to provide a common return path.
- Use multiple ground vias. Using as many vias as possible helps to improve the thermal performance of the board and creates necessary barriers separating analog and digital traces on the board at high frequencies.
- Separate analog and digital traces as much as possible, using vias to create high frequency barriers. This will reduce digital feedback that can reduce the signal-to-noise ratio (SNR) and dynamic range of the LTM9001.

The quality of the paste print is an important factor in producing high yield assemblies. It is recommended to use a type 3 or 4 printing no-clean solder paste. The solder stencil design should follow the guidelines outlined in Application Note 100. The µModule LGA Packaging Care and Assembly Instructions is available at http://www.linear.com/designtools/packaging/uModule_Instructions.

The LTM9001 employs gold-finished pads for use with Pb-based or tin-based solder paste. It is inherently Pb-free and complies with the JEDEC (e4) standard. The materials declaration is available online at http://www.linear.com/designtools/leadfree/mat_dec.jsp.

APPLICATIONS INFORMATION

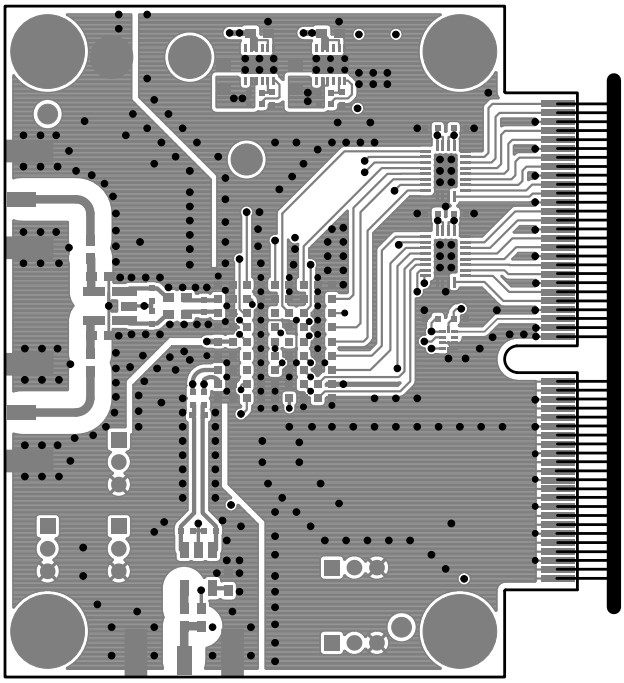


Figure 13. Layer 1

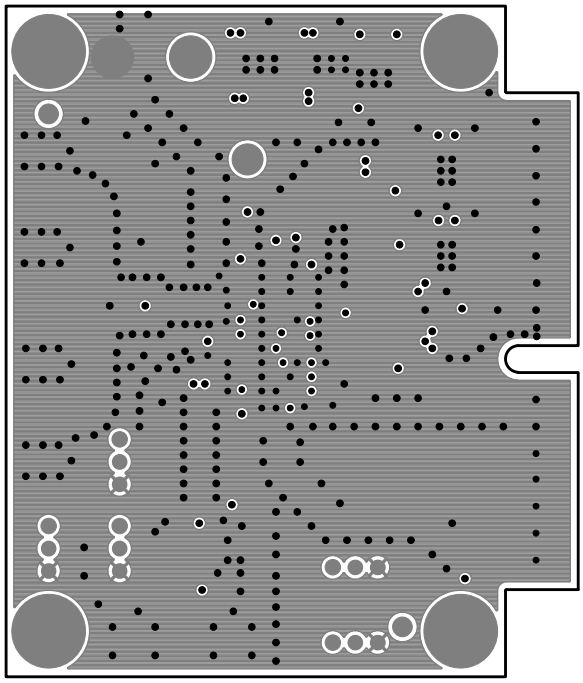


Figure 14. Layer 2

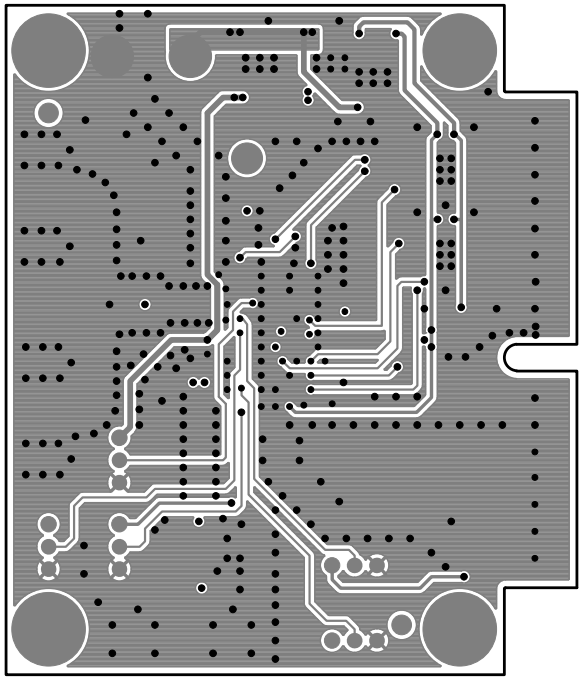


Figure 15. Layer 3

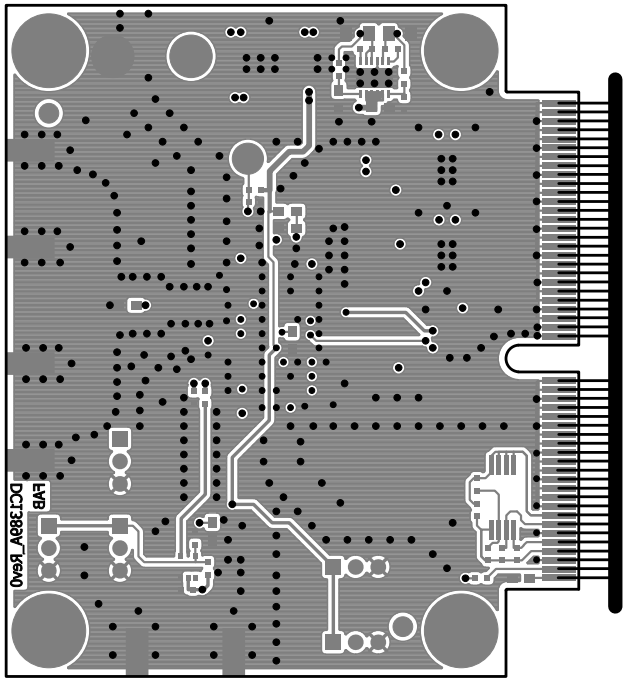
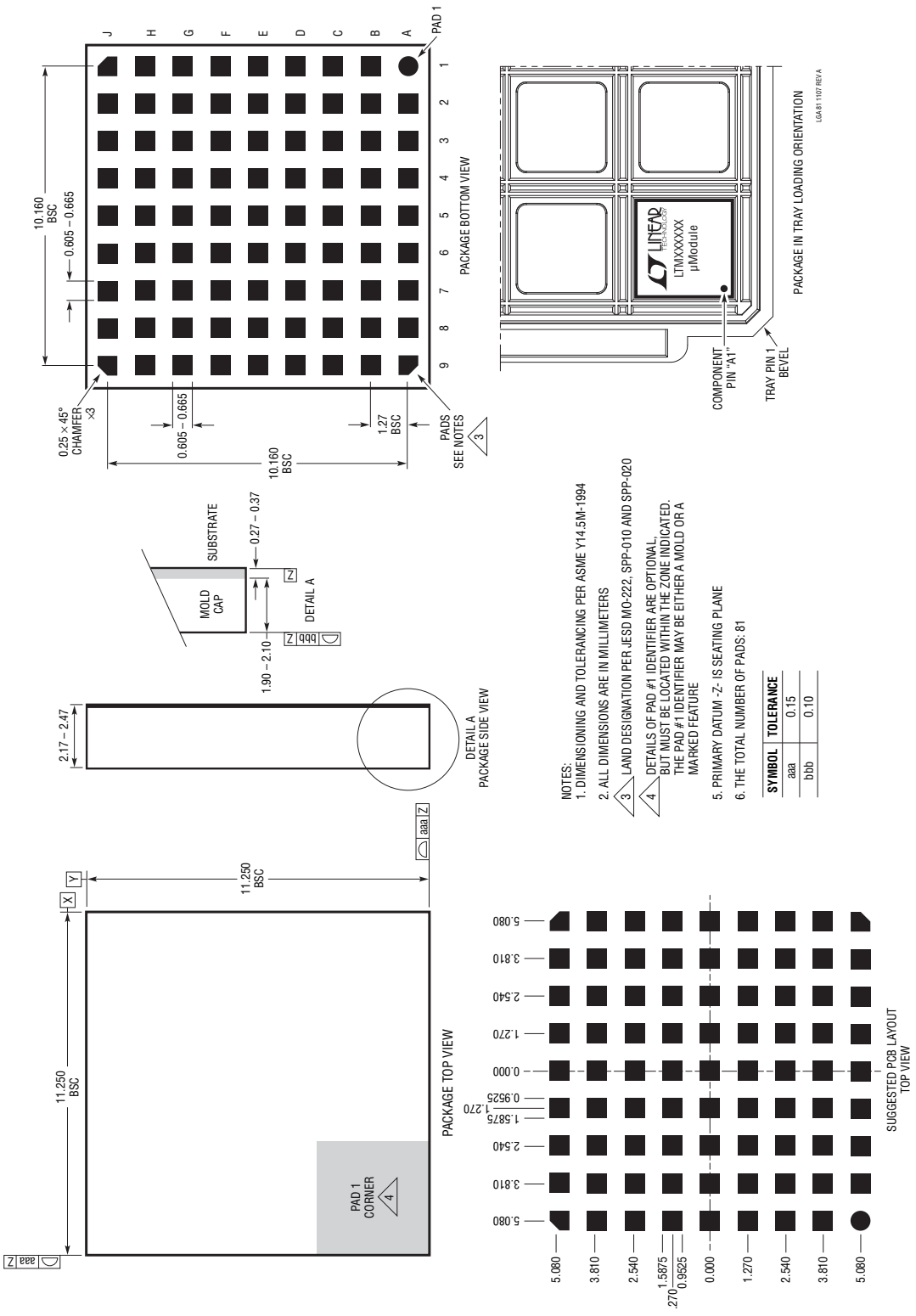


Figure 16. Layer 4

PACKAGE DESCRIPTION

LGA Package
81-Lead (11.25mm × 11.25mm × 2.32mm)
(Reference LTC DWG # 05-08-1809 Rev A)

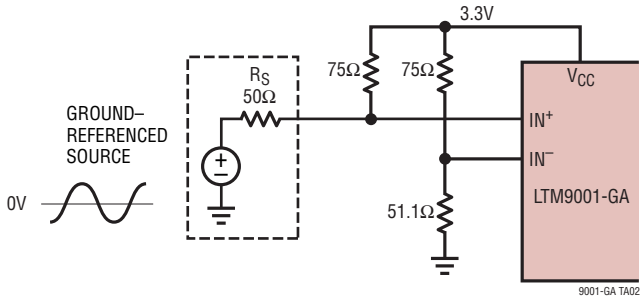


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010 AND SPP-020
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR A MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 81

SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10

TYPICAL APPLICATION

LTM9001 with Ground-Referenced Single-Ended Input



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2202	16-Bit, 10Msps ADC	140mW, 81.6dB SNR, 100dB SFDR
LTC2203	16-Bit, 25Msps ADC	220mW, 81.6dB SNR, 100dB SFDR
LTC2204	16-Bit, 40Msps ADC	480mW, 79.1dB SNR, 100dB SFDR
LTC2205	16-Bit, 65Msps ADC	610mW, 79dB SNR, 100dB SFDR
LTC2206	16-Bit, 80Msps ADC	725mW, 77.9dB SNR, 100dB SFDR
LTC2207	16-Bit, 105Msps ADC	900mW, 77.9dB SNR, 100dB SFDR
LTC2208	16-Bit, 130Msps ADC	1250mW, 77.7dB SNR, 100dB SFDR
LTC2209	16-Bit, 160Msps ADC	1450mW, 77.1dB SNR, 100dB SFDR
LTC6400-8/LTC6400-14/ LTC6400-20/LTC6400-26	Low Noise, Low Distortion Differential Amplifier for 300MHz IF, Fixed Gain of 8dB, 14dB, 20dB or 26dB	3V, 90mA, 39.5dBm OIP3 at 300MHz, 6dB NF
LTC6401-8/LTC6401-14/ LTC6401-20/LTC6401-26	Low Noise, Low Distortion Differential Amplifier for 140MHz IF, Fixed Gain of 8dB, 14dB, 20dB or 26dB	3V, 45mA, 45.5dBm OIP3 at 140MHz, 6dB NF

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0809 • PRINTED IN USA