ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages
- PV_{CC} to GND ..... –0.3V to 6V
- V_{CC} to GND ..... –0.3V to 6V
- V_L to GND ..... –0.3V to 6V

Isolated Supply Voltages
- V_{IN} to GND2 ..... –0.3V to 45V
- V_{L2} to GND2 ..... –0.3V to 6V

Logic Signals
- DI1, DI2, DI3, DO1, $\overline{DO1E}$, DO2P, DO3, ON, SCL, ST1, ST2 ..... GND – 0.3V to V_L + 0.3V
- DO2N, SDA ..... GND – 0.3V to 6.3V

Isolated Signals
- AV_{L2}, I1, I2, I3, O1, $\overline{O1E}$, O2P, O3, ON2, SCL2, SDA2 ..... GND2 – 0.3V to V_{L2} + 0.3V
- O2N ..... GND2 – 0.3V to 6.3V

Operating Temperature Range (Note 4)
- LTM2810C ..... 0°C to 70°C
- LTM2810I ..... –40°C to 85°C
- LTM2810H ..... –40°C to 125°C

Maximum Internal Operating Temperature ..... 125°C

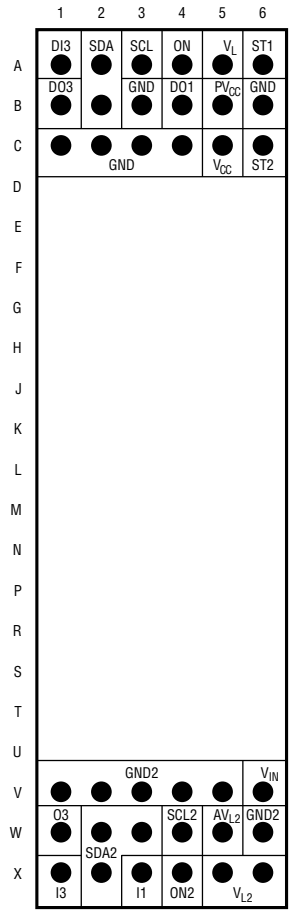
Storage Temperature Range ..... –55°C to 125°C

Peak Body Reflow Temperature ..... 260°C

PIN CONFIGURATION

LTM2810-I

TOP VIEW

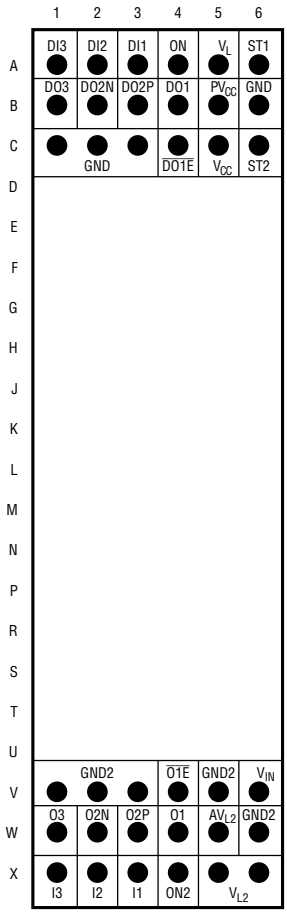


BGA PACKAGE
36-PIN (22mm × 6.25mm × 2.06mm)

T_{JMAX} = 125°C, θ_{JA} = 49.6°C/W, $\theta_{JCBOTOM}$ = 34°C/W,
θ_{JCTOP} = 26°C/W, θ_{JB} = 33.7°C/W
θ VALUES DETERMINED PER JESD51-9, WEIGHT = 0.5g

LTM2810-S

TOP VIEW



BGA PACKAGE
36-PIN (22mm × 6.25mm × 2.06mm)

T_{JMAX} = 125°C, θ_{JA} = 49.6°C/W, $\theta_{JCBOTOM}$ = 34°C/W,
θ_{JCTOP} = 26°C/W, θ_{JB} = 33.7°C/W
θ VALUES DETERMINED PER JESD51-9, WEIGHT = 0.5g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM2810CY-I#PBF	LTM2810CY-I#PBF	LTM2810Y-I	36-Lead (22mm × 6.25mm × 2.06mm) BGA	0°C to 70°C
LTM2810IY-I#PBF	LTM2810IY-I#PBF	LTM2810Y-I	36-Lead (22mm × 6.25mm × 2.06mm) BGA	–40°C to 85°C
LTM2810HY-I#PBF	LTM2810HY-I#PBF	LTM2810Y-I	36-Lead (22mm × 6.25mm × 2.06mm) BGA	–40°C to 125°C
LTM2810CY-S#PBF	LTM2810CY-S#PBF	LTM2810Y-S	36-Lead (22mm × 6.25mm × 2.06mm) BGA	0°C to 70°C
LTM2810IY-S#PBF	LTM2810IY-S#PBF	LTM2810Y-S	36-Lead (22mm × 6.25mm × 2.06mm) BGA	–40°C to 85°C
LTM2810HY-S#PBF	LTM2810HY-S#PBF	LTM2810Y-S	36-Lead (22mm × 6.25mm × 2.06mm) BGA	–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. PV_{CC} = V_{CC} = 5V, V_L = V_{L2} = 3.3V, V_{IN} = GND = GND2 = 0V, ON = V_L, and ON2 = V_{L2} unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supplies							
	Operating Voltage Range	V_{CC}, PV_{CC}, V_L (LTM2810-I), V_{L2}	●	3.0		5.5	V
		V_L (LTM2810-S)	●	1.62		5.5	V
		V_{IN}	●	3.6		38	V
V_{L2}	Output Variation (Note 7)	V_{L2} + 1V ≤ V_{IN} ≤ 38V, I_{LOAD} = 0 to 100mA	●	–0.2		0.2	V
AV_{L2}	Adjust Pin Voltage (Note 7)	V_{L2} + 1V ≤ V_{IN} ≤ 38V, I_{LOAD} = 0 to 100mA	●	580	600	620	mV
	Supply Current	I_{CC}, PI_{CC}, I_L, ON = ON2 = 0V	●		0	10	µA
		IV_{IN}, V_{IN} = 6V, ON2 = 0V	●		40	80	µA
		I_{CC}, PI_{CC}	●		3.2	5	mA
		IV_{IN}, V_{IN} = 5V, V_{L2} Adjusted to 3V	●		3.6	6	mA
		I_L (LTM2810-S)	●			10	µA
		I_L (LTM2810-I)				150	µA
	V_{L2} Current Limit	V_{IN} = 7V, V_{L2} = 0V			200		mA
		V_{IN} = $V_{L2(NOMINAL)}$ + 1V, ΔV_{L2} = –5%	●	110			mA
	ST1, ST2 Output Current	(Note 2)			400		mA
Logic – DI1, DI2, DI3, DO1, $\overline{DO1E}$, DO2N, DO2P, DO3, I1, I2, I3, O1, $\overline{O1E}$, O2N, O2P, O3, ON, ON2 (V_L = V_L or V_{L2})							
V_{ITH}	Input Threshold Voltage	1.62V ≤ V_L < 2.35	●	0.25 • V_L		0.75 • V_L	V
		2.35V ≤ V_L	●	0.33 • V_L		0.67 • V_L	V
I_{IN}	Input Current		●		0	±5	µA
V_O	Output Voltage	I_{LOAD} = 1mA, 1.62V ≤ V_L < 3V	●	0.4		V_L – 0.4	V
		I_{LOAD} = 4mA, 3V ≤ V_L	●	0.4		V_L – 0.4	V
		DO1 (LTM2810-I), I_{LOAD} = 2mA, 3V ≤ V_L	●	0.4		V_L – 0.4	V
		DO2N, I_{LOAD} = 1mA, 1.62V ≤ V_L < 3V	●	0.4			V
		DO2N, O2N, I_{LOAD} = 4mA, 3V ≤ V_L	●	0.4			V
		DO2P, I_{LOAD} = 1mA, 1.62V ≤ V_L < 3V	●			V_L – 0.4	V
		DO2P, O2P, I_{LOAD} = 4mA, 3V ≤ V_L	●			V_L – 0.4	V
	Output High Resistance	(Note 3)			40		Ω
	Output Low Resistance	(Note 3)			40		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. PV_{CC} = V_{CC} = 5V, V_L = V_{L2} = 3.3V, V_{IN} = GND = GND2 = 0V, ON = V_L, and ON2 = V_{L2} unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I^2C – SCL, SCL2, SDA, SDA2 (LTM2810-I) (V_L = V_L or V_{L2})							
V_{ITH}	Input Threshold Voltage	3V ≤ V_L ≤ 5.5V	●	0.3 • V_L		0.7 • V_L	V
V_{HYS}	Input Hysteresis	3V ≤ V_L ≤ 5.5V			0.05 • V_L		V
I_{IN}	Input Current		●		0	±5	µA
V_O	Output Voltage	SCL2, I_{LOAD} = 2mA, 3V ≤ V_L ≤ 5.5V	●	0.4		V_L – 0.4	V
V_{OL}	Output Low Voltage	SDA, I_{LOAD} = 3mA SDA2 = No Load, SDA = 0V, 4.5V ≤ V_L < 5.5V SDA2 = No Load, SDA = 0V, 3V ≤ V_L < 4.5V	● ● ●		 0.3	0.4 0.45 0.55	V V V
	SDA, SDA2 Slew Rate		●	1			V/µs
I_{SC}	Short-Circuit Current	SDA2 = 0, SDA = V_L 0V ≤ SCL2 ≤ V_L SDA = 0, SDA2 = V_L SDA = V_L, SDA2 = 0	●		 ±30 6 –1.8	100	mA mA mA mA
ESD (HBM) (Note 2)							
	Isolation Boundary	(V_{IN}, V_{L2}, GND2) to (PV_{CC}, V_{CC}, V_L, GND) in Any Combination			±25		kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. PV_{CC} = V_{CC} = 5V, V_L = V_{L2} = 3.3V, V_{IN} = GND = GND2 = 0V, ON = V_L, and ON2 = V_{L2} unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Driver – ST1, ST2							
	Drive Frequency				2		MHz
	Duty Cycle			49	50	51	%
Power Supply Generator							
	V_{L2} Supply Start-Up Time	V_{IN} ↑ to V_{L2} > 4.75V			50		ms
Logic Timing							
	Maximum Data Rate	Input → Output, C_L = 15pF (Note 3) Bidirectional SPI Communication Unidirectional SPI Communication	● ● ●	10 4 8			MHz MHz MHz
t_{PHL}, t_{PLH}	Propagation Delay	Input → Output, C_L = 15pF (Figure 1)	●	30	45	100	ns
t_{PZH}, t_{PZL}	DO1, O1 Enable Time (Figure 2)	$\overline{xO1E}$ = ↓ to xO1 High, R_{PD} = 1kΩ, xI1 = High	●			50	ns
	ONx Enable Time (Figure 4)	ONx = ↑ to xOx High, R_{PD} = 1kΩ, xIx = High	●			60	µs
t_{PHZ}, t_{PLZ}	DO1, O1 Disable Time (Figure 2)	$\overline{xO1E}$ = ↑ to xO1 Low, R_{PD} = 1kΩ, xI1 = High	●			50	ns
	ONx Disable Time (Figure 4)	ONx = ↓ to xOx Low, R_{PD} = 1kΩ, xIx = High	●			100	ns
I^2C Timing							
	Maximum Data Rate	(Note 3)	●	400			kHz
t_{PHL}, t_{PLH}	Propagation Delay (Figure 3)	SCL → SCL2 SDA → SDA2 SDA2 → SDA, R_{PU} = 1kΩ	● ● ●		150 150 300	250 300 500	ns ns ns
t_R	Rise Time (30% to 70%) (Figure 3)	SDA2, C_L = 200pF SDA, R_{PU} = 1kΩ, C_L = 200pF SCL2, C_L = 200pF	● ● ●	40 40		350 350 250	ns ns ns
t_F	Fall Time (70% to 30%) (Figure 3)	SDA2, C_L = 200pF SDA, R_{PU} = 1kΩ, C_L = 200pF SCL2, C_L = 200pF	● ● ●	40 40		250 250 250	ns ns ns

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. PV_{CC} = V_{CC} = 5V, V_L = V_{L2} = 3.3V, V_{IN} = GND = GND2 = 0V, ON = V_L, and ON2 = V_{L2} unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PZH}, t_{PZL}	ONx Enable Time	ON = ↑ to SDA Low, R_{PU} = 1kΩ, SDA2 = 0V ON2 = ↑ to (SCL2, SDA2) Low, (SCL, SDA) = 0V	● ●			60 60	µs µs
t_{PHZ}, t_{PLZ}	ONx Disable Time	ON = ↓ to SDA High, R_{PU} = 1kΩ, SDA2 = 0V ON2 = ↓ to SCL2 High, SCL = 0V ON2 = ↓ to SDA2 High, SDA = 0V	● ● ●			80 80 225	ns ns ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns

ISOLATION CHARACTERISTICS

T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage	1 Minute, Derived from 1 Second Test 1 Second (Notes 5, 6)	7500 9000			V_{RMS} V_{RMS}
	Common Mode Transient Immunity	PV_{CC} = V_{CC} = V_L = ON = 5V, V_{L2} = ON2 = 5V V_{CM} = 1kV, Δt = 20ns (Note 2)	50	75		kV/µs
V_{IORM}	Maximum Continuous Working Voltage	(Notes 2, 5)	1600 1000			V_{DC} V_{RMS}
	Partial Discharge	V_{PD} = 2650V_{PEAK} (Note 5)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2), Material Group I	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 2)		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.2		mm
	Input to Output Resistance	(Notes 2, 5)	1	5		TΩ
	Input to Output Capacitance	(Notes 2, 5)		2		pF
	Creepage Distance	(Note 2)		16.2		mm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not subject to production test.

Note 3: Guaranteed by other measured parameters and is not tested directly.

Note 4: This µModule isolator includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

Note 5: Device is considered a 2-terminal device. Pin group A1 through C6 shorted together and pin group V1 through X6 shorted together.

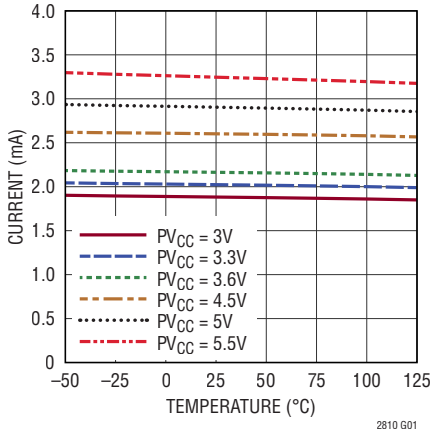
Note 6: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

Note 7: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at the maximum input-to-output voltage differential. Limit the input-to-output voltage differential if operating at maximum output current. Current limit foldback will limit the maximum output current as a function of input-to-output voltage.

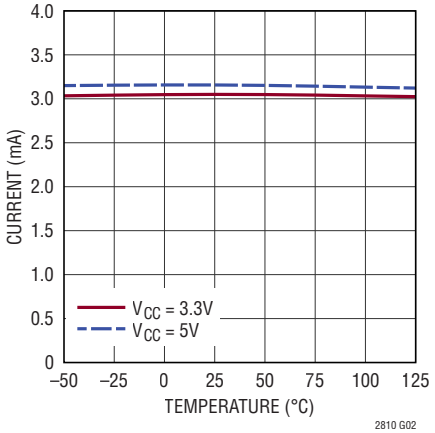
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, PV_{CC} = V_{CC} = 5V, V_L = V_{L2} = 3.3V, GND = GND2 = 0V, ON = V_L, and ON2 = V_{L2}, unless otherwise noted.

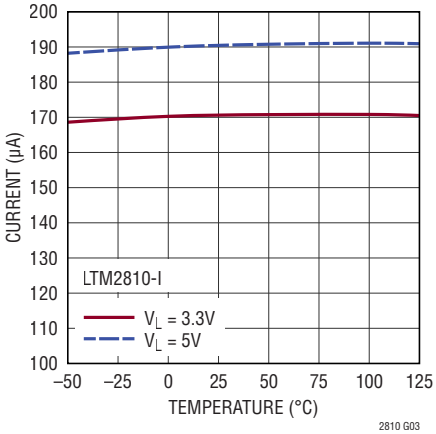
PV_{CC} Supply Current vs Temperature



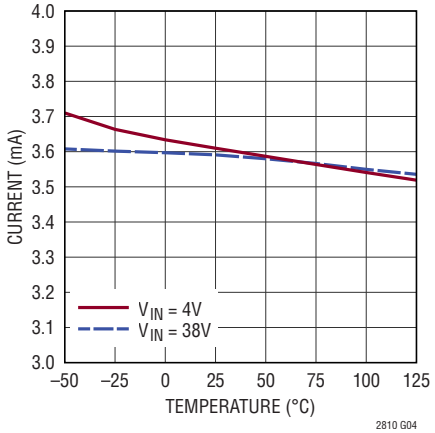
V_{CC} Supply Current vs Temperature



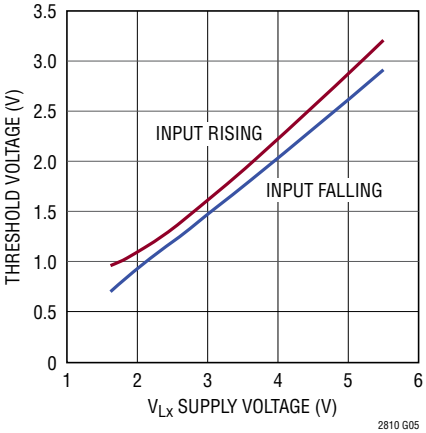
V_L Supply Current vs Temperature



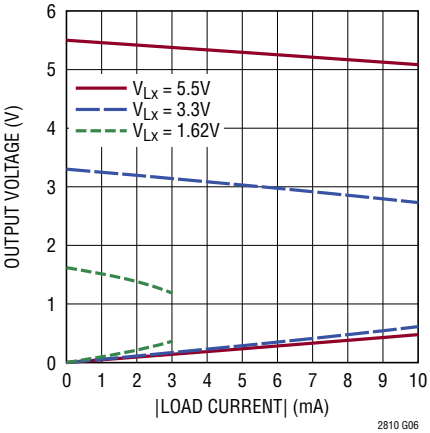
V_{IN} Supply Current vs Temperature



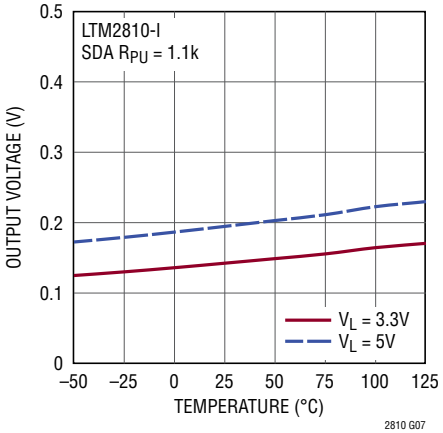
Logic Input Threshold vs V_L Supply Voltage



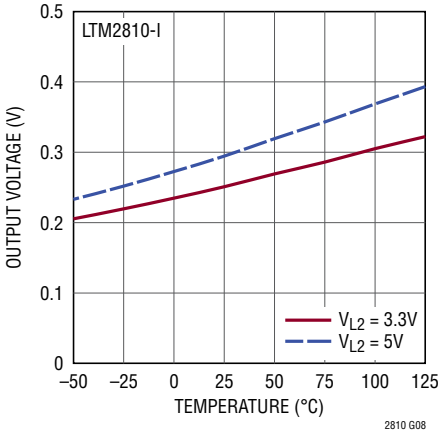
Logic Output Voltage vs Load Current



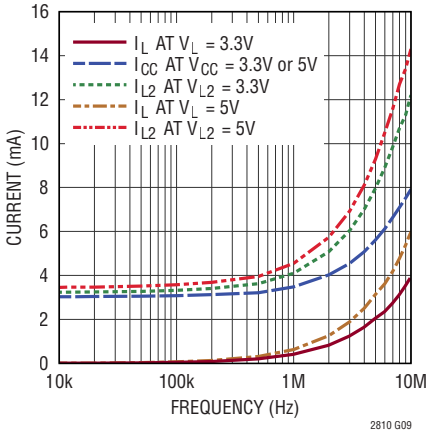
SDA Low Level Output Voltage vs Temperature



SDA2 Low Level Output Voltage vs Temperature



Supply Current vs Data Rate, All Channels

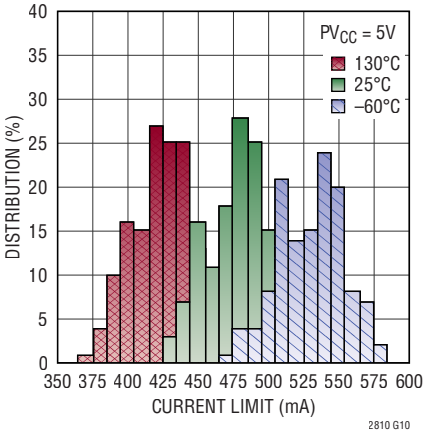


Rev 0

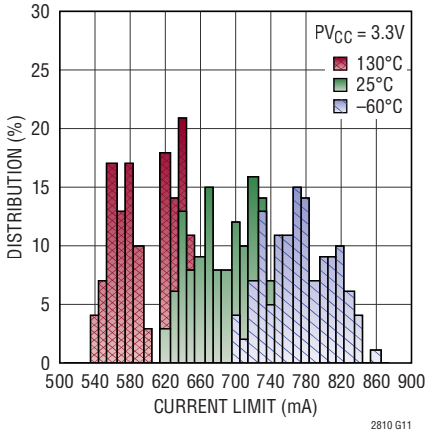
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, PV_{CC} = V_{CC} = 5V, V_L = V_{L2} = 3.3V, GND = GND2 = 0V, ON = V_L, and ON2 = V_{L2}, unless otherwise noted.

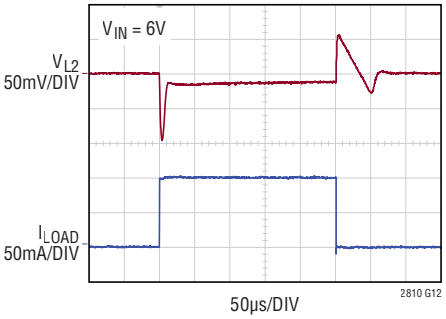
ST1 and ST2 Current Limit vs Temperature Histogram



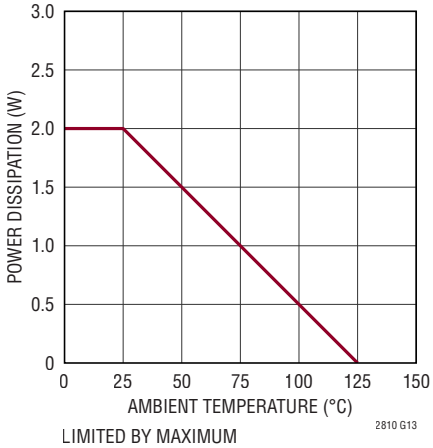
ST1 and ST2 Current Limit vs Temperature Histogram



V_{L2} Transient Response



Thermal Derating



PIN FUNCTIONS

LTM2810-S, Logic Side

DI3 (A1): Digital Input, Referenced to V_L and GND. Logic input connected to O3 through the isolation barrier. The logic state on DI3 translates to the same logic state on O3. Connect to GND or V_L if not used.

DI2 (A2): Digital Input, Referenced to V_L and GND. Logic input connected to O2N and O2P through the isolation barrier. The logic state on DI2 translates to the same logic state on O2N and O2P. Connect to GND or V_L if not used.

DI1 (A3): Digital Input, Referenced to V_L and GND. Logic input connected to O1 through the isolation barrier. The logic state on DI1 translates to the same logic state on O1. Connect to GND or V_L if not used.

ON (A4): Enable, Referenced to V_L and GND. Enables data communication through the isolation barrier. If ON is high the part is enabled and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state. Connect to V_L if not driven.

V_L (A5): Logic Supply. Interface supply voltage for pins DI1, DI2, DI3, DO1, DO2P, DO3, $\overline{DO1E}$, and ON. Operating voltage is 1.62V to 5.5V. Internally bypassed with 1µF.

ST1, ST2 (A6, C6): Bridge Driver Outputs, Referenced to PV_{CC} and GND. Each output runs at 50% duty cycle, ST1 is 180 degrees out of phase with ST2. Operating frequency is 2MHz. Bridge driver is enabled when PV_{CC} is between 3V to 5.5V and ON is high.

DO3 (B1): Digital Output, Referenced to V_L and GND. Logic output connected to I3 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO2N (B2): Open Drain Pull-Down Output to GND. Logic output connected to I2 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO2P (B3): Open Drain Pull-Up Output to V_L. Logic output connected to I2 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO1 (B4): Digital Output, Referenced to V_L and GND. Logic output connected to I1 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

PV_{CC} (B5): Bridge Driver Supply Voltage. Operating voltage is 3V to 5.5V, connect to GND to disable bridge driver. Internally bypassed with 2.2µF.

$\overline{DO1E}$ (C4): Digital Output Enable, Referenced to V_L and GND. A logic high on $\overline{DO1E}$ places the logic side DO1 pin in a high impedance state, a logic low enables the output. Connect to GND or V_L if not used.

V_{CC} (C5): Supply Voltage. Operating voltage is 3V to 5.5V. Internally bypassed with 1µF.

GND (B6, C1 to C3): Circuit Ground.

LTM2810-S, Isolated Side

$\overline{O1E}$ (V4): Digital Output Enable, Referenced to V_{L2} and GND2. A logic high on $\overline{O1E}$ places the isolated side O1 pin in a high impedance state, a logic low enables the output. Connect to GND2 or V_{L2} if not used.

V_{IN} (V6): Internal LDO Input Voltage. Operating voltage is 3.6V to 38V. Internally bypassed with 0.1µF.

O3 (W1): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to DI3 through the isolation barrier. Under the condition of an isolation communication failure O3 defaults to a high state.

O2N (W2): Open Drain Pull-Down Output to GND2. Logic output connected to DI2 through the isolation barrier. Under the condition of an isolation communication failure O2N defaults to a low state.

O2P (W3): Open Drain Pull-Up Output to V_{L2}. Logic output connected to DI2 through the isolation barrier. Under the condition of an isolation communication failure O2P defaults to a low state.

O1 (W4): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to DI1 through the isolation barrier. Under the condition of an isolation communication failure O1 defaults to a low state.

AV_{L2} (W5): V_{L2} LDO Adjust Pin.

PIN FUNCTIONS

I3 (X1): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO3 through the isolation barrier. The logic state on I3 translates to the same logic state on DO3. Connect to GND2 or V_{L2} if not used.

I2 (X2): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO2N and DO2P through the isolation barrier. The logic state on I2 translates to the same logic state on DO2N and DO2P. Connect to GND2 or V_{L2} if not used.

I1 (X3): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO1 through the isolation barrier. The logic state on I1 translates to the same logic state on DO1. Connect to GND2 or V_{L2} if not used.

ON2 (X4): Enable, Referenced to V_{L2} and GND2. Enables data communication through the isolation barrier. If ON2 is high the part is enabled and communications are functional to the logic side. If ON2 is low the isolated side is held in reset, O1, O2N and O2P are in a low state, and O3 is in a high state. Connect to V_{L2} if not driven.

V_{L2} (X5, X6): Logic Supply, Referred to GND2. Interface supply voltage for pins O1, O2P, O3, I1, I2, I3, $\overline{O1E}$, and ON2. Operating voltage is 3V to 5.5V. Internally bypassed with 6.6µF.

GND2 (V1 to V3, V5, W6): Isolated Ground.

LTM2810-I, Logic Side

DI3 (A1): Digital Input, Referenced to V_L and GND. Logic input connected to O3 through the isolation barrier. The logic state on DI3 translates to the same logic state on O3. Connect to GND or V_L if not used.

SDA (A2, B2): Serial I^2C Data Pins, Referenced to V_L and GND. Bidirectional logic pins connected to isolated side SDA2 pins through the isolation barrier. Under the condition of an isolation communication failure pins are in a high impedance state. Pull up to V_L if not used.

SCL (A3): Serial I^2C Clock Input, Referenced to V_L and GND. Logic input connected to isolated side SCL2 pin through the isolation barrier. Clock is unidirectional from logic to isolated side. Pull up to V_L if not used.

ON (A4): Enable, Referenced to V_L and GND. Enables data communication through the isolation barrier. If ON is high the part is enabled and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state. Connect to V_L if not driven.

V_L (A5): Logic Supply. Interface supply voltage for pins SCL, DI3, DO1, DO3, and ON. Operating voltage is 3V to 5.5V. Internally bypassed with 1µF.

ST1, ST2 (A6, C6): Bridge Driver Outputs, Referenced to PV_{CC} and GND. Each output runs at 50% duty cycle, ST1 is 180 degrees out of phase with ST2. Operating frequency is 2MHz. Bridge driver is enabled when PV_{CC} is between 3V to 5.5V and ON is high.

DO3 (B1): Digital Output, Referenced to V_L and GND. Logic output connected to I3 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO1 (B4): Digital Output, Referenced to V_L and GND. Logic output connected to I1 through the isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

PV_{CC} (B5): Bridge Driver Supply Voltage. Operating voltage is 3V to 5.5V, connect to GND to disable bridge driver. Internally bypassed with 2.2µF.

V_{CC} (C5): Supply Voltage. Operating voltage is 3V to 5.5V. Internally bypassed with 1µF.

GND (B3, B6, C1 to C4): Circuit Ground.

LTM2810-I, Isolated Side

V_{IN} (V6): Internal LDO Input Voltage. Operating voltage is 3.6V to 38V. Bypassed with 0.1µF.

O3 (W1): Digital Output, Referenced to V_{L2} and GND2. Logic output connected to DI3 through the isolation barrier. Under the condition of an isolation communication failure O3 defaults to a high state.

SDA2 (W2, W3, X2): Serial I^2C Data Pins, Referenced to V_{L2} and GND2. Bidirectional logic pins connected to logic side SDA pins through the isolation barrier. Output is biased high by a 1.8mA current source. Do not connect

PIN FUNCTIONS

an external pull-up device to SDA2. Under the condition of an isolation communication failure outputs default to a high state. Pins connected internally.

SCL2 (W4): Serial I^2C Clock Output, Referenced to V_{L2} and GND2. Logic output connected to logic side SCL pin through the isolation barrier. Clock is unidirectional from logic to isolated side. SCL2 has a push-pull output stage; do not connect an external pull-up device. Under the condition of an isolation communication failure this output defaults to a high state.

AV_{L2} (W5): V_{L2} LDO Adjust Pin.

I3 (X1): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO3 through the isolation barrier. The logic state on I3 translates to the same logic state on DO3. Connect to GND2 or V_{L2} if not used.

I1 (X3): Digital Input, Referenced to V_{L2} and GND2. Logic input connected to DO1 through the isolation barrier. The logic state on I1 translates to the same logic state on DO1. Connect to GND2 or V_{L2} if not used.

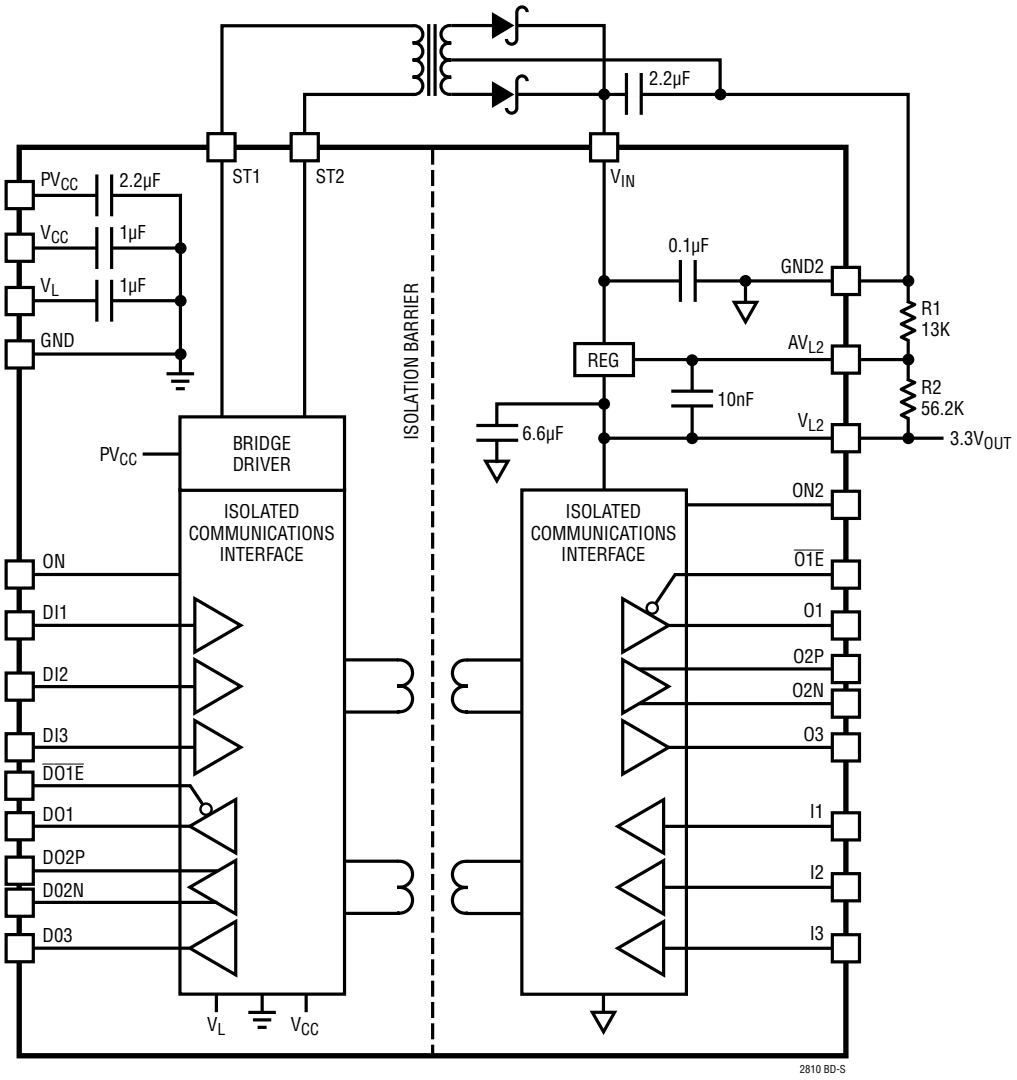
ON2 (X4): Enable, Referenced to V_{L2} and GND2. Enables data communication through the isolation barrier. If ON2 is high the part is enabled and communications are functional to the logic side. If ON2 is low the isolated side is held in reset, all digital outputs are in a high state. Connect to V_{L2} if not driven.

V_{L2} (X5, X6): Logic Supply, Referred to GND2. Interface supply voltage for pins SCL2, SDA2, I1, I3, O3, and ON2. Operating voltage is 3V to 5.5V. Internally bypassed with 6.6µF.

GND2 (W6, V1 to V5): Isolated Ground.

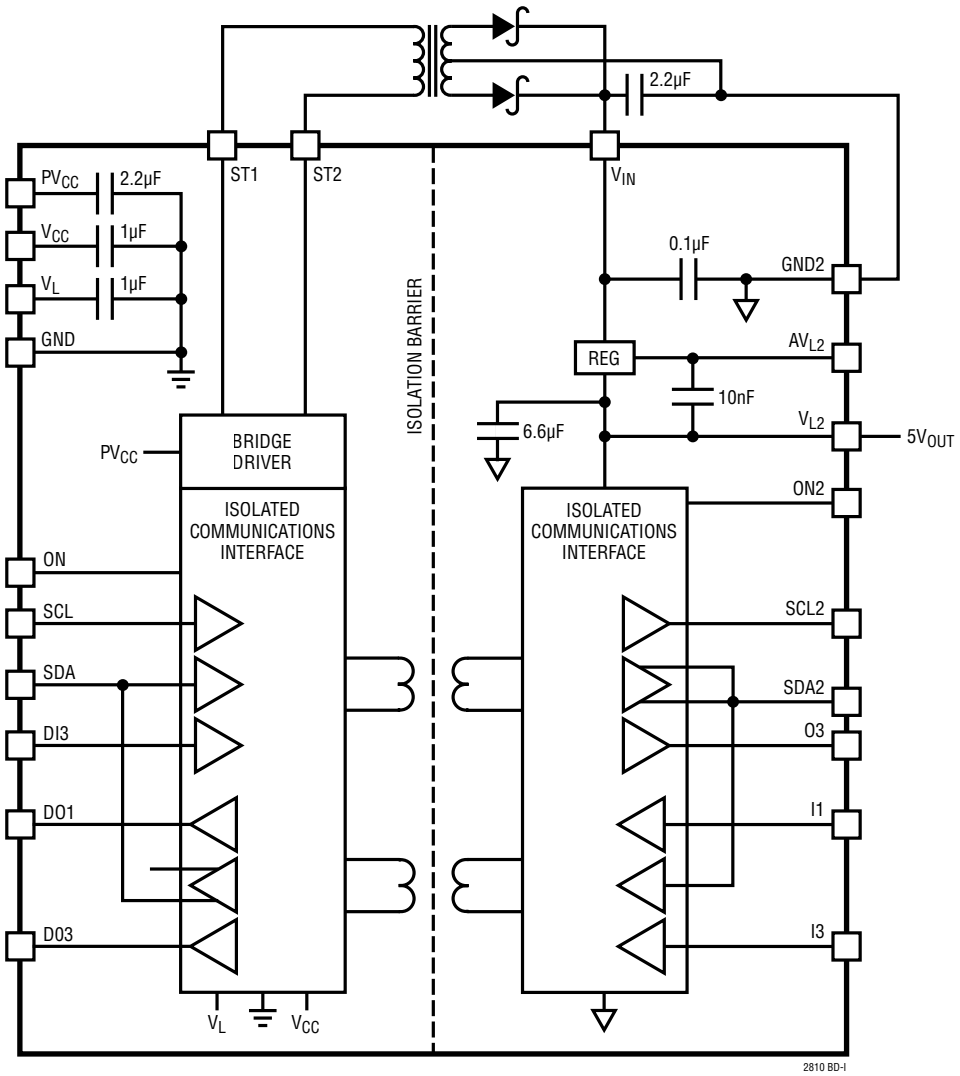
BLOCK DIAGRAM

LTM2810-S



BLOCK DIAGRAM

LTM2810-I



TEST CIRCUIT

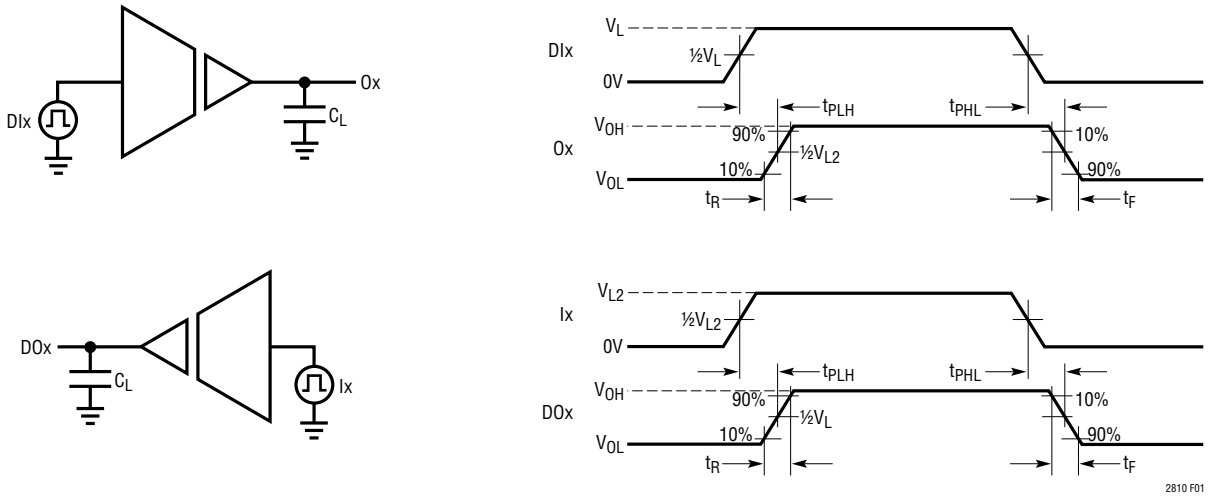


Figure 1. Logic Timing Measurements

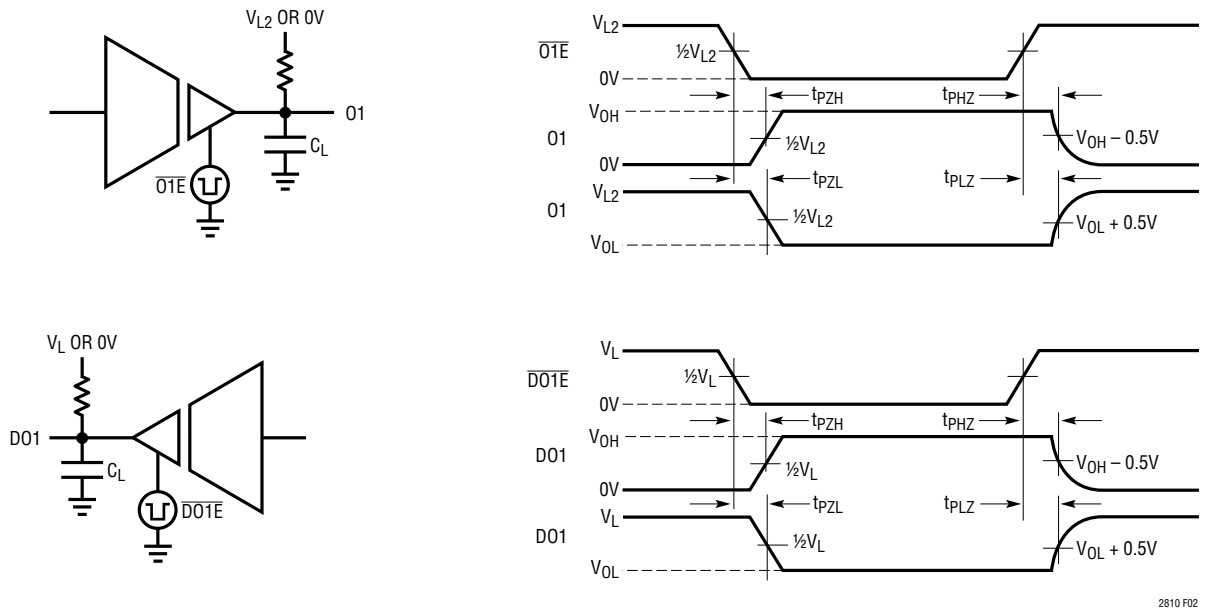


Figure 2. Logic Enable/Disable Time

TEST CIRCUIT

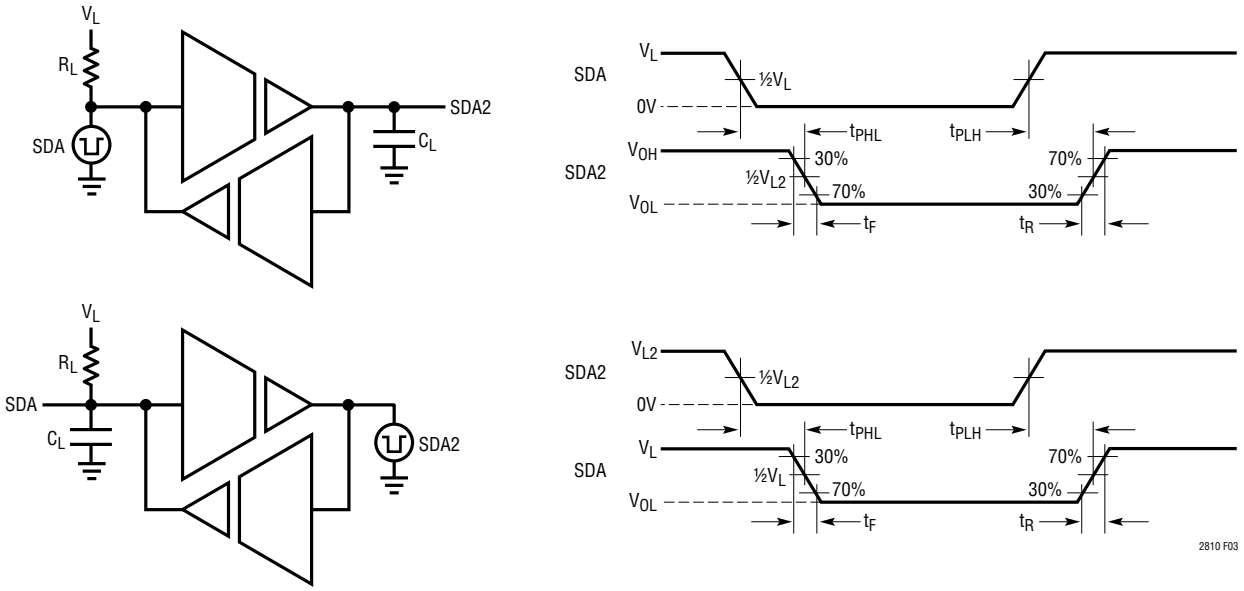


Figure 3. I²C Timing Measurements

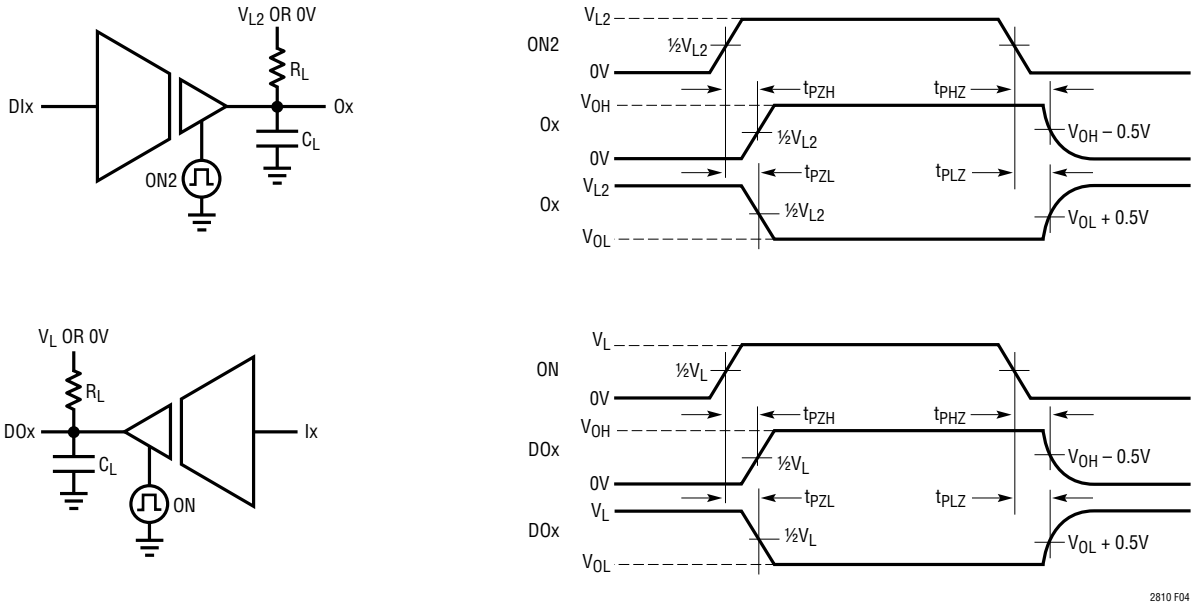


Figure 4. ONx Enable/Disable Time

APPLICATIONS INFORMATION

Overview

The LTM2810 digital µModule isolator provides a galvanically-isolated robust logic interface, complete with decoupling capacitors. The LTM2810 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2810 blocks high voltage differences and eliminates ground loops, and is extremely tolerant of common mode transients between ground planes. Error-free operation is maintained through common mode events as fast as 50kV/µs providing excellent noise isolation.

Input Supply (V_{CC})

The LTM2810 is powered by a 3V to 5.5V supply on the logic side of the isolation interface. The input supply provides power to the internal isolated communications interface and is completely independent of either the logic power supply or bridge driver supply. V_{CC} is bypassed internally with a 1µF ceramic capacitor.

Bridge Driver Supply (PV_{CC})

The integrated bridge driver is powered by a 3V to 5.5V supply on the logic side of the isolation interface. The bridge driver may be disabled by tying PV_{CC} to GND. PV_{CC} is bypassed internally with a 2.2µF ceramic capacitor.

LDO Input Supply (V_{IN})

The isolated side includes an integrated LDO powered by V_{IN}, with a nominal output voltage of 5V on V_{L2}. Input operating range is 4V to 38V. V_{IN} is bypassed internally with a 0.1µF ceramic capacitor. V_{IN} may be grounded or left unconnected if V_{L2} is driven by an external supply.

Logic Supplies (V_L, V_{L2})

Separate logic supply pins, V_L and V_{L2}, allow the LTM2810 to interface with any logic signal from 1.62V to 5.5V on the logic side of the SPI/Digital version, 3V to 5.5V for the logic and isolated sides of the I^2C version and isolated side of the SPI/Digital version, as shown in Figure 5.

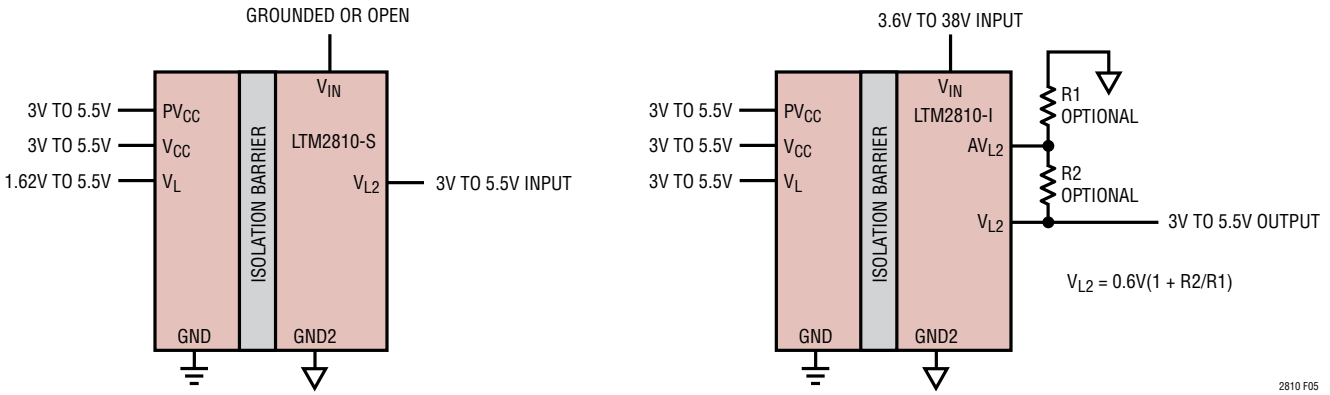


Figure 5. Supplies are Independent

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With V_{IN} driven, the V_{L2} output may be adjusted from the nominal 5V by connecting a voltage divider to the AV_{L2} pin as shown in Figure 5. Select the voltage divider ratio so that the AV_{L2} voltage is 0.6V. The value of R1 should be no greater than 13kΩ to minimize errors in the output voltage caused by the adjust pin bias current and internal voltage divider.

There is no interdependency between V_{CC}, V_L, and PV_{CC}. They may simultaneously operate at any voltage within their specified operating ranges and may sequence in any order. V_L is bypassed internally with a 1µF ceramic capacitor and V_{L2} is bypassed internally by a 6.6µF ceramic capacitor.

Hot Plugging Safely

Caution must be exercised in applications where power is plugged into the LTM2810's power supplies, V_{CC}, PV_{CC}, V_L, or V_{L2} due to the integrated ceramic decoupling capacitors. The parasitic cable inductance along with the high-Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTM2810. Refer to Application Note 88, entitled Ceramic Input Capacitors Can Cause Overvoltage Transients for a detailed discussion and mitigation of this phenomenon.

Isolation Transformer

Because of the wide voltage range for V_{IN}, there are many options for the isolation transformer and rectifier topology. The selected transformer should meet the application's isolation requirements, have a minimum volt-second rating greater than 0.5 • PV_{CC} µVS and a current rating sufficient for the LTM2810's IV_{IN} plus any application load. Different winding configurations and turns ratios allow the accommodation of different input or isolated output voltages as illustrated by Figures 14 to 18.

Channel Timing Uncertainty

Multiple channels are supported across the isolation boundary by encoding and decoding of the inputs and outputs. Up to three signals in each direction are assembled as serial packets and transferred across the isolation barrier. The time required to transfer all three bits is 100ns maximum, and sets the limit for how often a signal can change on the opposite side of the barrier. Encoding and transmission is independent for each data direction. The technique used assigns DI1(-S) or SCL(-I) on the logic side, and I1(-S or -I) on the isolated side, the highest priority such that there is no jitter on the associated output channels, only delay. This preemptive scheme will produce a certain amount of uncertainty on the other isolation channels. The resulting pulse width uncertainty on these low priority channels is typically ±6ns, but may vary up to ±44ns if the low priority channels are not encoded within the same high priority serial packet.

Serial Peripheral Interface (SPI) Bus

The LTM2810-S provides an SPI compatible isolated interface. The maximum data rate is a function of the inherent channel propagation delays, channel to channel pulse width uncertainty, and data direction requirements. Channel timing is detailed in Figures 6 through 9, Table 2, and Table 3. The SPI protocol supports four unique timing configurations defined by the clock polarity (CPOL) and clock phase (CPHA) summarized in Table 1.

Table 1. SPI Mode

CPOL	CPHA	DATA TO (CLOCK) RELATIONSHIP	
0	0	Sample (Rising)	Setup (Falling)
0	1	Setup (Rising)	Sample (Falling)
1	0	Sample (Falling)	Setup (Rising)
1	1	Setup (Falling)	Sample (Rising)

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The maximum data rate for bidirectional communication is 4MHz, based on a synchronous system, as detailed in the timing waveforms. Slightly higher data rates may be achieved by skewing the clock duty cycle and minimizing the DO1 (SDO) to DI1 (SCK) setup time, however the clock rate is still dominated by the system propagation delays. A discussion of the critical timing paths relative to Figure 6 and Figure 7 follows. For SPI communication DI1 = SCK, DI2 = SDI, DI3 = CS, DO1 = SDO, O1 = SCK2, O2N and O2P = SDI2, O3 = CS2, and I1 = SDO2.

- CS to SCK (master sample SDO, 1st SDO valid)

  $t_0 \rightarrow t_1$ ≈ 50ns, CS to CS2 propagation delay

  $t_1 \rightarrow t_1+$ Isolated slave device propagation (response time), asserts SDO2

  $t_1 \rightarrow t_3$ ≈ 50ns, SDO2 to SDO propagation delay

  $t_3 \rightarrow t_5$ Setup time for master SDO to SCK

- SDI to SCK (master data write to slave)

  $t_2 \rightarrow t_4$ ≈ 50ns, SDI to SDI2 propagation delay

  $t_5 \rightarrow t_6$ ≈ 50ns, SCK to SCK2 propagation delay

  $t_2 \rightarrow t_5$ ≥ 50ns, SDI to SCK, separate packet non-zero setup time

  $t_4 \rightarrow t_6$ ≥ 50ns, SDI2 to SCK2, separate packet non-zero setup time

- SDO to SCK (master sample SDO, subsequent SDO valid)

  t_8 Setup data transition SDI and SCK

  $t_8 \rightarrow t_{10}$ ≈ 50ns, SDI to SDI2 and SCK to SCK2 propagation delay

  t_{10} SDO2 data transition in response to SCK2

  $t_{10} \rightarrow t_{11}$ ≈ 50ns, SDO2 to SDO propagation delay

  $t_{11} \rightarrow t_{12}$ Setup time for master SDO to SCK

Maximum data rate for single direction communication, master to slave, is 8MHz, limited by the systems encoding/decoding scheme or propagation delay. Timing details for both variations of clock phase are shown in Figure 8, Figure 9, and Table 3.

Additional requirements to insure maximum data rate are:

- CS is transmitted prior to (asynchronous) or within the same (synchronous) data packet as SDI
- SDI and SCK setup data transition occur within the same data packet. Referencing Figure 6, SDI can precede SCK by up to 13ns ($t_7 \rightarrow t_8$) or lag SCK by 3ns ($t_8 \rightarrow t_9$) and not violate this requirement. Similarly in Figure 8, SDI can precede SCK by up to 13ns ($t_4 \rightarrow t_5$) or lag SCK by 3ns ($t_5 \rightarrow t_6$).

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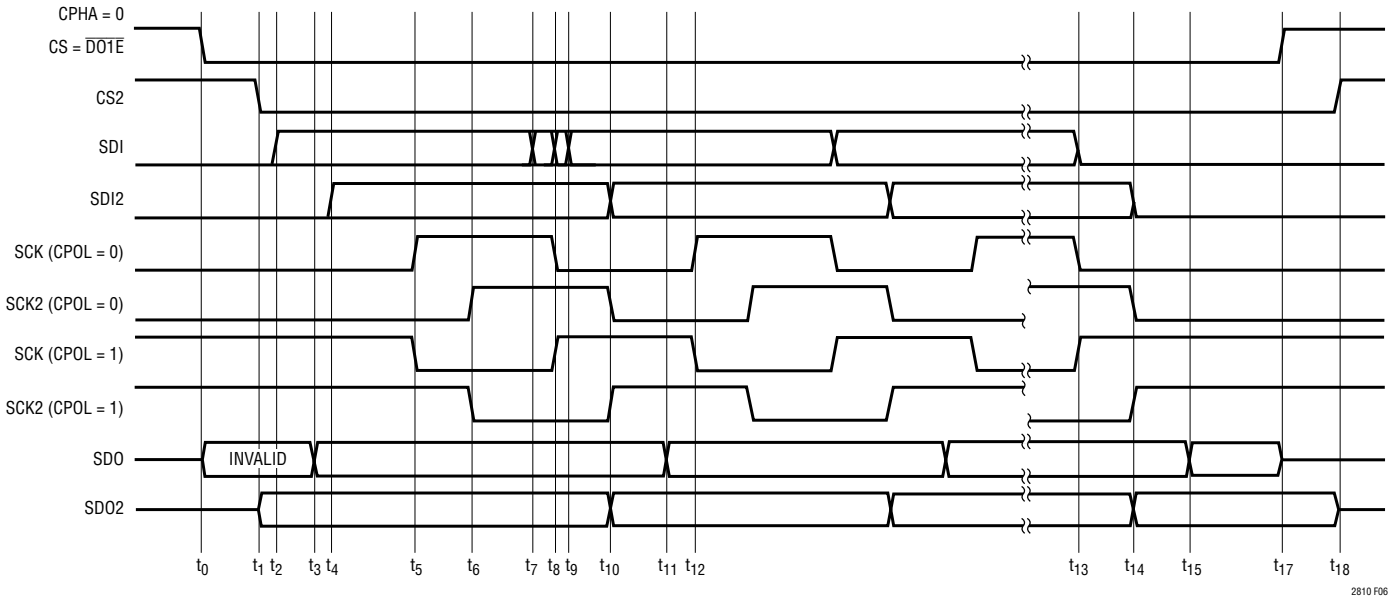

Figure 6. SPI Timing Bidirectional, CPHA = 0

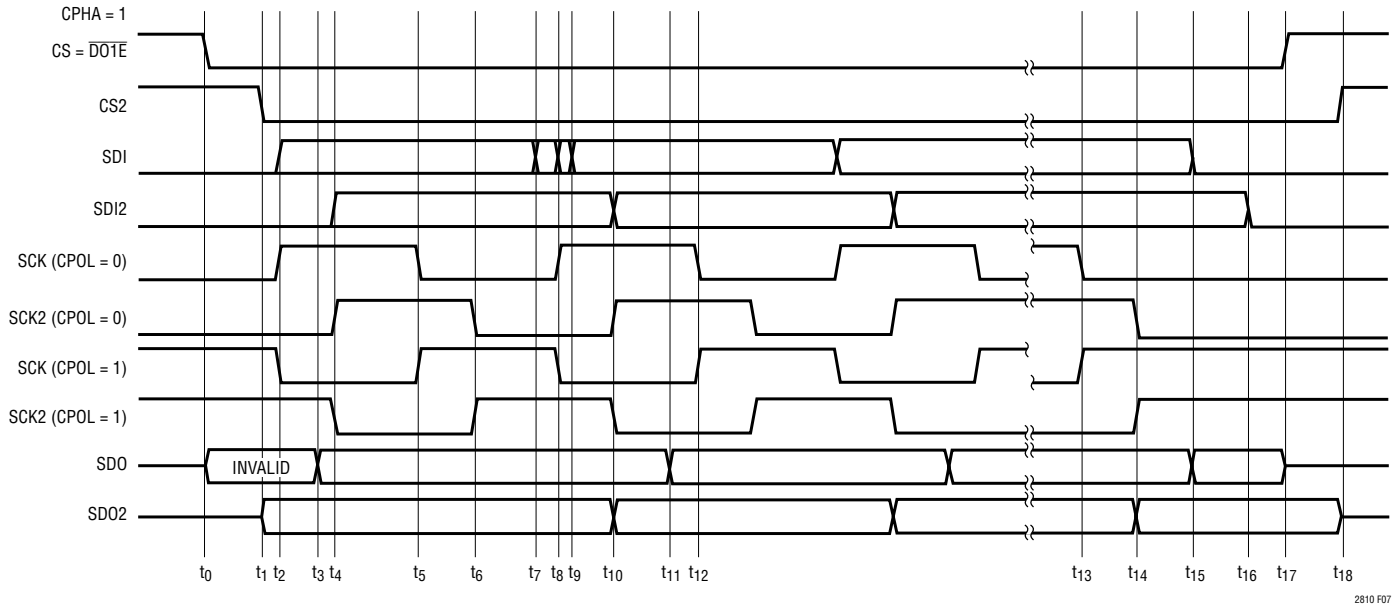

Figure 7. SPI Timing, Bidirectional, CPHA = 1

APPLICATIONS INFORMATION

Table 2. Bidirectional SPI Timing Event Description

TIME	CPHA	EVENT DESCRIPTION
t_0	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns. Logic side slave data output enabled, initial data is not equivalent to slave device data output.
t_0, t_1, t_{17}, t_{18}	0, 1	Propagation delay chip select, logic to isolated side, 50ns typical.
t_1	0, 1	Slave device chip select output data enable.
t_2	0	Start of data transmission, data setup.
	1	Start of transmission, data and clock setup. Data transition must be within –13ns to 3ns of clock edge.
t_1 to t_3	0, 1	Propagation delay of slave data, isolated to logic side, 50ns typical.
t_3	0, 1	Slave data output valid, logic side.
t_2 to t_4	0	Propagation delay of data, logic side to isolated side.
	1	Propagation delay of data and clock, logic side to isolated side.
t_5	0, 1	Logic side data sample time, half clock period delay from data setup transition.
t_5, t_6	0, 1	Propagation delay of clock, logic to isolated side.
t_6	0, 1	Isolated side data sample time.
t_8	0, 1	Synchronous data and clock transition, logic side.
t_7, t_8	0, 1	Data to clock delay, must be ≤ 13ns.
t_8, t_9	0, 1	Clock to data delay, must be ≤ 3ns.
t_8, t_{10}	0, 1	Propagation delay clock and data, logic to isolated side.
t_{10}, t_{14}	0, 1	Slave device data transition.
t_{10}, t_{11}, t_{14}, t_{15}	0, 1	Propagation delay slave data, isolated to logic side.
t_{11}, t_{12}	0, 1	Slave data output to sample clock setup time.
t_{13}	0	Last data and clock transition logic side.
	1	Last sample clock transition logic side.
t_{13}, t_{14}	0	Propagation delay data and clock, logic to isolated side.
	1	Propagation delay clock, logic to isolated side.
t_{15}	0	Last slave data output transition logic side.
	1	Last slave data output and data transition, logic side.
t_{15}, t_{16}	1	Propagation delay data, logic to isolated side.
t_{17}	0, 1	Asynchronous chip select transition, end of transmission. Disable slave data output logic side.
t_{18}	0, 1	Chip select transition isolated side, slave data output disabled.

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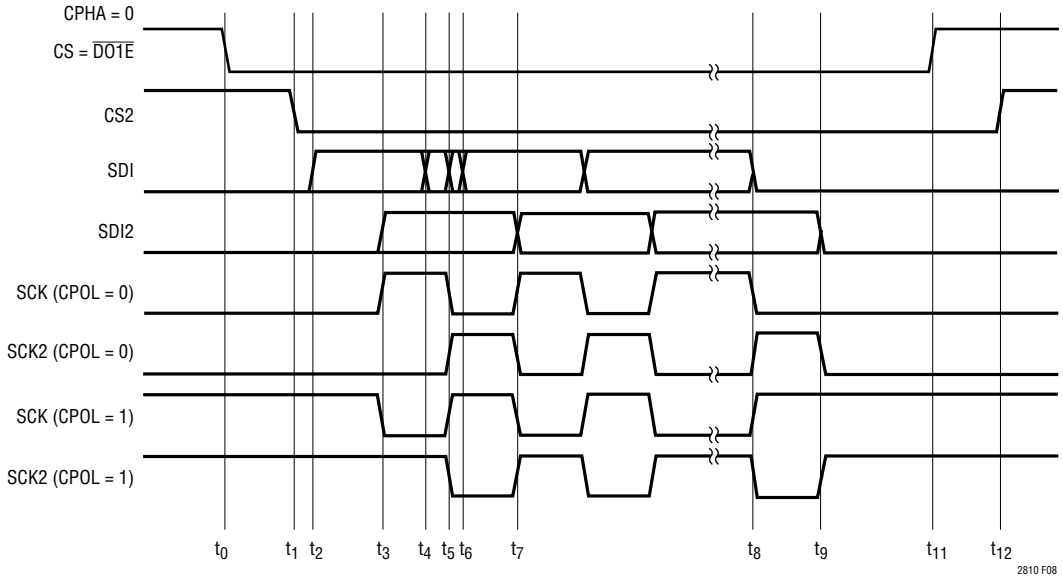

Figure 8. SPI Timing, Unidirectional, CPHA = 0

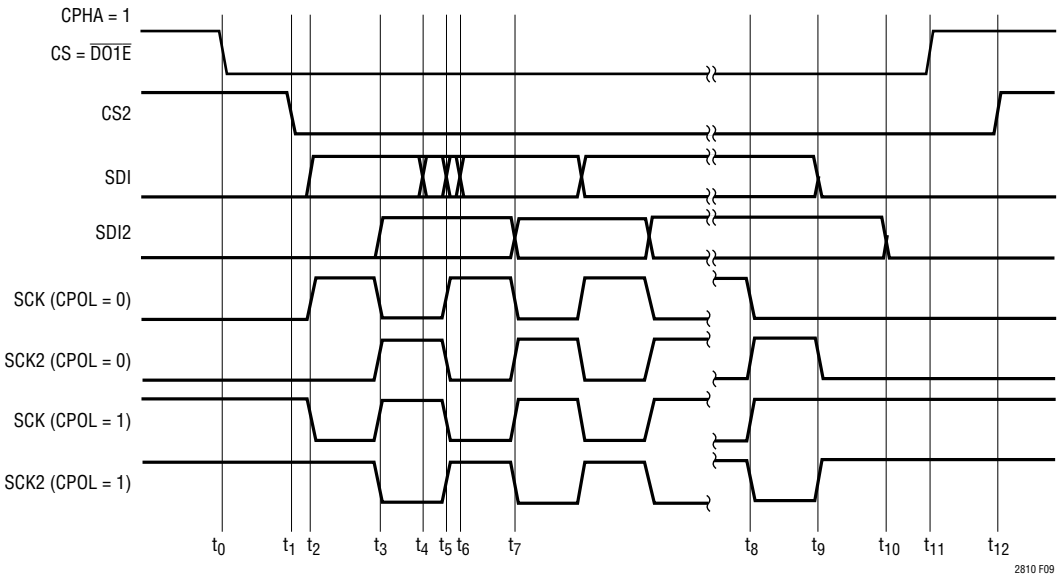

Figure 9. SPI Timing, Unidirectional, CPHA = 1

APPLICATIONS INFORMATION

Table 3. Unidirectional SPI Timing Event Description

TIME	CPHA	EVENT DESCRIPTION
t_0	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns.
t_0, t_1	0, 1	Propagation delay chip select, logic to isolated side.
t_2	0	Start of data transmission, data setup.
	1	Start of transmission, data and clock setup. Data transition must be within –13ns to 3ns of clock edge.
t_2, t_3	0	Propagation delay of data, logic side to isolated side.
	1	Propagation delay of data and clock, logic side to isolated side.
t_3	0, 1	Logic side data sample time, half clock period delay from data setup transition.
t_3 to t_5	0, 1	Clock propagation delay, clock and data transition.
t_4, t_5	0, 1	Data to clock delay, must be ≤ 13ns.
t_5, t_6	0, 1	Clock to data delay, must be ≤ 3ns.
t_5 to t_7	0, 1	Data and clock propagation delay.
t_8	0	Last clock and data transition.
	1	Last clock transition.
t_8, t_9	0	Clock and data propagation delay.
	1	Clock propagation delay.
t_9, t_{10}	1	Data propagation delay.
t_{11}	0, 1	Asynchronous chip select transition, end of transmission.
t_{12}	0, 1	Chip select transition isolated side.

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Inter-IC Communication (I^2C) Bus

The LTM2810-I provides an isolated I^2C compatible interface supporting master mode only, with a unidirectional clock (SCL), and bidirectional data (SDA). The maximum data rate is 400kHz which supports fast-mode I^2C. Timing is detailed in Figure 10. The data rate is limited by the slave acknowledge setup time ($t_{SU;ACK}$), consisting of the I^2C standard minimum setup time ($t_{SU;DAT}$) of 100ns, maximum clock propagation delay of 225ns, glitch filter and isolated data delay of 500ns maximum, and the combined isolated and logic data fall time of 300ns at maximum bus loading. The total setup time reduces the I^2C data hold time ($t_{HD;DAT}$) to a maximum of 175ns, guaranteeing sufficient data setup time ($t_{SU;ACK}$).

The isolated side bidirectional serial data pin, SDA2, simplified schematic is shown in Figure 11. An internal 1.8mA current source provides a pull-up for SDA2. Do not connect any other pull-up device to SDA2. This current source is sufficient to satisfy the system requirements for bus capacitances greater than 200pF in fast mode and greater than 400pF in standard mode.

Additional proprietary circuitry monitors the slew rate on the SDA and SDA2 signals to manage directional control across the isolation barrier. Slew rates on both pins must be greater than 1V/µs for proper operation.

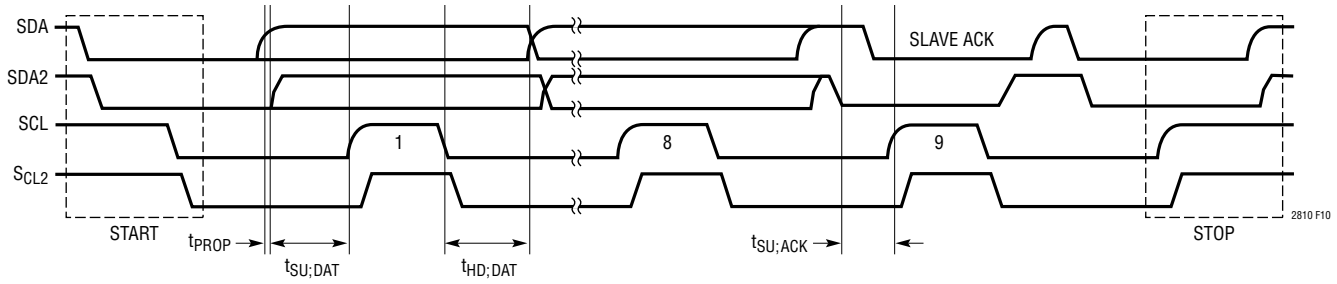


Figure 10. I^2C Timing Diagram

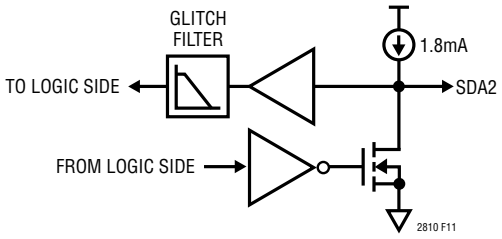


Figure 11. Isolated SDA2 Pin Schematic

APPLICATIONS INFORMATION

The logic side bidirectional serial data pin, SDA, requires a pull-up resistor or current source connected to V_L. Follow the requirements in Figure 12 and Figure 13 for the appropriate pull-up resistor on SDA that satisfies the desired rise time specifications and V_{OL} maximum limits for fast and standard modes. The resistance curves represent the maximum resistance boundary; any value may be used to the left of the appropriate curve.

The isolated side clock pin, SCL2, has a weak push-pull output driver; do not connect an external pull-up device. SCL2 is compatible with I^2C devices without clock stretching. On lightly loaded connections, a 100pF capacitor from SCL2 to GND2 or RC low pass filter (R = 500Ω, C = 100pF) can be used to decrease the rise and fall times and minimize noise.

Some consideration must be given to signal coupling between SCL2 and SDA2. Separate these signals on a printed circuit board or route with ground between. If these signals are wired off board, twist SCL2 with V_{L2} and/or GND2 and SDA2 with GND2 and/or V_{L2}; do not twist SCL2 and SDA2 together. If coupling between SCL2 and SDA2 is unavoidable, place the aforementioned RC filter at the SCL2 pin to reduce noise injection onto SDA2.

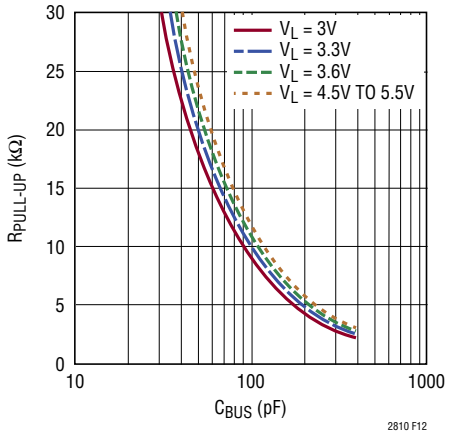


Figure 12. Maximum Standard Speed Pull-Up Resistance on SDA

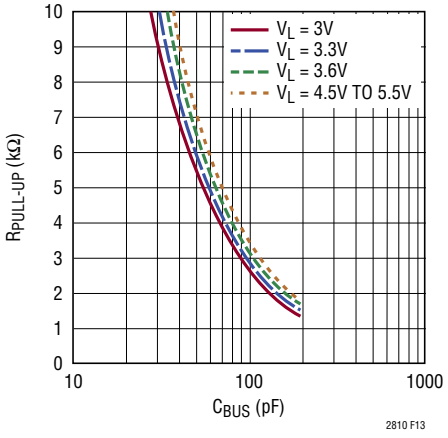


Figure 13. Maximum Fast Speed Pull-Up Resistance on SDA

APPLICATIONS INFORMATION

RF, Magnetic Field Immunity

The isolator µModule technology used within the LTM2810 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, radio-frequency, electromagnetic field immunity

EN 61000-4-8 Power frequency magnetic field immunity

EN 61000-4-9 Pulsed magnetic field immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 4.

Table 4. EMC Immunity Tests

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3 Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8 Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8 Level 5	60Hz	100A/m*
EN 61000-4-9 Level 5	Pulse	1000A/m

* Non IEC method.

PCB Layout

The high integration of the LTM2810 makes PCB layout very simple. However, to optimize its electrical isolation characteristics and EMI performance, some layout considerations are necessary.

- Input and output supply decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8µF to 22µF with 1Ω to 3Ω of ESR is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1µF to 4.7µF, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, and minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND and GND2. If ground planes are used, it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.
- For large ground planes a small capacitance (≤ 330pF) from GND to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be 4 layers. Care must be exercised in applying either technique to ensure the voltage rating of the barrier is not compromised.
- In applications without an embedded PCB substrate capacitance, a slot may be added between the logic side and isolated side device pins. The slot extends the creepage path between terminals on the PCB side, and may reduce leakage caused by PCB contamination. The slot should be placed in the middle of the device and extend beyond the package perimeter.

TYPICAL APPLICATIONS

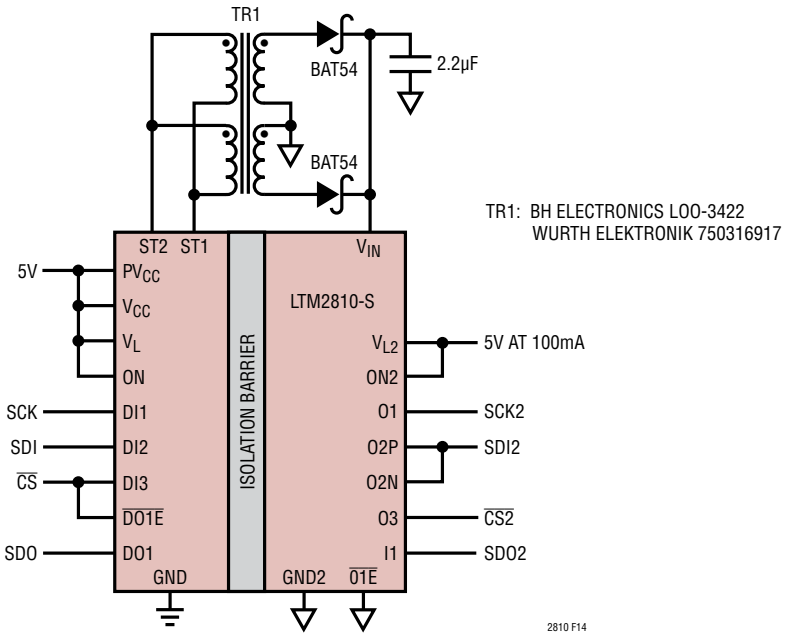


Figure 14. Isolated SPI with 5V Input and 5V Regulated Output

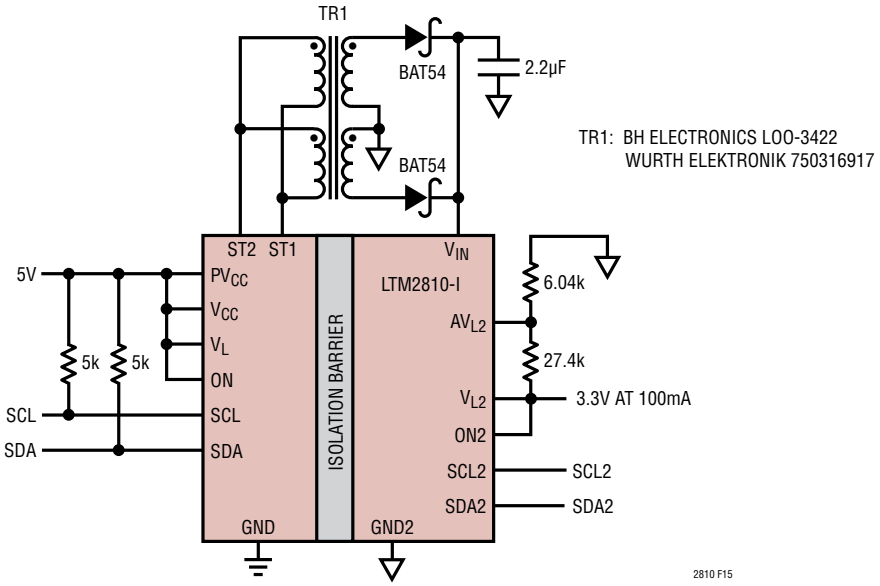


Figure 15. Isolated I²C with 5V Input and 3.3V Regulated Output

TYPICAL APPLICATIONS

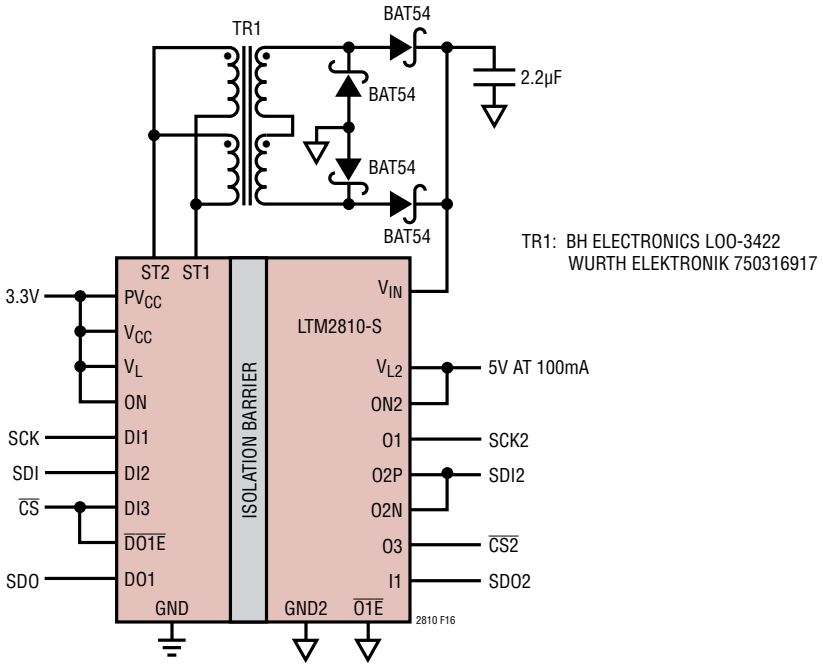


Figure 16. Isolated SPI with 3.3V Input and 5V Regulated Output

TYPICAL APPLICATIONS

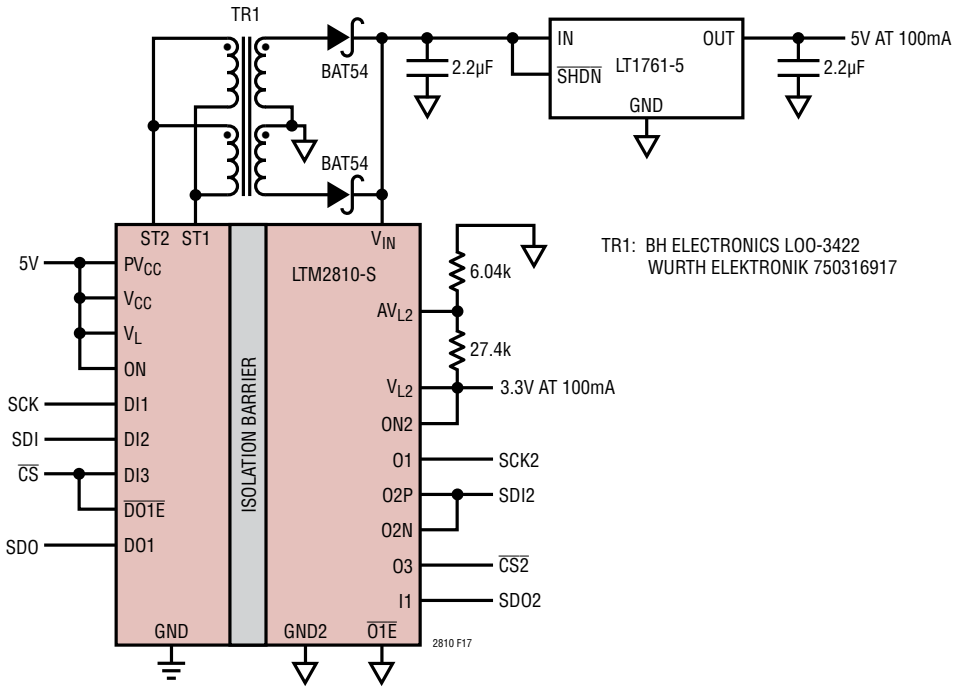


Figure 17. Isolated SPI with 3.3V Input with 3.3V and 5V Regulated Outputs

TYPICAL APPLICATIONS

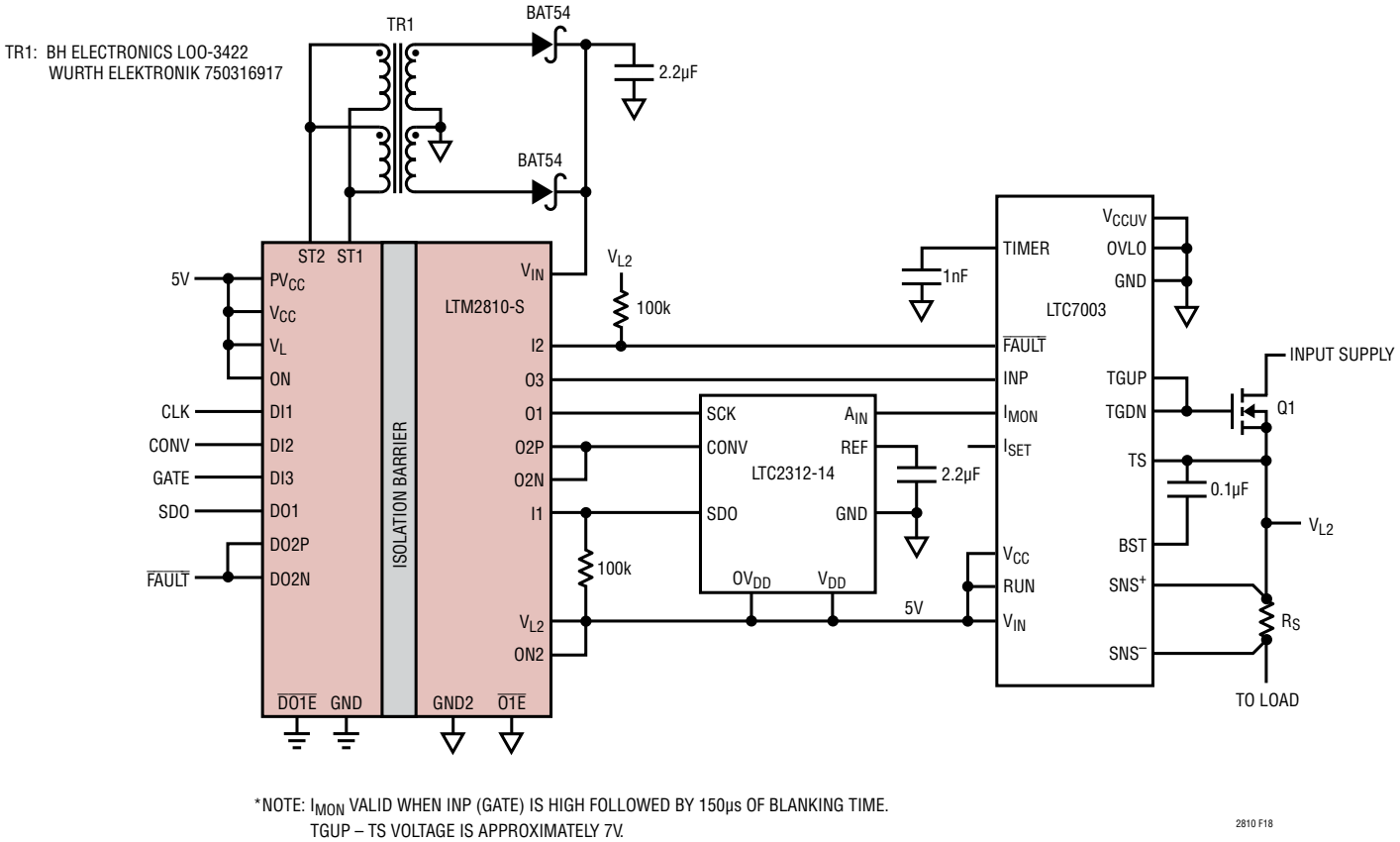
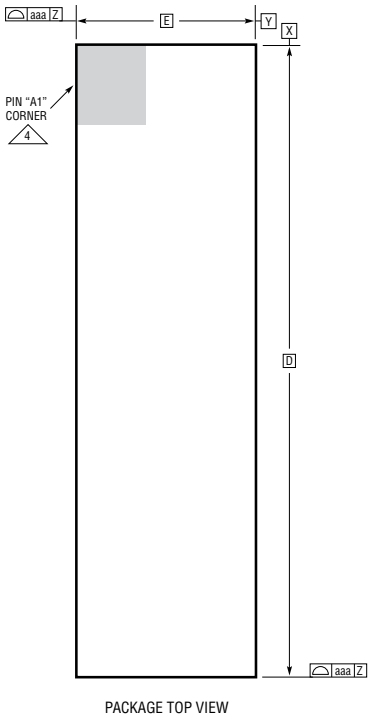


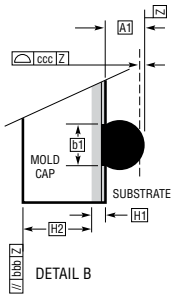
Figure 18. High Voltage Switch Controller with Current Readback

PACKAGE DESCRIPTION

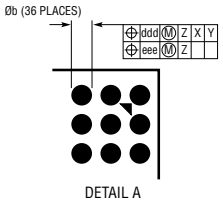
BGA Package
36-Lead (22mm × 6.25mm × 2.06mm)
(Reference LTC DWG# 05-08-1588 Rev Ø)



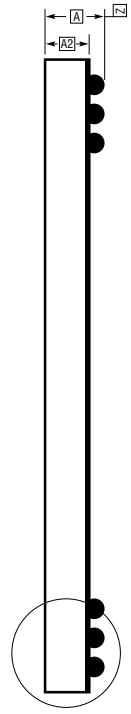
PACKAGE TOP VIEW



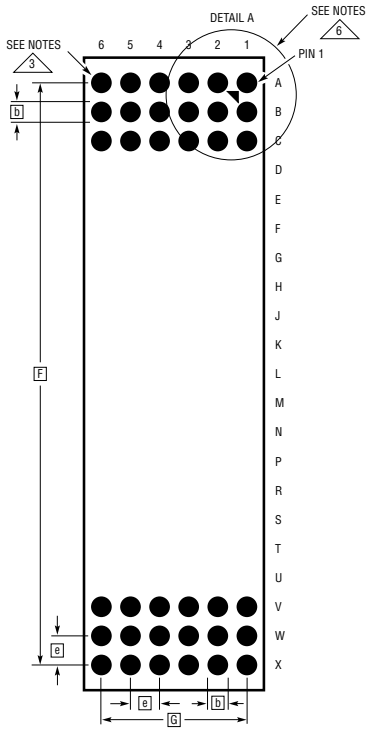
DETAIL B



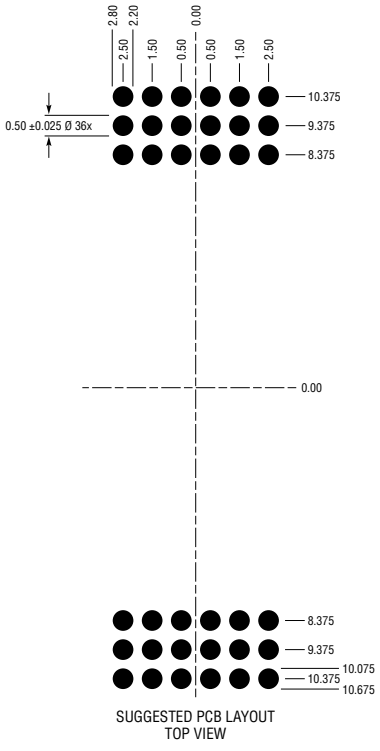
DETAIL A



DETAIL B
PACKAGE SIDE VIEW



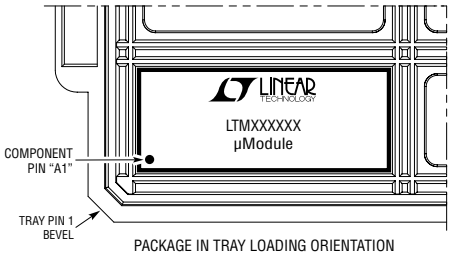
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	1.81	2.06	2.31	
A1	0.40	0.50	0.60	BALL HT
A2	1.41	1.56	1.71	
b	0.50	0.60	0.70	BALL DIMENSION
b1	0.47	0.50	0.53	PAD DIMENSION
D		22.0		
E		6.25		
e		1.0		
F		20.75		
G		5.0		
H1	0.46	0.56	0.66	SUBSTRATE THK
H2	0.95	1.00	1.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.15	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 36				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



PACKAGE IN TRAY LOADING ORIENTATION

BGA 36 0817 REV Ø

TYPICAL APPLICATION

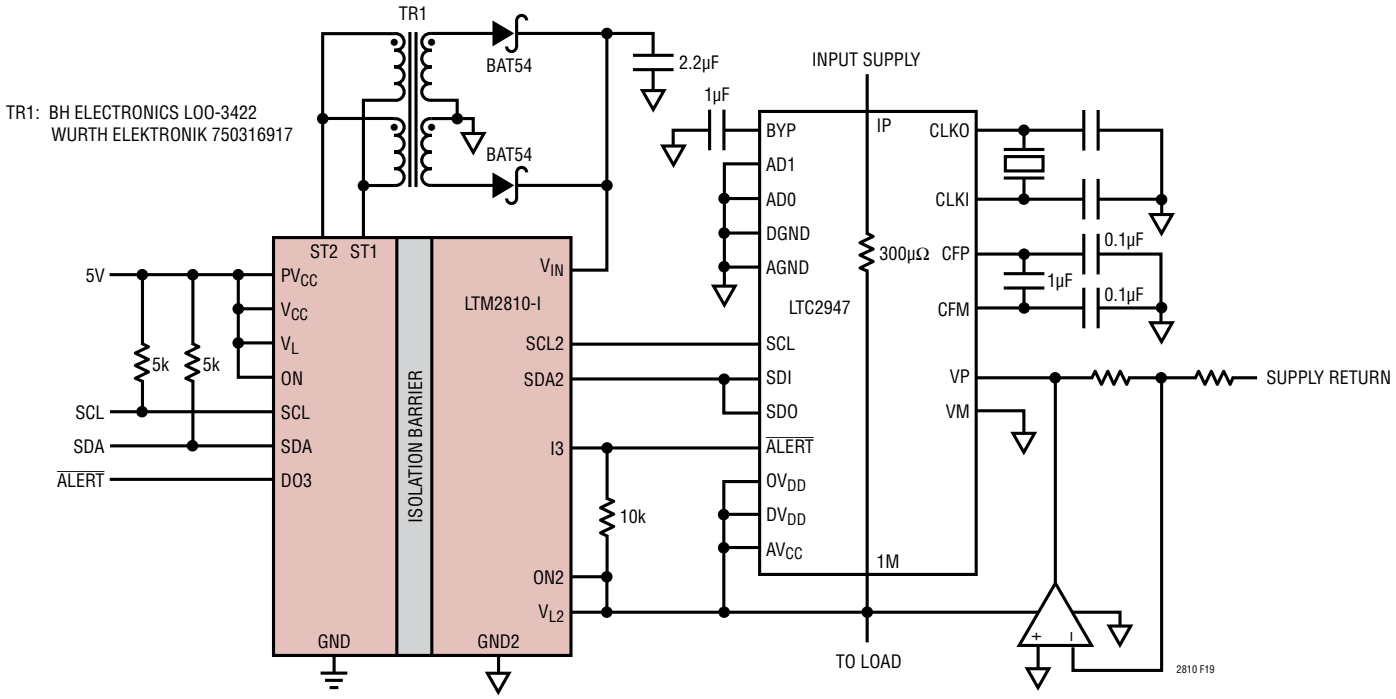


Figure 19. High Voltage 30A Power/Energy Monitor with Integrated Sense Resistor

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM2881	Isolated RS485/RS422 µModule Transceiver with Integrated DC/DC Converter	20Mbps 2500V_{RMS} Isolation with Power in LGA/BGA Package
LTM2882	Dual Isolated RS232 µModule Transceiver with Integrated DC/DC Converter	2500V_{RMS} Isolation with Power in LGA/BGA Package
LTM2883	SPI/Digital or I^2C Isolated µModule with Adjustable 5V, and ±12.5V Nominal Voltage Rails	2500V_{RMS} Isolation with Power in BGA Package
LTM2884	Isolated High Speed USB µModule with Integrated DC/DC Converter	2500V_{RMS} Isolation with Power in BGA Package
LTM2885	Isolated RS485/RS422 µModule Transceiver with Integrated DC/DC Converter	20Mbps 6500V_{RMS} Isolation with Power in BGA Package
LTM2886	SPI/Digital or I^2C Isolated µModule with Adjustable 5V, and Fixed ±5V Power Rails	2500V_{RMS} Isolation with Power in BGA Package
LTM2887	SPI/Digital or I^2C Isolated µModule with Two Adjustable 5V Rails	2500V_{RMS} Isolation with Power in BGA Package
LTM2889	Isolated CAN µModule Transceiver with Integrated DC/DC Converter	4Mbps 2500V_{RMS} Isolation with Power in BGA Package
LTM2892	SPI/Digital or I^2C Isolated µModule	3500V_{RMS} Isolation in BGA Package
LTM2893	Complete 100MHz SPI ADC µModule Isolator	6000V_{RMS} Isolation in BGA Package
LTM2894	Complete Isolated USB µModule Transceiver	7500V_{RMS} Isolation in BGA Package
LTM2895	Complete 100MHz DAC SPI Serial Interface µModule Isolator	6000V_{RMS} Isolation in BGA Package
LTM9100	Anyside™ Isolated Switch Controller with I^2C Command and Telemetry	5000V_{RMS} Isolation in BGA Package, 10-Bit Current
LTC®2946	Wide Range I^2C Power, Energy and Charge Monitor	0V to 100V Operation, 12-Bit ADC with ±0.4% TUE
LTC2947	30A Integrated Sense Resistor I^2C Power, Energy and Charge Monitor	0V to 15V Operation, 16-Bit ADC
LTC7003	Fast 60V Protected High Side NMOS Static Switch Driver	3.5V to 60V Operation, I_Q = 35µA, Turn-On (C_L = 1nF) = 35ns, Internal Charge Pump