

LA6585MC

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC} max	Supply Voltage		15	V
P _d max	Allowable Power Dissipation	Mounted on a specified board (Note 1)	750	mW
I _{OUT} max	Output Current		0.7	A
V _{OUT} max	Output Withstand Voltage		15	V
V _{RD/FG} max	RD/FG Output Pin Output Withstand Voltage		15	V
I _{RD/FG} max	RD/FG Output Current		10	mA
I _B max	HB Output Current		10	mA
T _{opr}	Operating Temperature		–30 to +90	°C
T _{stg}	Storage Temperature		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on a specified board: 114.3 mm × 76.1 mm × 1.6 mm glass epoxy.

OPERATING CONDITIONS (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply Voltage		2.2 to 14.0	V
V _{ICM}	Common-phase Input Voltage Range of Hall Input		0 to V _{CC} –1.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CC1}	Circuit Current	During drive (CT = L)	3	6	9	mA
I _{CC2}		During lock protection (CT = H)	2.5	5	7.5	mA
I _{CT1}	Lock Detection Capacitor Charge Current		0.9	1.2	1.5	μA
I _{CT2}	Capacitor Discharge Current		0.10	0.18	0.25	μA
R _{CT}	Capacitor Charge and Discharge Current Ratio	RCD = I _{CT1} /I _{CT2}	5	6.5	8	–
V _{CT1}	CT Charge Voltage		1.3	1.5	1.7	V
V _{CT2}	CT Discharge Voltage		0.3	0.5	0.7	V
V _{OL}	OUT Output L Saturation Voltage	I _O = 200 mA	–	0.25	0.45	V
V _{OH}	OUT Output H Saturation Voltage	I _O = 200 mA	–	0.95	1.2	V
V _{HN}	Hall Input Sensitivity	Zero peak value (including offset and hysteresis)	–	7	15	mV
V _{HB}	Hall Bias Voltage	I _{HB} = 5 mA	1.3	1.5	1.7	V
V _{FG/RD}	FG/RD Output Pin L Voltage	I _{RD/FG} = 5 mA	–	0.15	0.3	V
I _{FG/RDL}	FG/RD Output Pin Leak Current	V _{RD/FG} = 15 V	–	1	30	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TRUTH TABLE

IN-	IN+	CT	OUT1	OUT2	FG	RD	Mode
H	L	L	H	L	L	L	During rotation
L	H		L	H	H		
-	-	H	Off	Off	-	H	During overheat protection

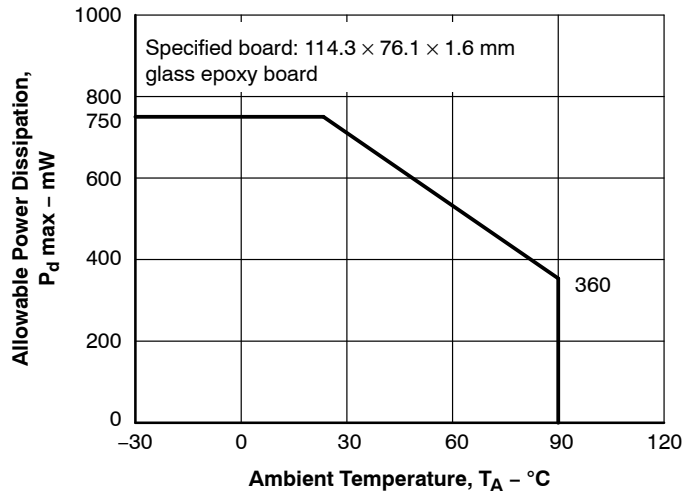


Figure 1. $P_d \text{ max} - T_A$

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BLOCK DIAGRAM

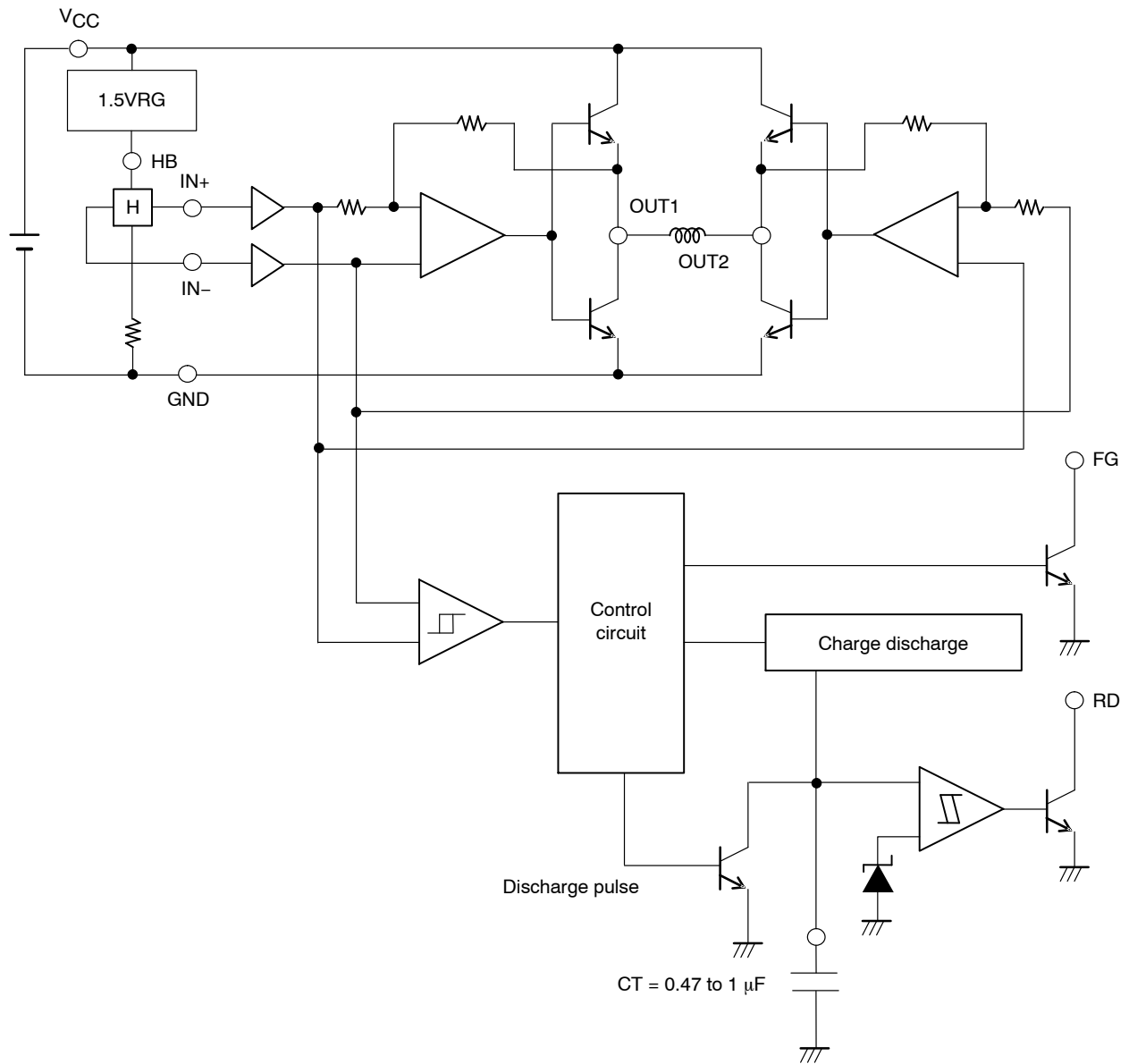


Figure 2. Block Diagram

APPLICATION CIRCUIT

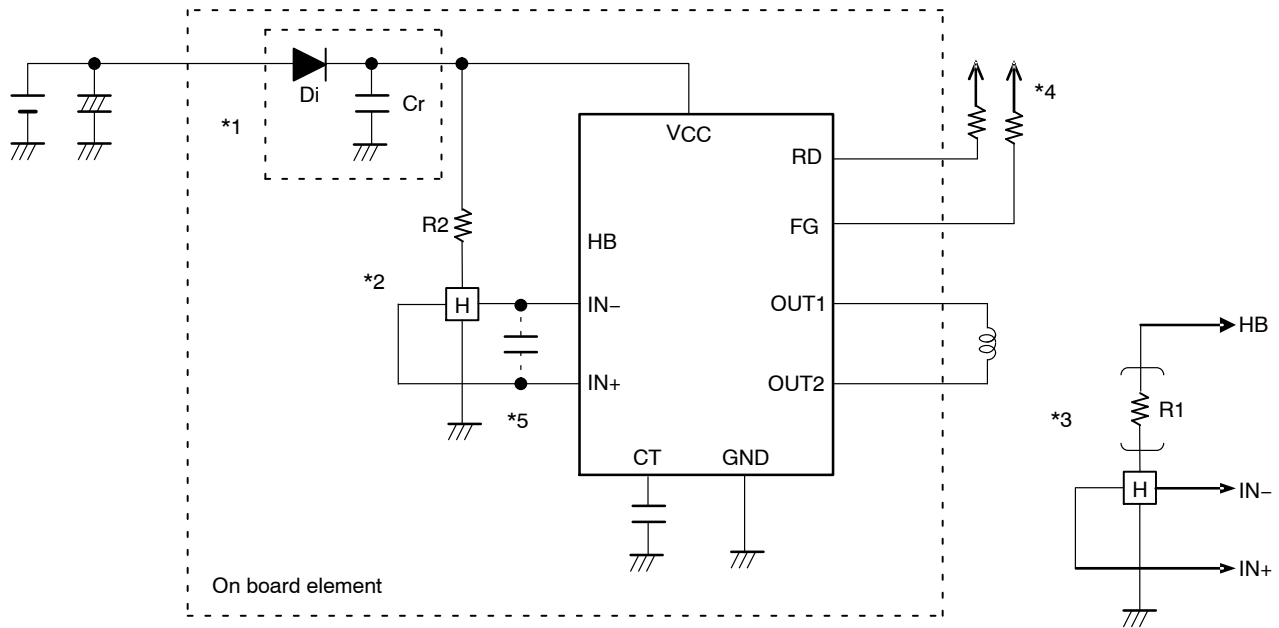


Figure 3. Sample Application Circuit

- *1: When the breakdown protective DI at reverse connection is to be used, it is necessary to insert the capacitor Cr to secure the regenerative current route. Similarly, Cr must be provided to enhance the reliability when there is no capacitor near the fan power line.
- *2: To obtain Hall bias from V_{CC}, carry out bias to V_{CC} with resistor R2 as shown in the figure. Linear driving is made through voltage control of the coil by amplifying the Hall output. When the Hall element output is large, the startup performance and efficiency are improved. Adjustment of the Hall element can reduce the noise further.

- *3: To obtain Hall bias from the HB pin, carry out constant-voltage bias at about 1.5 V, which enables the Hall element to generate the stable Hall output satisfactory in temperature characteristics. Adjustment of the Hall output amplitude is made with R1. (When V_{CC} = 12 V, the step *2 above proves advantageous for IC heat generation.)
- *4: Keep this open when not using.
- *5: When the wiring from the Hall output to IC Hall input is long, noise may be carried through the wiring. In this case, insert the capacitor as shown in the figure.

ORDERING INFORMATION

Device	Package	Wire Bond	Shipping [†] (Qty / Packing)
LA6585MC-AH	SOIC-10 NB (Pb-Free / Halogen Free)	Au wire	2,000 / Tape & Reel
LA6585MC-AH-M	SOIC-10 NB (Pb-Free / Halogen Free)	Au wire	2,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

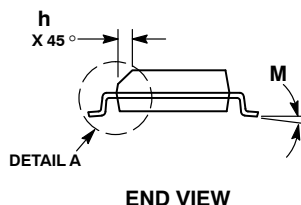
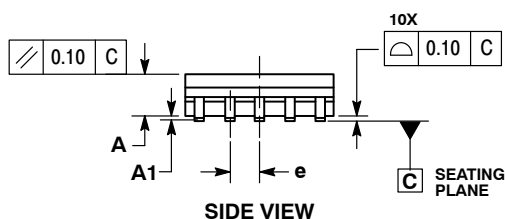
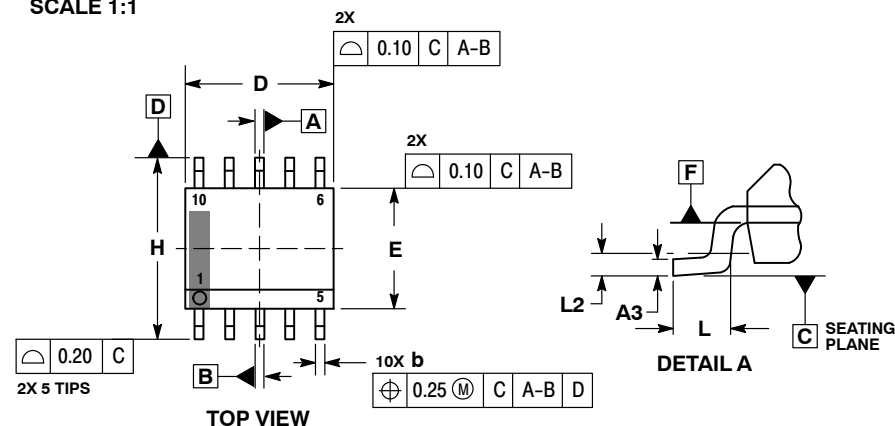
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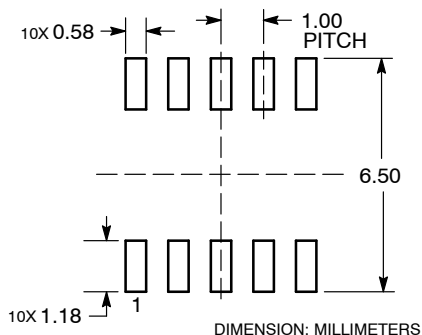
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SCALE 1:1

SOIC-10 NB
CASE 751BQ
ISSUE B

DATE 26 NOV 2013



RECOMMENDED SOLDERING FOOTPRINT*



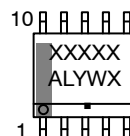
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

MILLIMETERS		
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	0.80
L2	0.25 BSC	
M	0°	8°

GENERIC MARKING DIAGRAM*




XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD	
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