

LA5693D,5693M

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	$V_{\text{CONT max}}$	1s	60	V
			41	V
Control pin current	$I_{\text{CONT max}}$		11	mA
CK input voltage	$V_{\text{CK max}}$		25	V
Reset pin voltage	$V_{\text{RES}(1) \text{ max,}}$ $V_{\text{RES}(2) \text{ max}}$		41	V
Allowable power dissipation	$P_d \text{ max}$	LA5693D	500	mW
		LA5693M	370	mW
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* : A PNP transistor is connected to the LA5693D, LA5693M externally to provide a low-saturation voltage regulator.

Therefore, $I_{\text{CONT}} \approx 100\text{mA}$ will flow, as starting current, in the VCC range where the output cannot be regulated.

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	V_{CONT}		6 to 40	V
Control pin current	$I_{\text{CONT max}}$		10	mA
Reset output current	$V_{\text{RES}(1) \text{ max,}}$ $V_{\text{RES}(2) \text{ max}}$	External R pull-up	8	mA
Reset detection voltage	$V_S \text{ min}$		4	V

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{\text{CC}} = 14\text{V}$, $I_O = 50\text{mA}$, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output voltage	V_O		4.8	5.0	5.2	V
Line regulation1	ΔV_{OLN1}	$9\text{V} \leq V_{\text{CC}} \leq 16\text{V}$		2	5	mV
Line regulation2	ΔV_{OLN2}	$6\text{V} \leq V_{\text{CC}} \leq 40\text{V}$		4	30	mV
Load regulation	ΔV_{OLD}	$1\text{mA} \leq I_O \leq 50\text{mA}$		4	30	mV
Current dissipation	I_{CC}	$I_O = 0$		4.4	6.5	mA
Output noise voltage	V_{NO}	$10\text{Hz} \leq f \leq 100\text{kHz}$, $V_{\text{CK}} = 0\text{V}$		150		μV
Temperature coefficient of output voltage	$\Delta V_O / \Delta T_a$	$I_O = 5\text{mA}$, $-40^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$		± 0.2		$\text{mV}/^\circ\text{C}$
Reference voltage	V_{REF}		1.13	1.18	1.23	V
'H'-level CK input voltage	V_{IH}		2			V
'L'-level CK input voltage	V_{IL}				0.8	V
'H'-level CK input current	I_{IH}	$V_{\text{CK}} = 5\text{V}$		0.3	0.7	mA
'L'-level CK input current	I_{IL}	$V_{\text{CK}} = 0\text{V}$	-1.0	-0.1		μA
'H'-level reset output voltage	$V_{\text{ORH}(1)}/$ $V_{\text{ORH}(2)}$	$\overline{\text{RES}}(2)$: $10\text{k}\Omega$ pull-up	4.8	5.0	5.2	V
'L'-level reset output voltage 1	$V_{\text{ORL}(1)}/$ $V_{\text{ORL}(2)1}$	$\overline{\text{RES}}(2)$: $10\text{k}\Omega$ pull-up		40	200	mV
'L'-level reset output voltage 2	$V_{\text{ORL}(1)2}/$ $V_{\text{ORL}(2)2}$	$I_{\text{RES}}(1) = I_{\text{RES}}(2) = 8\text{mA}$		0.16	0.8	V
CK input pulse width	t_{CKW}	$V_{\text{CK}} = 5\text{V}$	3			μs
Reset output delay time	t_d	$C_t = 1\mu\text{F}$	7.5	10	12.5	ms
Watchdog time	t_{WD}	$C_t = 1\mu\text{F}$	30	40	50	ms
Watchdog reset time	t_{WR}	$C_t = 1\mu\text{F}$	0.1	0.25	0.4	ms
Reset hysteresis voltage	V_{hys}	$V_S = 4.5\text{V}$	100	200	300	mV

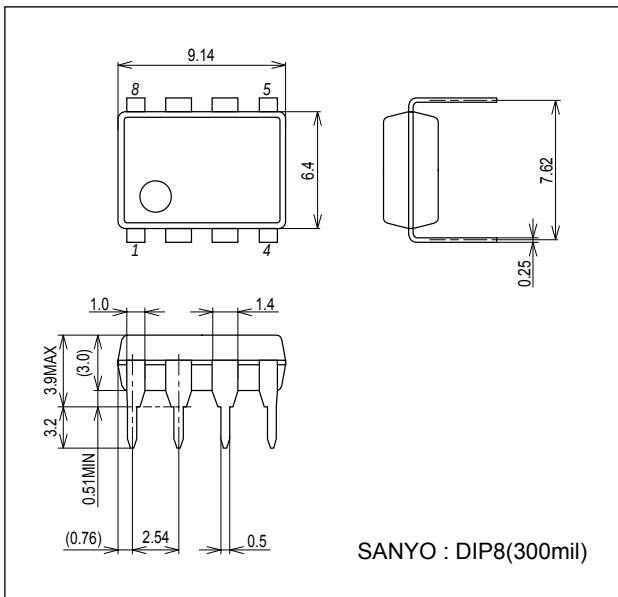
LA5693D,5693M

Package Dimensions

unit : mm (typ)

3001D

[LA5693D]

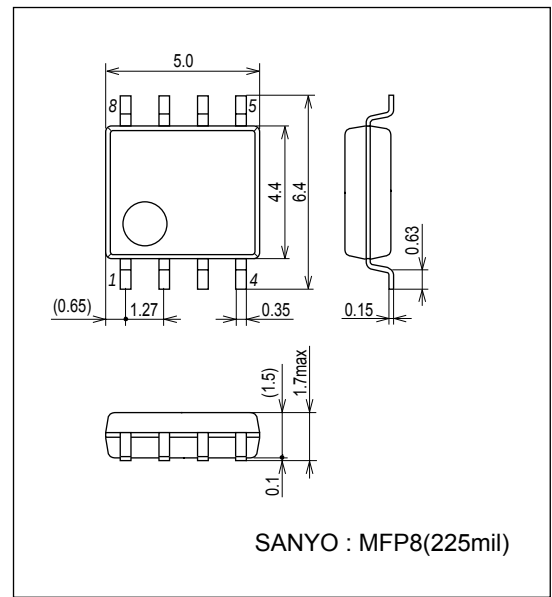


Package Dimensions

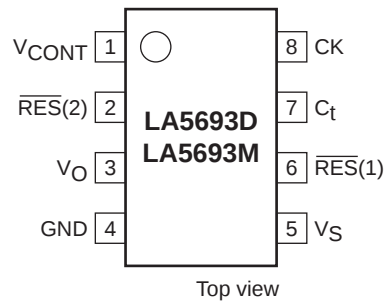
unit : mm (typ)

3032D

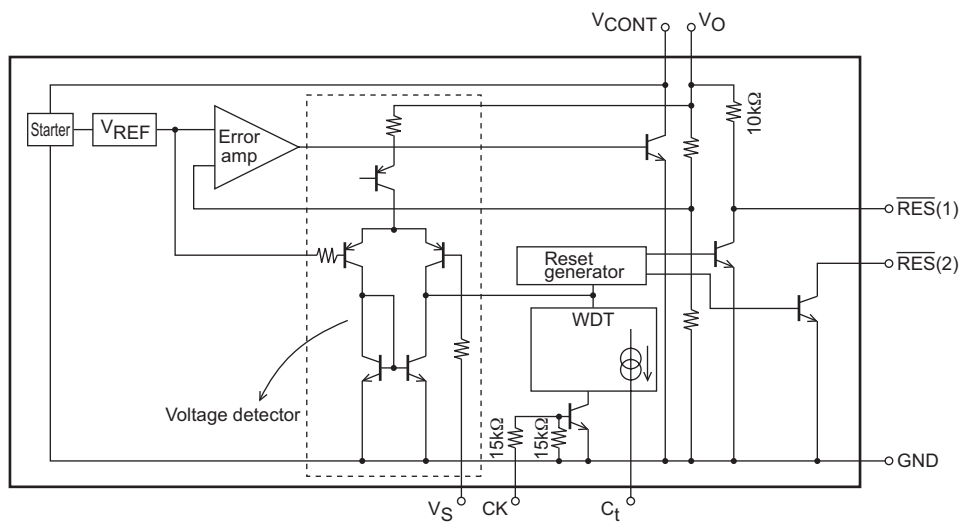
[LA5693M]



Pin Assignment

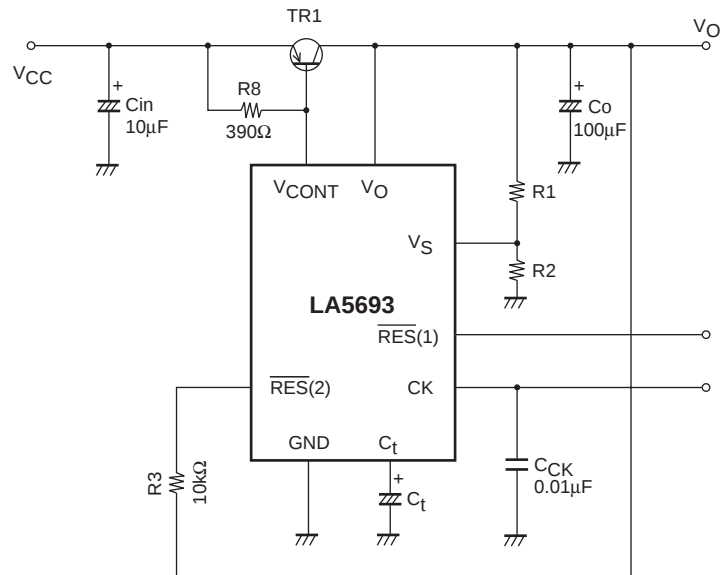


Block Diagram

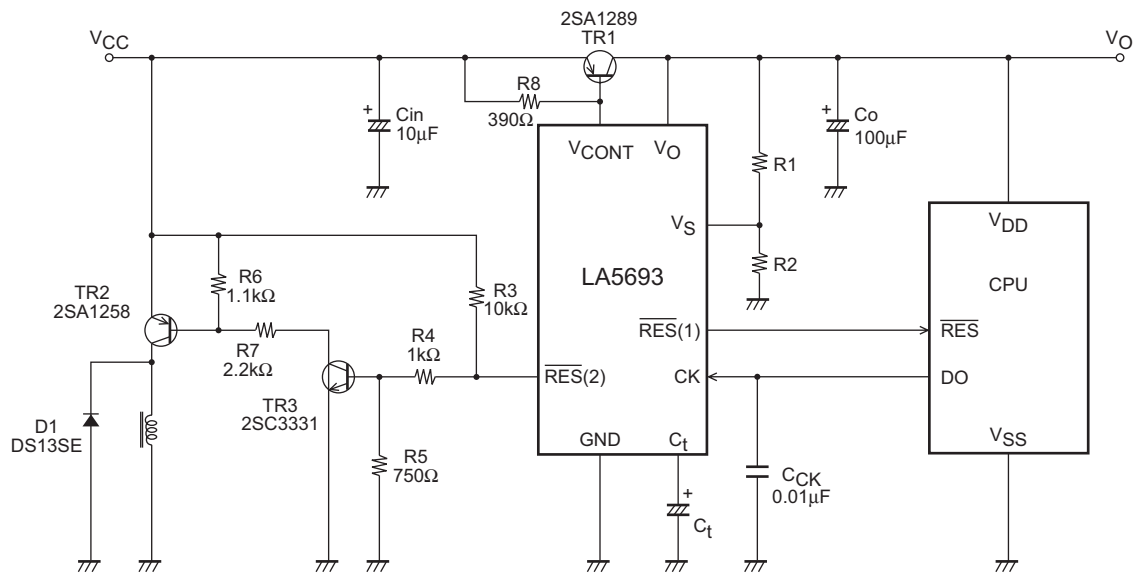


RES(1) : Contains a pull-up resistor of 10kΩ.
RES(2) : Open collector.

Test Circuit



Application Circuit Example



$$V_S = V_{REF} \times \left(\frac{R_1}{R_2} + 1 \right)$$

$$V_{REF} \approx 1.18[V]$$

$$t_d = 10 \times C_t (\mu F) \quad [ms]$$

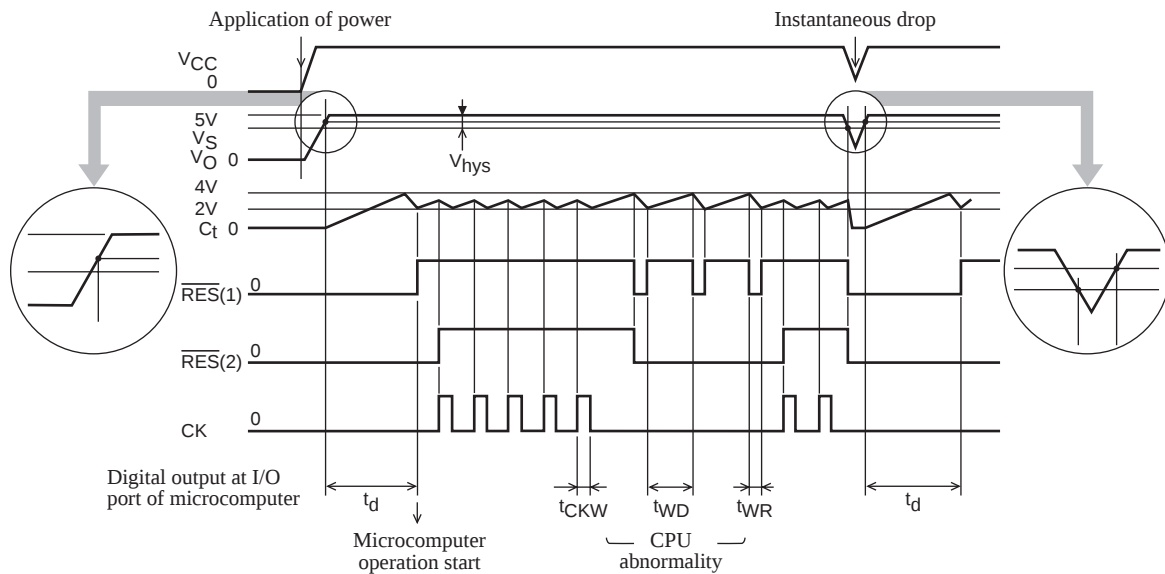
$$t_{WD} = 40 \times C_t (\mu F) \quad [ms]$$

$$t_{WR} = 0.25 \times C_t (\mu F) \quad [ms]$$

Note on application

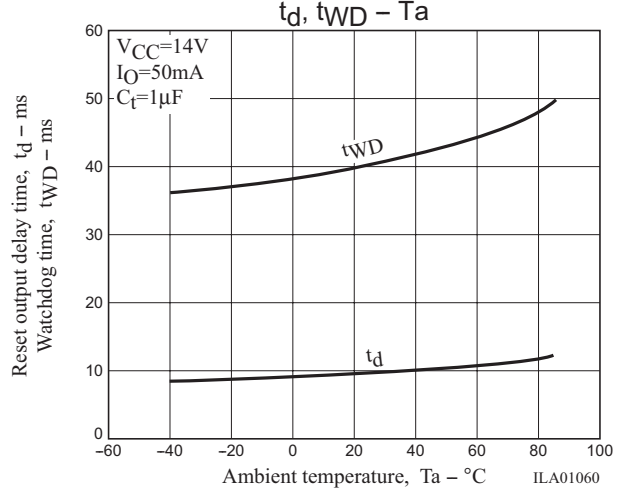
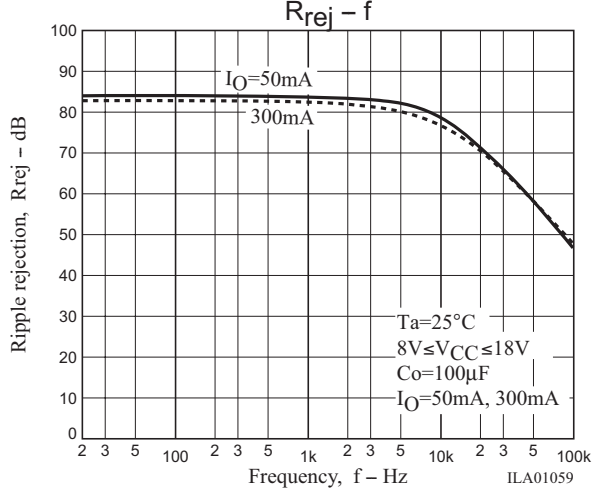
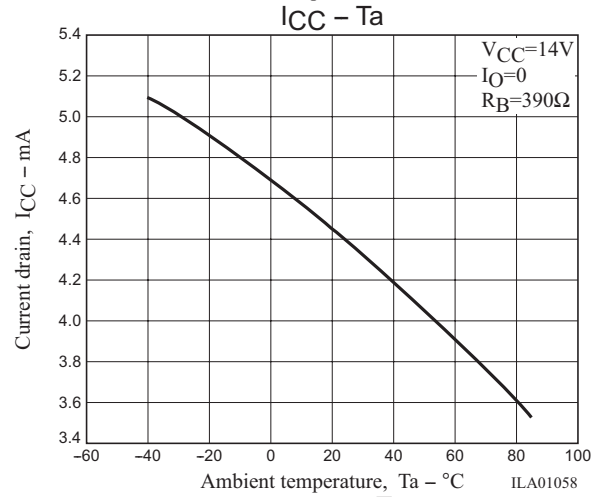
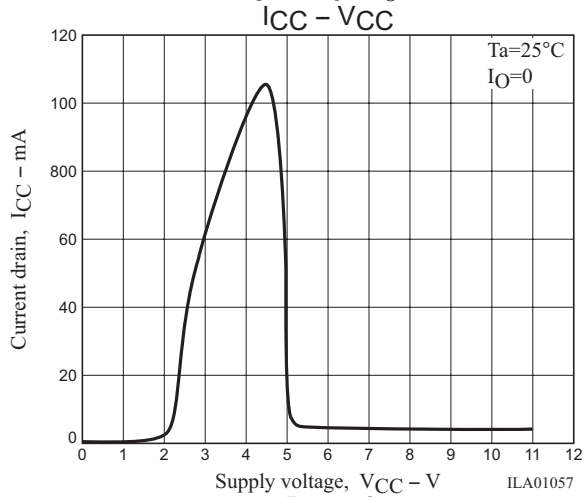
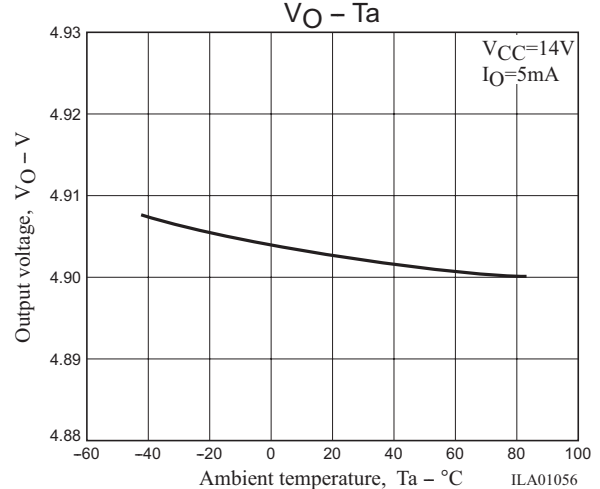
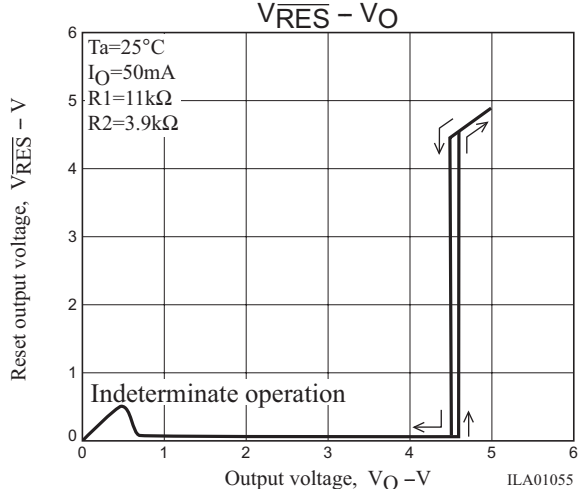
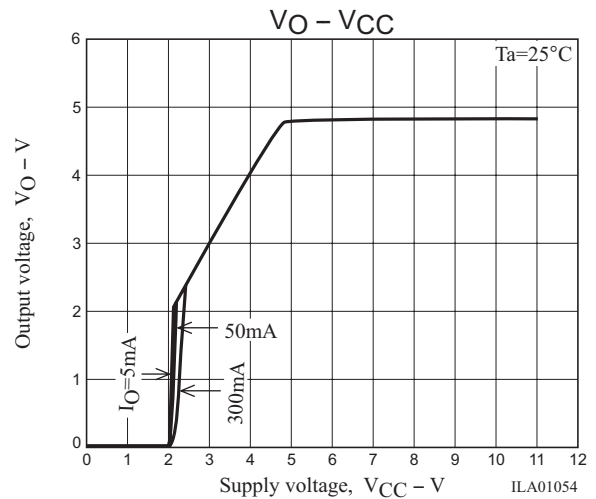
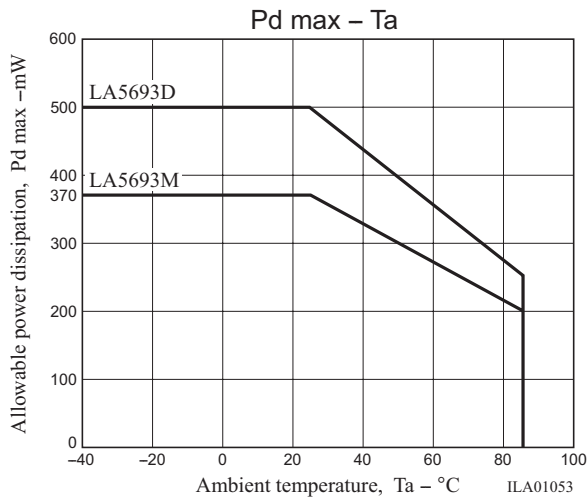
1. For stable operation, place C_{in} , C_O , and $TR1$ as near to the IC as possible.
2. When used in 0°C or below it, a capacitor of which impedance at high-frequency operation is low and has a good temperature characteristic (such as SANYO OS-CON capacitor or others) should be used to prevent oscillation.
3. Set V_S to the output voltage level where the circuit will be reset using external resistors $R1$ and $R2$. V_S should be set to 4V or greater due to internal circuit operation.
4. C_{CK} must be inserted to cut the high range element of clock noise to prevent it from becoming a reset output noise.
5. For C_t , a capacitor which less varies the capacitance according to the temperature should be used.

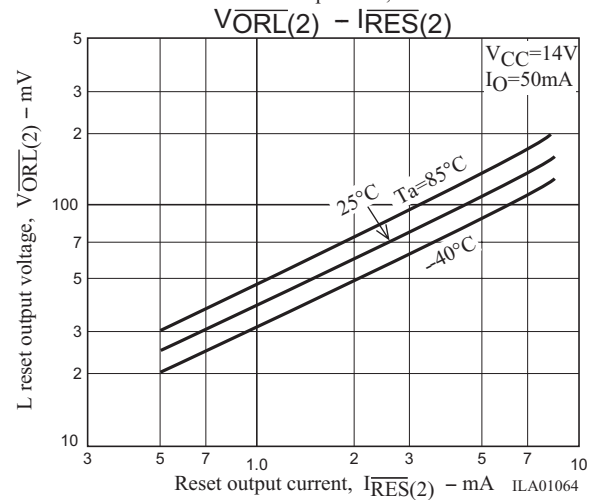
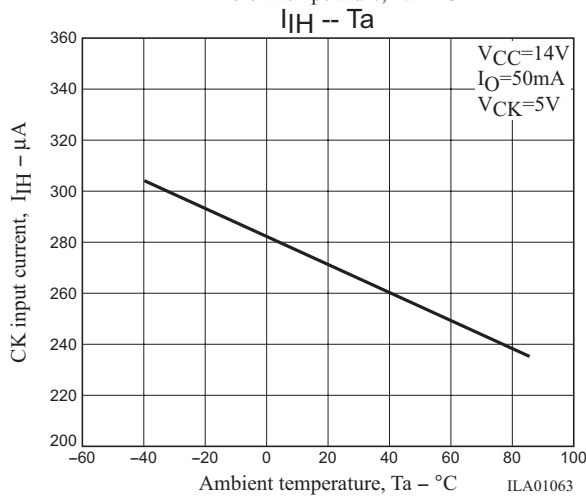
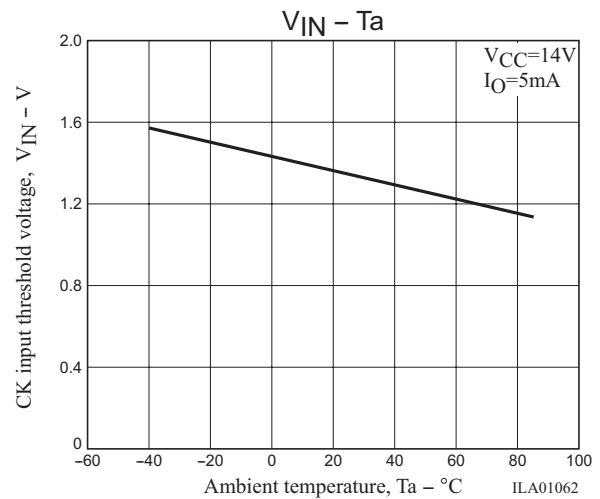
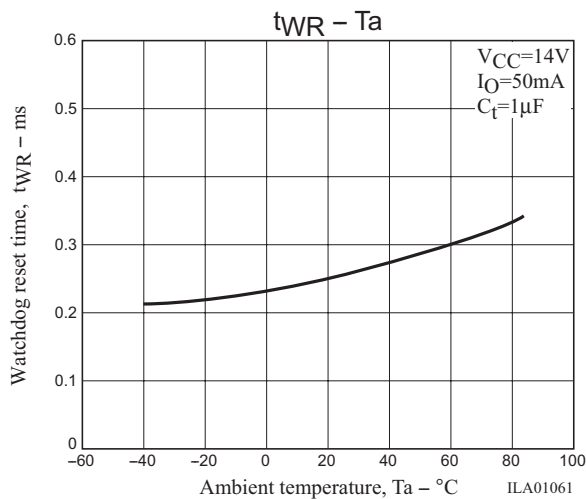
Timing Chart



Note : Edge-triggered at the point indicated by the arrow of CK signal.

LA5693D,5693M





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