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REVISION HISTORY

5/2018—Rev. A to Rev. B

Changed HMC1049 to HMC1049LP5E ... Throughout
Changes to Features Section and General Description Section . 1
Change to Figure 27 Caption and Figure 28 Caption ... 10
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 14

11/2014—Rev. 01.1213 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Updated Format ... Universal
Changes to General Description ... 1
Change to Table 2, Thermal Resistance Parameter Column ... 4
Added Figure 2 ... 5
Changes to Table 4 ... 5
Moved Figure 3 to Figure 9 to Interface Schematics Section ... 6
Change to Figure 8 and Figure 9 ... 6
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Added Ordering Guide Section ... 15

SPECIFICATIONS

T_A = 25°C, V_{DD} = 7 V, I_{DD} = 70 mA[1].

Table 1.

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
FREQUENCY RANGE	0.3		1	1		14	14		20	GHz
GAIN	13.5	16.5		12	15		10	13		dB
Gain Variation Over Temperature		0.006			0.019			0.017		dB/°C
NOISE FIGURE		2.5	3.5		1.8	2.5		2.7	4.0	dB
RETURN LOSS										
Input		15			13			14		dB
Output		8			15			13		dB
OUTPUT										
Output Power for 1 dB Compression (P1dB)		15			14.5			13		dBm
Saturated (P_{SAT})		18			17.5			16		dBm
Output Third-Order Intercept (IP3)[2]		31			29			26		dBm
TOTAL SUPPLY CURRENT		70			70			70		mA

[1] Adjust V_{GG} between −2 V to 0 V to achieve I_{DD} = 70 mA typical.
[2] Measurement taken at P_{OUT}/tone = 8 dBm.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (V_{DD})	10 V
Drain Bias Voltage (RF Out/V_{DD})	7 V
RF Input Power	18 dBm
Gate Bias Voltage, V_{GG}	−2 V to +0.2 V
Channel Temperature	175°C
Continuous P_{DISS} (T = 85°C) (Derate 37.1 mW/°C Above 85°C)	3.34 W
Thermal Resistance (Channel to Ground Paddle)	26.9°C/W
Temperature	
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
ESD Sensitivity (HBM)	Class 1A

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 3. Typical Supply Current vs. V_{DD}

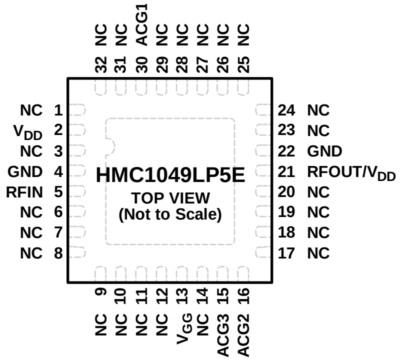
V_{DD} (V)	I_{DD}[1] (mA)
5	70
6	70
7	70

[1] Adjust V_{GG} to achieve I_{DD} = 70 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NC = NO CONNECT. THESE PINS ARE NOT CONNECTED INTERNALLY; HOWEVER, ALL DATA WAS MEASURED WITH THESE PINS CONNECTED TO RF/DC GROUND EXTERNALLY.
2. EXPOSED PAD. THE EXPOSED GROUND PADDLE MUST BE CONNECTED TO RF/DC GROUND.

Figure 2. Pin Configuration Diagram

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description[1]
1, 3, 6 to 12, 14, 17 to 20, 23 to 29, 31, 32	NC	No Connect. These pins are not connected internally; however, all data was measured with these pins connected to RF/dc ground externally (see the Typical Performance Characteristics section for data plots).
5	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω.
2	V_{DD}	Power Supply Voltage for the Amplifier. External bypass capacitors (100 pF and 0.01 µF) are required.
30	ACG1	Low Frequency Termination. An external bypass capacitor of 100 pF is required.
21	RFOUT/V_{DD}	RF Output/Alternate Power Supply Voltage for the Amplifier. An external bias tee is required when used as alternative V_{DD}. This pin is dc-coupled and matched to 50 Ω.
15, 16	ACG2, ACG3	Low Frequency Termination. External bypass capacitors of 100 pF are required.
13	V_{GG}	Gate Control for Amplifier. Adjust the voltage to achieve I_{DD} = 70 mA. External bypass capacitors of 100 pF, 0.01 µF, and 4.7µF are required.
4, 22	GND	Ground. Connect Pin 4 and Pin 22 to RF/dc ground.
0	EP	Exposed Pad. The exposed ground paddle must be connected to RF/dc ground.

[1] See the Interface Schematics section for pin interfaces.

INTERFACE SCHEMATICS

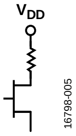


Figure 3. V_{DD} Interface

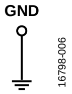


Figure 4. GND Interface

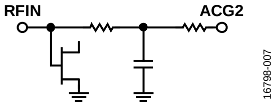


Figure 5. RFIN Interface

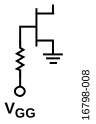


Figure 6. V_{GG} Interface

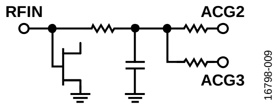


Figure 7. ACG2 and ACG3 Interface

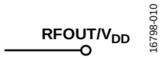


Figure 8. RFOUT/V_{DD} Interface

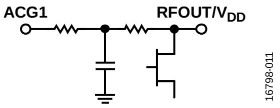


Figure 9. ACG1 Interface

TYPICAL PERFORMANCE CHARACTERISTICS

Data taken with V_{DD} applied to Pin 2, V_{DD} = 7 V.

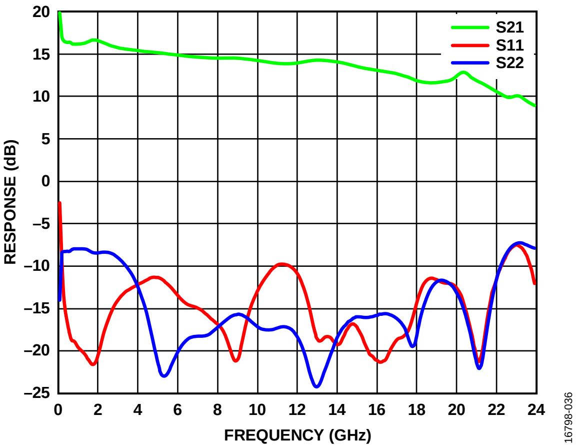


Figure 10. Broadband Gain and Return Loss

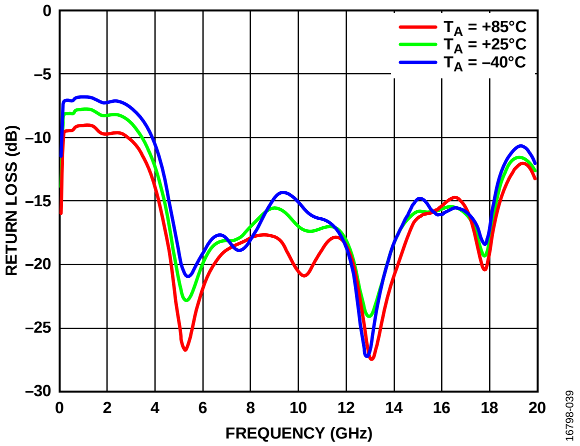


Figure 13. Output Return Loss vs. Temperature

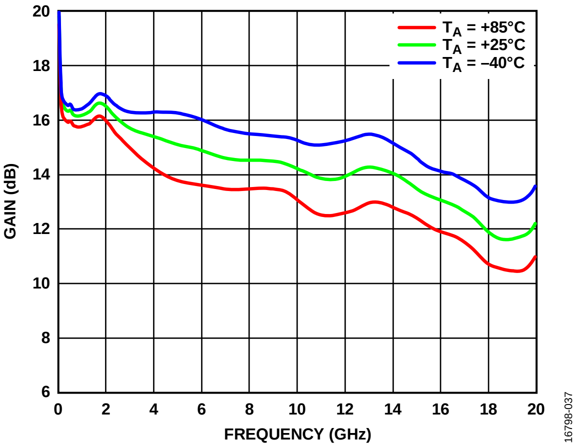


Figure 11. Gain vs. Temperature

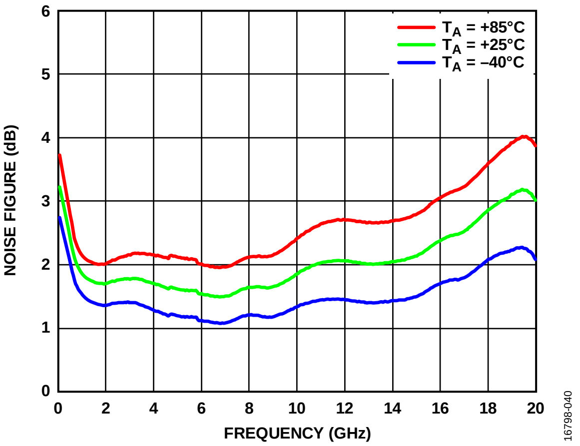


Figure 14. Noise Figure vs. Temperature

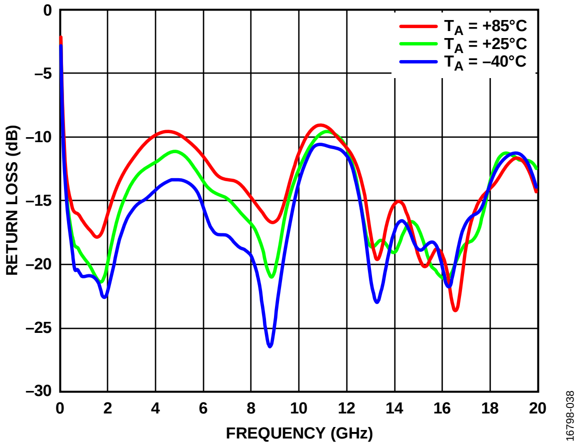


Figure 12. Input Return Loss vs. Temperature

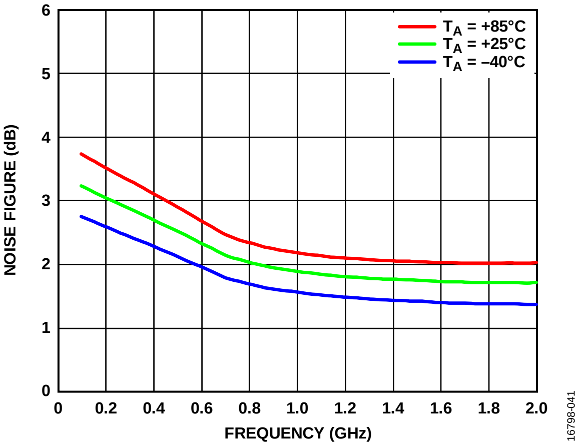


Figure 15. Noise Figure vs. Temperature, Low Frequency

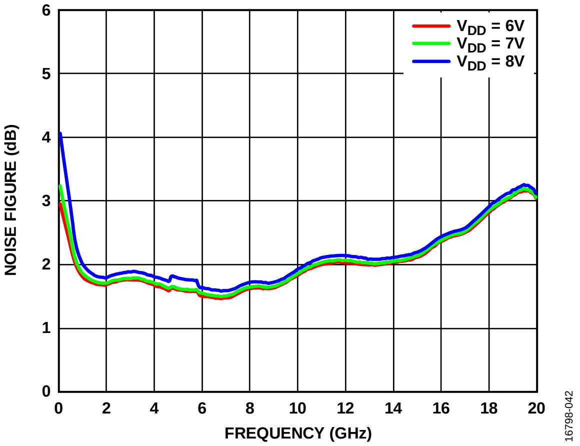


Figure 16. Noise Figure vs. V_{DD}

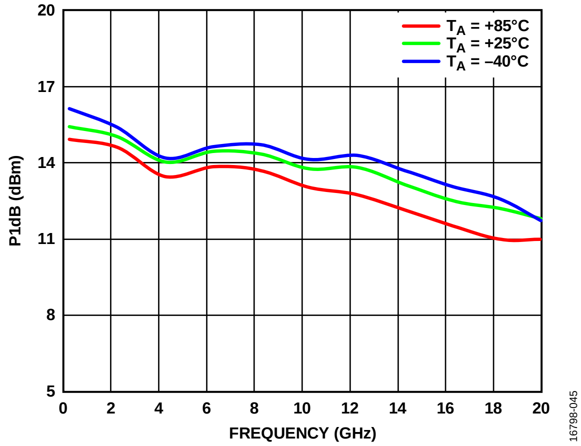


Figure 19. P1dB vs. Temperature

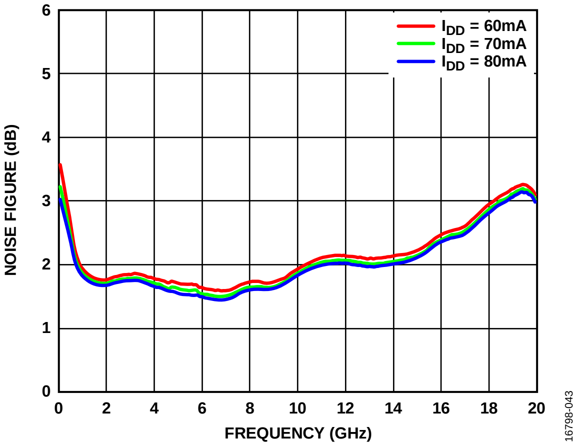


Figure 17. Noise Figure vs. I_{DD}

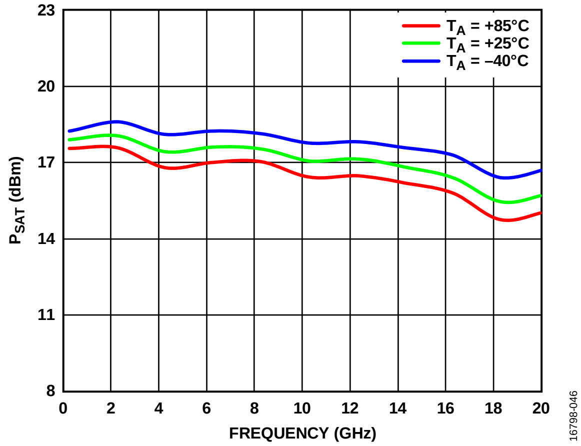


Figure 20. P_{SAT} vs. Temperature

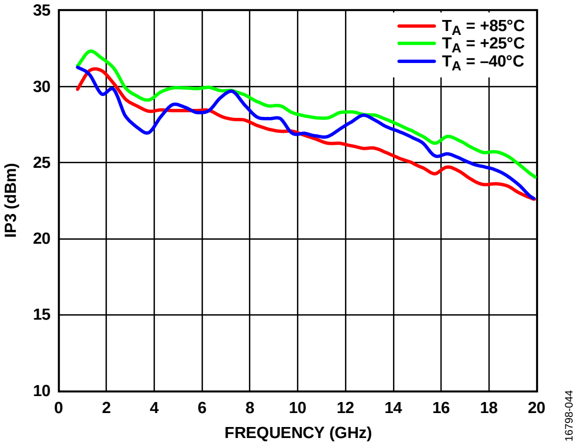


Figure 18. Output IP3 vs. Temperature

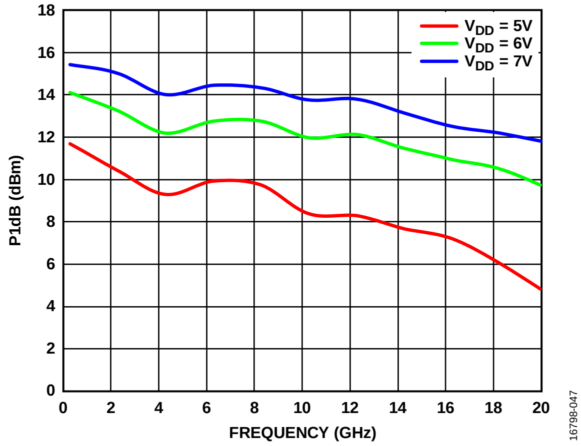


Figure 21. P1dB vs. V_{DD}

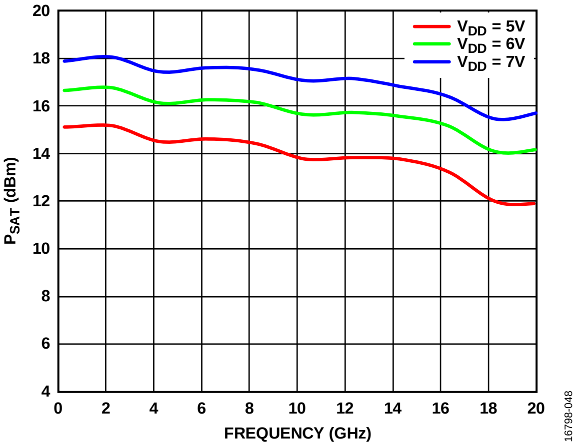


Figure 22. P_{SAT} vs. V_{DD}

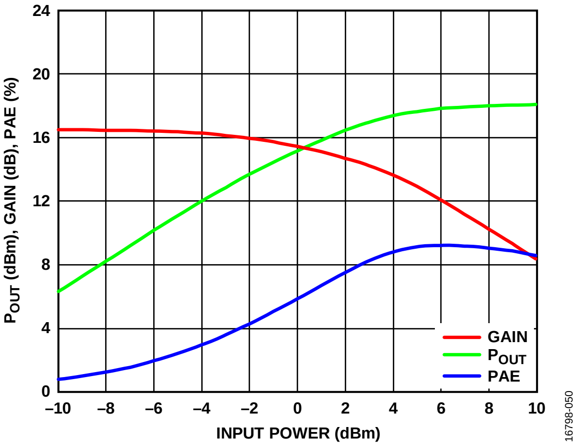


Figure 24. Power Compression at 2 GHz

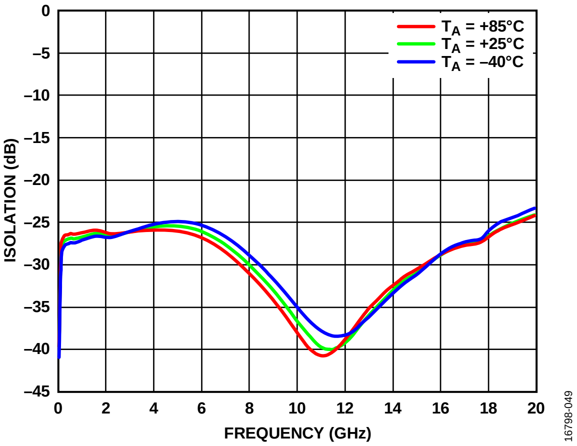


Figure 23. Reverse Isolation vs. Temperature

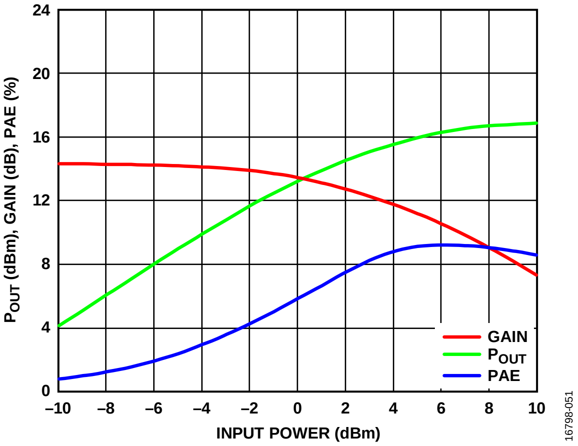


Figure 25. Power Compression at 10 GHz

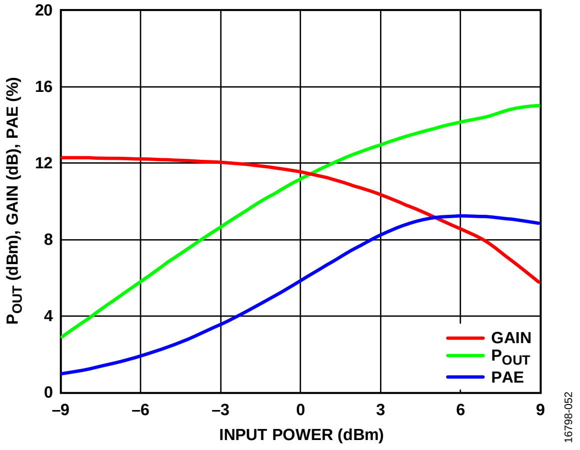


Figure 26. Power Compression at 18 GHz

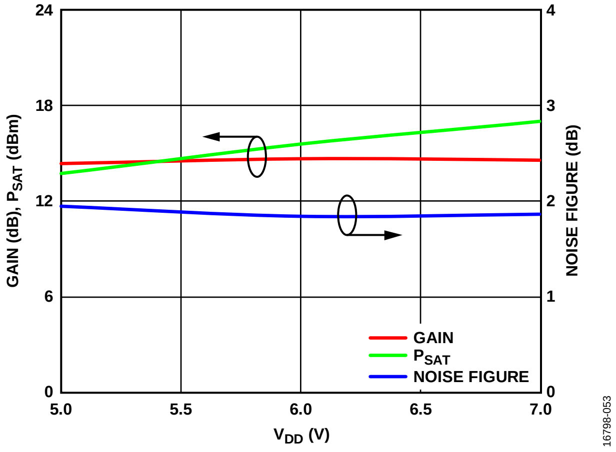


Figure 27. Gain, P_{SAT}, and Noise Figure vs. V_{DD} at 12 GHz

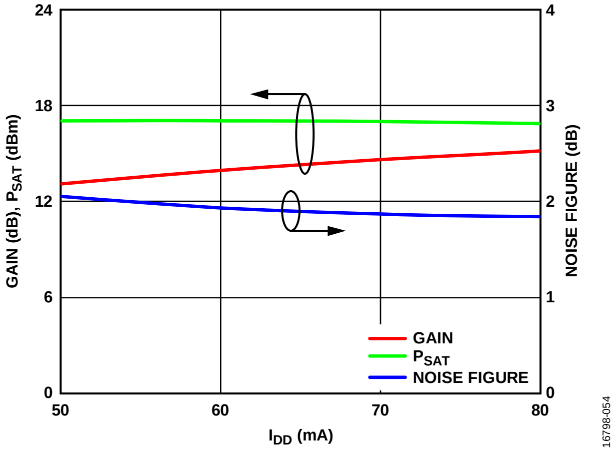


Figure 28. Gain, P_{SAT}, and Noise Figure vs. I_{DD} at 12 GHz

Data taken with V_{DD} applied to the bias tee at Pin 21.

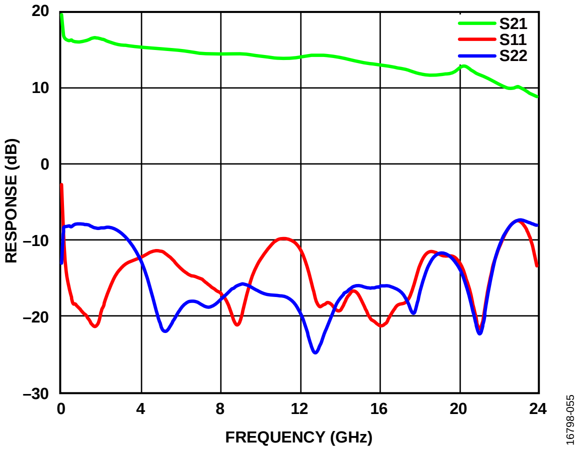


Figure 29. Broadband Gain and Return Loss, V_{DD} = 4 V, Supply to Bias Tee

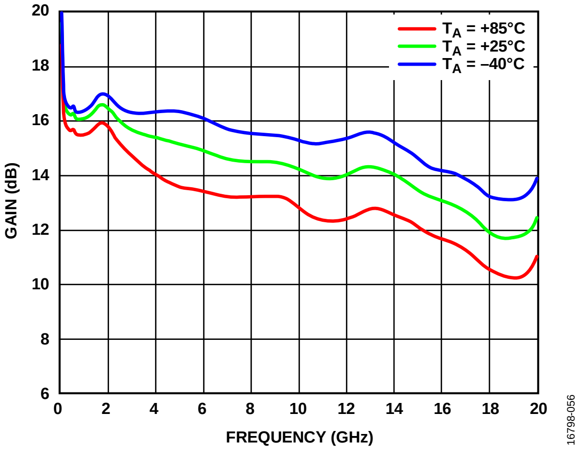


Figure 30. Gain vs. Temperature, V_{DD} = 4 V, Supply to Bias Tee

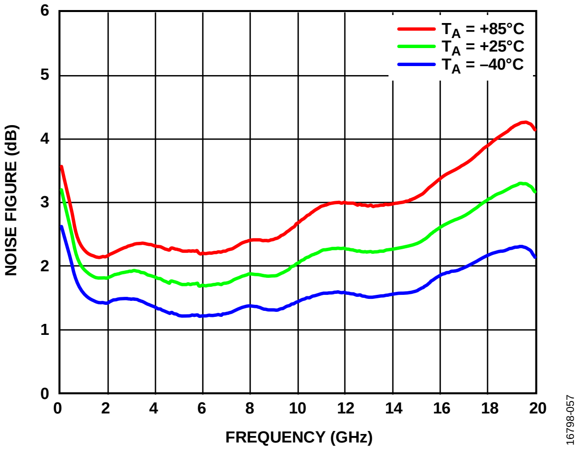


Figure 31. Noise Figure vs. Temperature, V_{DD} = 4 V, Supply to Bias Tee

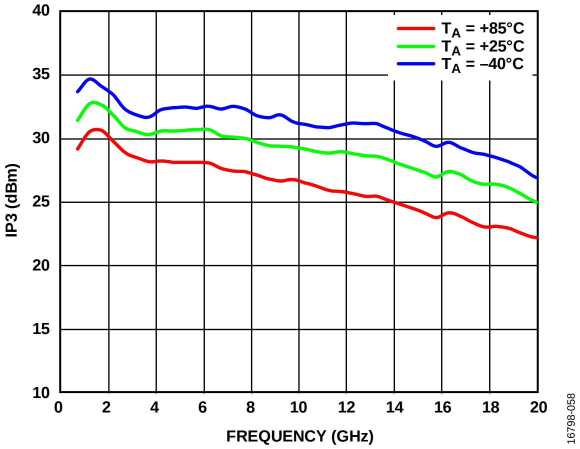


Figure 32. Output IP3 vs. Temperature, V_{DD} = 4 V, Supply to Bias Tee

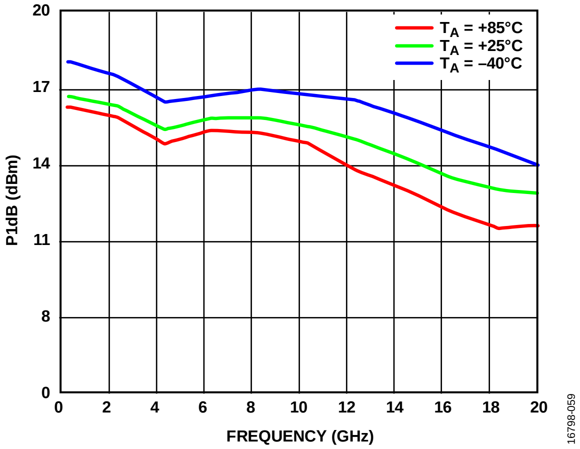


Figure 33. P1dB vs. Temperature, V_{DD} = 4 V, Supply to Bias Tee

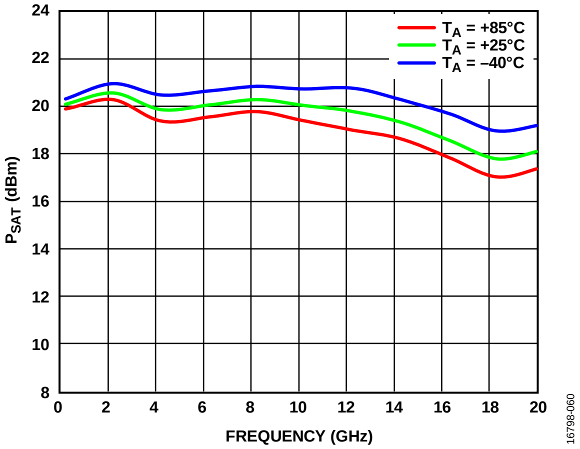


Figure 34. P_{SAT} vs. Temperature, V_{DD} = 4 V, Supply to Bias Tee

EVALUATION PRINTED CIRCUIT BOARD

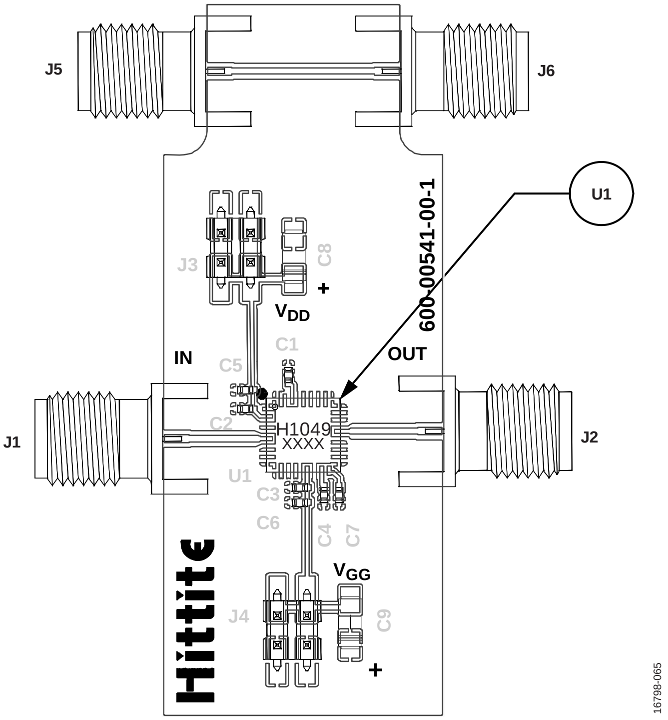


Figure 35. Evaluation Board Layout

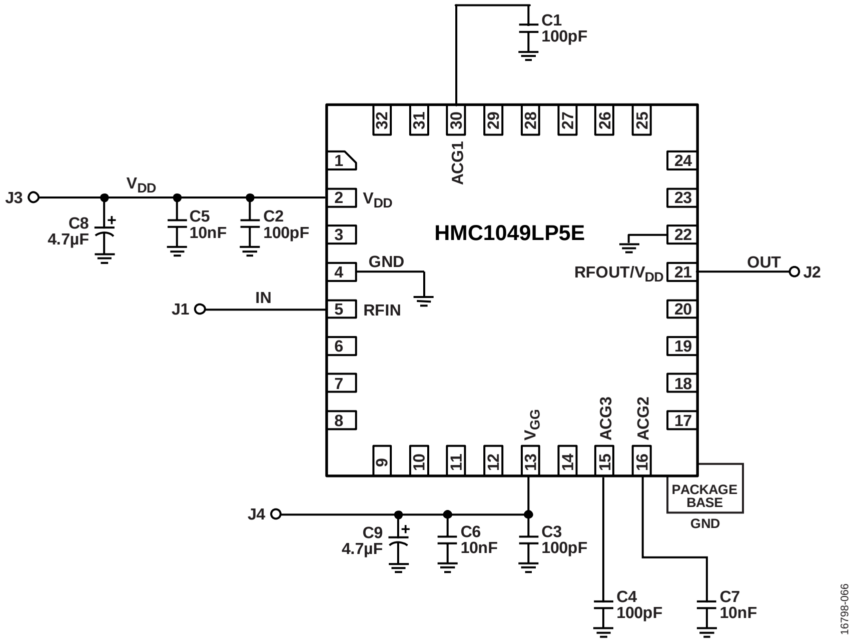


Figure 36. Evaluation Board Schematic

Table 5. List of Materials for Evaluation PCB

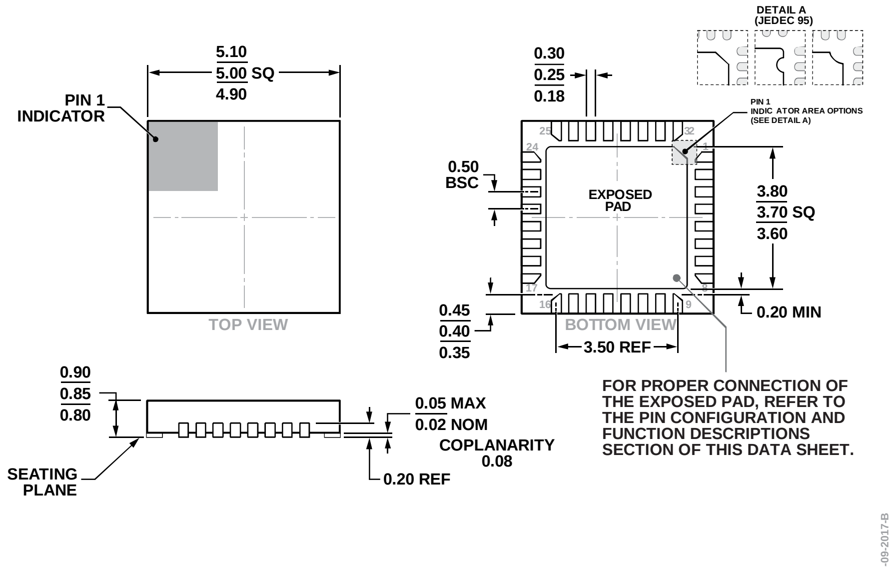
Item	Description
J1, J2, J5, J6	PCB mount SMA RF connector
J3, J4	DC pins
C1 to C4	100 pF capacitor, 0402 package
C5 to C7	10000 pF capacitor, 0402 package
C8, C9	4.7 µF capacitor, tantalum
U1	HMC1049LP5E
PCB[1]	600-00541-00-1 evaluation PCB

[1] Circuit board material: Rogers 4350 or Arlon 25FR.

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ω impedance; connect the package ground leads and exposed paddle directly to the ground plane. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices, Inc., upon request.

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-4.

Figure 37. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm and 0.85 mm Package Height
(HCP-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Lead Finish	Moisture Sensitivity Level (MSL) Rating[2]	Package Description	Ordering Quantity	Package Option
HMC1049LP5E	−40°C to +85°C	100% matte Sn	MSL1	32-Lead LFCSP		HCP-32-1
HMC1049LP5ETR	−40°C to +85°C	100% matte Sn	MSL1	32-Lead LFCSP, 7″Tape and Reel	500	HCP-32-1
EVAL01-HMC1049LP5				Evaluation Board		

[1] All models are RoHS Compliant Parts.
[2] MSL1 rating indicates a maximum peak reflow temperature of 260°C.