CY62128BN
MoBL®
1-Mbit (128K x 8) Static RAM

Features

- **Temperature Ranges**
  - **— Commercial: 0°C to 70°C**
  - **— Industrial: –40°C to 85°C**
  - **— Automotive-A: –40°C to 85°C**
  - **— Automotive-E: –40°C to 125°C**
- **4.5V–5.5V operation**
- **CMOS for optimum speed/power**
- **Low active power (70 ns Commercial, Industrial, Automotive-A)**
  - **— 82.5 mW (max.) (15 mA)**
- **Low standby power (55/70 ns Commercial, Industrial, Automotive-A)**
  - **— 110 µW (max.) (15 µA)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE_1}$, CE_2, and $\overline{OE}$ options**
- **Available in Pb-free and non-Pb-free 32-pin (450 mil-wide) SOIC, 32-pin STSOP and 32-pin TSOP-I**

Functional Description[1]

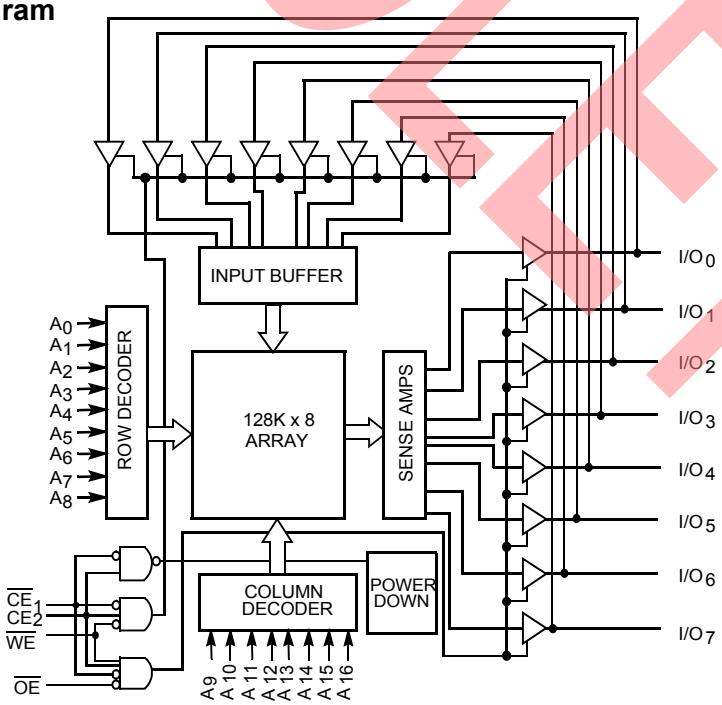
The CY62128BN is a high-performance CMOS static RAM organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE_1}$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking Chip Enable One ($\overline{CE_1}$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable Two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable One ($\overline{CE_1}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

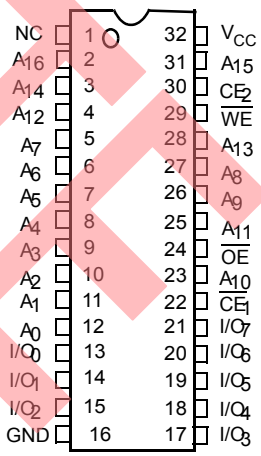
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE_1}$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE_1}$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

Logic Block Diagram



Pin Configuration

Top View
SOIC

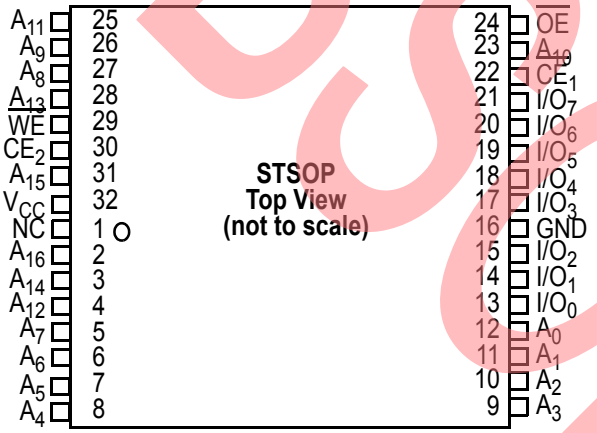


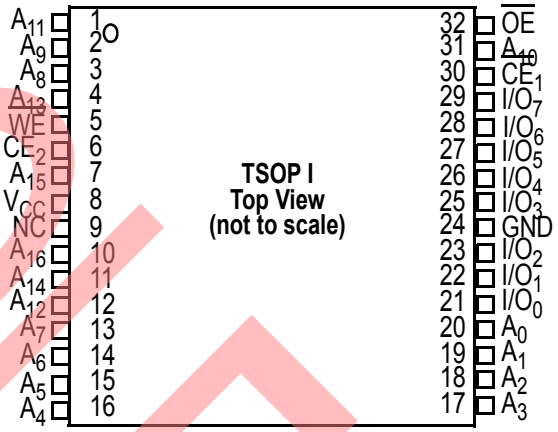
Note:
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Product Portfolio

Product		V_{CC} Range (V)			Speed (ns)	Power Dissipation			
						Operating, I_{CC} (mA)		Standby, I_{SB2} (µA)	
		Min.	Typ.[2]	Max.		Typ.[2]	Max.	Typ.[2]	Max.
CY62128BNLL	Commercial	4.5	5.0	5.5	55	7.5	20	2.5	15
					70	6	15	2.5	15
	Industrial				55	7.5	20	2.5	15
					70	6	15	2.5	15
	Automotive-A				70	6	15	2.5	15
	Automotive-E				70	6	25	2.5	25

Pin Configurations





Pin Definitions

Input	**A_0–A_{16}**. Address Inputs
Input/Output	**I/O_0–I/O_7**. Data lines. Used as input or output lines depending on operation
Input/Control	**$\overline{WE}$**. Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/Control	**$\overline{CE_1}$**. Chip Enable 1, Active LOW.
Input/Control	**CE_2**. Chip Enable 2, Active HIGH.
Input/Control	**$\overline{OE}$**. Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
Ground	**GND**. Ground for the device
Power Supply	**V_{CC}**. Power supply for the device

Note:
2. Typical values are included for reference only and are not tested or guaranteed. Typical values are an average of the distribution across normal production variations as measured at V_{CC} = 5.0V, T_A = 25°C, and t_{AA} = 70 ns.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[3] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[3].....–0.5V to V_{CC} + 0.5V

DC Input Voltage[3].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW).....20 mA

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Operating Range

Range	Ambient Temperature (T_A)[4]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	
Automotive-A	–40°C to +85°C	
Automotive-E	–40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-55 Min.	-55 Typ.[2]	-55 Max.	-70 Min.	-70 Typ.[2]	-70 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[3]			–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Commercial/ Industrial	–1		+1	–1		+1	µA
			Automotive-A				–1		+1	µA
			Automotive-E				–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	Commercial/ Industrial	–1		+1	–1		+1	µA
			Automotive-A				–1		+1	µA
			Automotive-E				–10		+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Commercial/ Industrial		7.5	20		6	15	mA
			Automotive-A					6	15	mA
			Automotive-E					6	25	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE_1}$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Commercial/ Industrial		0.1	2		0.1	1	mA
			Automotive-A					0.1	1	mA
			Automotive-E					0.1	2	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, CE_1 ≥ V_{CC} – 0.3V, or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Commercial/ Industrial		2.5	15		2.5	15	µA
			Automotive-A					2.5	15	µA
			Automotive-E					2.5	25	µA

Notes:
3. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
4. T_A is the "Instant On" case temperature.

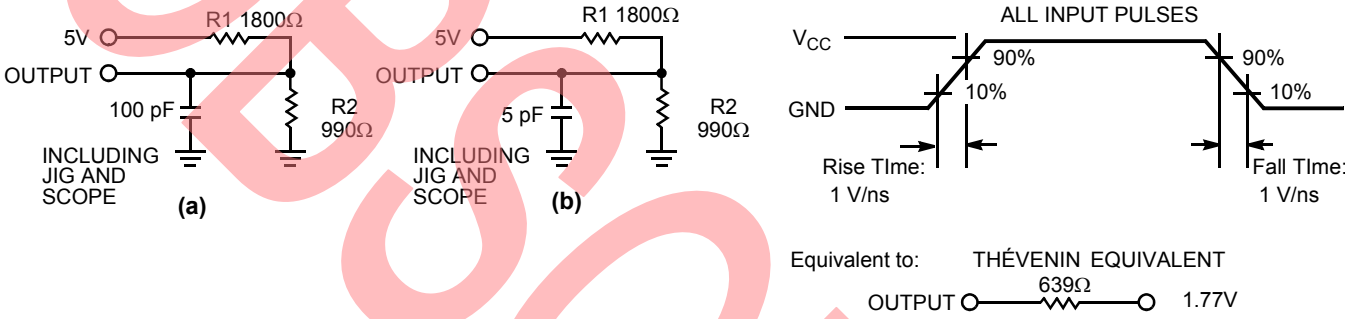
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9	pF
C_{OUT}	Output Capacitance		9	pF

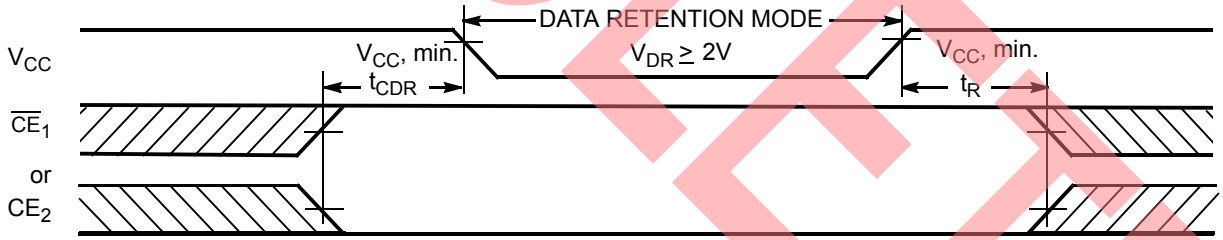
Thermal Resistance[5]

Parameter	Description	Test Conditions	32 SOIC	32 STSOP	32 TSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	66.17	105.14	97.44	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		30.87	14.09	26.05	°C/W

AC Test Loads and Waveforms



Data Retention Waveform



Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[6]		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0			V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE}_1 \geq V_{CC} - 0.3V$, or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$	Commercial/ Industrial Automotive-A		1.5	15	µA
			Automotive-E		1.5	25	µA
t_{CDR}	Chip Deselect to Data Retention Time			0			ns
t_R	Operation Recovery Time			70			ns

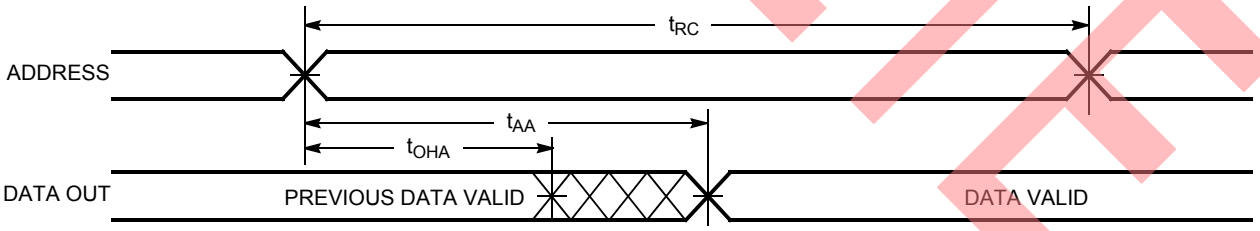
Note:
5. Tested initially and after any design or process changes that may affect these parameters.
6. No input may exceed V_{CC} + 0.5V.

Switching Characteristics[7] Over the Operating Range

Parameter	Description	CY62128BN-55		CY62128BN-70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 9]		20		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[9]	5		5		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[8, 9]		20		25	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-up, CE_2 HIGH to Power-up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-down, CE_2 LOW to Power-down		55		70	ns
WRITE CYCLE[10]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	45		50		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		20		25	ns

Switching Waveforms

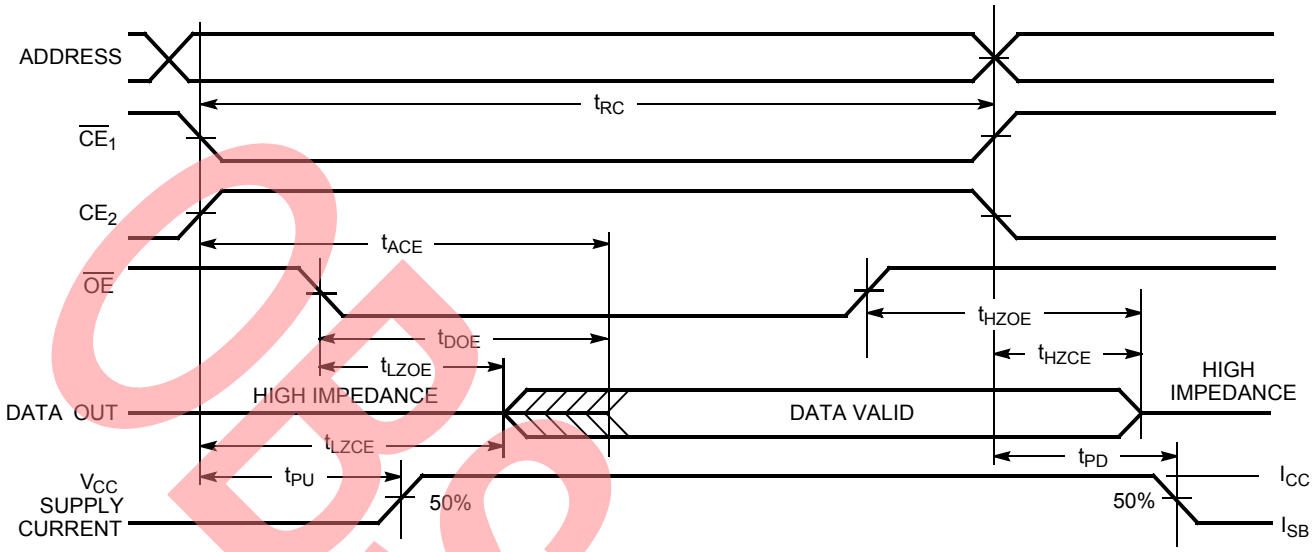
Read Cycle No.1[11, 12]



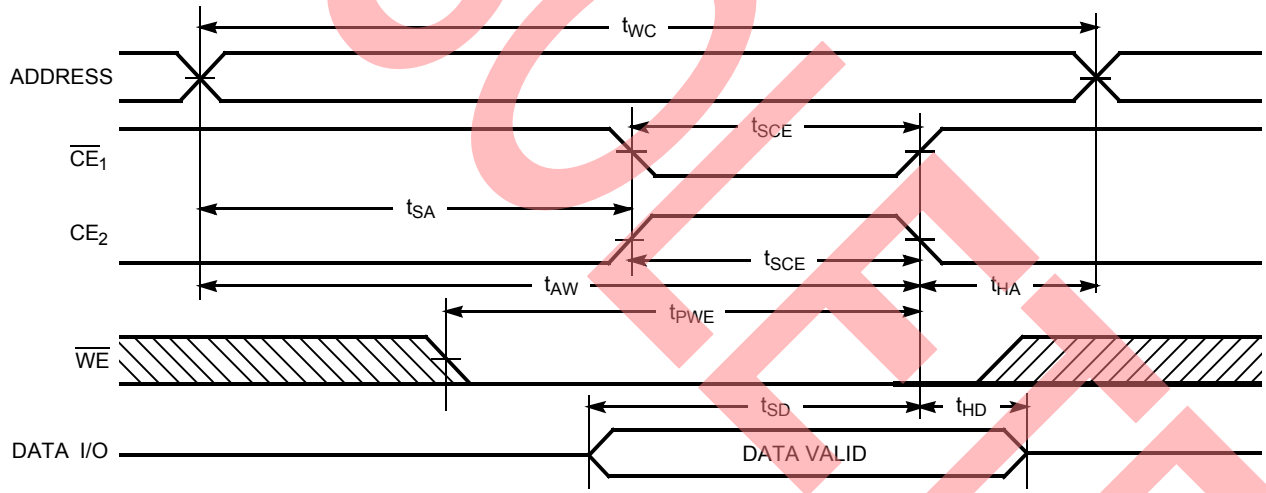
Notes:
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
12. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]



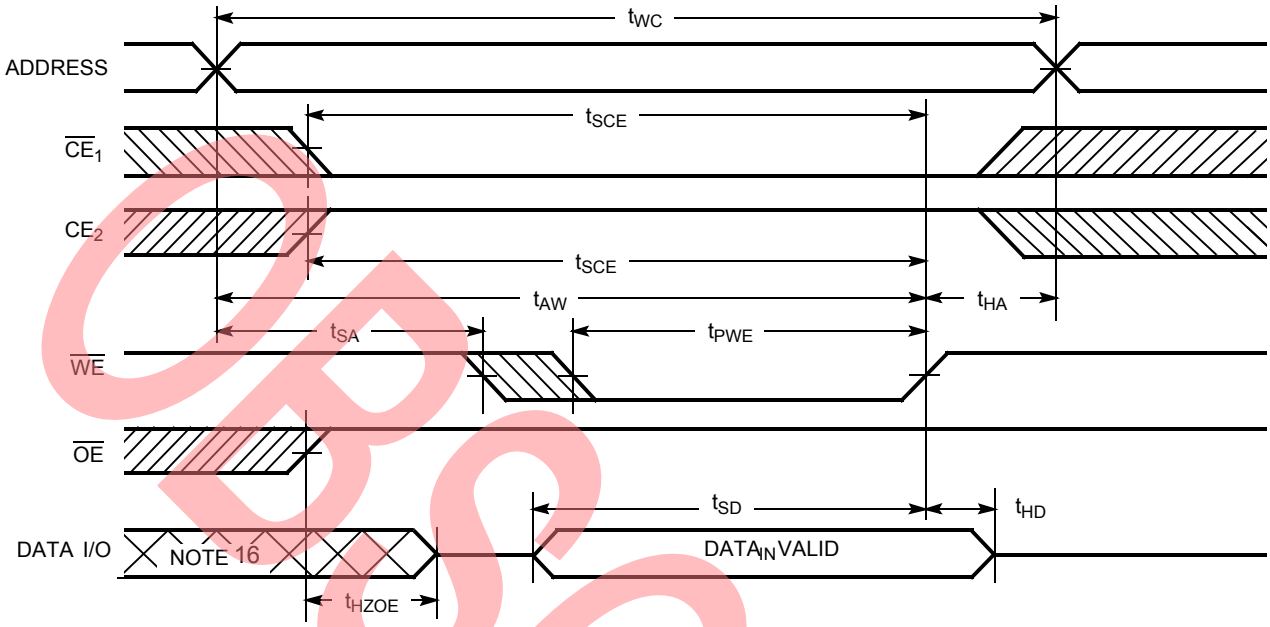
Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[14, 15]



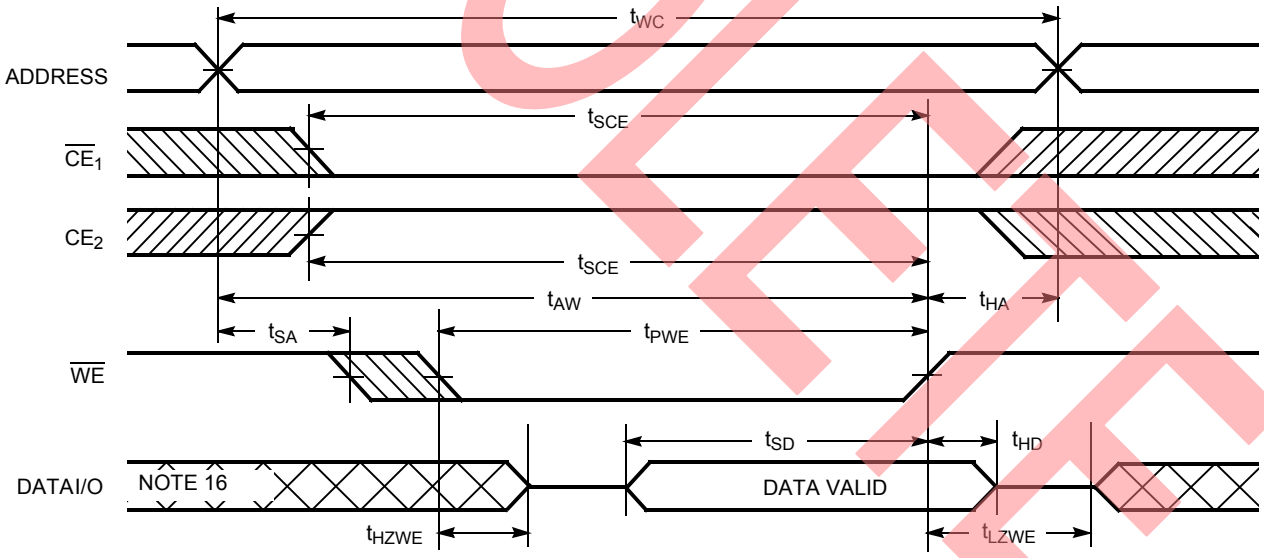
Notes:
13. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 (WE Controlled, OE HIGH During Write)[14, 15]



Write Cycle No.3 (WE Controlled, OE LOW)[14, 15]



Note:
16. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

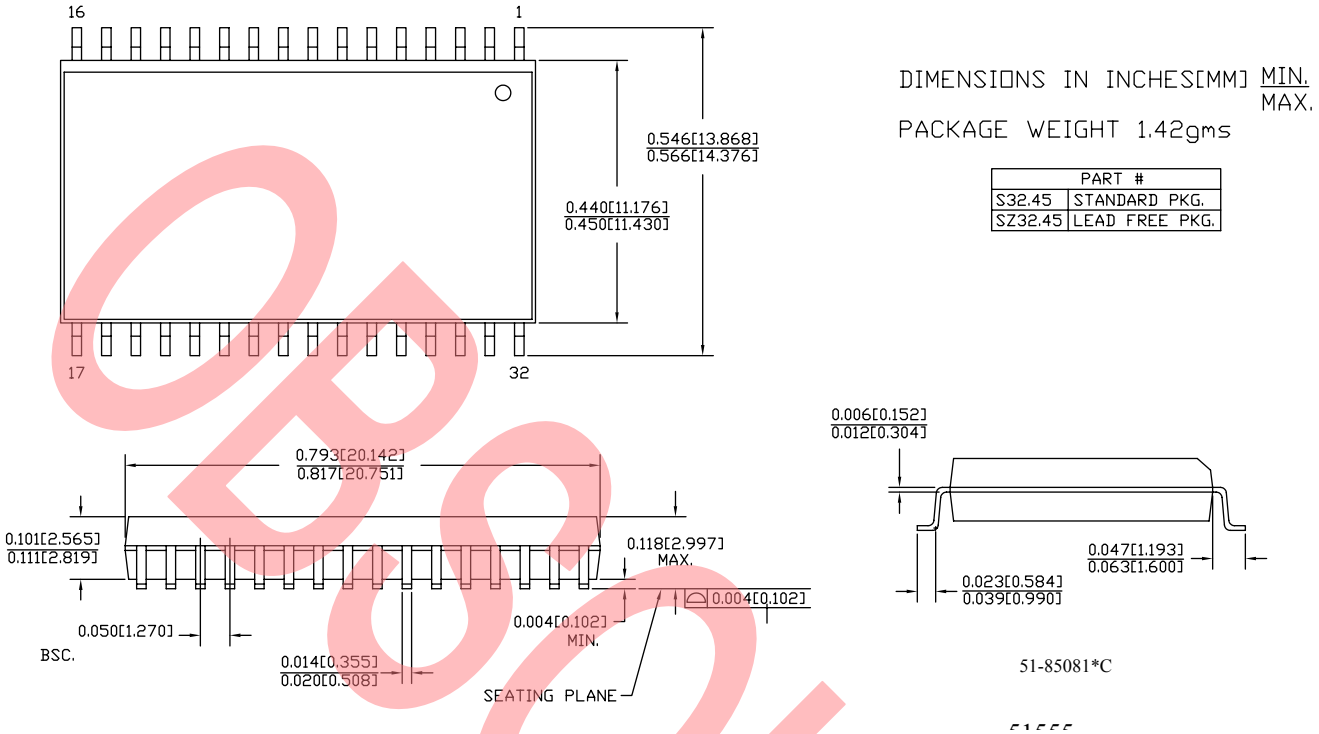
$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I_{SB})
X	L	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

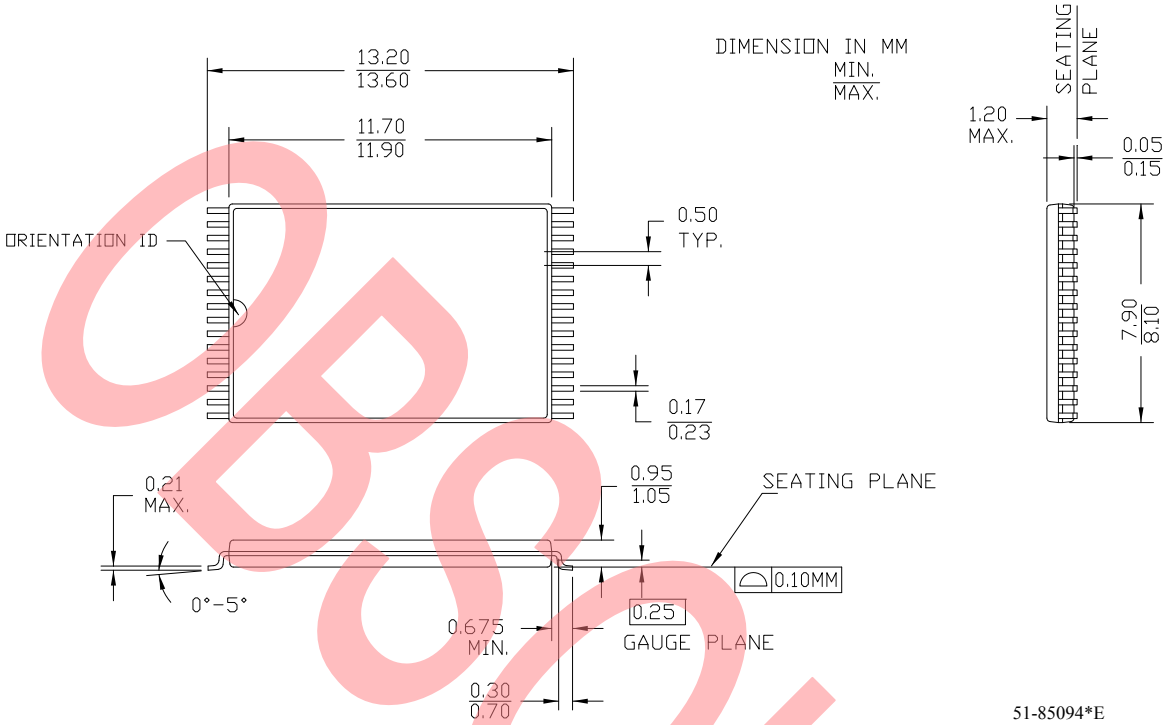
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62128BNLL-55SXI	51-85081	32-pin 450-Mil SOIC (Pb-Free)	Commercial
	CY62128BNLL-55ZXI	51-85056	32-pin TSOP Type I (Pb-Free)	Industrial
70	CY62128BNLL-70SXA	51-85081	32-pin 450-Mil SOIC (Pb-Free)	Automotive-A

Please contact your local Cypress sales representative for availability of these parts

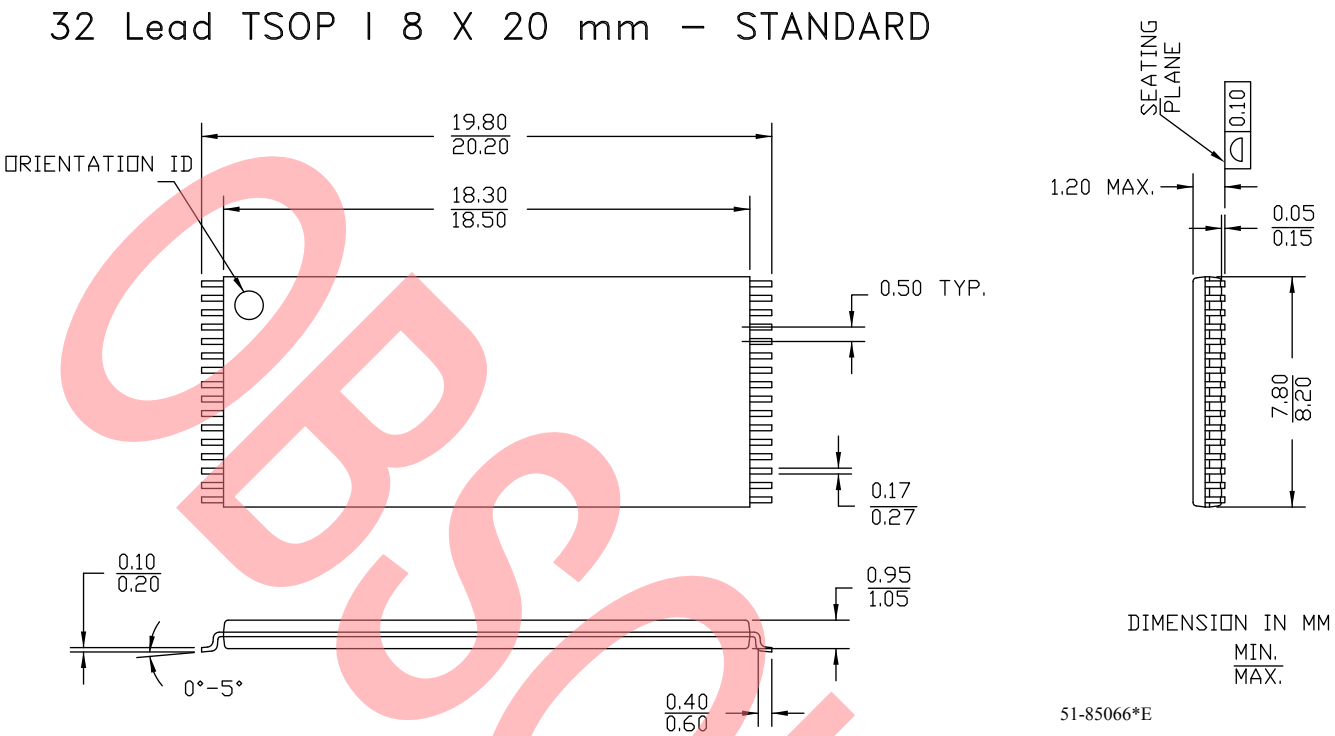
Package Diagrams



Package Diagrams (continued)



Package Diagrams (continued)



Document History Page

Document Title: CY62128BN MoBL® 1-Mbit (128K x 8) Static RAM Document Number: 001-06498				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	426503	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Removed RTSOP Package Updated ordering Information table
*B	2898985	03/25/2010	AJU	Removed inactive parts from Ordering Information table. Updated package diagram.
*C	3090906	11/19/2010	RAME	All specified parts in the ordering information table are being pruned.