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## Description

The AUIRS2004S is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive N-channel power MOSFET or IGBT in the high side configuration which operates from 10V to 200 volts.

## Qualification Information<sup>†</sup>

<b>Qualification Level</b>		Automotive (per AEC-Q100 <sup>††</sup> )
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.
<b>Moisture Sensitivity Level</b>		MSL3 <sup>†††</sup> 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M2 (+/-200V) (per AEC-Q100-003)
	Human Body Model	Class H1C (+/-2000V) (per AEC-Q100-002)
	Charged Device Model	Class C4 (+/-1000V) (per AEC-Q100-011)
<b>IC Latch-Up Test</b>		Class II, Level B <sup>††††</sup> (per AEC-Q100-004)
<b>RoHS Compliant</b>		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

†††† LIN and HIN stressed to +/-20mA

### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which permanent damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the “Recommended Operating Condition” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_B$	High Side Floating Supply Voltage	-0.3	225	V
$V_S$	High Side Floating Offset Voltage	$V_B - 20$	$V_B + 0.3$	
$V_{HO}$	High Side Floating Output Voltage	$V_S - 0.3$	$V_B + 0.3$	
$V_{CC}$	Low Side and Logic Fixed Supply Voltage	-0.3	25	
$V_{LO}$	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$	
$V_{IN}$	Logic Input Voltage ( $IN, \overline{SD}$ )	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
$dV_S/dt$	Allowable Offset Supply Voltage Transient	—	50	V/ns
$P_D$	Package Power Dissipation @ $T_A \leq +25\text{ }^{\circ}\text{C}$	—	0.625	W
$R_{thJA}$	Thermal Resistance, Junction to Ambient	—	200	$^{\circ}\text{C/W}$
$T_J$	Junction Temperature	—	150	$^{\circ}\text{C}$
$T_S$	Storage Temperature	-55	150	
$T_L$	Lead Temperature (soldering, 10 seconds)	—	300	

### Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltage referenced to COM. The  $V_S$  offset rating is tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
$V_B$	High Side Floating Supply Voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	Static High side floating offset voltage	Note1	200	
$V_{HO}$	High Side Floating Output Voltage	$V_S$	$V_B$	
$V_{CC}$	Low Side and Logic Fixed Supply Voltage	10	20	
$V_{LO}$	Low Side Output Voltage	0	$V_{CC}$	
$V_{IN}$	Logic Input Voltage ( $IN$ & $\overline{SD}$ )	0	$V_{CC}$	
$T_A$	Ambient temperature	-40	125	$^{\circ}\text{C}$

**Note 1:** Logic operational for  $V_S$  of -5 V to +200 V. Logic state held for  $V_S$  of -5 V to  $-V_{BS}$ .

## Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $V_{\text{BIAS}}$  ( $V_{\text{CC}}, V_{\text{BS}}$ ) = 15 V,  $C_L = 1000 \text{ pF}$ .

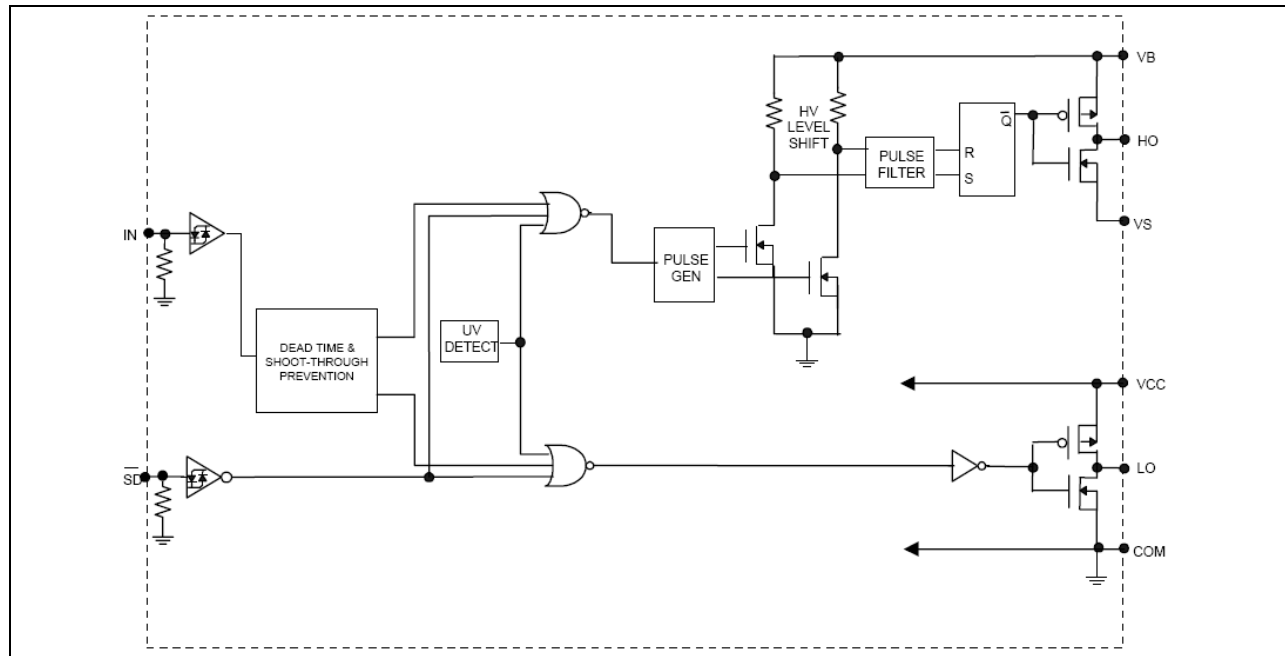
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{\text{on}}$	Turn-on propagation delay	--	680	880	ns	$V_S = 0 \text{ V}$
$t_{\text{off}}$	Turn-off propagation delay	--	150	220		$V_S = 200 \text{ V}$
$t_r$	Turn-on rise time	—	160	220		
$t_f$	Turn-off fall time	—	70	170		
$DT_{25}$	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		$T_j = 25^{\circ}\text{C}$
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	---	800		
$MT_{25}$	Delay matching HS & LS turn-on/off	—	—	80		$T_j = 25^{\circ}\text{C}$
MT	Delay matching HS & LS turn-on/off	—	—	150		

## Static Electrical Characteristics

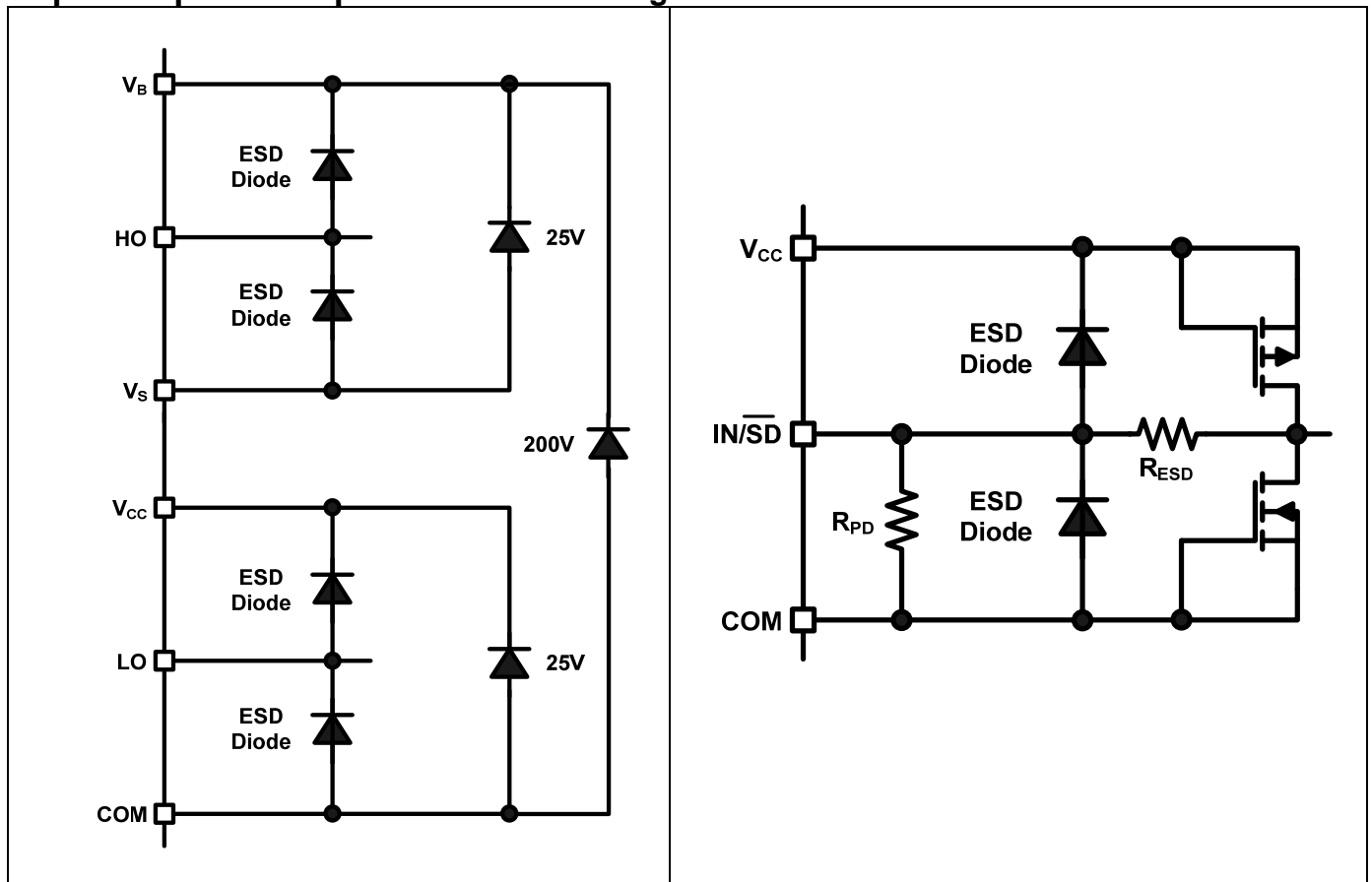
Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $V_{\text{BIAS}}$  ( $V_{\text{CC}}, V_{\text{BS}}$ ) = 15 V. The  $V_{\text{IN}}$ ,  $V_{\text{TH}}$  and  $I_{\text{IN}}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{\text{IH}}$	Logic "1" (HO) & Logic "0" (LO) input Voltage	2.5	—	--	V	$V_{\text{CC}} = 10 \text{ V to } 20 \text{ V}$
$V_{\text{IL}}$	Logic "0" (HO) & Logic "1" (LO) input Voltage	---	—	0.8		
$V_{\text{SD,TH+}}$	SD Input Positive Going Threshold	2.5	---	---		
$V_{\text{SD,TH-}}$	SD Input Negative Going Threshold	---	---	0.8		
$V_{\text{OH}}$	High Level Output Voltage, $V_{\text{BIAS}} - V_O$	—	0.05	0.2	$\mu\text{A}$	$I_O = 2 \text{ mA}$
$V_{\text{OL}}$	Low Level Output Voltage, $V_O$	—	0.02	0.1		
$I_{\text{LK}}$	Offset Supply Leakage Current	—	—	50		$V_B = V_S = 200 \text{ V}$
$I_{\text{QBS}}$	Quiescent $V_{\text{BS}}$ Supply Current	—	30	55		$V_{\text{IN}} = 0 \text{ V or } 5 \text{ V}$
$I_{\text{QCC}}$	Quiescent $V_{\text{CC}}$ Supply Current	—	150	270		$V_{\text{IN}} = 5 \text{ V}$
$I_{\text{IN+}}$	Logic "1" Input Bias Current	---	3	10		$V_{\text{IN}} = 0 \text{ V}$
$I_{\text{IN-}}$	Logic "0" Input Bias Current	---	---	5		SD pin = 5 V
$I_{\text{SD+}}$	Bias Current at SD pin, shut down disabled	---	3	10		SD pin = 0 V
$I_{\text{SD-}}$	Bias Current at SD pin, shut down enabled	---	---	5		
$V_{\text{CCUV+}}$	$V_{\text{CC}}$ Supply Undervoltage Positive going Threshold	8	8.9	9.8	V	
$V_{\text{CCUV-}}$	$V_{\text{CC}}$ Supply Undervoltage Negative Going Threshold	7.4	8.2	9		
$I_{\text{O+}}$	Output High Short Circuit Pulsed Current	130	290	---	mA	$V_O = 0 \text{ V},$ $PW \leq 10 \mu\text{s}$
$I_{\text{O-}}$	Output Low Short Circuit Pulsed Current	270	600	---		$V_O = 15 \text{ V},$ $PW \leq 10 \mu\text{s}$

## Functional Block Diagram



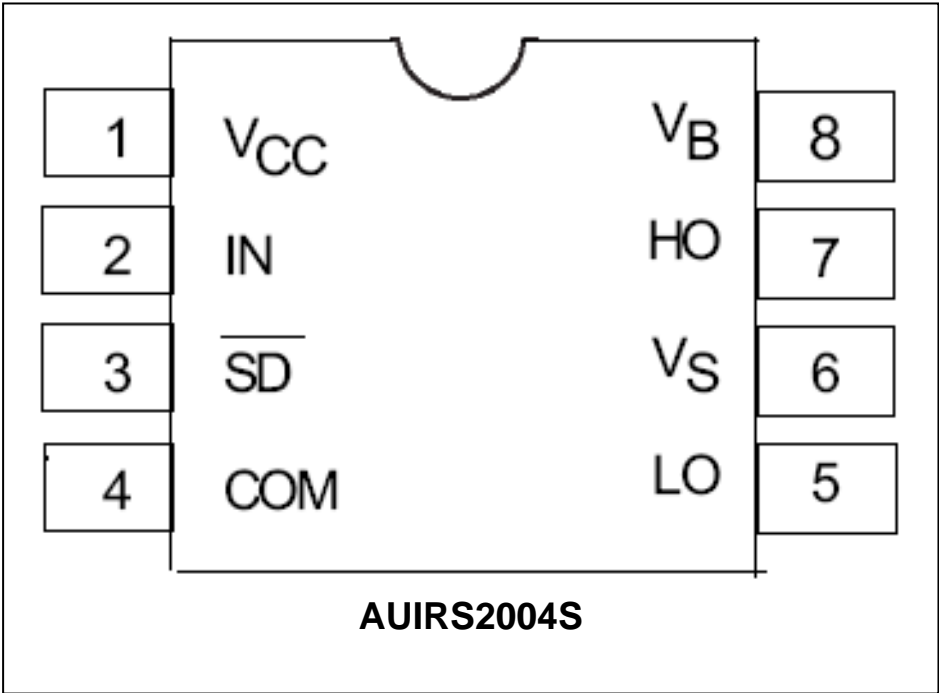
## Input/Output Pin Equivalent Circuit Diagrams: AUIRS2004



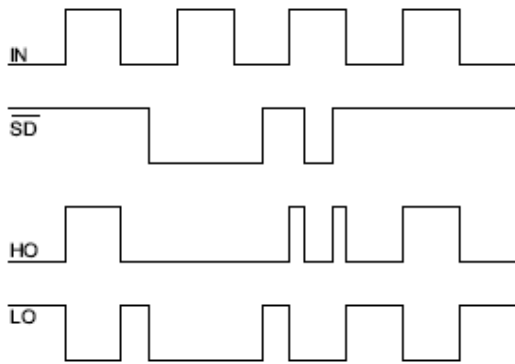
**Lead Definitions**

Symbol	Description
IN	Logic input for high side and low side gate driver outputs (HO and LO), in phase with HO
SD	Logic input for shutdown
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

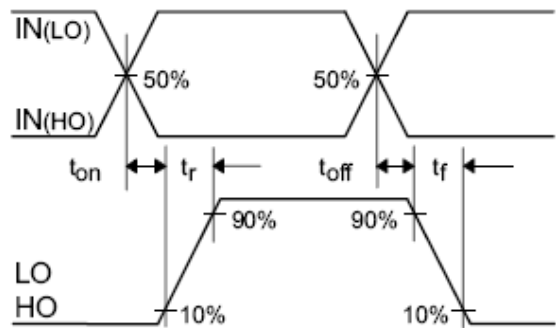
**Lead Assignments**



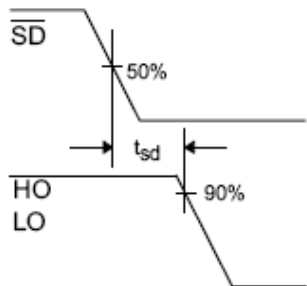
**Application Information and Additional Details**



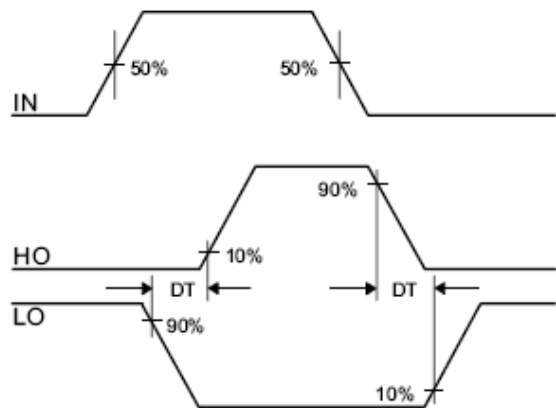
**Figure 1: Input/Output Timing Diagram**



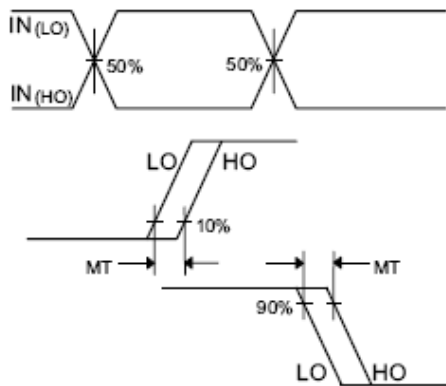
**Figure 2: Switching Time Waveform Definitions**



**Figure3: Shutdown Waveform Definitions**



**Figure 4: Deadtime Waveform Definitions**



**Figure 5: Delay Matching Waveform Definitions**



## Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS2004S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

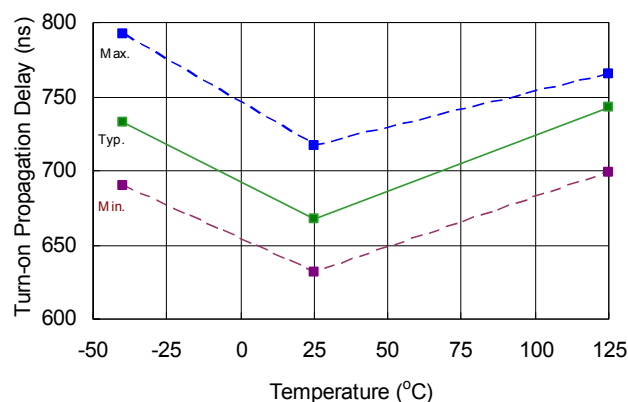


Figure 6:  $T_{ON}$  vs. temperature

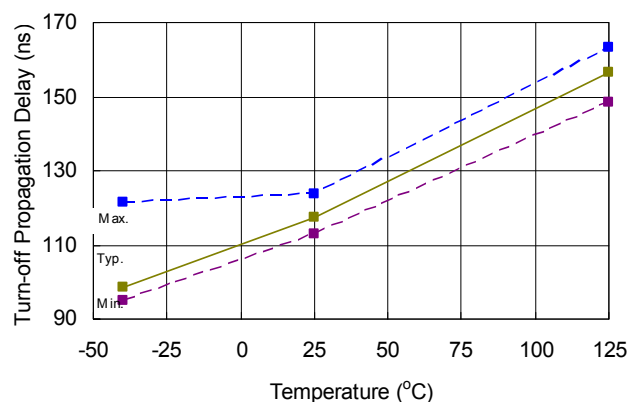


Figure 7:  $T_{OFF}$  vs. temperature

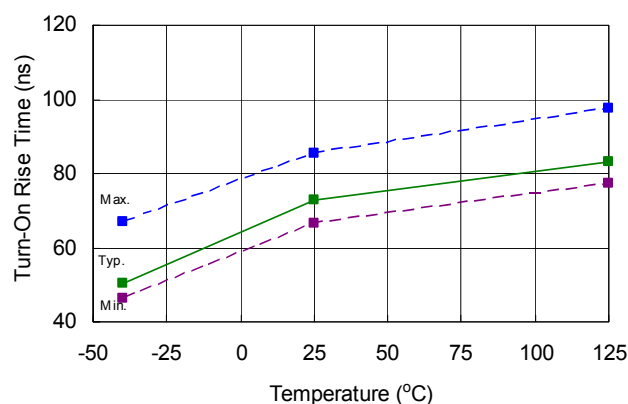


Figure 8:  $T_R$  vs. temperature

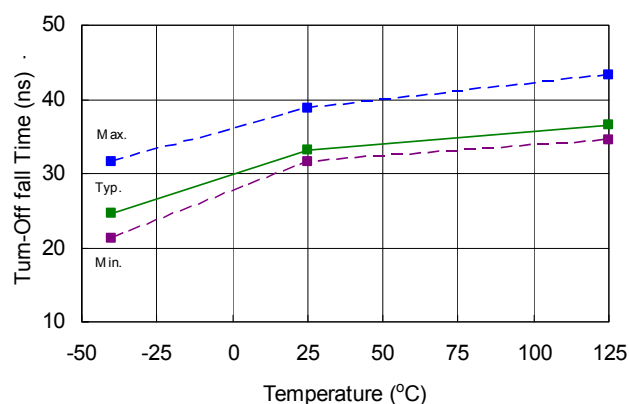
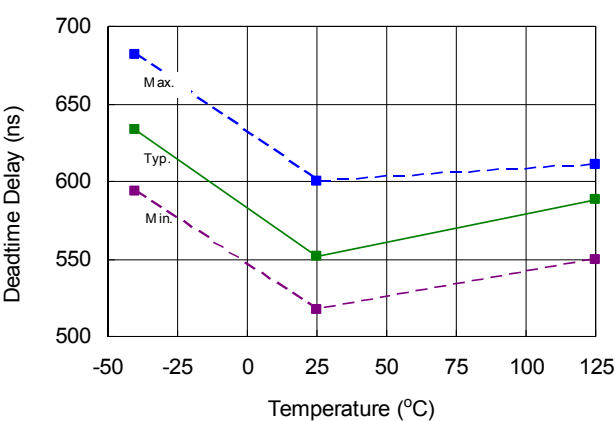
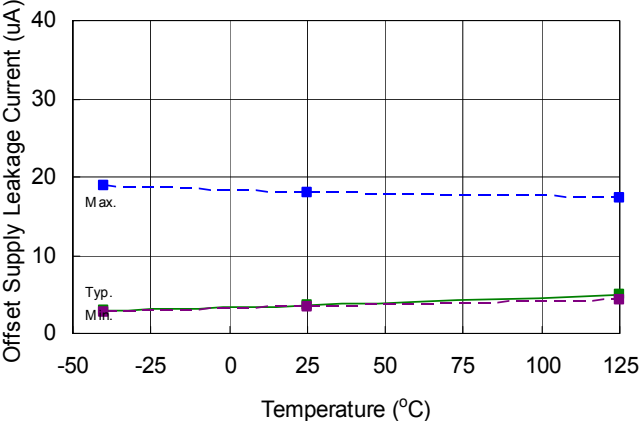


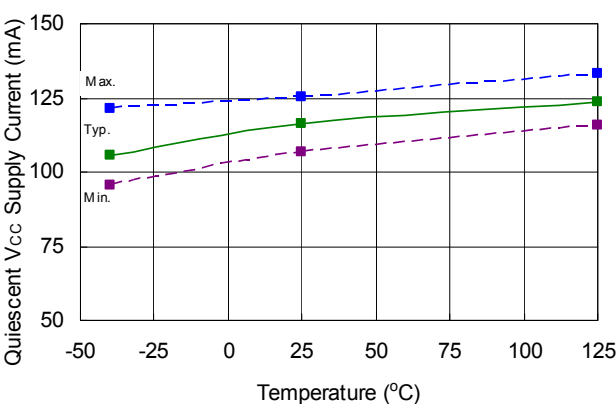
Figure 9:  $T_F$  vs. temperature



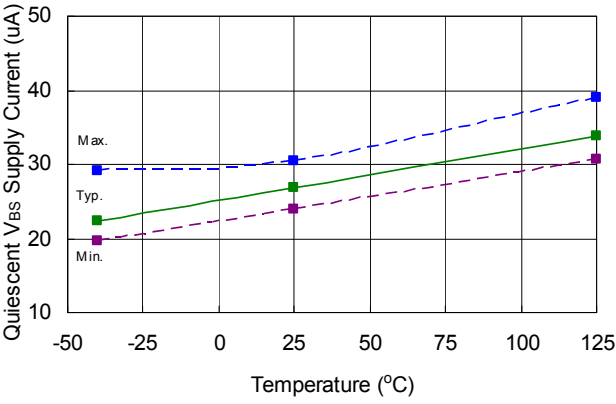
**Figure 10: Deadtime vs. temperature**



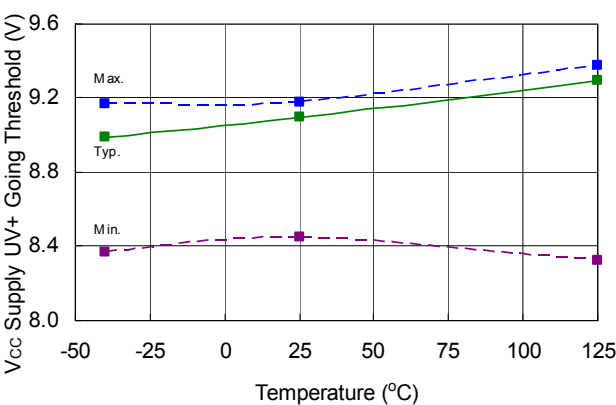
**Figure 11: Offset Leakage Current vs. temperature**



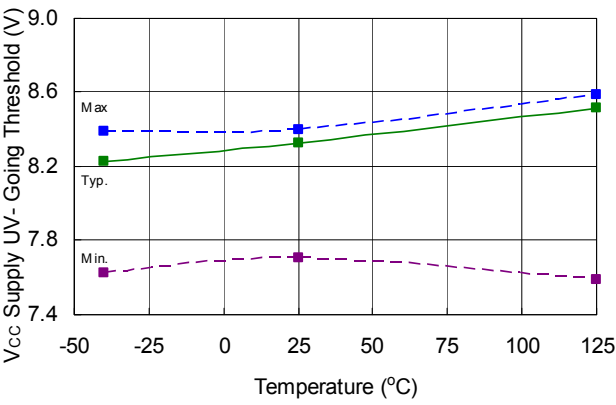
**Figure 12: V<sub>CC</sub> Supply Current vs. Temperature**



**Figure 13: V<sub>BS</sub> Supply Current vs. temperature**



**Figure 14: V<sub>CCUV+</sub> vs. temperature**



**Figure 15: V<sub>CCUV-</sub> vs. temperature**

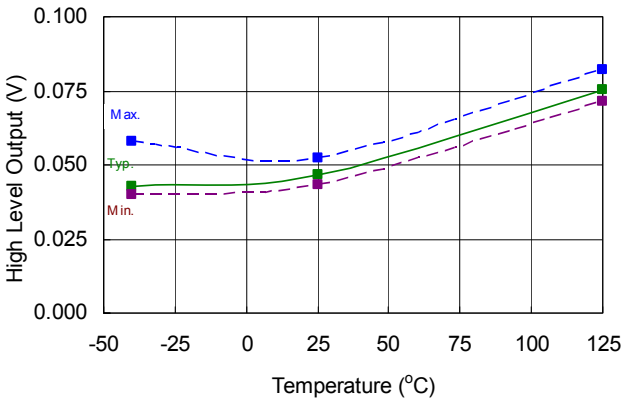


Figure 16:  $V_{OH}$  ( $I_O = 2mA$ ) vs. temperature

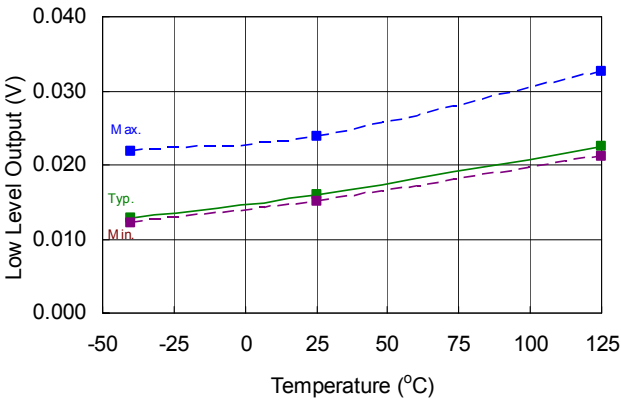
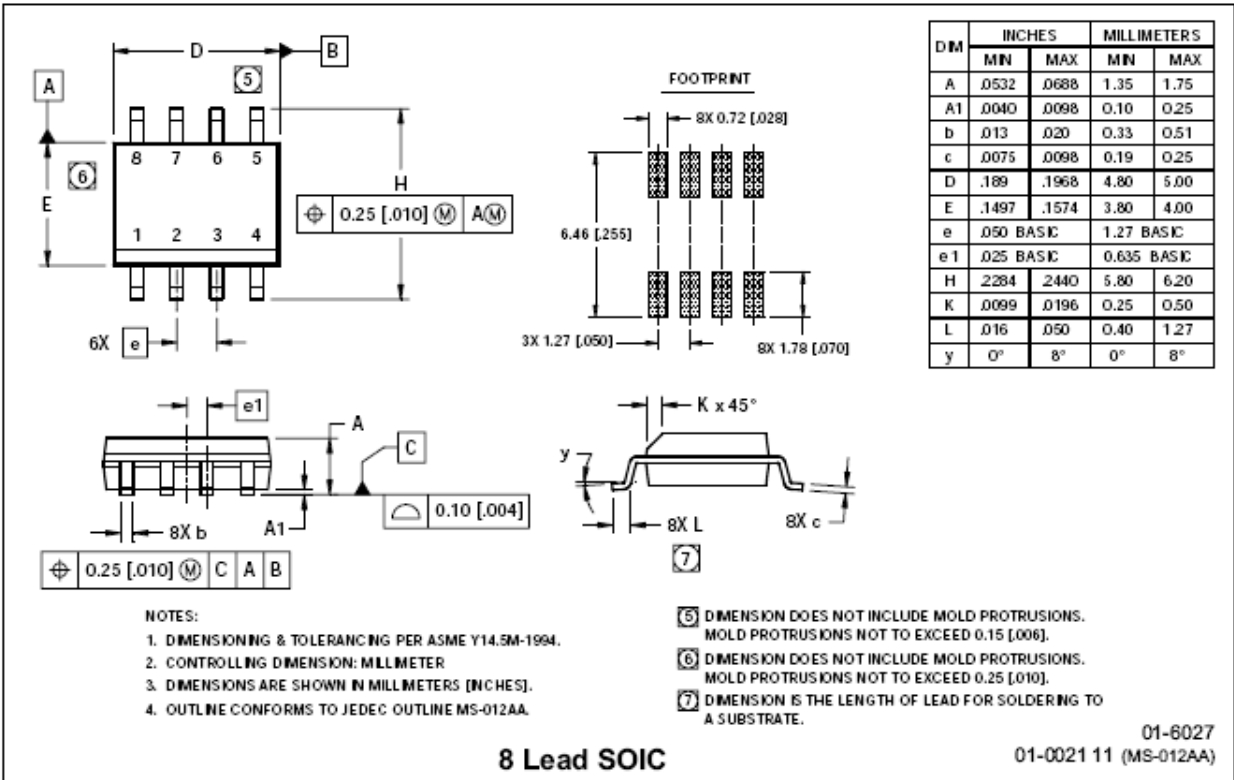
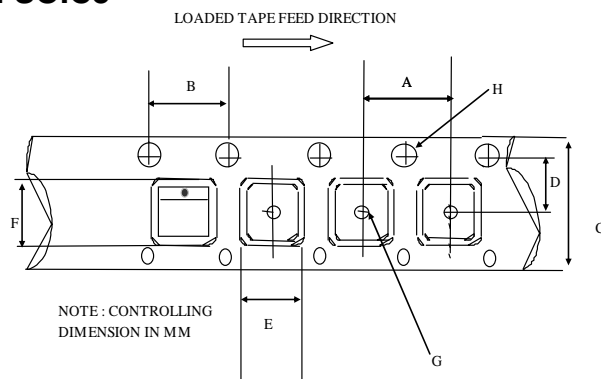


Figure 17:  $V_{OL}$  ( $I_O = 2mA$ ) vs. temperature

**Case Outlines**

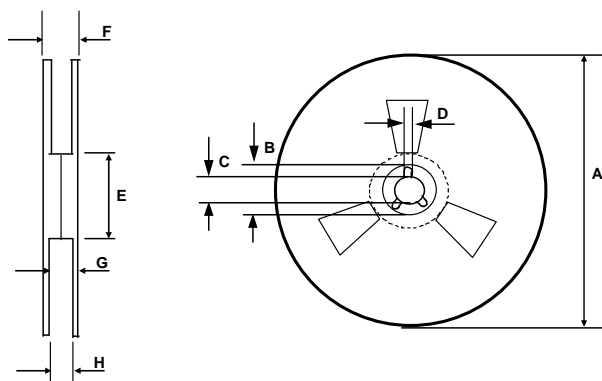


## Tape and Reel Details: SOIC8



CARRIER TAPE DIMENSION FOR 44PLCC

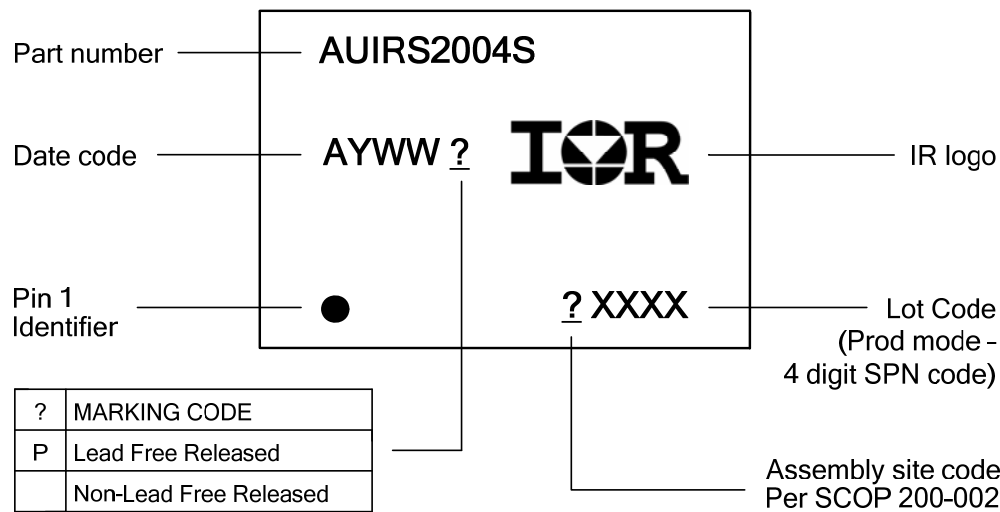
Code	Metric		Imperial	
	Min	Max	Min	Max
A	23.90	24.10	0.94	0.948
B	3.90	4.10	0.153	0.161
C	31.70	32.30	1.248	1.271
D	14.10	14.30	0.555	0.562
E	17.90	18.10	0.704	0.712
F	17.90	18.10	0.704	0.712
G	2.00	n/a	0.078	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 44PLCC

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	38.4	n/a	1.511
G	34.7	35.8	1.366	1.409
H	32.6	33.1	1.283	1.303

**Part Marking Information**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2004S	SOIC8	Tube/Bulk	95	AUIRS2004S
		Tape and Reel	2500	AUIRS2004STR

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**WORLD HEADQUARTERS:**  
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Tel: (310) 252-7105

## Revision History

Date	Comment
Jul. 30, 2010	Converted from industrial datasheet
Aug. 30, 2010	Update qualification ESD/LU class
Aug. 31, 2010	Changed Deadtime typical to 700ns on 1 <sup>st</sup> page, TON max to 880, MT max to 150, 60, DT min to 400, typ to 600. Added tri-temp graph, I/O equivalent circuit. Modified block diagram, SD pull up now.
Sep. 19, 2010	Typ Deadtime back to 520ns; DTmax=650ns at 25°C; DTmax=800ns; MT max to 150ns, (60ns at 25°C). ISD+ and ISD- parameters added to specify SD input impedance.
Sep. 28, 2010	Updated MT <sub>25</sub> to 80; updated block diagram and SD pin I/O circuit
Sep. 30, 2010	ISD+ and ISD- parameters exchanged because SD is pull down.
Oct. 14, 2010	Typ application section filled up
Oct. 19, 2010	Update reflow temp to 260C
Nov. 2, 2010	Changed 1 <sup>st</sup> page header. Minor update characteristics table format and corrected SD pin lead definition