$\label{eq:added_add} ADG758/ADG759 \\ -SPECIFICATIONS^1 (v_{DD} = 5 \ v \ \pm \ 10\%, \ v_{ss} = 0 \ v, \ \text{GND} = 0 \ v, \ \text{unless otherwise noted.})$

	B Version			
D. (12590	-40°C	T T •.	
Parameter	+25°C	to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH Analog Signal Range ON Resistance (Row)	3	0 V to V_{DD}	V Ω typ	$V_{s} = 0 V to V_{DD}$, $I_{Ds} = 10 mA$;
ON Resistance Match Between Channels (ΔR_{ON})	4.5	5 0.4 0.8	$\Omega \max$ Ωtyp $\Omega \max$	Test Circuit 1 $V_s = 0 V$ to V_{DD} , $I_{DS} = 10 \text{ mA}$
ON Resistance Flatness (R _{FLAT(ON)})	0.75	1.2	Ω typ Ω max	$V_{\rm S} = 0$ V to $V_{\rm DD}$, $I_{\rm DS} = 10$ mA
LEAKAGE CURRENTS				$V_{DD} = 5.5 V$
Source OFF Leakage I _S (OFF)	$\pm 0.01 \\ \pm 0.1$	±0.3	nA typ nA max	$V_D = 4.5 \text{ V/1 V}, V_S = 1 \text{ V/4.5 V};$ Test Circuit 2
Drain OFF Leakage I_D (OFF)	$\pm 0.01 \\ \pm 0.1$	±0.75	nA typ nA max	$V_D = 4.5 \text{ V/1 V}, V_S = 1 \text{ V/4.5 V};$ Test Circuit 3
Channel ON Leakage I _D , I _S (ON)	$\pm 0.01 \\ \pm 0.1$	±0.75	nA typ nA max	$V_D = V_S = 1 V$, or 4.5 V, Test Circuit 4
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, V _{INL} Input Current		0.8	V max	
I _{INI} or I _{INH}	0.005		μA typ	$V_{IN} = V_{INI}$ or V_{INH}
		± 0.1	μA max	
C _{IN} , Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS ²				
t _{TRANSITION}	14	25	ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$; Test Circuit 5
Break-Before-Make Time Delay, to	8	25	ns max	$V_{S1} = 3 V/0 V, V_{S8} = 0 V/3 V$ $R_r = 300 Q, C_r = 35 pF$
Dieux Derore Mune Time Derug, c	0	1	ns min	$V_S = 3 V$; Test Circuit 6
t _{on} (EN)	14		ns typ	$R_{L} = 300 \Omega, C_{L} = 35 pF$
	_	25	ns max	$V_s = 3 V$; Test Circuit 7
t _{OFF} (EN)	1	12	ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$ $V_c = 3 V$: Toot Circuit 7
Charge Injection	±3	12	pC typ	$V_{\rm S} = 5$ V, rest Circuit 7 $V_{\rm S} = 2.5$ V, $R_{\rm S} = 0$ Ω , $C_{\rm L} = 1$ nF; Test Circuit 8
Off Isolation	-60		dB typ	$R_{\rm L} = 50 \Omega, C_{\rm L} = 5 \text{ pF}, f = 10 \text{ MHz}$
	-80		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Test Circuit 9
Channel-to-Channel Crosstalk	-60		dB typ	$R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz$
	-80		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; Test Circuit 10
-3 dB Bandwidth	55		MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Test Circuit 11
$C_{\rm S}$ (OFF) $C_{\rm D}$ (OFF)	13		pF typ	f = 1 MHz
ADG758	85		pF typ	f = 1 MHz
ADG759	42		pF typ	f = 1 MHz
$C_D, C_S(ON)$			_	
ADG758	96		pF typ	f = 1 MHz
ADG/39	48		pr typ	I = I MHZ
POWER REQUIREMENTS				$V_{DD} = 5.5 V$
l _{DD}	0.001	1.0	μA typ μA max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

$\label{eq:specifications} SPECIFICATIONS^{1} \ (v_{\text{DD}} = 3 \ \text{V} \pm 10\%, \ v_{\text{SS}} = 0 \ \text{V}, \ \text{GND} = 0 \ \text{V}, \ \text{unless otherwise noted.})$

	B Version			
		-40°C		
Parameter	+25°C	to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
ON Resistance (R_{ON})	8		Ω typ	$V_{s} = 0 V$ to V_{DD} , $I_{Ds} = 10 mA$;
	11	12	$\Omega \max$	Test Circuit 1
ON Resistance Match Between		0.4	Ω typ	$V_s = 0$ V to V_{DD} , $I_{Ds} = 10$ mA
Channels (ΔR_{ON})		1.2	Ω max	
LEAKAGE CURRENTS				$V_{DD} = 3.3 \text{ V}$
Source OFF Leakage Is (OFF)	± 0.01		nA typ	$V_{S} = 3 V/1 V, V_{D} = 1 V/3 V;$
	+0.1	+0.3	nA max	Test Circuit 2
Drain OFF Leakage ID (OFF)	± 0.01		nA typ	$V_{s} = 3 V/1 V, V_{D} = 1 V/3 V;$
	± 0.1	± 0.75	nA max	Test Circuit 3
Channel ON Leakage ID, Is (ON)	+0.01		nA typ	$V_s = V_D = 1$ V or 3 V: Test Circuit 4
	± 0.1	± 0.75	nA max	
DIGITAL INPUTS				
Input High Voltage, VINH		2.0	V min	
Input Low Voltage, V _{INI}		0.8	V max	
Input Current				
I _{INI} or I _{INH}	0.005		uA typ	$V_{IN} = V_{INI}$ or V_{INH}
		± 0.1	μA max	
C _{IN} , Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS ²				
transition	18		ns typ	$R_{I} = 300 \Omega$, $C_{I} = 35 pF$; Test Circuit 5
		30	ns max	$V_{S1} = 2 V/0 V, V_{S2} = 0 V/2 V$
Break-Before-Make Time Delay, t _D	8		ns typ	$R_{L} = 300 \Omega, C_{L} = 35 pF$
-		1	ns min	$V_{\rm S} = 2$ V; Test Circuit 6
t _{on} (EN)	18		ns typ	$R_L = 300 \Omega, C_L = 35 pF$
		30	ns max	$V_{\rm S}$ = 2 V; Test Circuit 7
t _{OFF} (EN)	8		ns typ	$R_L = 300 \Omega, C_L = 35 pF$
		15	ns max	$V_S = 2 V$; Test Circuit 7
Charge Injection	±3		pC typ	$V_{\rm S} = 1.5 \text{ V}, \text{ R}_{\rm S} = 0 \Omega, \text{ C}_{\rm L} = 1 \text{ nF};$
	(0)		10.	Test Circuit 8 $\mathbf{D} = 50.0$, $\mathbf{C} = 5$, \mathbf{E} , $\mathbf{C} = 10$ MH
Off Isolation	-60		dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 10 \text{ MHz}$
	-80		dB typ	$R_L = 50 \Omega_2, C_L = 5 \text{ pF}, I = 1 \text{ MHz};$ Test Circuit 9
Channel-to-Channel Crosstalk	-60		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 10 MHz$
	-80		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$;
				Test Circuit 10
–3 dB Bandwidth	55		MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Test Circuit 11
C _S (OFF)	13		pF typ	f = 1 MHz
C _D (OFF)				
ADG758	85		pF typ	f = 1 MHz
ADG759	42		pF typ	f = 1 MHz
$C_D, C_S(ON)$				
ADG758	96		pF typ	f = 1 MHz
ADG759	48		pF typ	t = 1 MHz
POWER REQUIREMENTS				$V_{DD} = 3.3 V$
I _{DD}	0.001		μA typ	Digital Inputs = 0 V or 3.3 V
		1.0	μA max	

NOTES

¹Temperature ranges are as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG758/ADG759-SPECIFICATIONS¹

DUAL SUPPLY (V_{DD} = +2.5 V ± 10%, V_{SS} = -2.5 V ± 10%, GND = 0 V, unless otherwise noted.)

	B Version				
Donomotor	+25%	-40°C	I lait	Test Conditional Comments	
Farameter	+23 C	10 +83 C	Unit	Test Conditions/Comments	
ANALOG SWITCH		X 7 . X 7	\$7		
Analog Signal Range		V_{SS} to V_{DD}	V		
ON Resistance (R _{ON})	2.5	_	Ω typ	$V_{\rm S} = V_{\rm SS}$ to $V_{\rm DD}$, $I_{\rm DS} = 10$ mA;	
	4.5	5	Ω max	Test Circuit 1	
ON Resistance Match Between		0.4	Ω typ		
Channels (ΔR_{ON})		0.8	Ω max	$V_{\rm S} = V_{\rm SS}$ to $V_{\rm DD}$, $I_{\rm DS} = 10$ mA	
ON Resistance Flatness (R _{FLAT(ON)})	0.6		Ω typ	$V_{\rm S} = V_{\rm SS}$ to $V_{\rm DD}$, $I_{\rm DS} = 10$ mA	
		1.0	Ω max		
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = -2.75 V	
Source OFF Leakage I _S (OFF)	± 0.01		nA typ	$V_{\rm S}$ = +2.25 V/-1.25 V, $V_{\rm D}$ = -1.25 V/+2.25 V;	
	± 0.1	±0.3	nA max	Test Circuit 2	
Drain OFF Leakage I _D (OFF)	± 0.01		nA typ	$V_{\rm S}$ = +2.25 V/-1.25 V, $V_{\rm D}$ = -1.25 V/+2.25 V;	
	± 0.1	± 0.75	nA max	Test Circuit 3	
Channel ON Leakage I _D , I _S (ON)	± 0.01		nA typ	$V_{\rm S} = V_{\rm D} = +2.25 \text{ V/}-1.25 \text{ V}$; Test Circuit 4	
	± 0.1	± 0.75	nA max		
DIGITAL INPUTS					
Input High Voltage, V _{INH}		1.7	V min		
Input Low Voltage, V _{INI}		0.7	V max		
Input Current					
I _{INI} or I _{INH}	0.005		μA typ	$V_{IN} = V_{INI}$ or V_{INH}	
		± 0.1	µA max		
C _{IN} , Digital Input Capacitance	2		pF typ		
DYNAMIC CHARACTERISTICS ²					
TTRANSITION	14		ns typ	$R_{\rm r} = 300 \Omega$, $C_{\rm r} = 35 \text{ pF}$; Test Circuit 5	
		25	ns max	$V_s = 1.5 \text{ V/0 V}$; Test Circuit 5	
Break-Before-Make Time Delay, tp	8	-	ns typ	$R_{I} = 300 \Omega, C_{I} = 35 pF$	
		1	ns min	$V_s = 1.5 V$; Test Circuit 6	
$t_{ON}(EN)$	14		ns tvp	$R_{\rm I} = 300 \Omega, C_{\rm I} = 35 \mathrm{pF}$	
		25	ns max	$V_s = 1.5 V$; Test Circuit 7	
$t_{OFF}(EN)$	8		ns tvp	$R_{\rm I} = 300 \Omega, C_{\rm I} = 35 \mathrm{pF}$	
		15	ns max	$V_s = 1.5 V$; Test Circuit 7	
Charge Injection	±3		pC typ	$V_{s} = 0 V, R_{s} = 0 \Omega, C_{t} = 1 nF;$	
C ,			1 71	Test Circuit 8	
Off Isolation	-60		dB typ	$R_{I} = 50 \Omega, C_{I} = 5 pF, f = 10 MHz$	
	-80		dB typ	$R_{I} = 50 \Omega, C_{I} = 5 pF, f = 1 MHz;$	
				Test Circuit 9	
Channel-to-Channel Crosstalk	-60		dB typ	$R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz$	
	-80		dB typ	$R_{L} = 50 \Omega, C_{L} = 5 pF, f = 1 MHz;$	
				Test Circuit 10	
-3 dB Bandwidth	55		MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Test Circuit 11	
C _s (OFF)	13		pF typ	f = 1 MHz	
C _D (OFF)					
ADG758	85		pF typ	f = 1 MHz	
ADG759	42		pF typ	f = 1 MHz	
$C_D, C_S(ON)$					
ADG758	96		pF typ	f = 1 MHz	
ADG759	48		pF typ	f = 1 MHz	
POWER REOUIREMENTS				$V_{DD} = +2.75 V$	
Inn	0.001		uA tvp	Digital Inputs = $0 \text{ V or } 2.75 \text{ V}$	
עע		1.0	uA max		
Iss	0.001		uA tvp	$V_{SS} = -2.75 V$	
		1.0	µA max	Digital Inputs = 0 V or 2.75 V	

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

 $T_A = 25^{\circ}C$, unless otherwise noted.

Parameter	Rating
V _{DD} to V _{SS}	7 V
V _{DD} to GND	–0.3 V to +7 V
Vss to GND	+0.3 V to -3.5 V
Analog Inputs ¹	V _{ss} – 0.3 V to V _{DD} +0.3 V or 30 mA, Whichever Occurs First
Digital Inputs ¹	–0.3 V to V _{DD} +0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Chip Scale Package, θ _{JA} Thermal Impedance	32°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

¹ Overvoltages at EN, A, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table I. ADG758 Truth Table

A2	A1	A0	EN	Switch Condition
Х	Х	Х	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table II. ADG759 Truth Table

A1	A0	EN	ON Switch Pair
Х	Х	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

PIN CONFIGURATIONS



TERMINOLOGY

V _{DD}	Most Positive Power Supply Potential
V _{SS}	Most Negative Power Supply in a dual-supply application. In single-supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input
R _{ON}	Ohmic Resistance between D and S
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of ON resistance as measured over the specified analog signal range.
I _S (OFF)	Source Leakage Current with the Switch OFF
I _D (OFF)	Drain leakage Current with the Switch OFF
$I_D, I_S (ON)$	Channel Leakage current with the Switch ON
$V_{\rm D}$ (V _S)	Analog Voltage on Terminals D, S
C _S (OFF)	OFF Switch Source Capacitance. Measured with reference to ground.
C _D (OFF)	OFF Switch Drain Capacitance. Measured with reference to ground.
C_D, C_S (ON)	ON Switch Capacitance. Measured with reference to ground.
C _{IN}	Digital Input Capacitance
t _{TRANSITION}	Delay Time measured between the 50% and 90% points of the digital inputs and the switch ON condition when switching from one address state to another.
t _{ON} (EN)	Delay Time between the 50% and 90% points of the EN digital input and the switch ON condition.
t _{OFF} (EN)	Delay Time between the 50% and 90% points of the EN digital input and the switch OFF condition.
t _{OPEN}	OFF Time measured between the 80% points of both switches when switching from one address state to another.
Off Isolation	A measure of unwanted signal coupling through an OFF switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
On Response	The Frequency Response of the ON Switch.
On Loss	The Loss Due to the ON Resistance of the Switch
V _{INL}	Maximum Input Voltage for Logic "0"
V _{INH}	Minimum Input Voltage for Logic "1"
$I_{INL} \left(I_{INH} \right)$	Input Current of the Digital Input
I_{DD}	Positive Supply Current
I _{SS}	Negative Supply Current

Typical Performance Characteristics-ADG758/ADG759



TPC 1. ON Resistance as a Function of V_{D} (V_{\text{S}}) for Single Supply



TPC 2. ON Resistance as a Function of V_D (V_S) for Dual Supply



TPC 3. ON Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

TPC 4. ON Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

TPC 5. ON Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

TPC 6. Leakage Currents as a Function of V_D (V_S)

TPC 7. Leakage Currents as a Function of V_D (V_S)

TPC 8. Leakage Currents as a Function of V_D (V_S)

TPC 9. Leakage Currents as a Function of Temperature

TPC 10. Leakage Currents as a Function of Temperature

TPC 11. Supply Current vs. Input Switching Frequency

TPC 12. OFF Isolation vs. Frequency

TPC 13. Crosstalk vs. Frequency

TPC 15. Charge Injection vs. Source Voltage

TPC 14. ON Response vs. Frequency

Test Circuits

Test Circuit 1. ON Resistance

Test Circuit 2. I_S (OFF)

Test Circuit 3. I_D (OFF)

Test Circuit 4. I_D (ON)

Test Circuit 5. Switching Time of Multiplexer, t_{TRANSITION}

*SIMILAR CONNECTION FOR ADG759

Test Circuit 6. Break-Before-Make Delay, t_{OPEN}

Test Circuit 7. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

*SIMILAR CONNECTION FOR ADG759

Test Circuit 8. Charge Injection

Test Circuit 9. OFF Isolation

Test Circuit 10. Channel-to-Channel Crosstalk

Test Circuit 11. Bandwidth

Power-Supply Sequencing

When using CMOS devices, care must be taken to ensure correct power-supply sequencing. Incorrect power-supply sequencing can result in the device being subjected to stresses beyond the maximum ratings listed in the data sheet. Digital and analog inputs should always be applied after power supplies and ground. For single-supply operation, V_{SS} should be tied to GND as close to the device as possible.

Downloaded from Arrow.com.

OUTLINE DIMENSIONS

20-Lead Lead Frame Chip Scale Package [LFCSP_WQ] 4 mm × 4 mm Body, Very Very Thin Quad (CP-20-6) Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG758BCPZ	–40°C to +85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6
ADG758BCPZ-REEL7	–40°C to +85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6
ADG759BCPZ	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6
ADG759BCPZ-REEL	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6
ADG759BCPZ-REEL7	–40°C to +85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6

¹ Z = RoHS Compliant Part.

REVISION HISTORY

3/13—Rev. A to Rev. B	
Updated Outline Dimensions	12
5/02—Rev. 0 to Rev. A	12
Edits to General Description section Updated Outline Drawings	1 12

©2013 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. D02371-0-3/13(B)

www.analog.com