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REVISION HISTORY

11/12—Rev. A to Rev. B

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5/09—Rev. 0 to Rev. A

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Added DC Restore Function Section, Figure 43, Clamp Amplifier Section, and Figure 44 ... 15

10/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 5 V, G = 2, R_F = 301 Ω, R_F = 402 Ω for G = 1, R_L = 150 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p, G = 1		600		MHz
	V_{OUT} = 0.1 V p-p		350		MHz
	V_{OUT} = 2 V p-p, G = 1		165		MHz
	V_{OUT} = 2 V p-p		175		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p		85		MHz
Slew Rate	V_{OUT} = 2 V step		600		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		18		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f_C = 1 MHz, V_{OUT} = 2 V p-p		−86/−94		dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p		−71/−84		dBc
Crosstalk	f = 5 MHz		−60		dB
Input Voltage Noise	f = 1 MHz		4		nV/√Hz
Input Current Noise	f = 1 MHz (+IN/−IN)		2/9		pA/√Hz
Differential Gain Error			0.01		%
Differential Phase Error			0.02		Degrees
DC PERFORMANCE					
Input Offset Voltage		−14	+0.5	+14	mV
+ Input Bias Current		−2	+0.7	+2	µA
− Input Bias Current		−13	+8	+13	µA
Open-Loop Transimpedance		300	390		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+IN1/+IN2		15		MΩ
	−IN1/−IN2		90		Ω
Input Capacitance	+IN1/+IN2		1.5		pF
Input Common-Mode Voltage Range	Typical	−1.8		+3.8	V
Common-Mode Rejection Ratio			−61	−54	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		−1.4 to +3.6	−1.7 to +3.7		V
Output Overdrive Recovery Time	Rise/fall, f = 5 MHz		15		ns
Maximum Linear Output Current @ V_{OUT} = 1 V_{PEAK}	f_C = 1 MHz, HD2 ≤ −50 dBc		21		mA
POWER-DOWN					
Input Voltage	Enabled		1.9		V
	Powered down		2		V
Bias Current		−0.1		+0.1	µA
Turn-On Time			0.3		µs
Turn-Off Time			1.6		µs
POWER SUPPLY					
Operating Range		3		5.5	V
Total Quiescent Current					
Amplifiers		15	19	21	mA
Charge Pump			23		mA
Total Quiescent Current When Powered Down					
Amplifiers		0.15	0.25	0.3	mA
Charge Pump			4		mA
Positive Power Supply Rejection Ratio			−64	−60	dB
Negative Power Supply Rejection Ratio			−58	−54	dB
Charge Pump Output Voltage		−3.3	−3	−2.5	V
Charge Pump Sink Current				150	mA

T_A = 25°C, V_S = 3.3 V, G = 2, R_F = 301 Ω, R_F = 402 Ω for G = 1, R_L = 150 Ω, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p, G = 1		540		MHz
	V_{OUT} = 0.1 V p-p		340		MHz
	V_{OUT} = 2 V p-p, G = 1		140		MHz
	V_{OUT} = 2 V p-p		145		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p		70		MHz
Slew Rate	V_{OUT} = 2 V step		430		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		20		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f_C = 1 MHz, V_{OUT} = 2 V p-p		−88/−91		dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p		−75/−78		dBc
Crosstalk	f = 5 MHz		−60		dB
Input Voltage Noise	f = 1 MHz		4		nV/√Hz
Input Current Noise	f = 1 MHz (+IN/−IN)		2/9		pA/√Hz
Differential Gain Error			0.02		%
Differential Phase Error			0.03		Degrees
DC PERFORMANCE					
Input Offset Voltage		−14	+0.7	+14	mV
+ Input Bias Current		−2	+0.6	+2	µA
− Input Bias Current		−13	+7	+13	µA
Open-Loop Transimpedance		300	350		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+IN1/+IN2		15		MΩ
	−IN1/−IN2		90		Ω
Input Capacitance	+IN1/+IN2		1.5		pF
Input Common-Mode Voltage Range	Typical	−0.9		+2.2	V
Common-Mode Rejection Ratio			−60	−54	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		−0.6 to +2.1	−0.9 to +2.2		V
Output Overdrive Recovery Time	Rise/fall, f = 5 MHz		15		ns
Maximum Linear Output Current @ V_{OUT} = 1 V_{PEAK}	f_C = 1 MHz, HD2 ≤ −50 dBc		20		mA
POWER-DOWN					
Input Voltage	Enabled		1.25		V
	Powered down		1.35		V
Bias Current		−0.1		+0.1	µA
Turn-On Time			0.3		µs
Turn-Off Time			1.6		µs
POWER SUPPLY					
Operating Range		3		5.5	V
Total Quiescent Current					
Amplifiers		14	19	20	mA
Charge Pump			21		mA
Total Quiescent Current When Powered Down					
Amplifiers		0.15	0.25	0.3	mA
Charge Pump			2		mA
Positive Power Supply Rejection Ratio			−63	−60	dB
Negative Power Supply Rejection Ratio			−57	−54	dB
Charge Pump Output Voltage		−2.1	−2	−1.8	V
Charge Pump Sink Current				45	mA

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Internal Power Dissipation[1]	
16-Lead LFCSP	See Figure 2
Input Voltage (Common Mode)	$(-V_S - 0.2\,V)$ to $(+V_S - 1.2\,V)$
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Observe power derating curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for device in free air.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADA4858-3 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

To ensure proper operation, it is necessary to observe the maximum power derating curves in Figure 2.

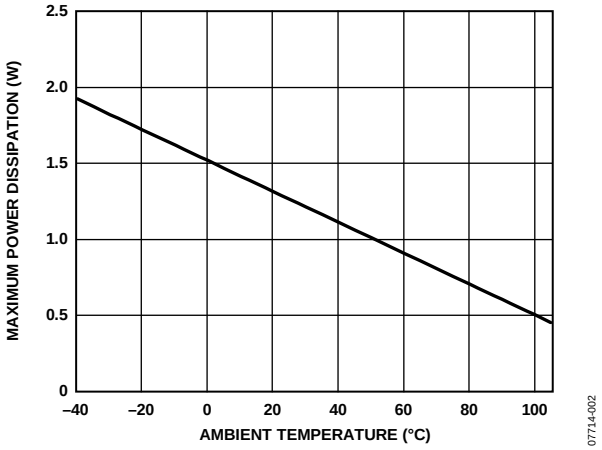

Figure 2. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

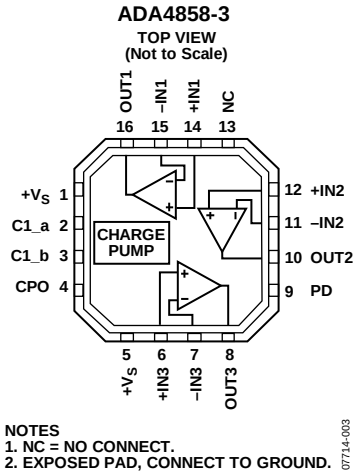

Figure 3. Pin Configuration.

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$+V_S$	Positive Supply for Charge Pump.
2	C1_a	Charge Pump Capacitor Side a.
3	C1_b	Charge Pump Capacitor Side b.
4	CPO	Charge Pump Output.
5	$+V_S$	Positive Supply.
6	+IN3	Noninverting Input 3.
7	–IN3	Inverting Input 3.
8	OUT3	Output 3.
9	PD	Power-Down.
10	OUT2	Output 2.
11	–IN2	Inverting Input 2.
12	+IN2	Noninverting Input 2.
13	NC	No Connect.
14	+IN1	Noninverting Input 1.
15	–IN1	Inverting Input 1.
16	OUT1	Output 1.
EPAD	Exposed Pad (EPAD)	The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5 V, G = 2, R_F = 301 Ω, R_F = 402 Ω for G = 1, R_F = 200 Ω for G = 5, R_L = 150 Ω, large signal V_{OUT} = 2 V p-p, and small signal V_{OUT} = 0.1 V p-p, unless otherwise noted.

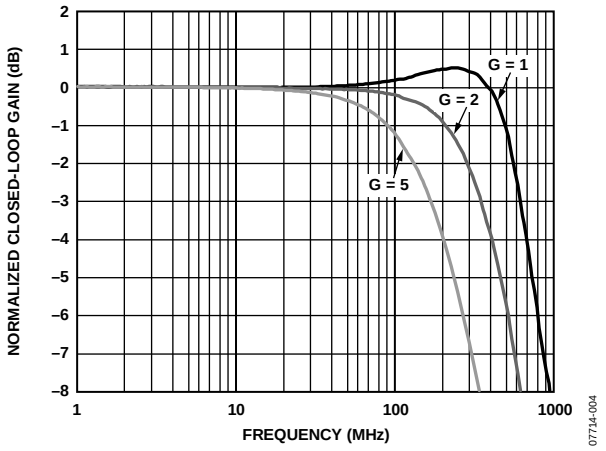

Figure 4. Small Signal Frequency Response vs. Gain

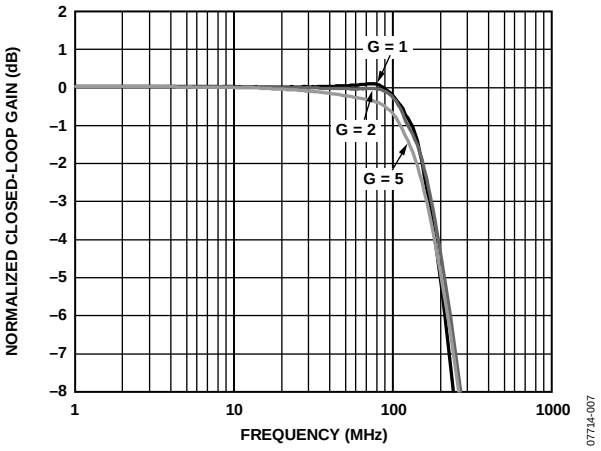

Figure 7. Large Signal Frequency Response vs. Gain

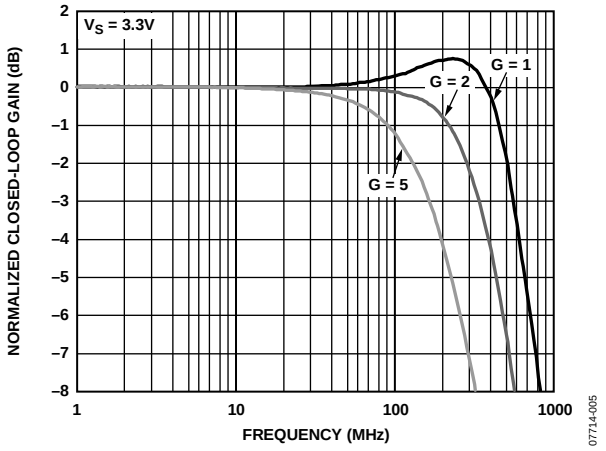

Figure 5. Small Signal Frequency Response vs. Gain

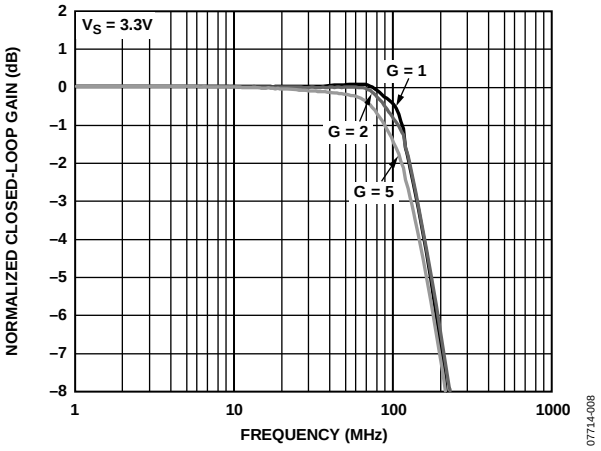

Figure 8. Large Signal Frequency Response vs. Gain

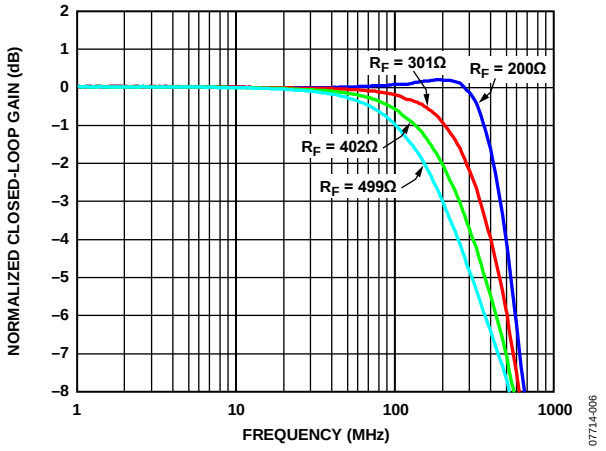

Figure 6. Small Signal Frequency Response vs. Feedback Resistor

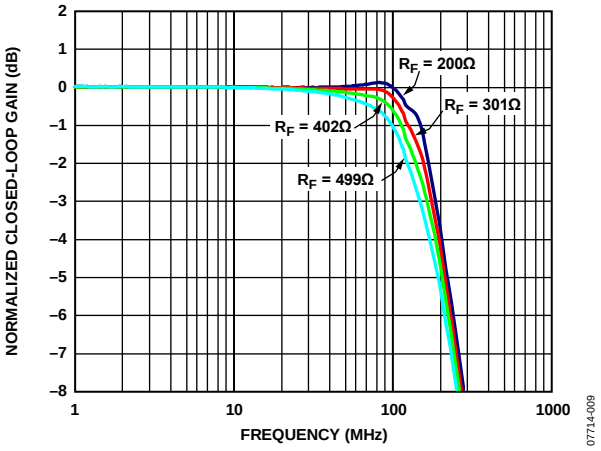

Figure 9. Large Signal Frequency Response vs. Feedback Resistor

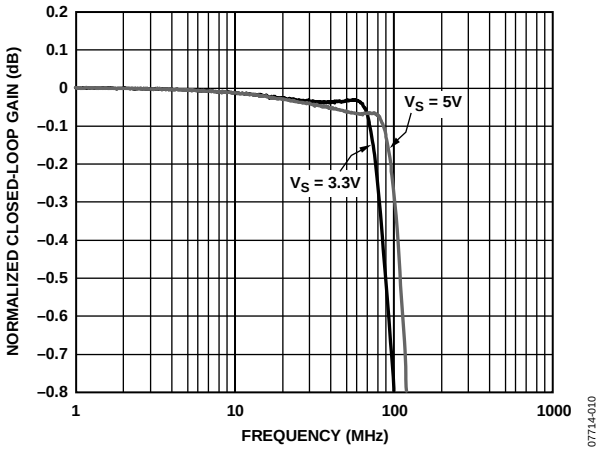

Figure 10. Large Signal 0.1 dB Flatness vs. Supply Voltage

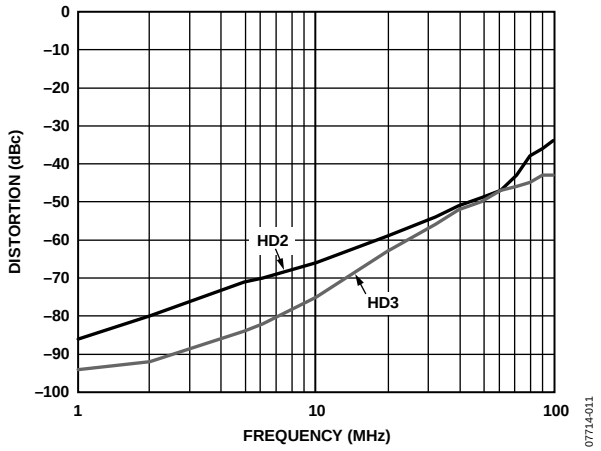

Figure 11. Harmonic Distortion vs. Frequency

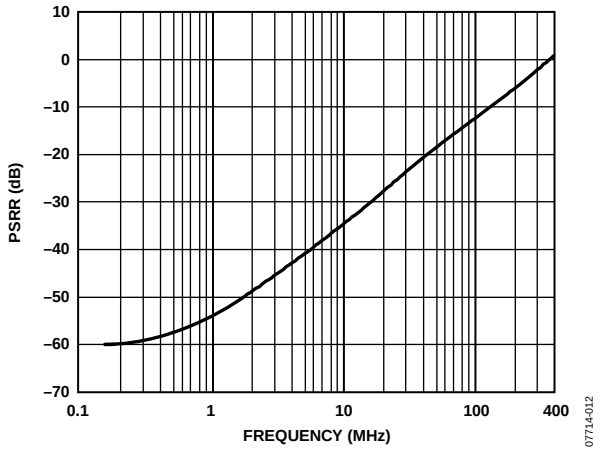

Figure 12. Power Supply Rejection Ratio (PSRR) vs. Frequency

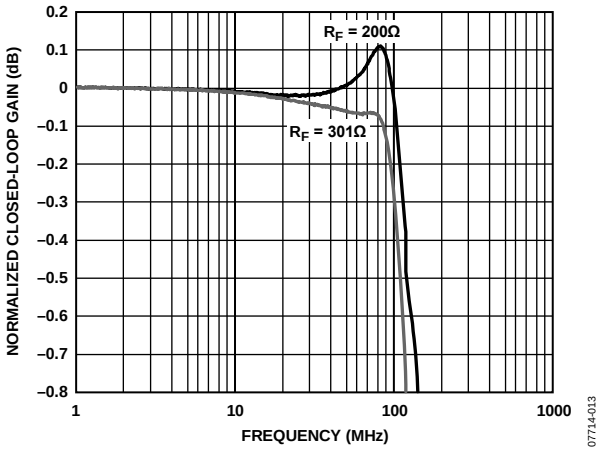

Figure 13. Large Signal 0.1 dB Flatness vs. Feedback Resistor

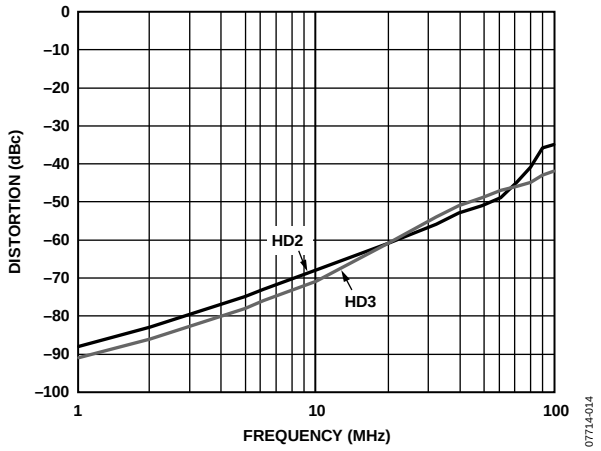

Figure 14. Harmonic Distortion vs. Frequency, V_S = 3.3 V

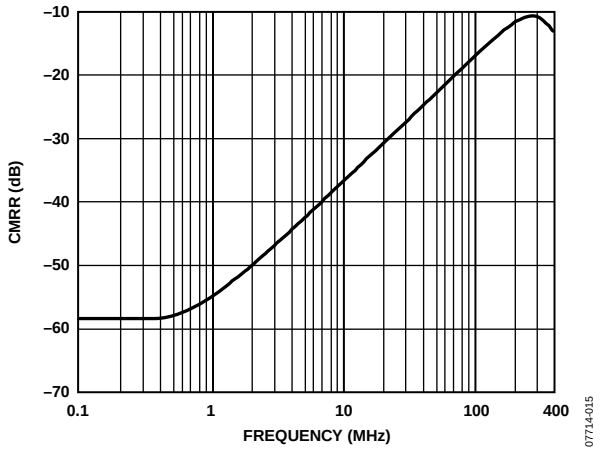

Figure 15. Common-Mode Rejection Ratio (CMRR) vs. Frequency

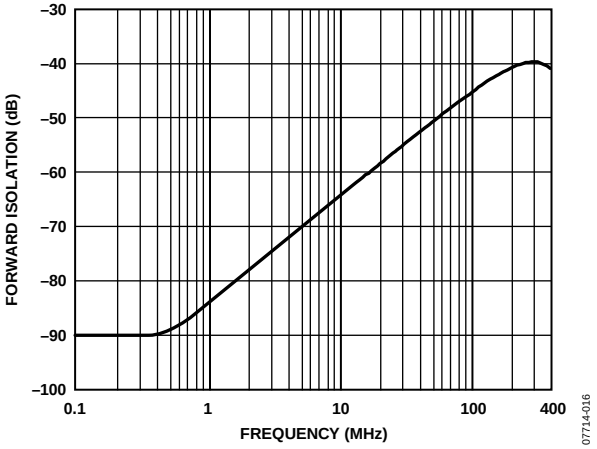

Figure 16. Forward Isolation vs. Frequency

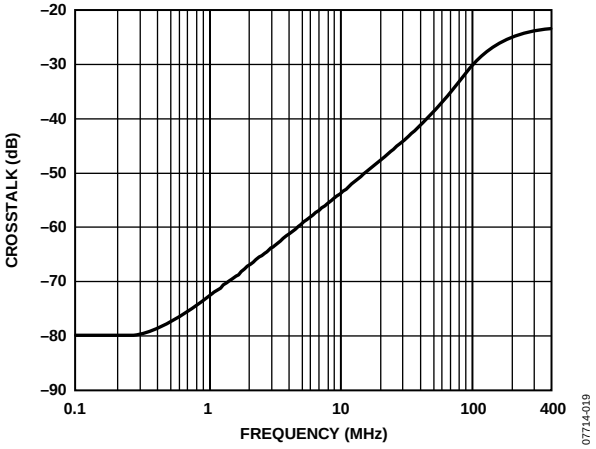

Figure 19. Crosstalk vs. Frequency

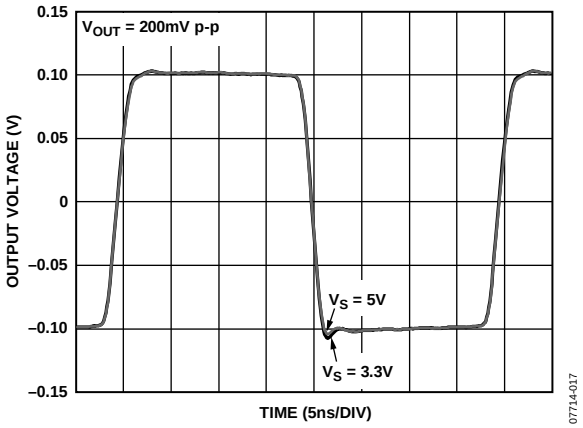

Figure 17. Small Signal Transient Response vs. Supply Voltage

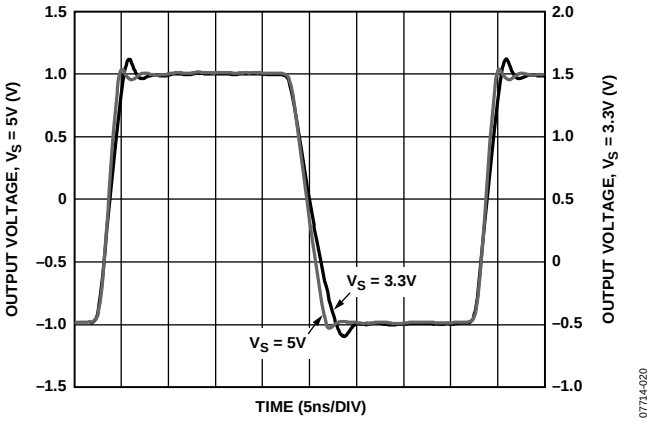

Figure 20. Large Signal Transient Response vs. Supply Voltage

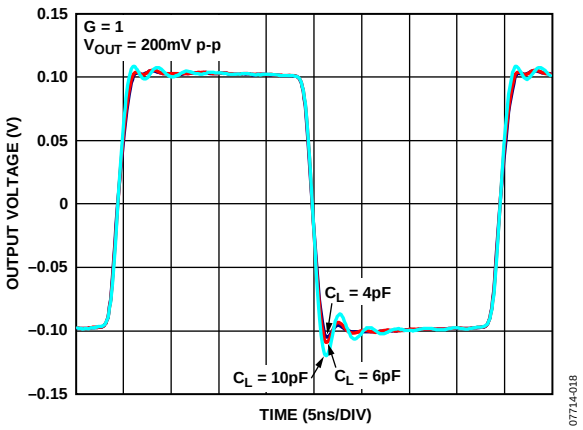

Figure 18. Small Signal Transient Response vs. Capacitive Load

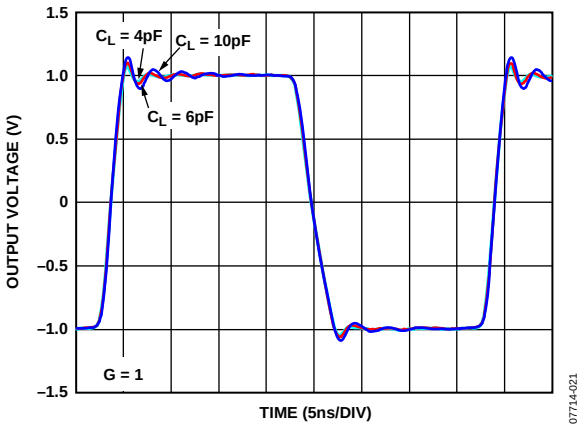

Figure 21. Large Signal Transient Response vs. Capacitive Load

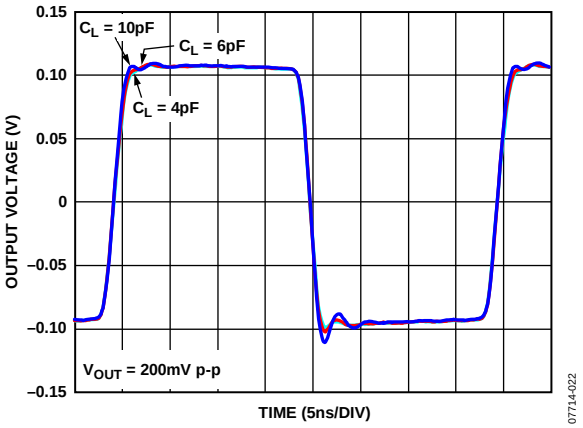

Figure 22. Small Signal Transient Response vs. Capacitive Load

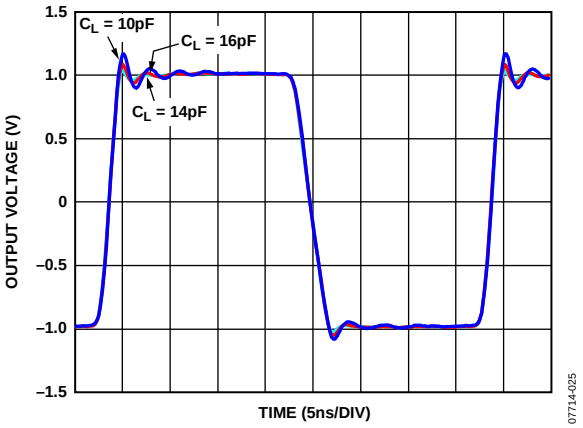

Figure 25. Large Signal Transient Response vs. Capacitive Load

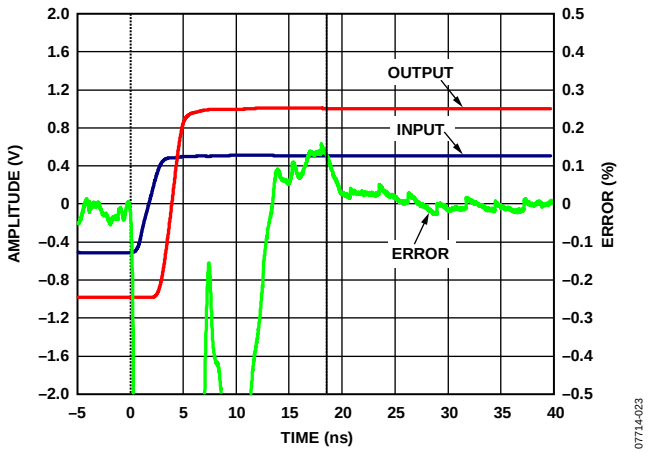

Figure 23. Settling Time (Rise)

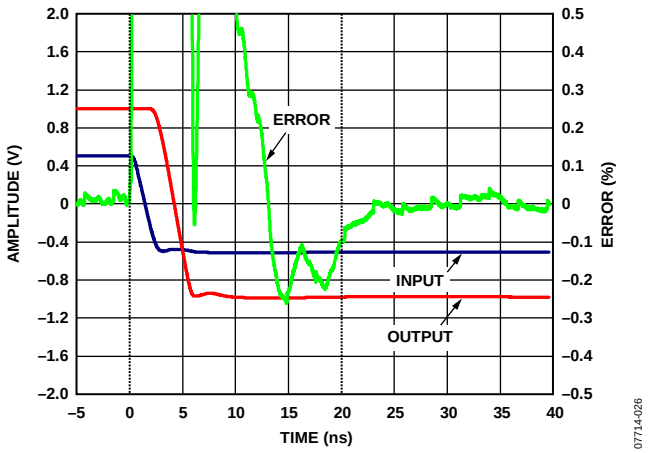

Figure 26. Settling Time (Fall)

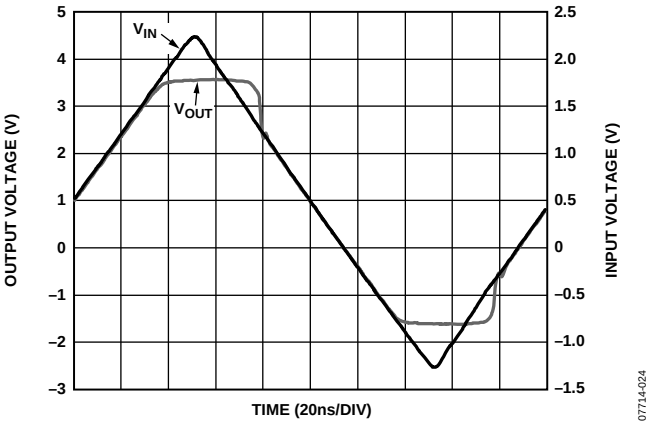

Figure 24. Output Overdrive Recovery

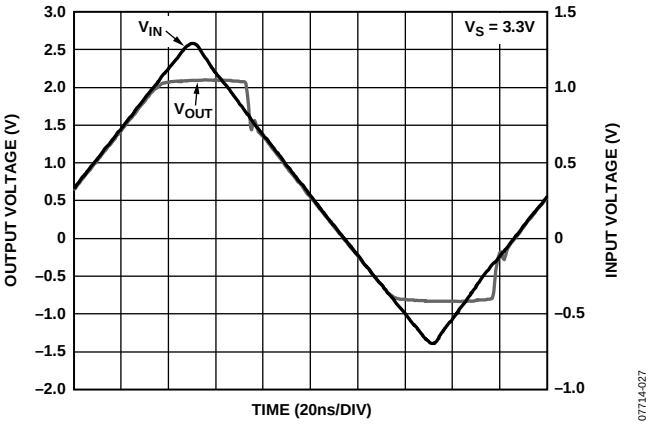

Figure 27. Output Overdrive Recovery, V_S = 3.3 V

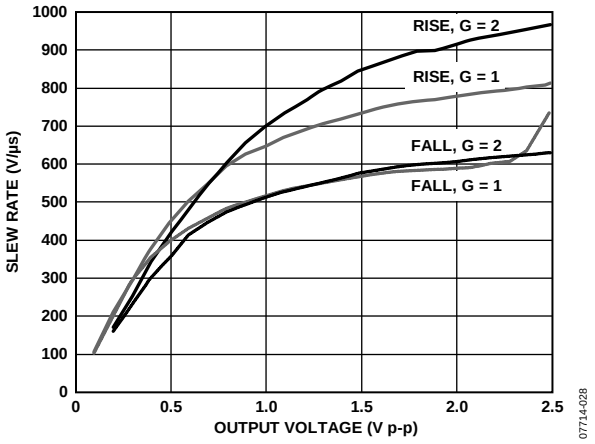

Figure 28. Slew Rate vs. Output Voltage

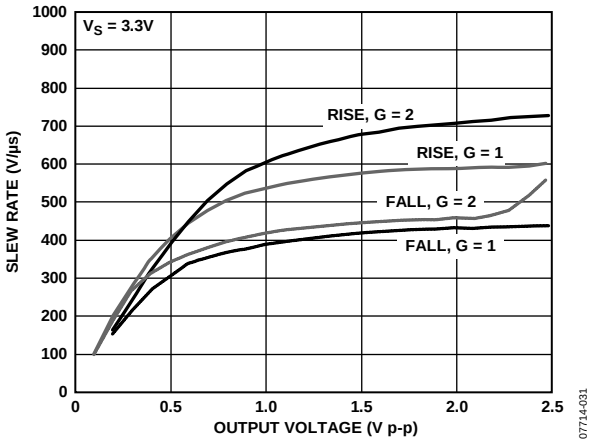

Figure 31. Slew Rate vs. Output Voltage, V_S = 3.3 V

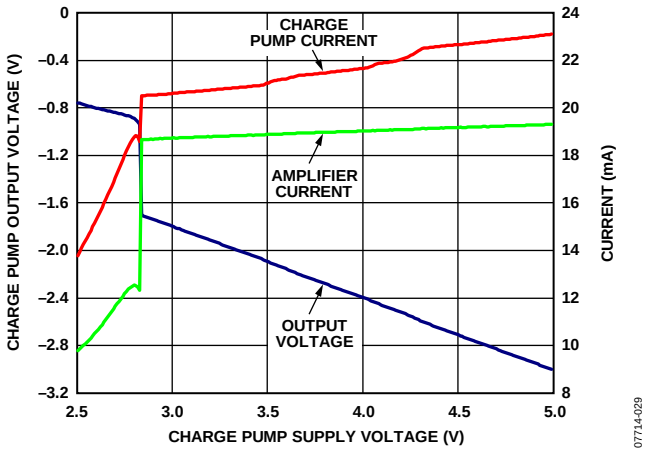

Figure 29. Charge Pump Output Voltage and Current vs. Charge Pump Supply Voltage

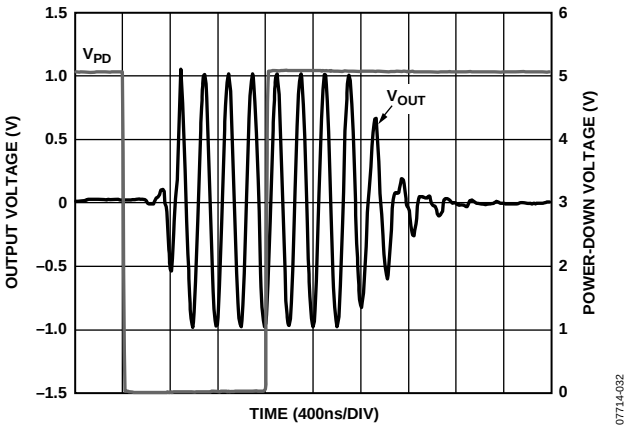

Figure 32. Enable/Power-Down Time

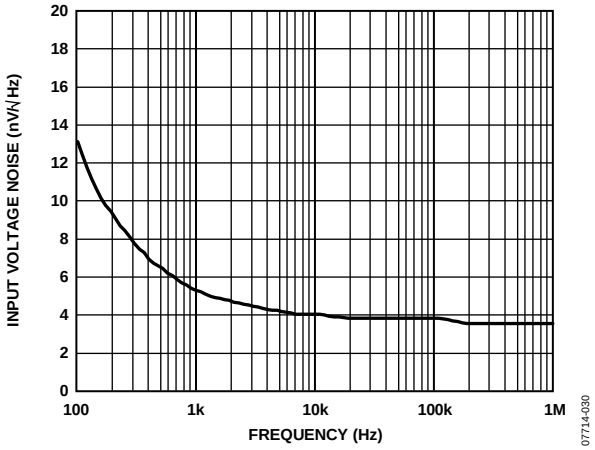

Figure 30. Input Voltage Noise vs. Frequency

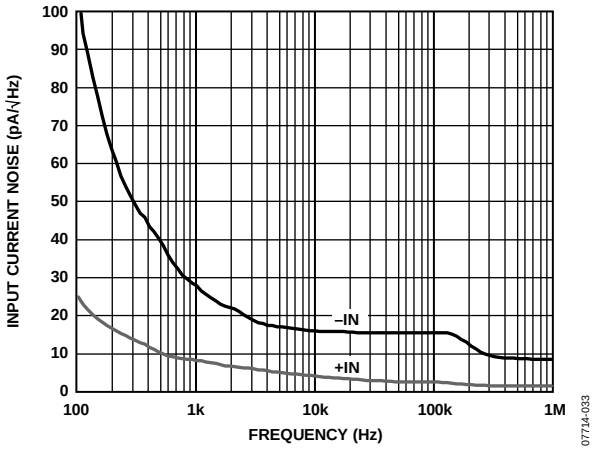

Figure 33. Input Current Noise vs. Frequency

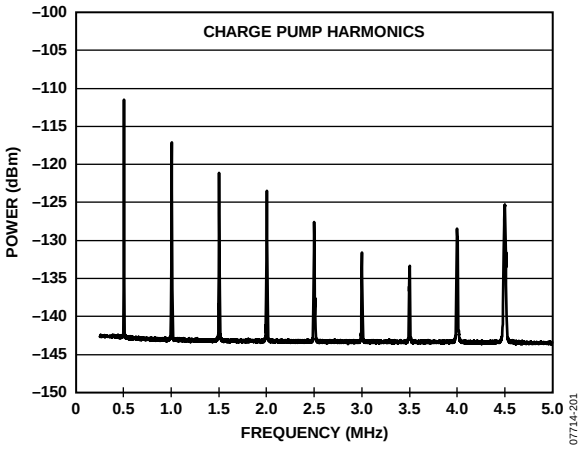

Figure 34. Output Spectrum vs. Frequency

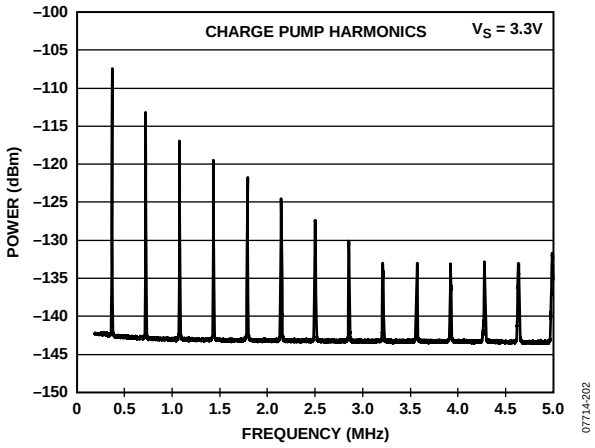

Figure 35. Output Spectrum vs. Frequency, V_S = 3.3 V

THEORY OF OPERATION

OVERVIEW

The ADA4858-3 is a current feedback amplifier designed for exceptional performance as a triple amplifier with a variable gain capability. Its specifications make it especially suitable for SD and HD video applications. The ADA4858-3 provides HD video output on a single supply as low as 3.0 V while only consuming 13 mA per amplifier. It also features a power-down pin (PD) that reduces the total quiescent current to 2 mA when activated.

The ADA4858-3 can be used in applications that require both ac- and dc-coupled inputs and outputs. The output stage on the ADA4858-3 is capable of driving 2 V p-p video signals into two doubly terminated video loads (150 Ω each) on a single 5 V supply. The input range of the ADA4858-3 includes ground, and the output range is limited by the output headroom set by the voltage drop across the two diodes from each rail, which occurs 1.2 V from the positive supply and the charge pump negative supply rails.

CHARGE PUMP OPERATION

The on-board charge pump creates a negative supply for the amplifier. It provides different negative voltages depending on the power supply voltage. For a +5 V supply, the negative supply generated is equal to −3 V with 150 mA of output supply current, and for a +3.3 V supply, the negative supply is equal to −2 V with 45 mA of output supply current.

Figure 36 shows the charging cycle when the supply voltage $+V_S$ charges C1 through Φ_1 to ground. During this cycle, C1 quickly charges to reach the $+V_S$ voltage. The discharge cycle then begins with switching Φ_1 off and switching Φ_2 on, as shown in Figure 37. When C1 = C2, the charge in C1 is divided between the two capacitors and slowly increases the voltage in C2 until it reaches a predetermined voltage (−3 V for +5 V supply and −2 V for +3.3 V supply). The typical charge pump charging and discharging frequency is 550 kHz with a 150 Ω load and no input signal; however, this frequency changes with different loads and supply conditions.

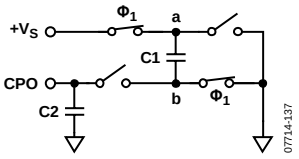

Figure 36. C1 Charging Cycle

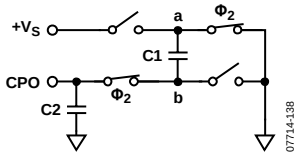

Figure 37. C1 Discharging Cycle

The ADA4858-3 specifications make it especially suitable for SD and HD video applications. It also allows dc-coupled video signals with its black level set to 0 V and its sync tip at −300 mV for YPbPr video.

The charge pump is always on, even when the power-down pin (PD) is enabled and the amplifiers are off. However, if a negative current is not used, the charge pump is in an idle state. Each amplifier needs −6.3 mA of current, which totals −19 mA for all three amplifiers. This means additional negative current may be available by the charge pump for external use. Pin 4 (CPO) is the charge pump output that provides access to the negative supply generated by the charge pump.

If the negative supply is used to power another device in the system, it is only possible for the 5 V supply operation. In the 3.3 V supply operation, the charge pump output current is very limited. The capacitor C2 placed at the CPO pin, which regulates the ripple of the negative voltage, can be used as a coupling capacitor for the external device. However, the charge pump current should be limited to a maximum of 50 mA for external use. When powering down the ADA4858-3, the charge pump is not affected and its output voltage and current are still available for external use.

It is recommended to use 1 µF low ESR and low ESL capacitors for C1 and C2. These capactiors should be placed very close to the part. C1 should be placed between Pin C1_a and Pin C1_b, and C2 should be placed between Pin CPO and ground. If the charge pump ripple at the CPO pin is too high, larger capacitors (that is, 4.7 µF) can replace the 1 µF at C1 and C2.

APPLICATIONS INFORMATION

GAIN CONFIGURATIONS

The ADA4858-3 is a single-supply, high speed, voltage feedback amplifier. Table 5 provides a convenient reference for quickly determining the feedback and gain set resistor values and bandwidth for common gain configurations.

Table 5. Recommended Values and Frequency Performance[1]

Gain	R_F (Ω)	R_G (Ω)	Small Signal −3 dB BW (MHz)	Large Signal 0.1 dB Flatness (MHz)
1	402	N/A	600	88
2	301	301	350	85
5	200	40	160	35

[1] Conditions: V_S = 5 V, T_A = 25°C, R_L = 150 Ω.

Figure 38 and Figure 39 show the typical noninverting and inverting configurations and the recommended bypass capacitor values.

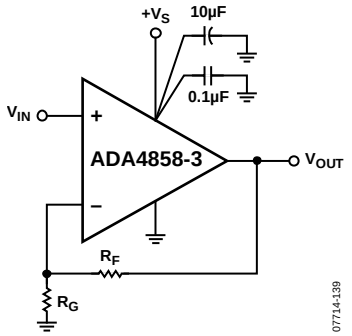

Figure 38. Noninverting Gain Configuration

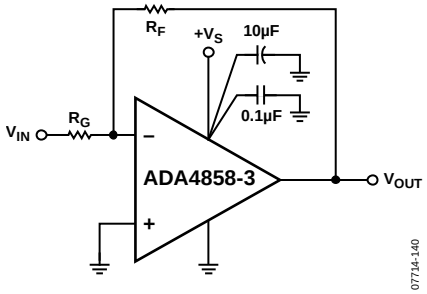

Figure 39. Inverting Gain Configuration

DC-COUPLED VIDEO SIGNAL

The ADA4858-3 does not have a rail-to-rail output stage. The output can be within 1 V of the rails. Having a charge pump on board that can provide −3 V on a +5 V supply and −2 V on +3.3 V supply makes this part excellent for video applications. In dc-coupled applications, the black color has a 0 V voltage reference. This means that the output voltage should be able to reach 0 V, which is feasible with the presence of the charge pump. Figure 40 shows the schematic of a dc-coupled, single-supply application. It is similar to the dual-supply application in which the input is properly terminated with a 50 Ω resistor to ground. The amplifier itself is set at a gain of 2 to account for the input termination loss.

The choice of R_F and R_G should be carefully considered for maximum flatness vs. power dissipation trade-off. In this case, the flatness is over 90 MHz, which is more than the high definition video requirement.

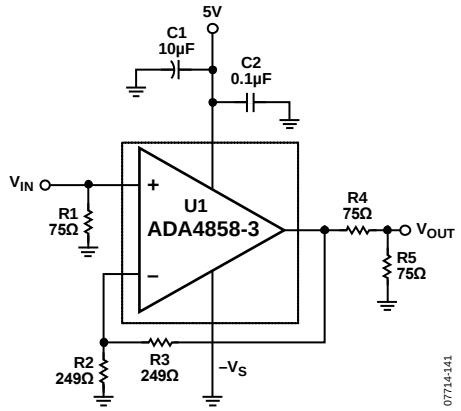

Figure 40. DC-Coupled, Single-Supply Schematic

MULTIPLE VIDEO DRIVER

In applications requiring that multiple video loads be driven simultaneously, the ADA4858-3 can deliver 5 V supply operation. Figure 41 shows the ADA4858-3 configured with two video loads, and Figure 42 shows the two video load performances.

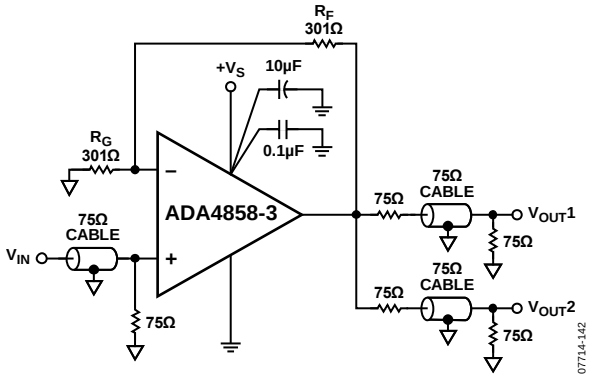

Figure 41. Video Driver Schematic for Two Video Loads

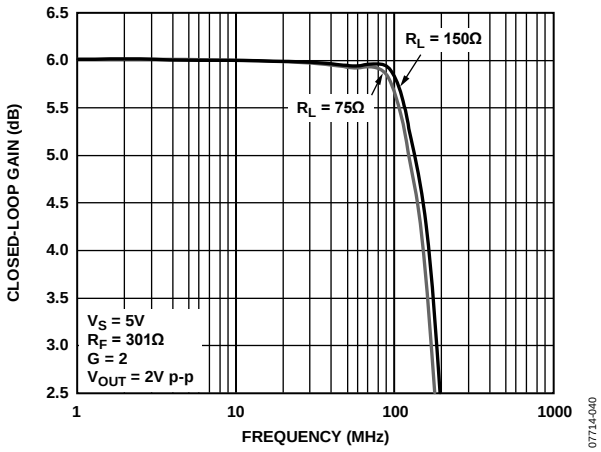

Figure 42. Large Signal Frequency Response for Various Loads

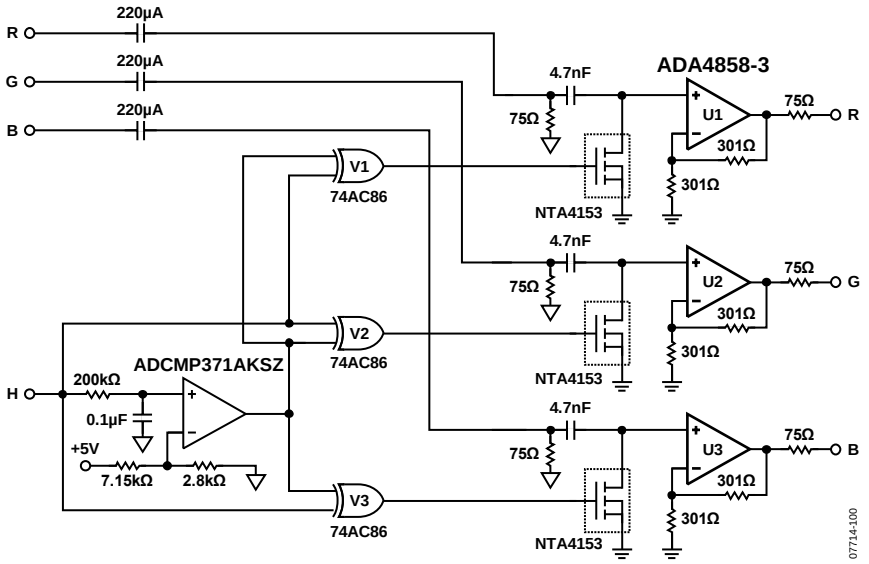

Figure 43. AC-Coupled Video Input with DC Restored Output

DC RESTORE FUNCTION

Having a charge pump gives the ability to take an ac-coupled input signal and restore its dc 0 V reference. The simplest way of accomplishing this is to use the blanking interval and the H-sync signal to set the 0 V reference. Use the H-sync to sample the dc level during the blanking interval to charge a capacitor and hold the charge during the video signal. Figure 43 shows the schematic of the dc restored circuit.

The H-sync coming out of the video source can be either positive or negative. This is why a polarity correction circuit is used to produce only a positive going H-sync. The H-sync is fed to a comparator that produces a high voltage if H-sync is negative and a low voltage if the H-sync is positive. The H-sync is then fed to an XOR with the output of the comparator. If the original H-sync was negative, the output of the XOR is positive because of the logic high coming from the comparator, causing the XOR to act as an inverter. However, if the original H-sync is positive, it stays the same because the output of the comparator is low and the XOR acts as a buffer.

The result is a positive going H-sync triggering the MOSFET during the blanking interval. This shorts the 4.7 nF capacitor to ground, which causes it to charge up by the dc level of the current signal. When the H-sync goes low, the MOSFET opens and the capacitor holds the charge during the video signal, making the output signal referenced to ground or 0 V level.

CLAMP AMPLIFIER

In some applications, a current output DAC driving a resistor may not have a negative supply available. In such case, the YPbPr video signal may be shifted up by 300 mV to avoid clamping the sync tip. These applications require a signal dc clamp on the output of the video driver to restore the dc level to 0 V reference. The ADA4858-3 has a charge pump that allows the output to swing negative; twice the sync tip (−600 mV) in G = 2 configuration.

Figure 44 shows the ADA4858-3 in a difference amplifier configuration. The video signal is connected to the noninverting side, and a dc bias of 600 mV is injected on the inverting side.

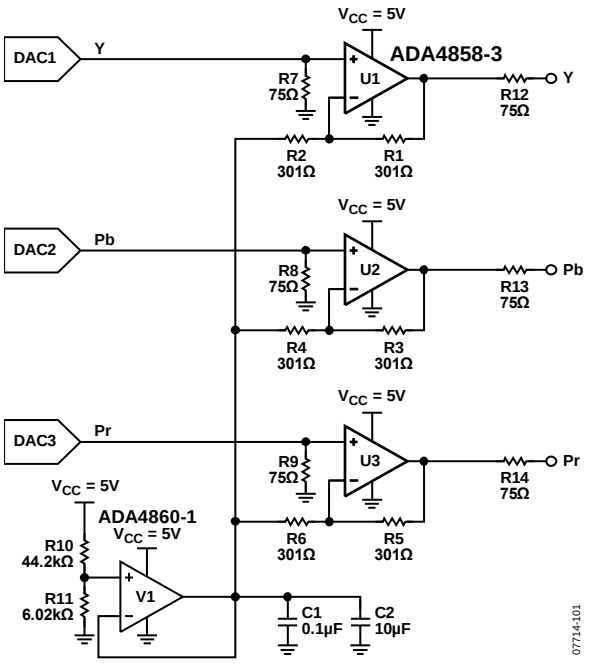

Figure 44. Clamp Amp

PD (POWER-DOWN) PIN

The ADA4858-3 is equipped with a PD (power-down) pin for all three amplifiers. This allows the user to reduce the quiescent supply current when an amplifier is not active. The power-down threshold levels are derived from ground level. The amplifiers are powered down when the voltage applied to the PD pin is greater than a certain voltage from ground. In a 5 V supply application, the voltage is greater than 2 V, and in a 3.3 V supply application, the voltage is greater than 1.5 V. The amplifier is enabled whenever the PD pin is connected to ground. If the PD pin is not used, it is best to connect it to ground. Note that the power-down feature does not control the charge pump output voltage and current.

Table 6. Power-Down Voltage Control

PD Pin	5 V	3.3 V
Not active	<1.5 V	<1 V
Active	>2 V	>1.5 V

POWER SUPPLY BYPASSING

Careful attention must be paid to bypassing the power supply pins of the ADA4858-3. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize supply voltage ripple and power dissipation. A large, usually tantalum, capacitor between 2.2 µF to 47 µF located in proximity to the ADA4858-3 is required to provide good decoupling for lower frequency signals. The actual value is determined by the circuit transient and frequency requirements. In addition, place 0.1 µF MLCC decoupling capacitors as close to each of the power supply pins and across from both supplies as is physically possible, no more than 1/8 inch away. The ground returns should terminate immediately into the ground plane. Placing the bypass capacitor return close to the load return minimizes ground loops and improves performance.

LAYOUT

As is the case with all high speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. The ADA4858-3 can operate at up to 600 MHz; therefore, proper RF design techniques must be employed. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near and under the input and output pins reduces stray capacitance. Keep signal lines connecting the feedback and gain resistors as short as possible to minimize the inductance and stray capacitance associated with these traces. Place termination resistors and loads as close as possible to their respective inputs and outputs. Keep input and output traces as far apart as possible to minimize coupling (crosstalk) through the board. Adherence to microstrip or stripline design techniques for long signal traces (greater than 1 inch) is recommended. For more information on high speed board layout, see "A Practical Guide to High-Speed Printed-Circuit-Board Layout," Analog Dialogue, Volume 39, Number 3, September 2005.

OUTLINE DIMENSIONS

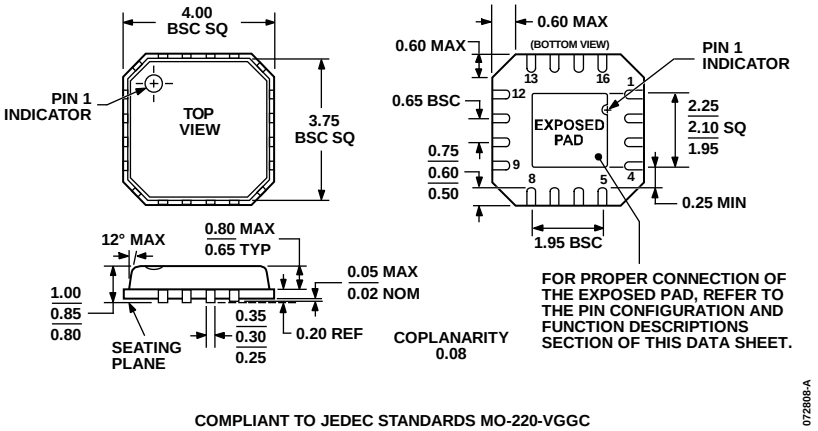

Figure 45.16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4858-3ACPZ-R2	–40°C to +105°C	16-Lead LFCSP_VQ	CP-16-4	250
ADA4858-3ACPZ-R7	–40°C to +105°C	16-Lead LFCSP_VQ	CP-16-4	1,500
ADA4858-3ACPZ-RL	–40°C to +105°C	16-Lead LFCSP_VQ	CP-16-4	5,000
ADA4858-3ACP-EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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