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1/2013—Revision 0: Initial Version

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SPECIFICATIONS

DC SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C.

Table 1.

	AD9119			AD9129			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		11			14		Bits
ACCURACY							
Integral Nonlinearity (INL)		0.2			1.4		LSB
Differential Nonlinearity (DNL)		0.15			1.1		LSB
ANALOG OUTPUTS							
Gain Error (with Internal Reference)		+2.5			+2.5		%
Full-Scale Output Current Maximum	33.4	34.2	34.9	33.4	34.2	34.9	mA
Full-Scale Output Current Minimum	9.1	9.4	9.6	9.1	9.4	9.6	mA
Output Compliance Range	1.5		2.5	1.5		2.5	V
Output Impedance[1]							
DAC CLOCK INPUT (DACCLK_P, DACCLK_N)							
Differential Peak-to-Peak Voltage	0.4	1	2	0.4	1	2	V
Common-Mode Voltage		1.2			1.2		V
TEMPERATURE DRIFT							
Gain		60			60		ppm/°C
Reference Voltage		20			20		ppm/°C
REFERENCE							
Internal Reference Voltage		1.0			1.0		V
Output Resistance		5			5		kΩ
ANALOG SUPPLY VOLTAGES							
VDDA	1.70	1.80	1.90	1.70	1.80	1.90	V
FIR40 Enabled, DACCLK > 2600 MSPS	1.8	1.9	2.0	1.8	1.9	2.0	V
VSSA	−1.4	−1.5	−1.6	−1.4	−1.5	−1.6	V
DIGITAL SUPPLY VOLTAGES							
VDD	1.70	1.8	1.90	1.70	1.8	1.90	V
FIR40 Enabled, DACCLK > 2600 MSPS	1.8	1.9	2.0	1.8	1.9	2.0	V
SUPPLY CURRENTS AND POWER DISSIPATION, 2.3 GSPS (NORMAL MODE)							
I_{VDDA}		202	209		202	209	mA
I_{VSSA}		53	54		53	54	mA
I_{DVDD}		307	327		307	327	mA
Power Dissipation							
Normal Mode		1.0	1.05		1.0	1.05	W
FIR25 Enabled		1.17	1.24		1.17	1.24	W
FIR40 Enabled		1.3	1.4		1.3	1.4	W
Reduced Power Mode, Power-Down Enabled (Register 0x01 = 0xEF)							
I_{VDDA}		7.6			7.6		mA
I_{VSSA}		6			6		µA
I_{VDD}		0.4			0.4		mA
SUPPLY CURRENTS AND POWER DISSIPATION, 2.8 GSPS (NORMAL MODE)							
I_{VDDA}		230			230		mA
I_{VSSA}		53			53		mA
I_{DVDD}		336			336		mA
Power Dissipation (Normal Mode)		1.1			1.1		W

[1] For more information about output impedance, see the Output Stage Configuration section.

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LVDS DIGITAL SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C. LVDS drivers and receivers are compatible with the IEEE Standard 1596.3-1996, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LVDS DATA INPUTS (P1_D[13:0]P, P1_D[13:0]N, P0_D[13:0]P, P0_D[13:0]N, FRM_P, FRM_N)		Px_DxP = V_{IA}, Px_DxN = V_{IB}				
Input Voltage Range	V_{IA}, V_{IB}		825		1575	mV
Input Differential Threshold	V_{IDTH}		−100		+100	mV
Input Differential Hysteresis	$V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance	R_{IN}		80		120	Ω
LVDS Input Rate			1425			MSPS
Input Capacitance				1.2		pF
LVDS CLOCK INPUTS (DCI_P, DCI_N)		DCI_P = V_{IA}, DCI_N = V_{IB}				
Input Voltage Range	V_{IA}, V_{IB}		825		1575	mV
Input Differential Threshold	V_{IDTH}		−225		+225	mV
Input Differential Hysteresis	$V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance	R_{IN}		80		120	Ω
Maximum Clock Rate			712.5			MHz
LVDS CLOCK OUTPUTS (DCO_P, DCO_N)		DCO_P = V_{OA}, DCO_N = V_{OB}, 100 Ω termination				
Output Voltage High	V_{OA}, V_{OB}				1375	mV
Output Voltage Low	V_{OA}, V_{OB}		1025			mV
Output Differential Voltage	$\|V_{OA}\|$, $\|V_{OB}\|$	Register 0x7C[7:6] = 01b (default)	200	225	250	mV
Output Offset Voltage	V_{OS}		1150		1250	mV
Output Impedance, Single-Ended	R_O		80	100	120	Ω
R_O Mismatch Between A and B	ΔR_O				10	%
Change in $\|V_{OD}\|$ Between Setting 0 and Setting 1	$\|\Delta V_{OD}\|$				25	mV
Change in V_{OS} Between Setting 0 and Setting 1	ΔV_{OS}				25	mV
Output Current						
Driver Shorted to Ground	I_{SA}, I_{SB}				20	mA
Drivers Shorted Together	I_{SAB}				4	mA
Power-Off Output Leakage	$\|I_{XA}\|$, $\|I_{XB}\|$				10	µA
Maximum Clock Rate			712.5			MHz

HSTL DIGITAL SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C. HSTL receiver levels are compatible with the EIA/JEDEC JESD8-6 standard, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
HSTL DATA INPUTS (P1_D[13:0]P, P1_D[13:0]N, P0_D[13:0]P, P0_D[13:0]N, FRM_P, FRM_N)		Px_DxP = V_{IA}, Px_DxN = V_{IB}				
Common-Mode Input Voltage Range	V_{IA}, V_{IB}		0.68		0.9	V
Differential Input Voltage			200			mV
Receiver Differential Input Impedance	R_{IN}		80		120	Ω
HSTL Input Rate			1425			MSPS
Input Capacitance				1.2		pF
HSTL CLOCK INPUT (DCI_P, DCI_N)		DCI_P = V_{IA}, DCI_N = V_{IB}				
Common-Mode Input Voltage Range	V_{IA}, V_{IB}		0.68		0.9	mV
Differential Input Voltage			450			mV
Receiver Differential Input Impedance	R_{IN}		80		120	Ω
Maximum Clock Rate			712.5			MHz

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SERIAL PORT AND CMOS PIN SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C.

Table 4.

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
WRITE OPERATION		See Figure 126				
SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$				20	MHz
SCLK Clock High	t_{HIGH}		20			ns
SCLK Clock Low	t_{LOW}		20			ns
SDIO to SCLK Setup Time	t_{DS}		10			ns
SCLK to SDIO Hold Time	t_{DH}		5			ns
$\overline{CS}$ to SCLK Setup Time	t_S		10			ns
SCLK to $\overline{CS}$ Hold Time	t_H		5			ns
READ OPERATION		See Figure 127				
SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$				20	MHz
SCLK Clock High	t_{HIGH}		20			ns
SCLK Clock Low	t_{LOW}		20			ns
SDIO to SCLK Setup Time	t_{DS}		10			ns
SCLK to SDIO Hold Time	t_{DH}		5			ns
$\overline{CS}$ to SCLK Setup Time	t_S		10			ns
SCLK to SDIO (or SDO) Data Valid Time	t_{DV}				10	ns
$\overline{CS}$ to SDIO (or SDO) Output Valid to High-Z	t_{EZ}			2		
INPUTS (SDI, SDIO, SCLK, $\overline{CS}$)						
Voltage In High	V_{IH}		1.2	1.8		V
Voltage In Low	V_{IL}			0	0.4	V
Current In High	I_{IH}				+75	µA
Current In Low	I_{IL}		−150			µA
OUTPUTS (SDIO, SYNC)						
Voltage Out High	V_{OH}		1.3		2.0	V
Voltage Out Low	V_{OL}		0		0.3	V
Current Out High	I_{OH}			4		mA
Current Out Low	I_{OL}			4		mA

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AC SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C, unless otherwise noted.

Table 5.

Parameter	AD9119 Min	AD9119 Typ	AD9119 Max	AD9129 Min	AD9129 Typ	AD9129 Max	Unit
DYNAMIC PERFORMANCE							
DAC Update Rate (DACCLK_x Inputs)							
Normal Mode, FIR25 Enabled, or FIR40 Enabled with VDD = 1.9 V	1400		2850	1400		2850	MSPS
FIR40 Filter Enabled, VDD = 1.8 V	1400		2600	1400		2600	MSPS
Adjusted DAC Update Rate[1]	1400		2850	1400		2850	MSPS
Output Settling Time to 0.1%		13			13		ns
SPURIOUS-FREE DYNAMIC RANGE (SFDR)							
f_{DAC} = 2600 MSPS							
f_{OUT} = 100 MHz		−76			−76		dBc
f_{OUT} = 350 MHz		−65			−65		dBc
f_{OUT} = 550 MHz		−63			−64		dBc
f_{OUT} = 950 MHz		−55			−55		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)							
f_{DAC} = 2600 MSPS, $f_{OUT2} = f_{OUT1}$ + 1.4 MHz							
f_{OUT} = 100 MHz		−82			−86		dBc
f_{OUT} = 350 MHz		−78			−85		dBc
f_{OUT} = 550 MHz		−73			−83		dBc
f_{OUT} = 950 MHz		−67			−76		dBc
NOISE SPECTRAL DENSITY (NSD)							
Single Tone, f_{DAC} = 2800 MSPS							
f_{OUT} = 100 MHz		−157			−166		dBm/Hz
f_{OUT} = 350MHz		−157			−162		dBm/Hz
f_{OUT} = 550 MHz		−155			−158		dBm/Hz
f_{OUT} = 850 MHz		−154			−157		dBm/Hz
DOCSIS ACLR PERFORMANCE (50 MHz to 1000 MHz) at ≥6 MHz OFFSET							
f_{DAC} = 2782 MSPS							
8 Contiguous Carriers		64			64		dBc
16 Contiguous Carriers		62			63		dBc
32 Contiguous Carriers		60			61		dBc
W-CDMA ACLR (SINGLE CARRIER)							
Adjacent Channel							
f_{DAC} = 2605.056 MSPS, f_{OUT} = 750 MHz		75			75		dBc
f_{DAC}= 2605.056 MSPS, f_{OUT} = 950 MHz		74			74		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 1700 MHz (Mix-Mode)		73.5			73.5		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 2100 MHz (Mix-Mode)		69			69		dBc
Alternate Adjacent Channel							
f_{DAC} = 2605.056 MSPS, f_{OUT} = 750 MHz		80			80		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 950 MHz		78			78		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 1700 MHz (Mix-Mode)		74			74		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 2100 MHz (Mix-Mode)		72			72		dBc

[1] Adjusted DAC update rate is calculated as f_{DAC} divided by the minimum required interpolation factor. For the AD9119/AD9129, the minimum interpolation factor is 1. Thus, with f_{DAC} = 2850 MSPS, f_{DAC} adjusted = 2850 MSPS.

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ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
DCI, DCO to VSS	−0.3 V to VDD + 0.3 V
LVDS Data Inputs to VSS	−0.3 V to VDD + 0.3 V
IOUTP, IOUTN to VSSA	VSSA − 0.3V to +2.5V
I250U, VREF to VSSA	VSSA − 0.3 V to VDDA + 0.3 V
IRQ, $\overline{CS}$, SCLK, SDO, SDIO, RESET, SYNC to VSS	−0.3 V to VDD + 0.3 V
Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
160-Ball CSP_BGA	31.2	7.0	°C/W[1]

[1] With no airflow movement.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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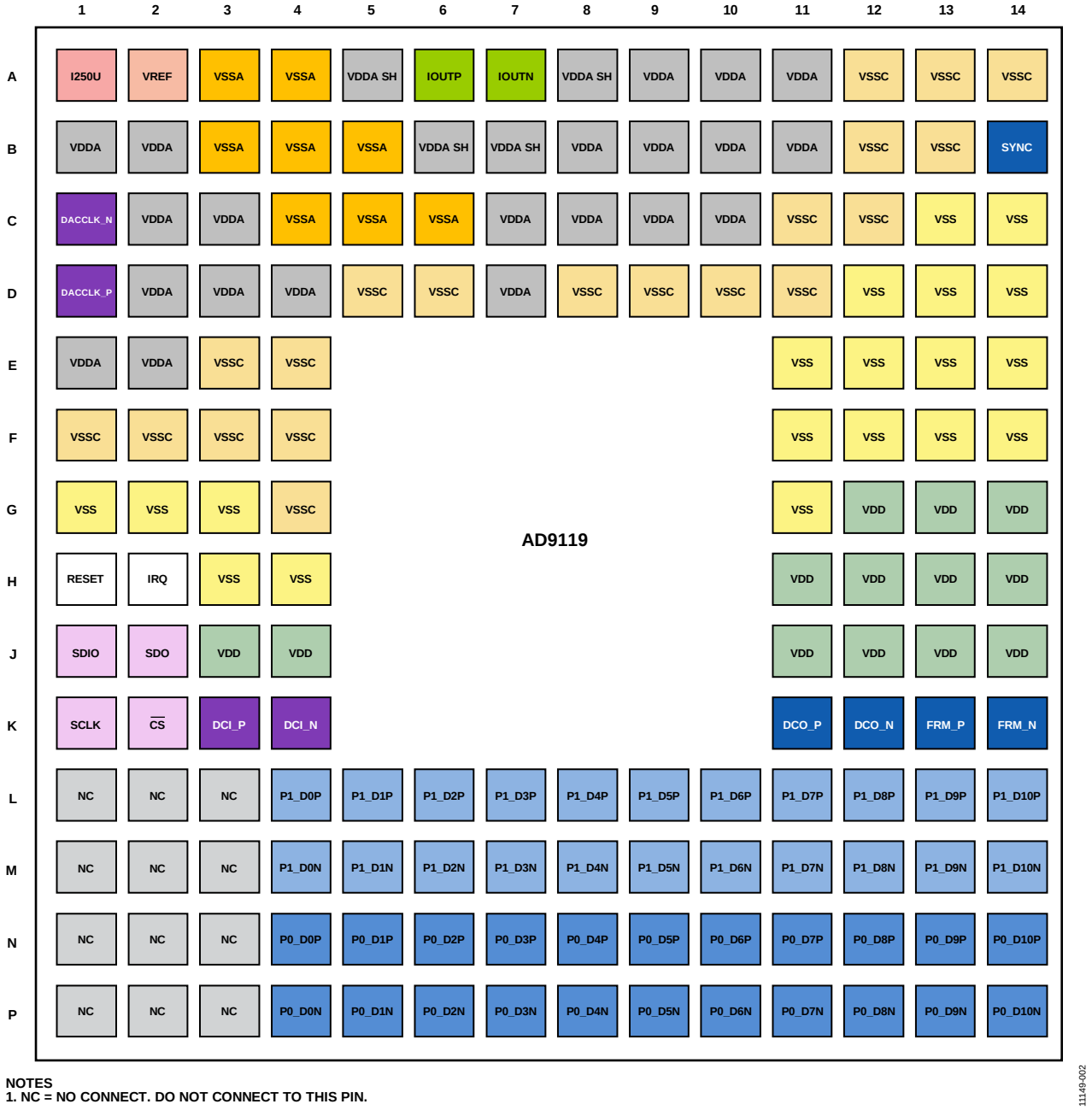
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 2. AD9119 Pin Configuration

Table 8. AD9119 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	I250U	Nominal 1.0 V Reference. Tie this pin to VSSA via a 4.0 kΩ resistor to generate a 250 µA reference current.
A2	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
A3, A4, B3, B4, B5, C4, C5, C6	VSSA	−1.5 V Analog Supply Voltage Input.
A5, A8, B6, B7	VDDA SH	+1.8 V Analog Supply Shield. Tie these pins to VDDA at the DAC.
A9, A10, A11, B1, B2, B8, B9, B10, B11, C2, C3, C7, C8, C9, C10, D2, D3, D4, D7, E1, E2	VDDA	+1.8 V Analog Supply Voltage Input.

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Pin No.	Mnemonic	Description
G12, G13, G14, H11, H12, H13, H14, J3, J4, J11, J12, J13, J14	VDD	+1.8 V Digital Supply Voltage Input.
C13, C14, D12, D13, D14, E11, E12, E13, E14, F11, F12, F13, F14, G1, G2, G3, G11, H3, H4	VSS	+1.8 V Digital Supply Return.
A12, A13, A14, B12, B13, C11, C12, D5, D6, D8, D9, D10, D11, E3, E4, F1, F2, F3, F4, G4	VSSC	Analog Supply Return.
A6	IOUTP	DAC Positive Current Output Source.
A7	IOUTN	DAC Negative Current Output Source.
B14	SYNC	Synchronization Signal Output.
C1, D1	DACCLK_N, DACCLK_P	Negative/Positive DAC Clock Input.
H1	RESET	Reset Input. Active high. If unused, tie this pin to VSS.
H2	IRQ	Interrupt Request Open Drain Output. Active high. Pull up this pin to VDD with a 1 kΩ resistor.
J1	SDIO	Serial Port Data Input/Output.
J2	SDO	Serial Port Data Output.
K1	SCLK	Serial Port Clock Input.
K2	$\overline{CS}$	Serial Port Enable Input.
K3, K4	DCI_P, DCI_N	Positive, Negative Data Clock Input (DCI).
K11, K12	DCO_P, DCO_N	Positive, Negative Data Clock Output (DCO).
K13, K14	FRM_P, FRM_N	Positive, Negative Data Frame/Parity Signal (FRAME/PARITY).
L1, M1	NC, NC	No Connect. Do not connect to this pin.
L2, M2	NC, NC	No Connect. Do not connect to this pin.
L3, M3	NC, NC	No Connect. Do not connect to this pin.
L4, M4	P1_D0P, P1_D0N	Data Port 1 Positive/Negative Data Input Bit 0. LSB.
L5, M5	P1_D1P, P1_D1N	Data Port 1 Positive/Negative Data Input Bit 1.
L6, M6	P1_D2P, P1_D2N	Data Port 1 Positive/Negative Data Input Bit 2.
L7, M7	P1_D3P, P1_D3N	Data Port 1 Positive/Negative Data Input Bit 3.
L8, M8	P1_D4P, P1_D4N	Data Port 1 Positive/Negative Data Input Bit 4.
L9, M9	P1_D5P, P1_D5N	Data Port 1 Positive/Negative Data Input Bit 5.
L10, M10	P1_D6P, P1_D6N	Data Port 1 Positive/Negative Data Input Bit 6.
L11, M11	P1_D7P, P1_D7N	Data Port 1 Positive/Negative Data Input Bit 7.
L12,M12	P1_D8P, P1_D8N	Data Port 1 Positive/Negative Data Input Bit 8.
L13, M13	P1_D9P, P1_D9N	Data Port 1 Positive/Negative Data Input Bit 9.
L14, M14	P1_D10P, P1_D10N	Data Port 1 Positive/Negative Data Input Bit 10. MSB.
N1, P1	NC, NC	No Connect. Do not connect to this pin.
N2, P2	NC, NC	No Connect. Do not connect to this pin.
N3, P3	NC, NC	No Connect. Do not connect to this pin.
N4, P4	P0_D0P, P0_D0N	Data Port 0 Positive/Negative Data Input Bit 0. LSB.
N5, P5	P0_D1P, P0_D1N	Data Port 0 Positive/Negative Data Input Bit 1.
N6, P6	P0_D2P, P0_D2N	Data Port 0 Positive/Negative Data Input Bit 2.
N7, P7	P0_D3P, P0_D3N	Data Port 0 Positive/Negative Data Input Bit 3.
N8, P8	P0_D4P, P0_D4N	Data Port 0 Positive/Negative Data Input Bit 4.
N9, P9	P0_D5P, P0_D5N	Data Port 0 Positive/Negative Data Input Bit 5.
N10, P10	P0_D6P, P0_D6N	Data Port 0 Positive/Negative Data Input Bit 6.
N11, P11	P0_D7P, P0_D7N	Data Port 0 Positive/Negative Data Input Bit 7.
N12, P12	P0_D8P, P0_D8N	Data Port 0 Positive/Negative Data Input Bit 8.
N13, P13	P0_D9P, P0_D9N	Data Port 0 Positive/Negative Data Input Bit 9.
N14, P14	P0_D10P, P0_D10N	Data Port 0 Positive/Negative Data Input Bit 10. MSB.

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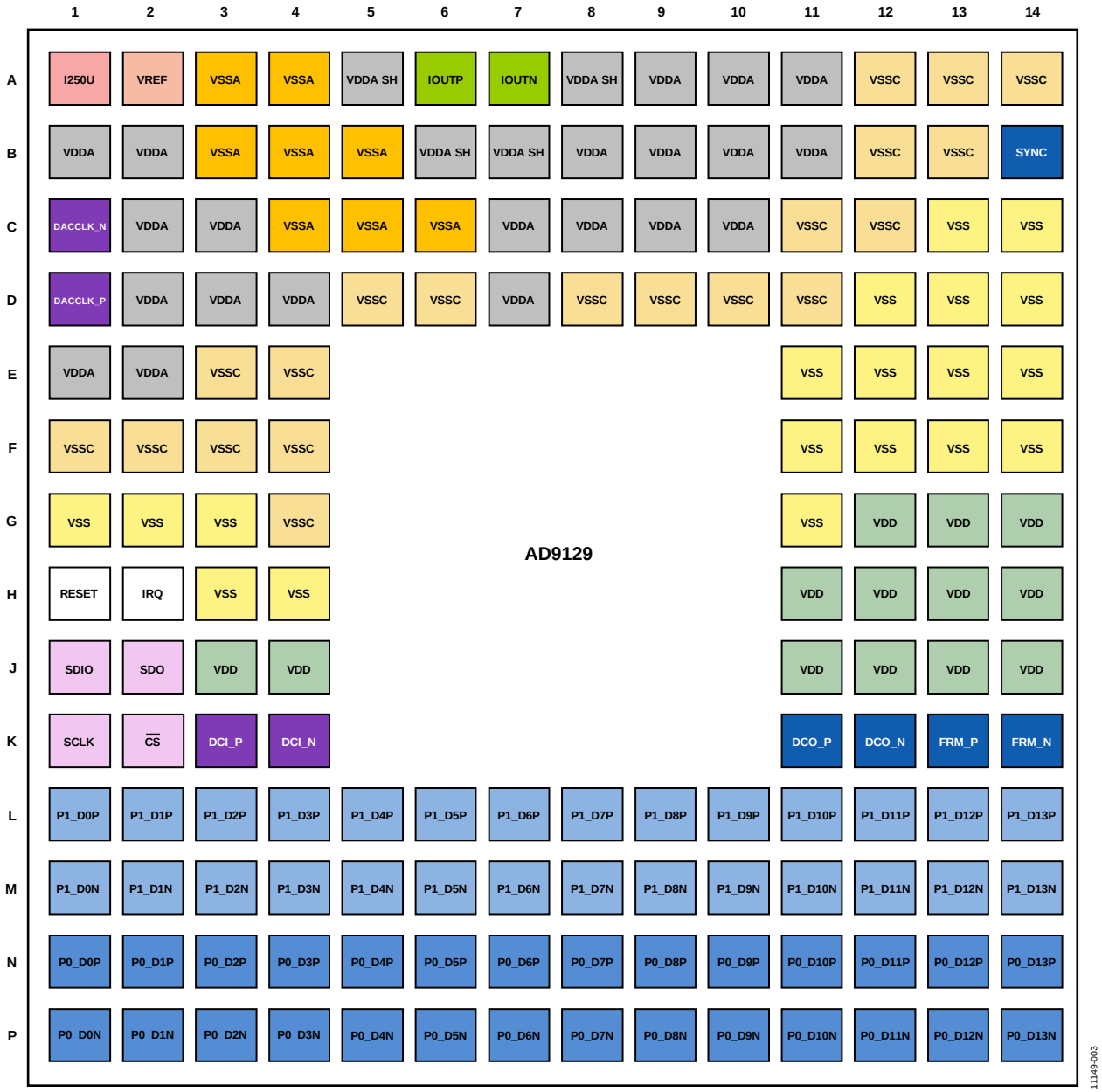

Figure 3. AD9129 Pin Configuration

Table 9. AD9129 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	I250U	Nominal 1.0 V Reference. Tie this pin to VSSA via a 4.0 kΩ resistor to generate a 250 µA reference current.
A2	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
A3, A4, B3, B4, B5, C4, C5, C6	VSSA	−1.5 V Analog Supply Voltage Input.
A5, A8, B6, B7	VDDA SH	+1.8 V Analog Supply Shield. Tie these pins to VDDA at the DAC.
A9, A10, A11, B1, B2, B8, B9, B10, B11, C2, C3, C7, C8, C9, C10, D2, D3, D4, D7, E1, E2	VDDA	+1.8 V Analog Supply Voltage Input.
G12, G13, G14, H11, H12, H13, H14, J3, J4, J11, J12, J13, J14	VDD	+1.8 V Digital Supply Voltage Input.
C13, C14, D12, D13, D14, E11, E12, E13, E14, F11, F12, F13, F14, G1, G2, G3, G11, H3, H4	VSS	+1.8 V Digital Supply Return.

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Pin No.	Mnemonic	Description
A12, A13, A14, B12, B13, C11, C12, D5, D6, D8, D9, D10, D11, E3, E4, F1, F2, F3, F4, G4	VSSC	Analog Supply Return.
A6	IOUTP	DAC Positive Current Output Source.
A7	IOUTN	DAC Negative Current Output Source.
B14	SYNC	Synchronization Signal Output.
C1, D1	DACCLK_N, DACCLK_P	Negative/Positive DAC Clock Input.
H1	RESET	Reset Input. Active high. If unused, tie this pin to VSS.
H2	IRQ	Interrupt Request Open-Drain Output. Active high. Pull up this pin to VDD with a 1 kΩ resistor.
J1	SDIO	Serial Port Data Input/Output.
J2	SDO	Serial Port Data Output.
K1	SCLK	Serial Port Clock Input.
K2	$\overline{CS}$	Serial Port Enable Input.
K3, K4	DCI_P, DCI_N	Positive, Negative Data Clock Input (DCI).
K11, K12	DCO_P, DCO_N	Positive, Negative Data Clock Output (DCO).
K13, K14	FRM_P, FRM_N	Positive, Negative Data Frame/Parity Signal (FRAME/PARITY).
L1, M1	P1_D0P, P1_D0N	Data Port 1 Positive/Negative Data Input Bit 0. LSB.
L2, M2	P1_D1P, P1_D1N	Data Port 1 Positive/Negative Data Input Bit 1.
L3, M3	P1_D2P, P1_D2N	Data Port 1 Positive/Negative Data Input Bit 2.
L4, M4	P1_D3P, P1_D3N	Data Port 1 Positive/Negative Data Input Bit 3.
L5, M5	P1_D4P, P1_D4N	Data Port 1 Positive/Negative Data Input Bit 4.
L6, M6	P1_D5P, P1_D5N	Data Port 1 Positive/Negative Data Input Bit 5.
L7, M7	P1_D6P, P1_D6N	Data Port 1 Positive/Negative Data Input Bit 6.
L8, M8	P1_D7P, P1_D7N	Data Port 1 Positive/Negative Data Input Bit 7.
L9, M9	P1_D8P, P1_D8N	Data Port 1 Positive/Negative Data Input Bit 8.
L10, M10	P1_D9P, P1_D9N	Data Port 1 Positive/Negative Data Input Bit 9.
L11, M11	P1_D10P, P1_D10N	Data Port 1 Positive/Negative Data Input Bit 10.
L12,M12	P1_D11P, P1_D11N	Data Port 1 Positive/Negative Data Input Bit 11.
L13, M13	P1_D12P, P1_D12N	Data Port 1 Positive/Negative Data Input Bit 12.
L14, M14	P1_D13P, P1_D13N	Data Port 1 Positive/Negative Data Input Bit 13. MSB.
N1, P1	P0_D0P, P0_D0N	Data Port 0 Positive/Negative Data Input Bit 0. LSB.
N2, P2	P0_D1P, P0_D1N	Data Port 0 Positive/Negative Data Input Bit 1.
N3, P3	P0_D2P, P0_D2N	Data Port 0 Positive/Negative Data Input Bit 2.
N4, P4	P0_D3P, P0_D3N	Data Port 0 Positive/Negative Data Input Bit 3.
N5, P5	P0_D4P, P0_D4N	Data Port 0 Positive/Negative Data Input Bit 4.
N6, P6	P0_D5P, P0_D5N	Data Port 0 Positive/Negative Data Input Bit 5.
N7, P7	P0_D6P, P0_D6N	Data Port 0 Positive/Negative Data Input Bit 6.
N8, P8	P0_D7P, P0_D7N	Data Port 0 Positive/Negative Data Input Bit 7.
N9, P9	P0_D8P, P0_D8N	Data Port 0 Positive/Negative Data Input Bit 8.
N10, P10	P0_D9P, P0_D9N	Data Port 0 Positive/Negative Data Input Bit 9.
N11, P11	P0_D10P, P0_D10N	Data Port 0 Positive/Negative Data Input Bit 10.
N12, P12	P0_D11P, P0_D11N	Data Port 0 Positive/Negative Data Input Bit 11.
N13, P13	P0_D12P, P0_D12N	Data Port 0 Positive/Negative Data Input Bit 12.
N14, P14	P0_D13P, P0_D13N	Data Port 0 Positive/Negative Data Input Bit 13. MSB.

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TYPICAL PERFORMANCE CHARACTERISTICS

AD9119

Static Linearity

I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

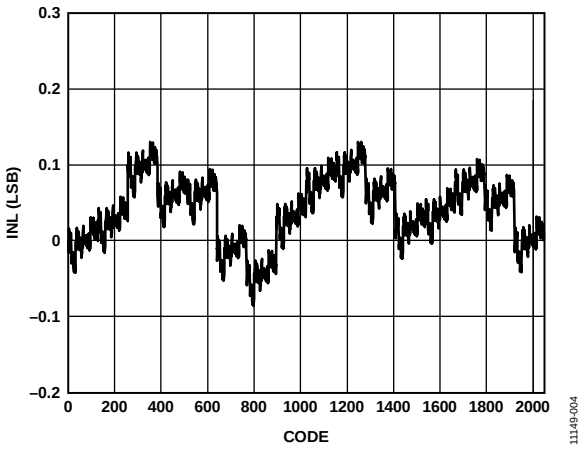

Figure 4. Typical INL, 11 mA at 25°C

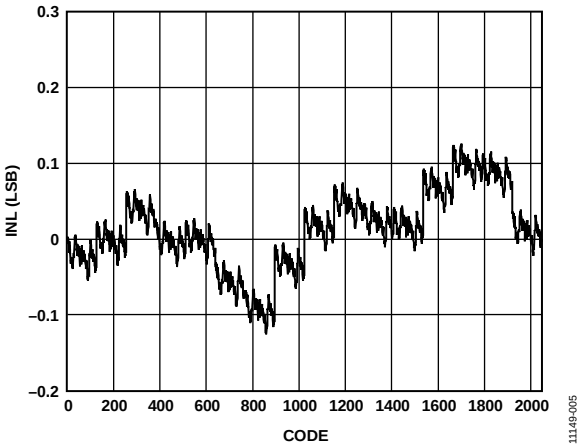

Figure 5. Typical INL, 22 mA at 25°C

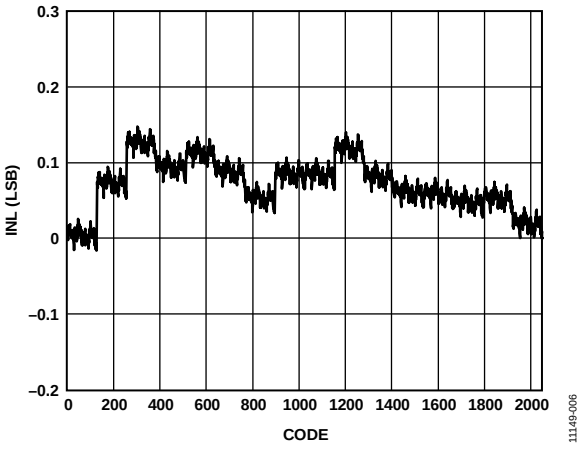

Figure 6. Typical INL, 33 mA at 25°C

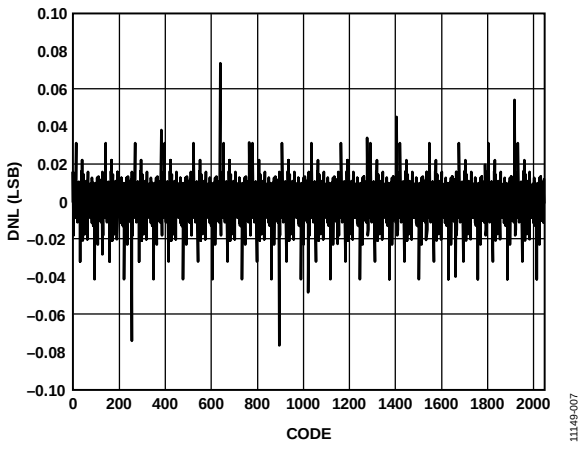

Figure 7. Typical DNL, 11 mA at 25°C

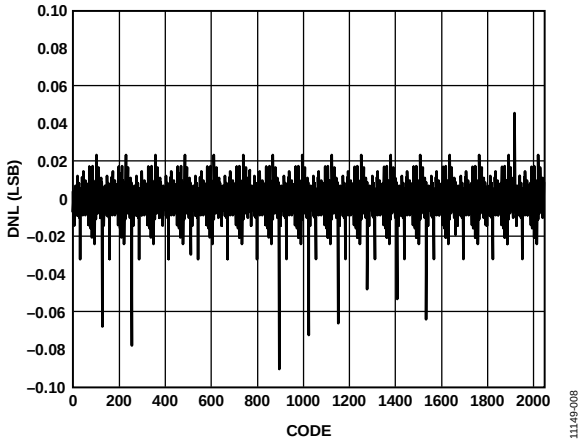

Figure 8. Typical DNL, 22 mA at 25°C

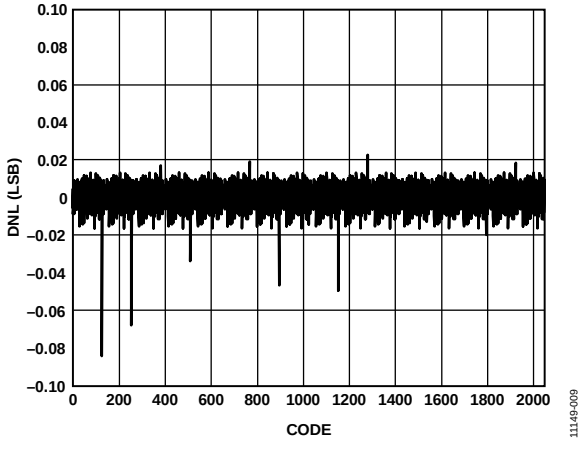

Figure 9. Typical DNL, 33 mA at 25°C

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AC (Normal Mode)

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

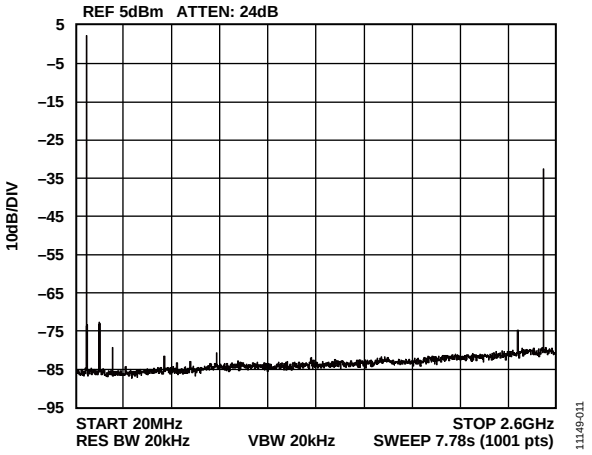

Figure 10. Single-Tone Spectrum at f_{OUT} = 70 MHz

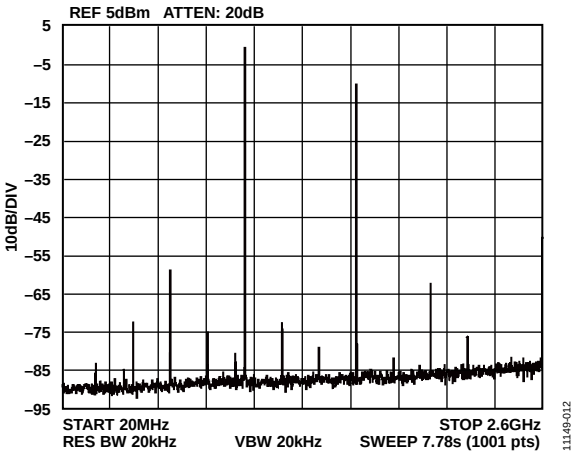

Figure 13. Single-Tone Spectrum at f_{OUT} = 1000 MHz

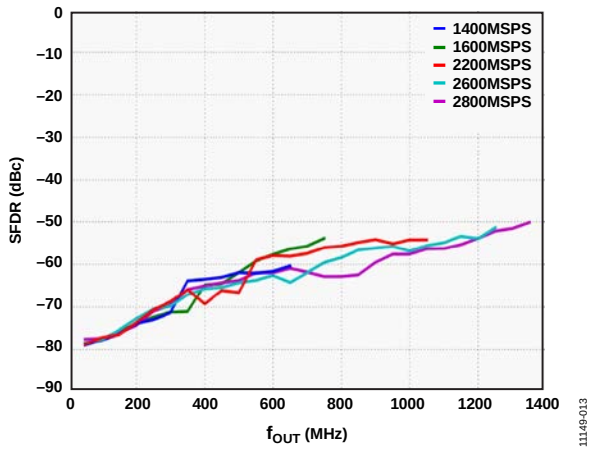

Figure 11. SFDR vs. f_{OUT} over f_{DAC}

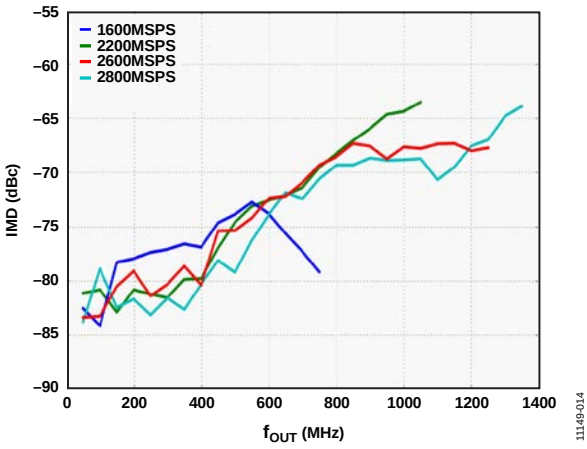

Figure 14. IMD vs. f_{OUT} over f_{DAC}

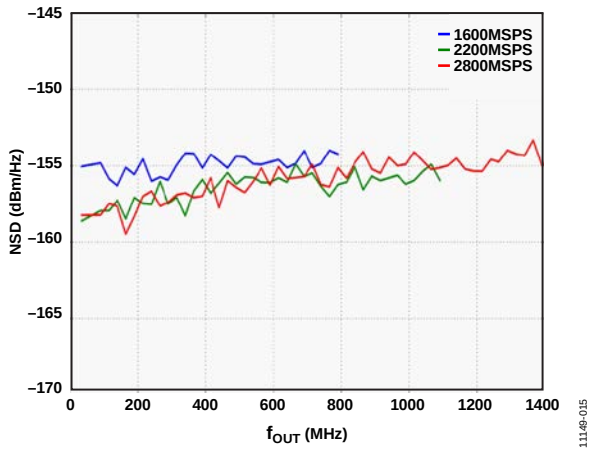

Figure 12. Single-Tone NSD vs. f_{OUT}

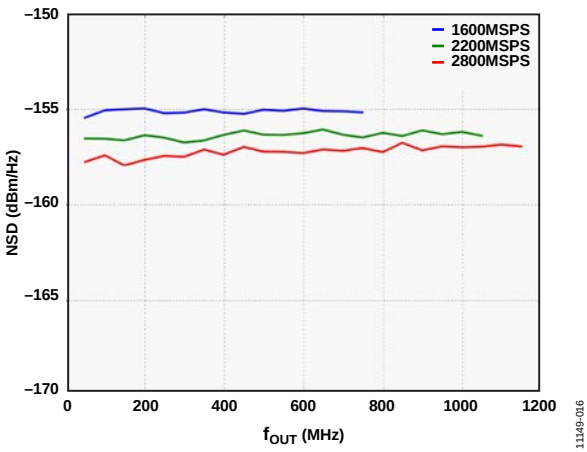

Figure 15. W-CDMA NSD vs. f_{OUT}

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

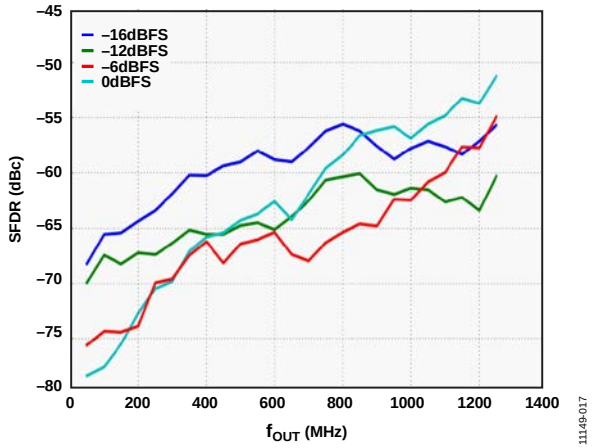

Figure 16. SFDR vs. f_{OUT} over Digital Full Scale

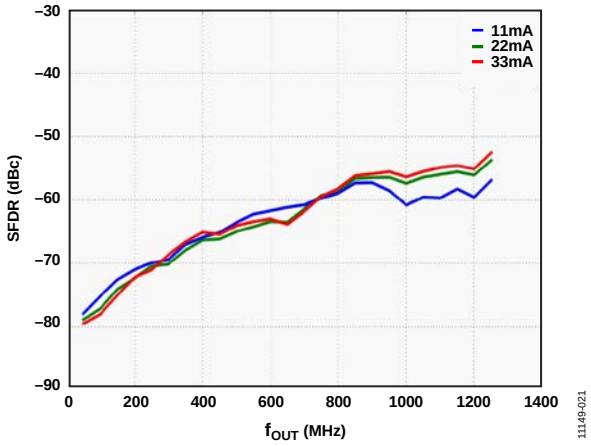

Figure 18. SFDR vs. f_{OUT} over DAC I_{OUTFS}

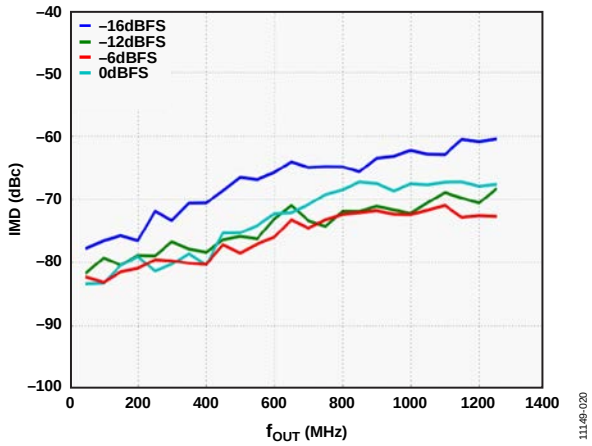

Figure 17. IMD vs. f_{OUT} over Digital Full Scale

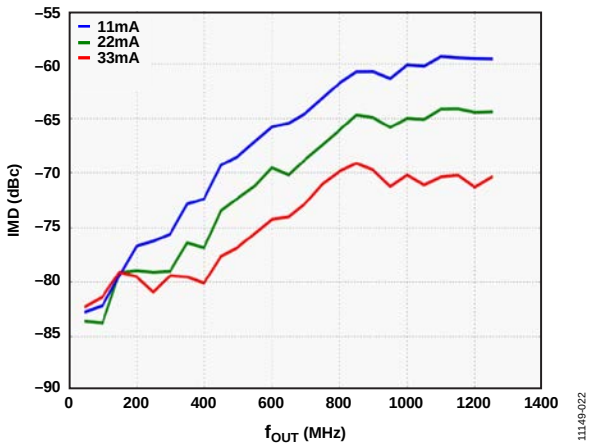

Figure 19. IMD vs. f_{OUT} over DAC I_{OUTFS}

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

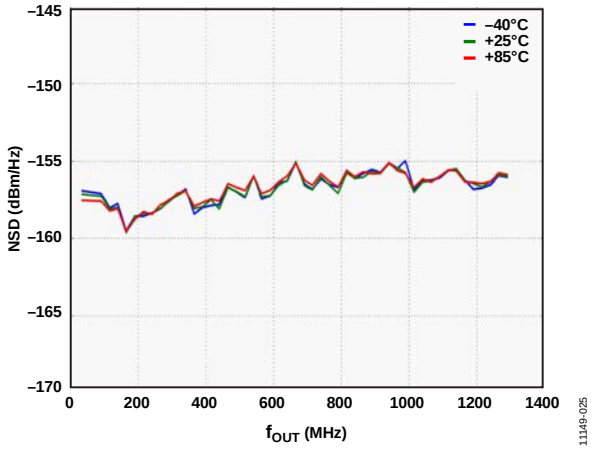

Figure 20. Single-Tone NSD vs. f_{OUT} over Temperature

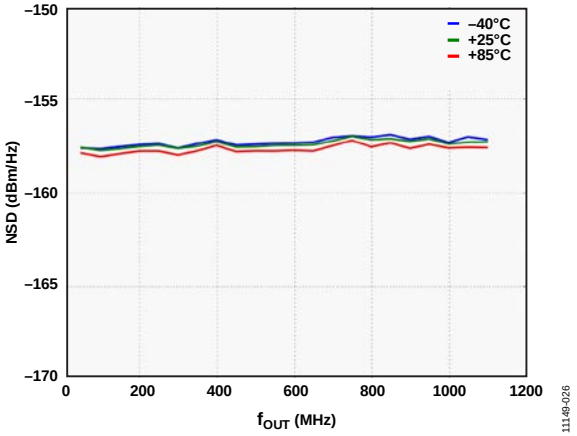

Figure 22. W-CDMA NSD vs. f_{OUT} over Temperature

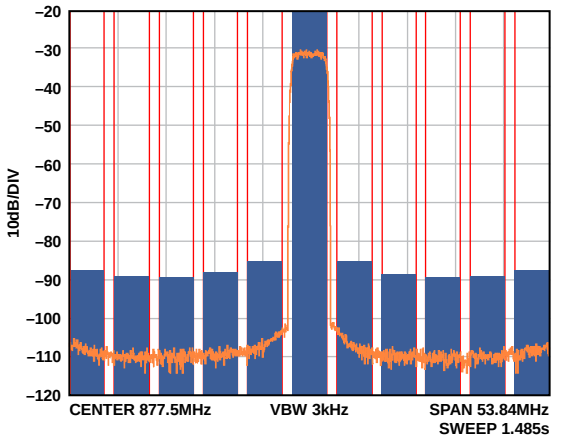

Figure 21. Single-Carrier W-CDMA at 877.5 MHz

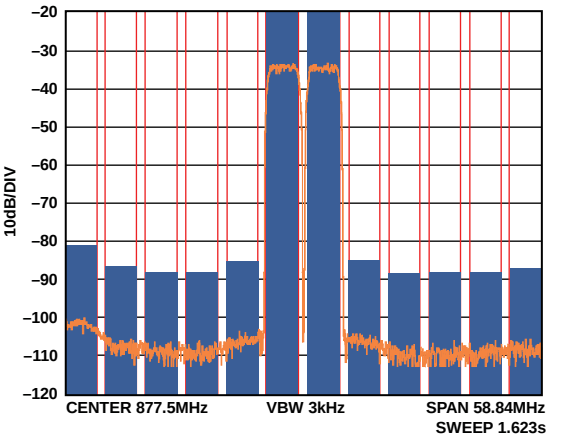

Figure 23. Two-Carrier W-CDMA at 877.5 MHz

Downloaded from Arrow.com.

AC (Mix-Mode)

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

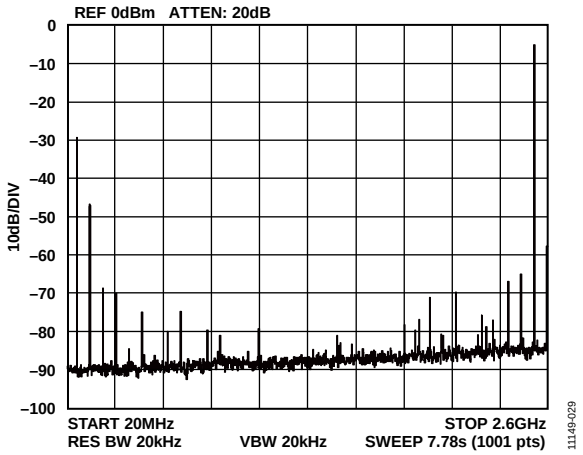

Figure 24. Single Tone Spectrum at f_{OUT} = 2350 MHz

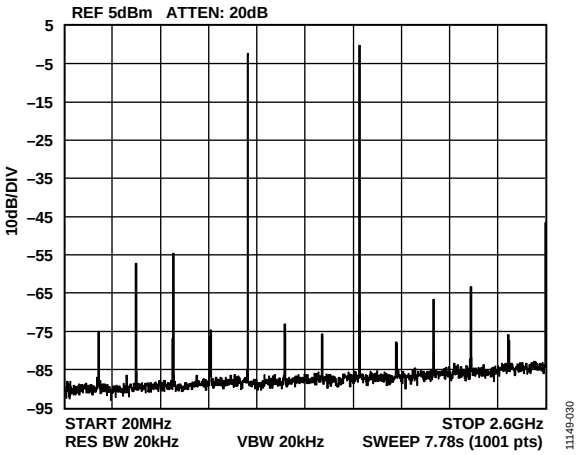

Figure 27. Single-Tone Spectrum at f_{OUT} = 1600 MHz

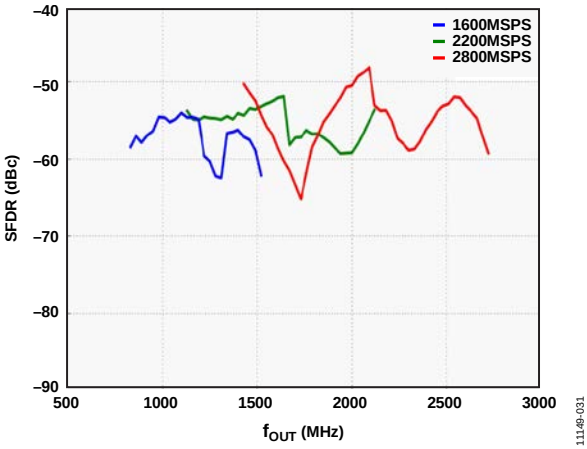

Figure 25. SFDR vs. f_{OUT} over f_{DAC}

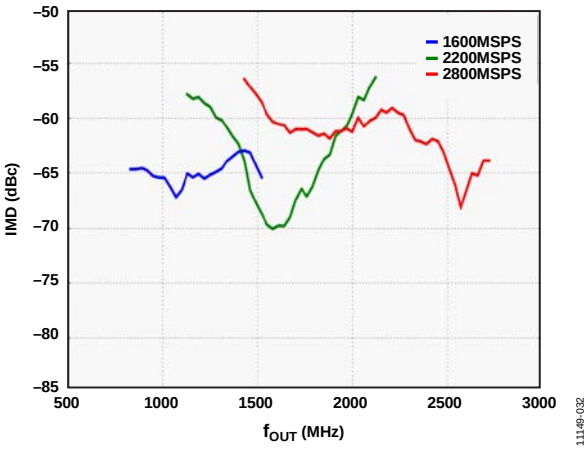

Figure 28. IMD vs. f_{OUT} over f_{DAC}

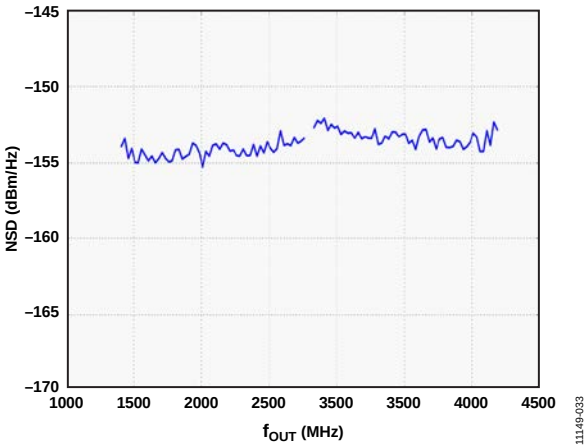

Figure 26. Single-Tone NSD vs. f_{OUT}

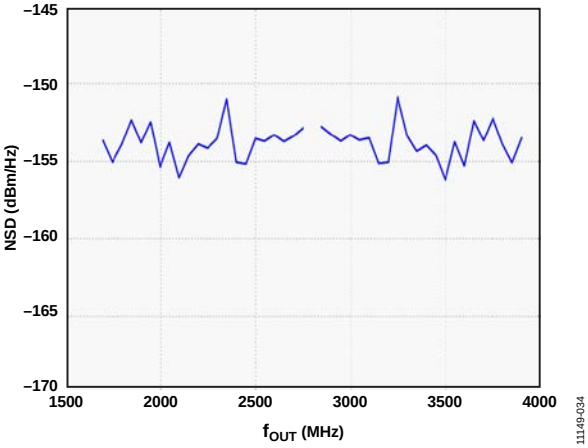

Figure 29. W-CDMA NSD vs. f_{OUT}

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

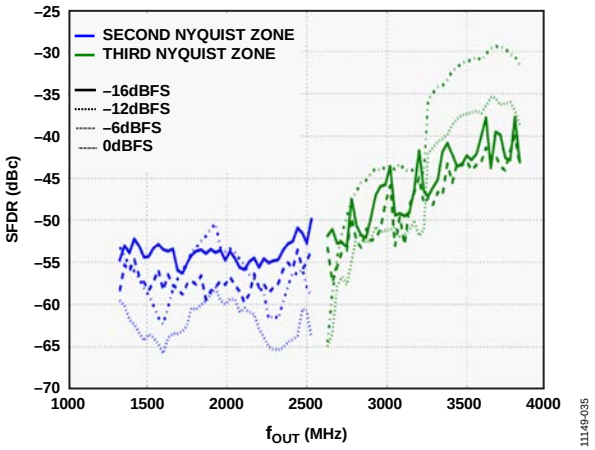

Figure 30. SFDR vs. f_{OUT} over Digital Full Scale

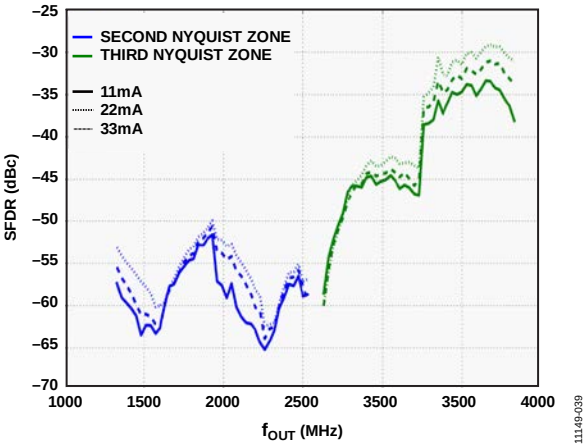

Figure 32. SFDR vs. f_{OUT} over DAC I_{OUTFS}

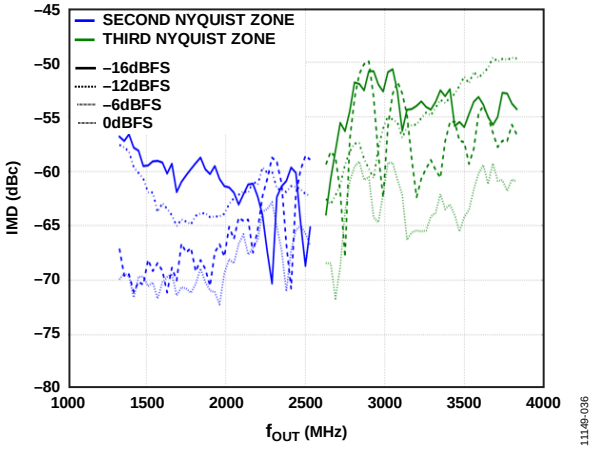

Figure 31. IMD vs. f_{OUT} over Digital Full Scale

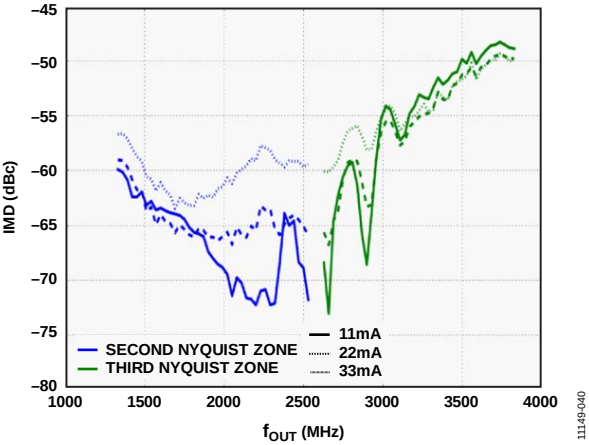

Figure 33. IMD vs. f_{OUT} over DAC I_{OUTFS}

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

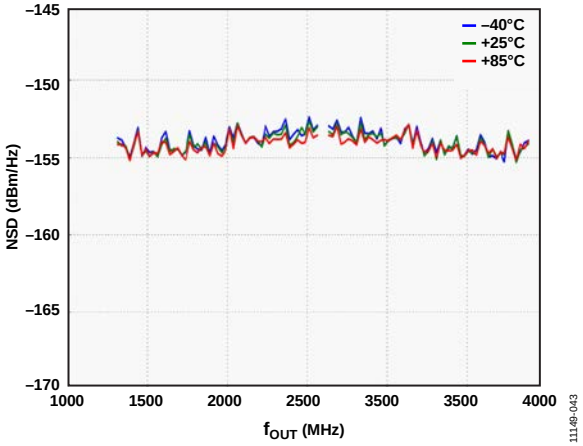

Figure 34. Single-Tone NSD vs. f_{OUT} over Temperature

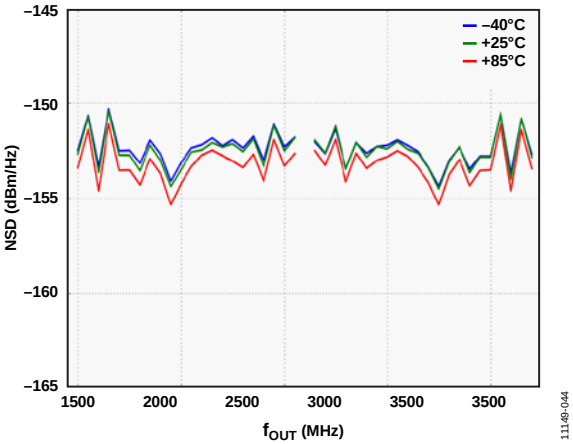

Figure 36. W-CDMA NSD vs. f_{OUT} over Temperature

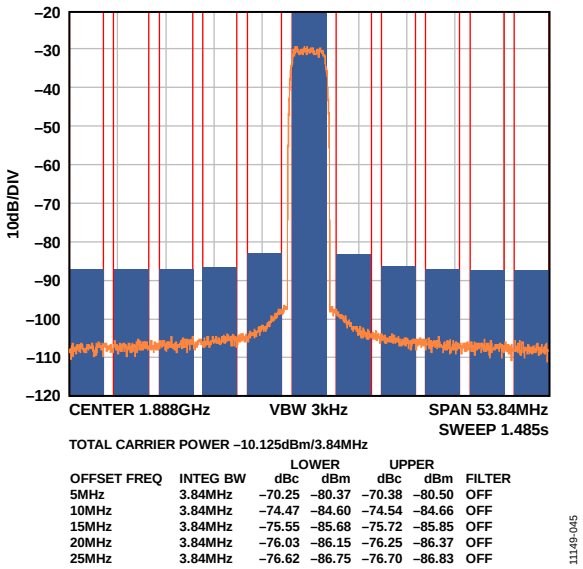

Figure 35. Single-Carrier W-CDMA at 1887.5 MHz

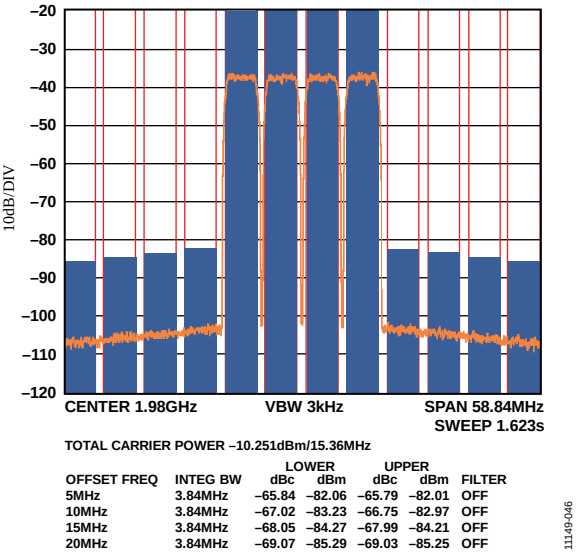

Figure 37. Four-Carrier W-CDMA at 1980 MHz

Downloaded from Arrow.com.

DOCSIS Performance (Normal Mode)

I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

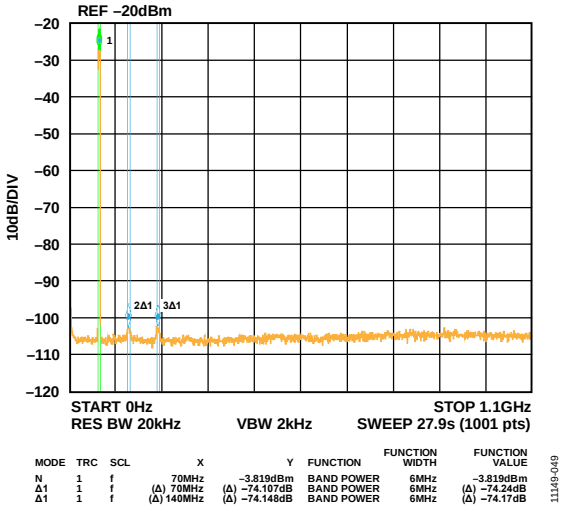

Figure 38. Single Carrier at 70 MHz Output

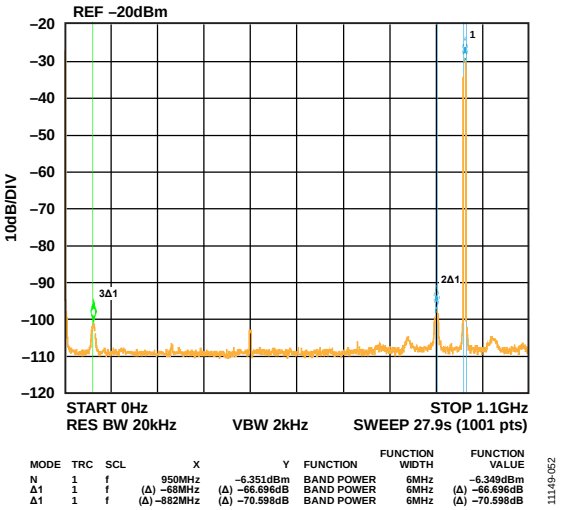

Figure 41. Single Carrier at 950 MHz Output

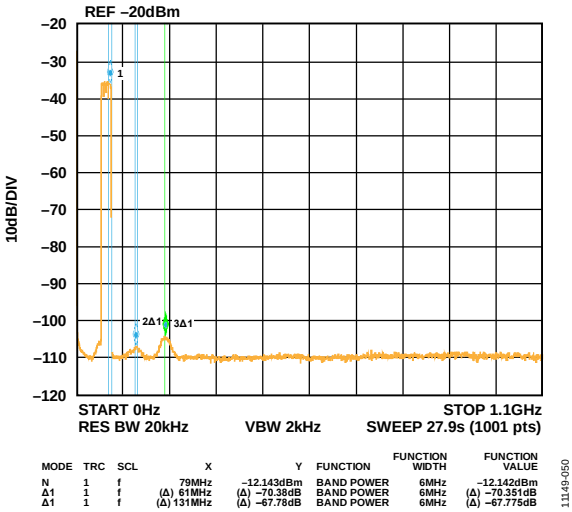

Figure 39. Four Carrier at 70 MHz Output

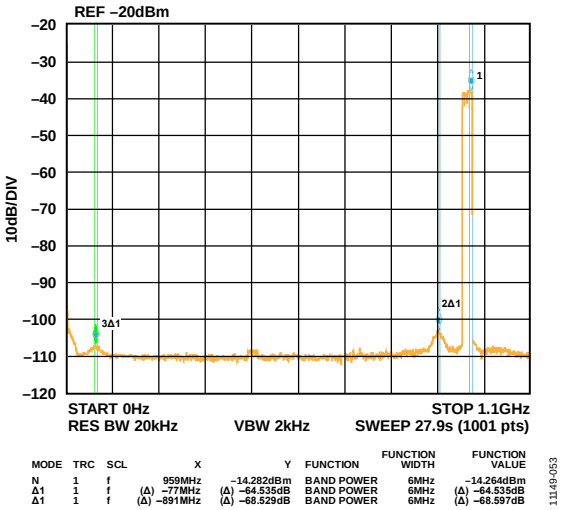

Figure 42. Four Carrier at 950 MHz Output

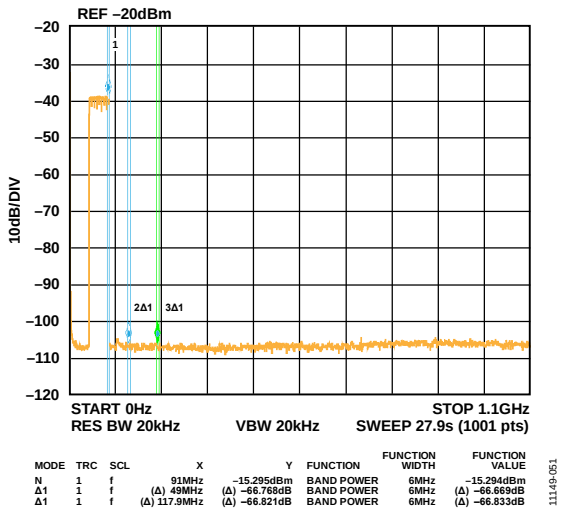

Figure 40. Eight Carrier at 70 MHz Output

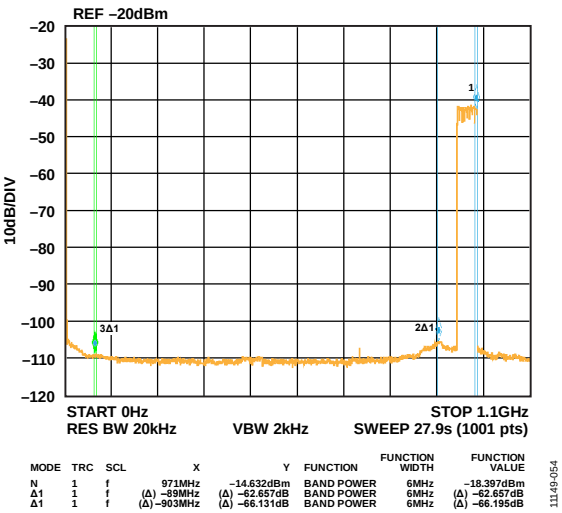

Figure 43. Eight Carrier at 950 MHz Output

Downloaded from Arrow.com.

I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

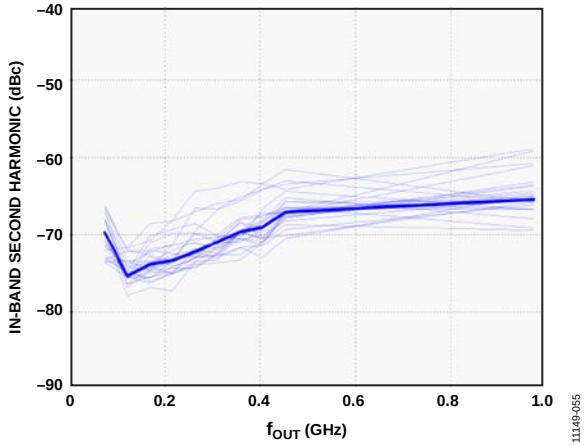

Figure 44. Second Harmonic vs. f_{OUT} Performance for One DOCSIS Carrier

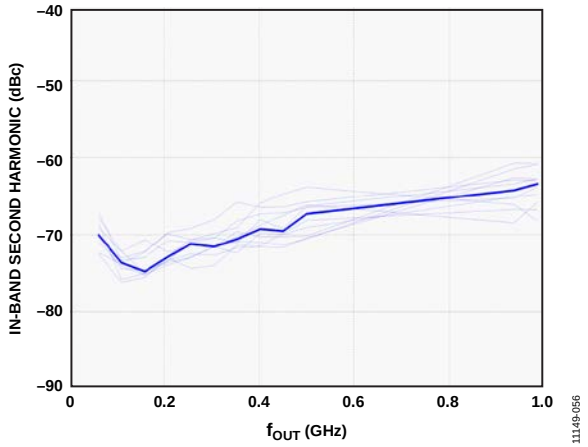

Figure 45. Second Harmonic vs. f_{OUT} Performance for Four DOCSIS Carriers

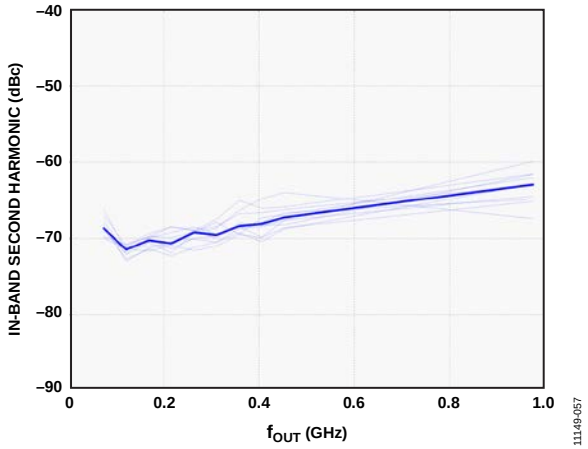

Figure 46. Second Harmonic vs. f_{OUT} Performance for Eight DOCSIS Carriers

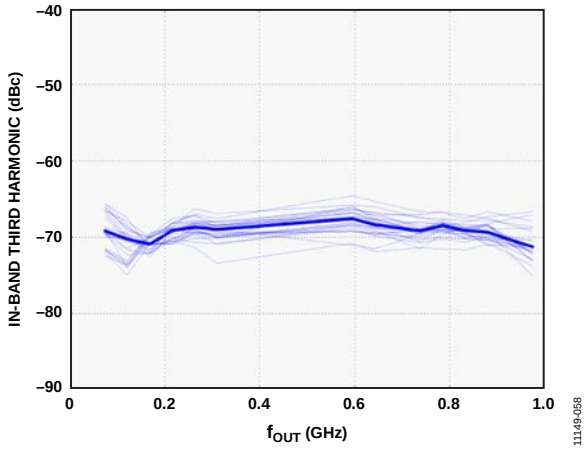

Figure 47. Third Harmonic vs. f_{OUT} Performance for One DOCSIS Carrier

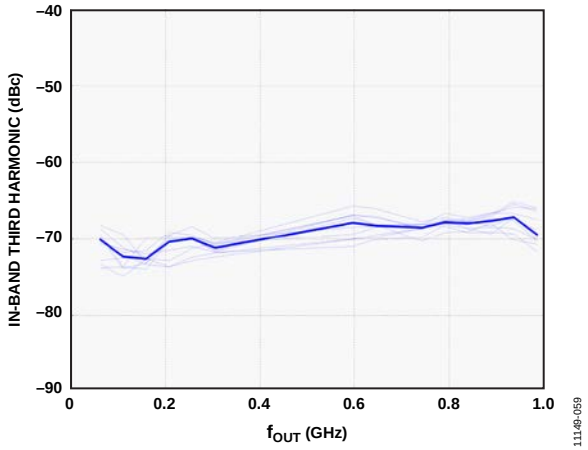

Figure 48. Third Harmonic vs. f_{OUT} Performance for Four DOCSIS Carriers

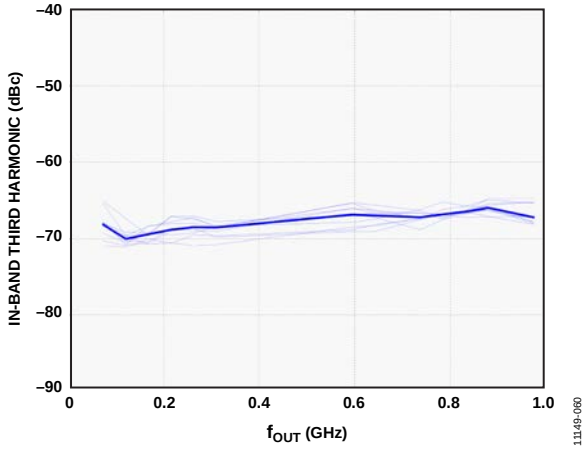

Figure 49. Third Harmonic vs. f_{OUT} Performance for Eight DOCSIS Carriers

Downloaded from Arrow.com.

I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

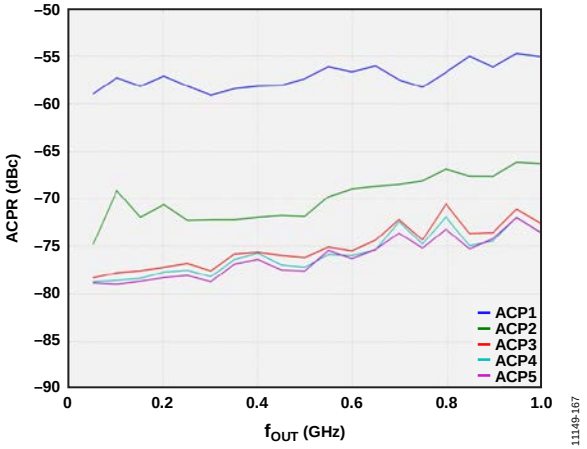

Figure 50. Single-Carrier ACPR vs. f_{OUT}

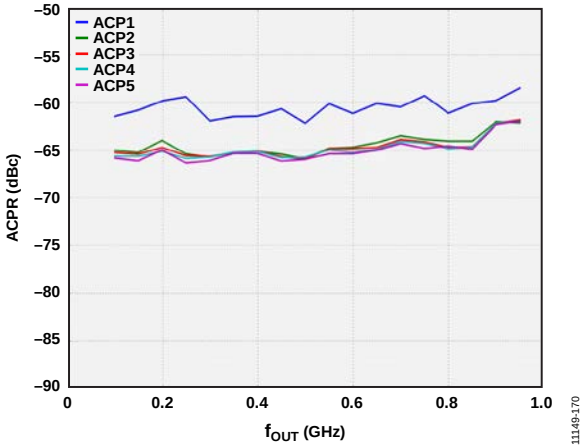

Figure 53. 16-Carrier ACPR vs. f_{OUT}

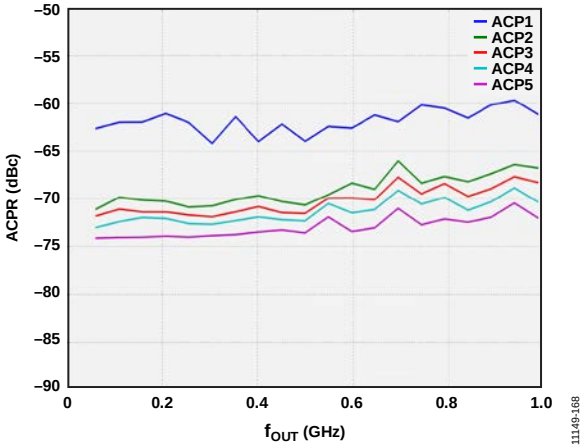

Figure 51. Four-Carrier ACPR vs. f_{OUT}

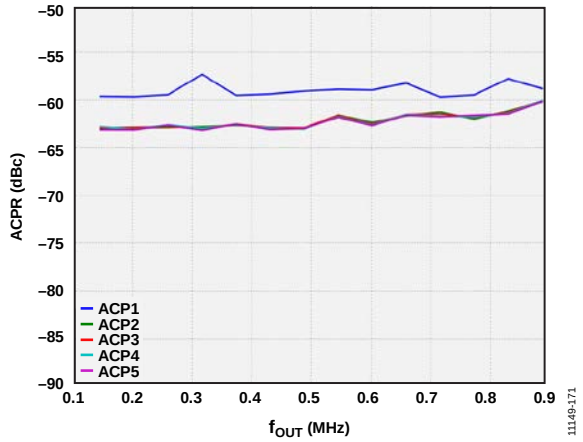

Figure 54. 32-Carrier ACPR vs. f_{OUT}

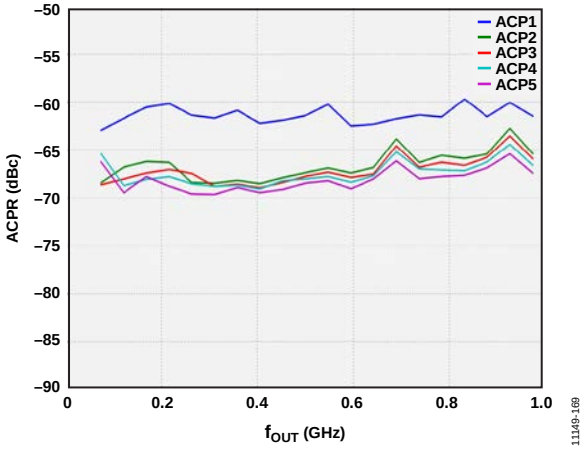

Figure 52. Eight-Carrier ACPR vs. f_{OUT}

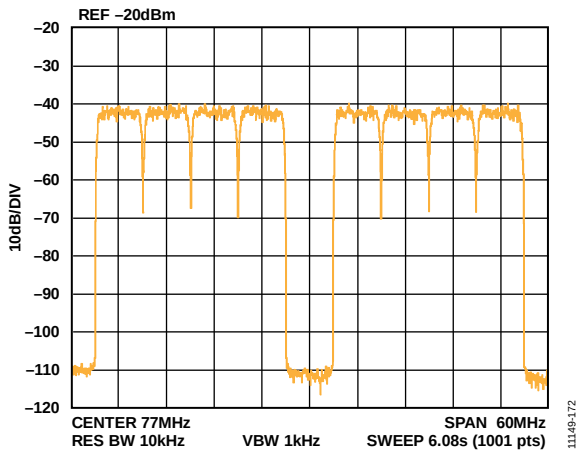

Figure 55. Gap Channel ACPR at 77 MHz

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AD9129

Static Linearity

I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

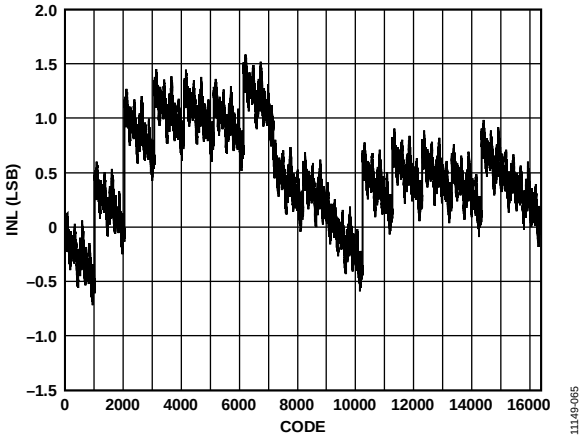

Figure 56. Typical INL, 11 mA at 25°C

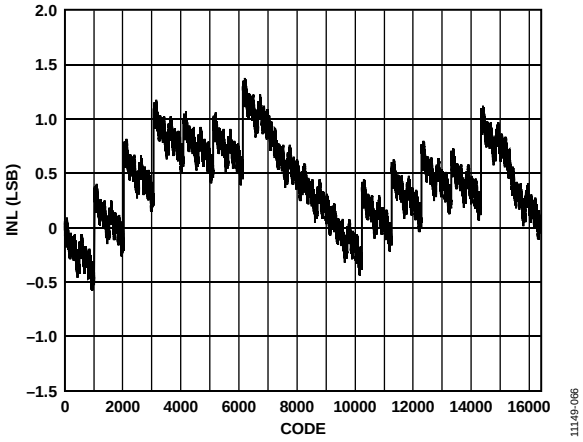

Figure 57. Typical INL, 22 mA at 25°C

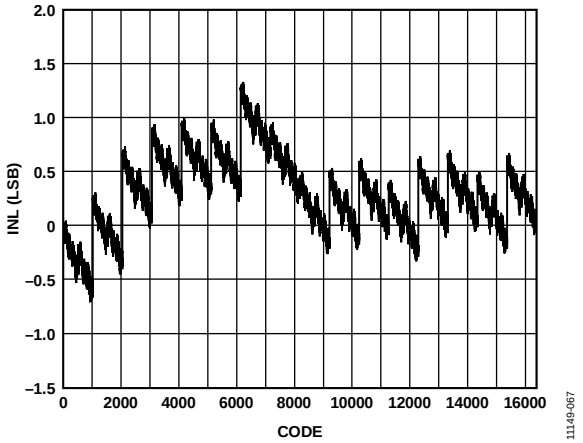

Figure 58. Typical INL, 33 mA at 25°C

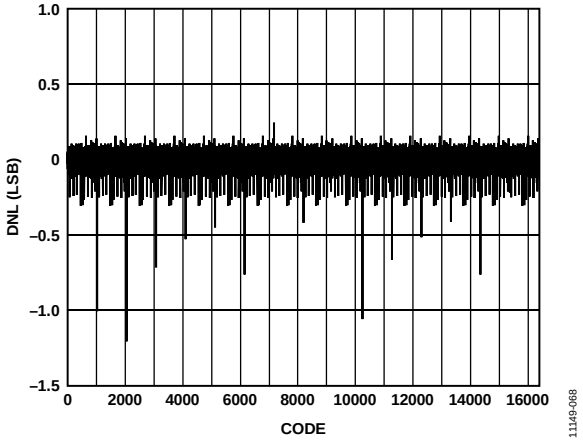

Figure 59. Typical DNL, 11 mA at 25°C

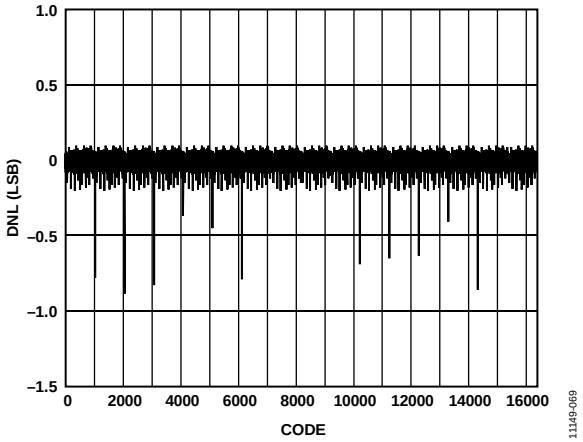

Figure 60. Typical DNL, 22 mA at 25°C

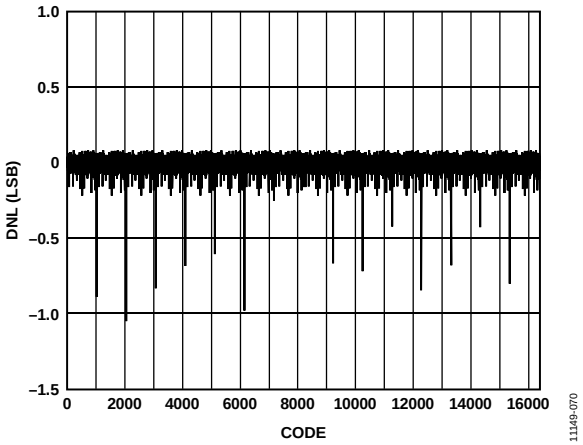

Figure 61. Typical DNL, 33 mA at 25°C

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AC (Normal Mode)

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

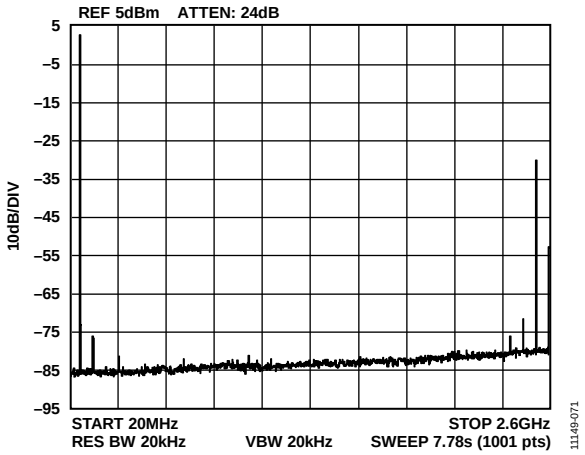


Figure 62. Single-Tone Spectrum at f_{OUT} = 70 MHz

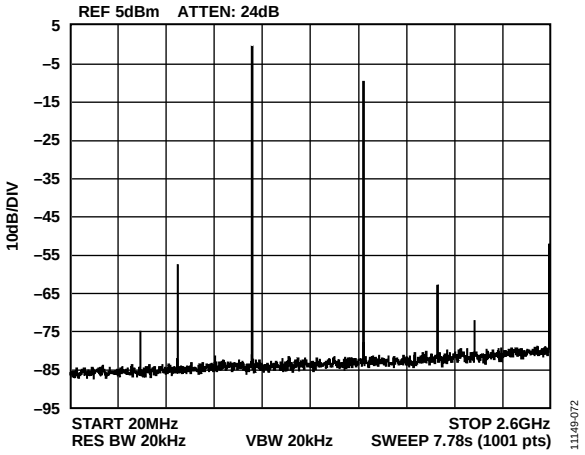


Figure 65. Single-Tone Spectrum at f_{OUT} = 1000 MHz

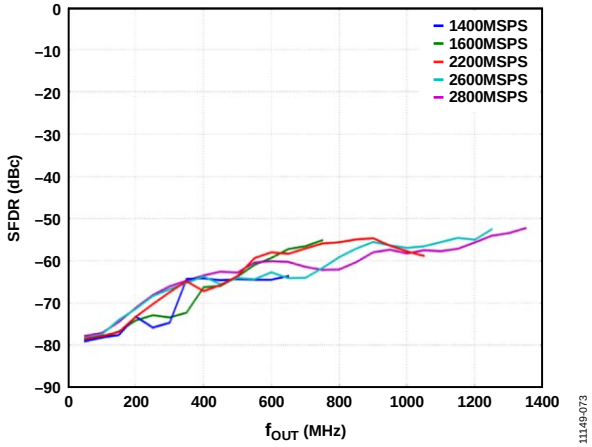


Figure 63. SFDR vs. f_{OUT} over f_{DAC}

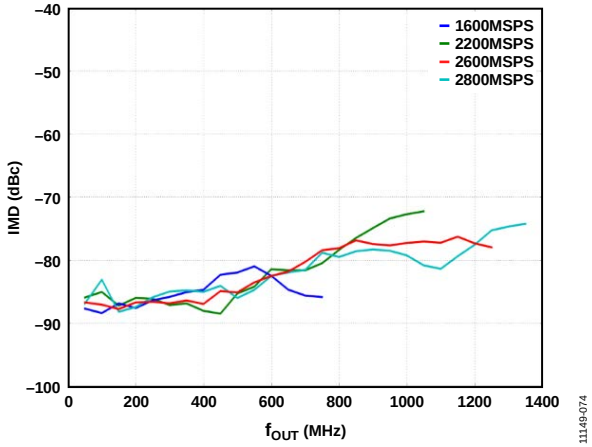


Figure 66. IMD vs. f_{OUT} over f_{DAC}

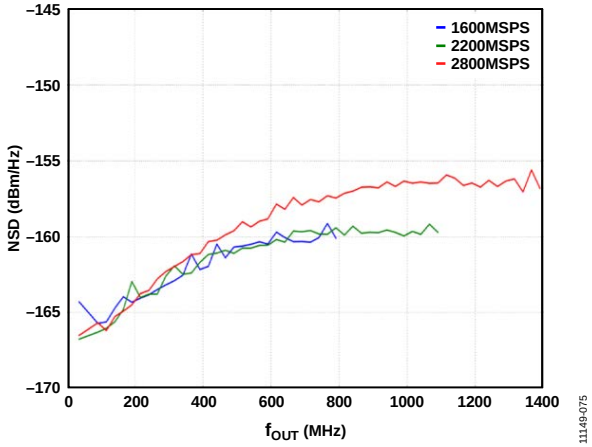


Figure 64. Single-Tone NSD vs. f_{OUT}

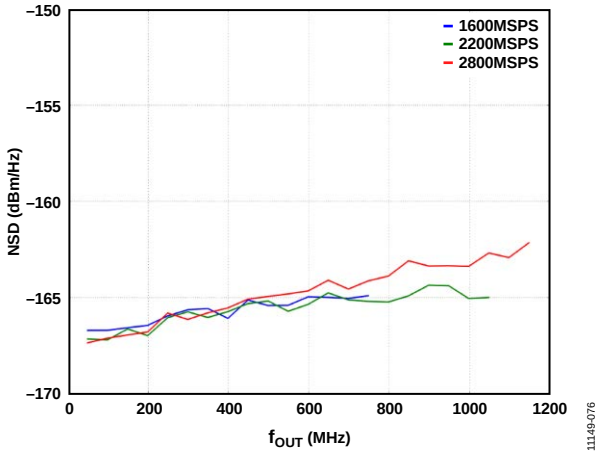


Figure 67. W-CDMA NSD vs. f_{OUT}

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

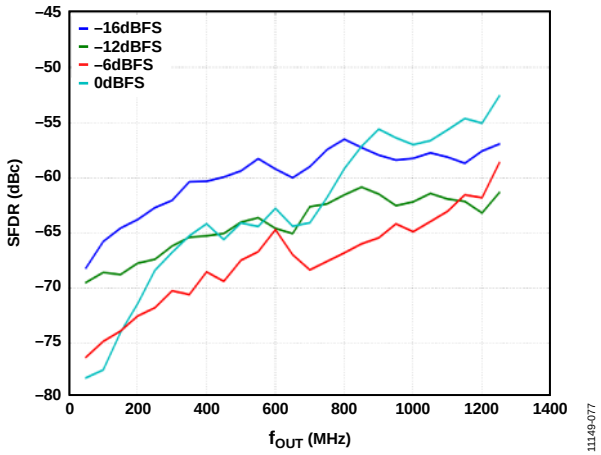


Figure 68. SFDR vs. f_{OUT} over Digital Full Scale

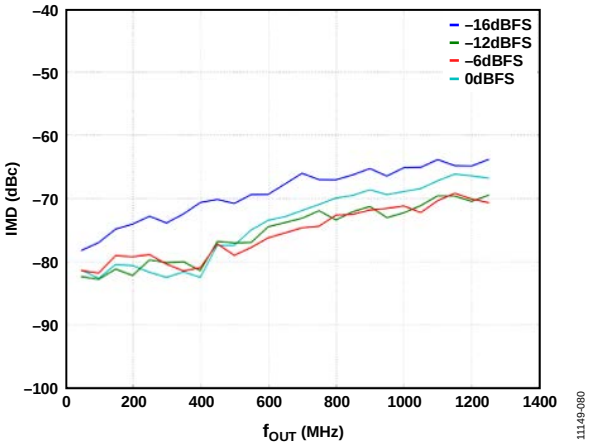


Figure 71. IMD vs. f_{OUT} over Digital Full Scale

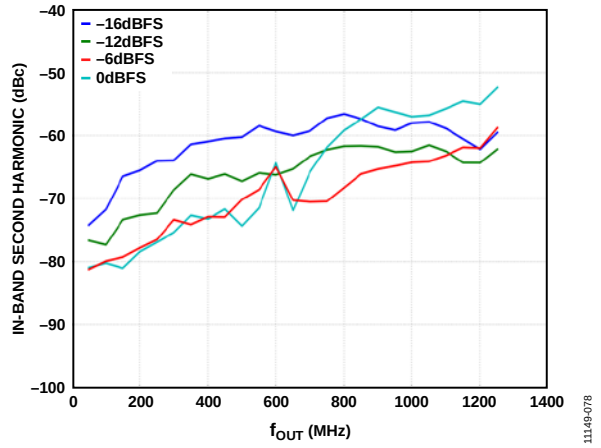


Figure 69. SFDR for Second Harmonic vs. f_{OUT} over Digital Full Scale

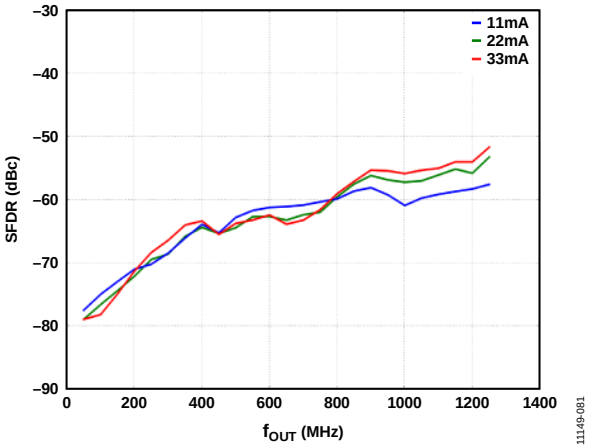


Figure 72. SFDR vs. f_{OUT} over DAC I_{OUTFS}

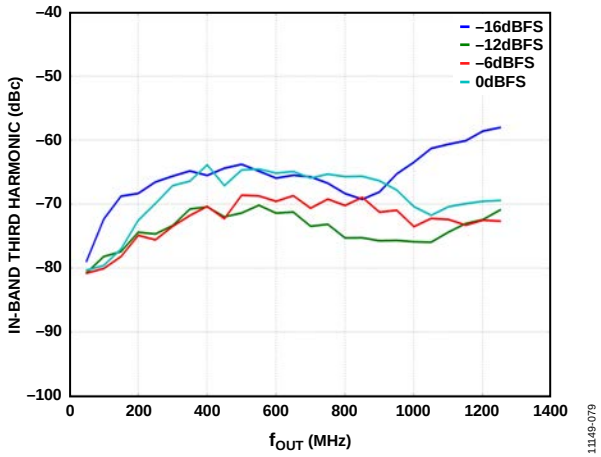


Figure 70. SFDR for Third Harmonic vs. f_{OUT} over Digital Full Scale

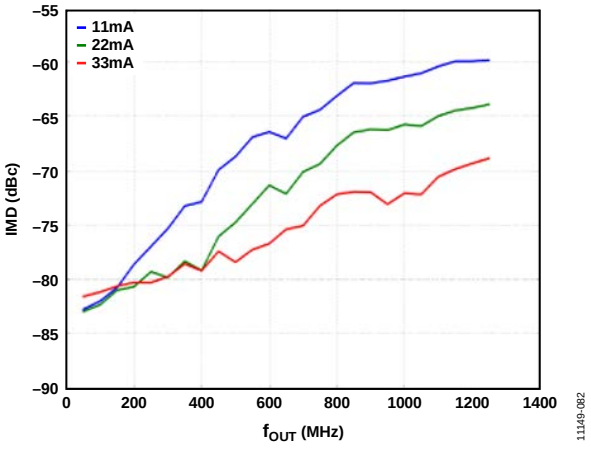


Figure 73. IMD vs. f_{OUT} over DAC I_{OUTFS}

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

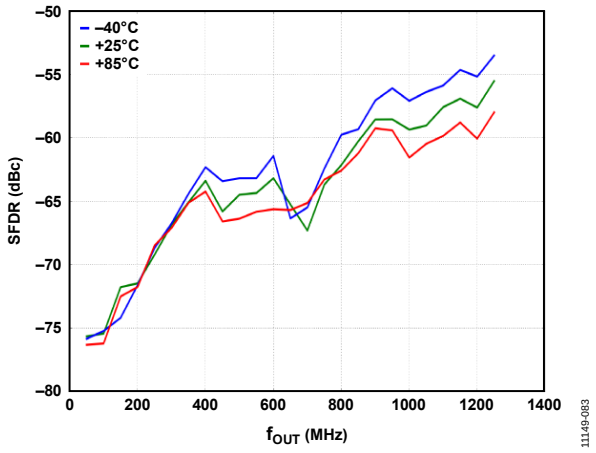


Figure 74. SFDR vs. f_{OUT} over Temperature

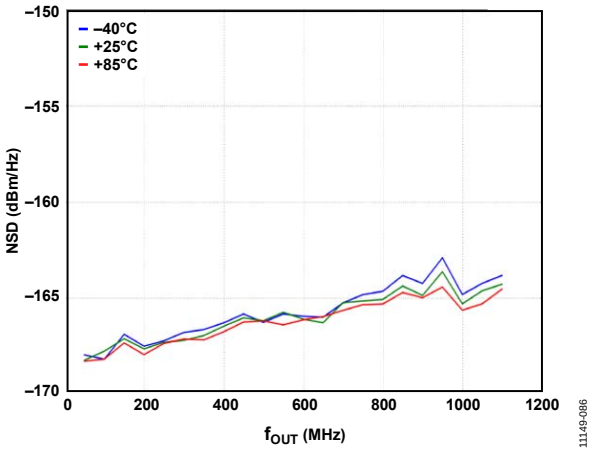


Figure 77. W-CDMA NSD vs. f_{OUT} over Temperature

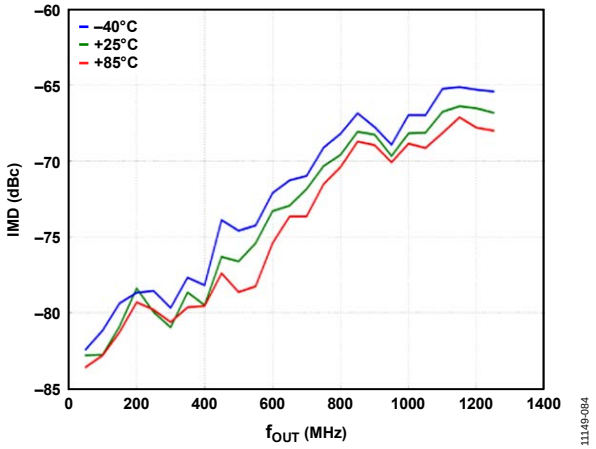


Figure 75. IMD vs. f_{OUT} over Temperature

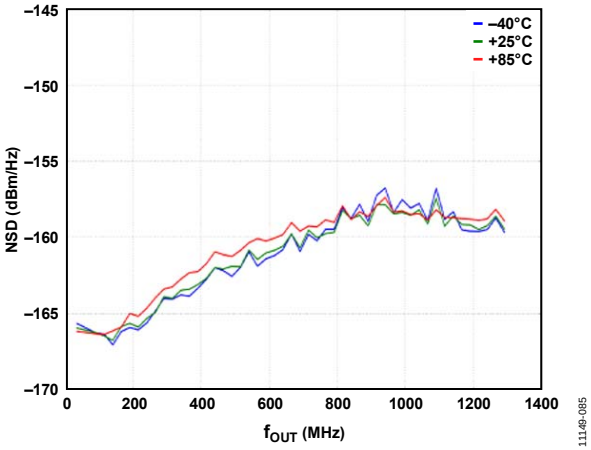


Figure 78. Single-Tone NSD vs. f_{OUT} over Temperature

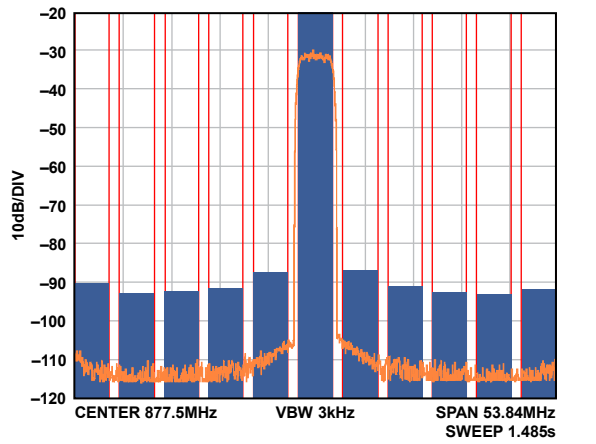


Figure 76. Single-Carrier W-CDMA at 877.5 MHz

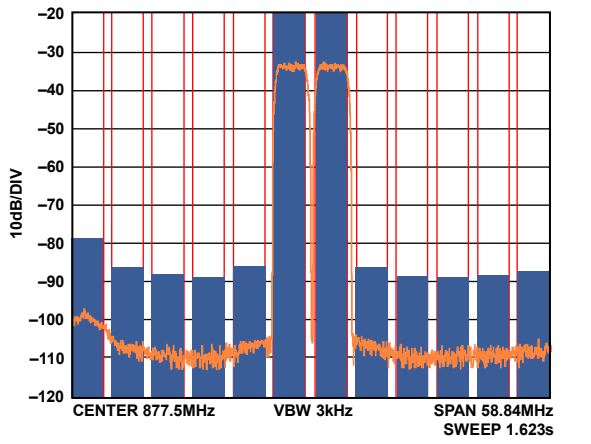


Figure 79. Two-Carrier W-CDMA at 875 MHz

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

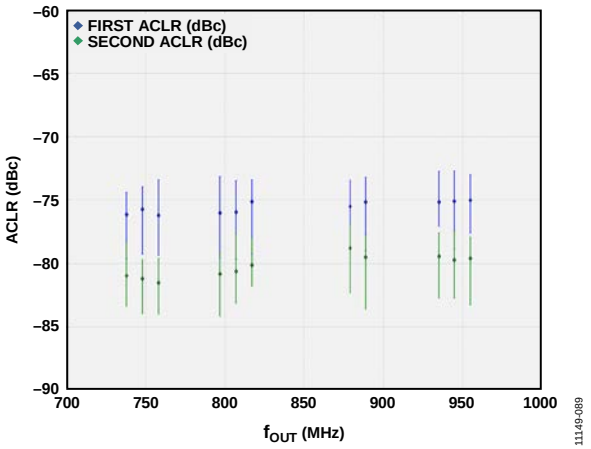


Figure 80. Single-Carrier W-CDMA ACLR vs. f_{OUT} (First ACLR, Second ACLR)

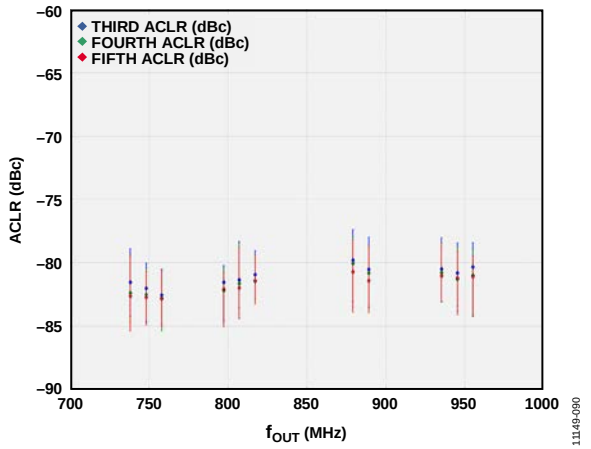


Figure 81. Single-Carrier W-CDMA ACLR vs. f_{OUT} (Third ACLR, Fourth ACLR, Fifth ACLR)

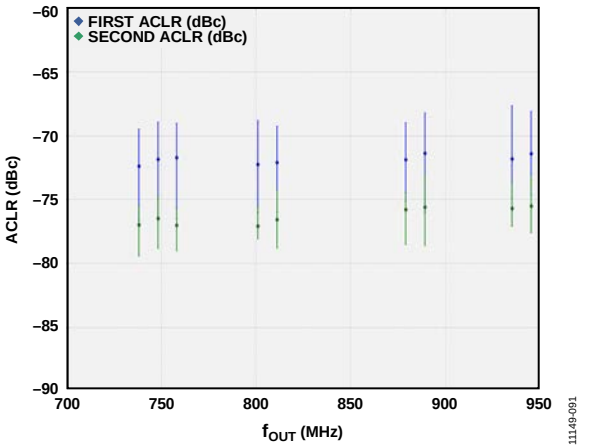


Figure 82. Two-Carrier W-CDMA ACLR vs. f_{OUT} (First ACLR, Second ACLR)

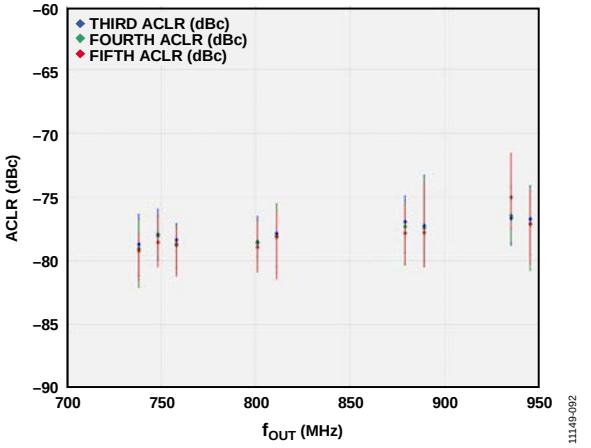


Figure 83. Two-Carrier W-CDMA ACLR vs. f_{OUT} (Third ACLR, Fourth ACLR, Fifth ACLR)

Downloaded from Arrow.com.

AC (Mix-Mode)

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

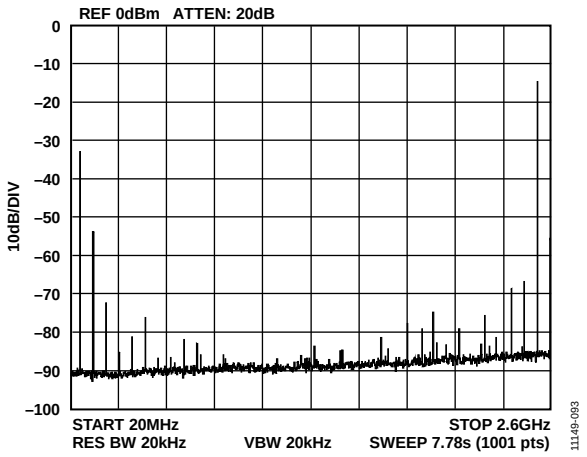


Figure 84. Single-Tone Spectrum at f_{OUT} = 2350 MHz

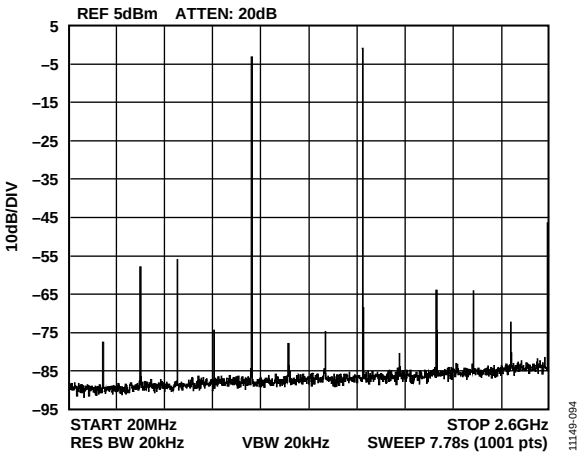


Figure 87. Single-Tone Spectrum at f_{OUT} = 1600 MHz

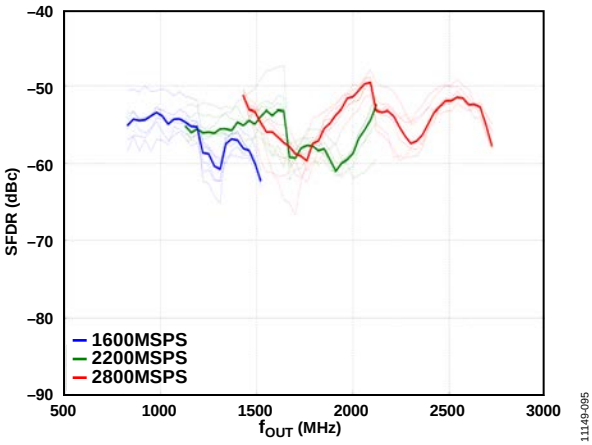


Figure 85. SFDR vs. f_{OUT} over f_{DAC}

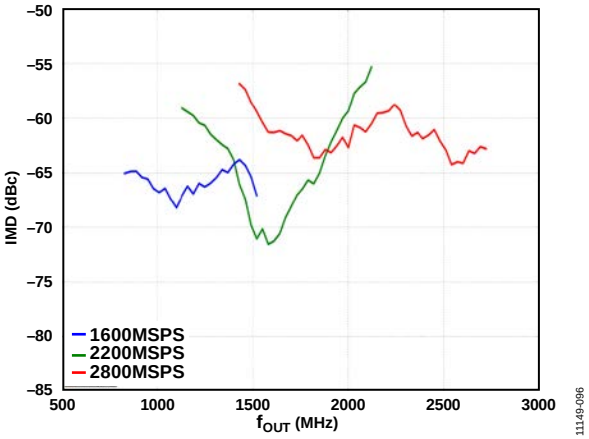


Figure 88. IMD vs. f_{OUT} over f_{DAC}

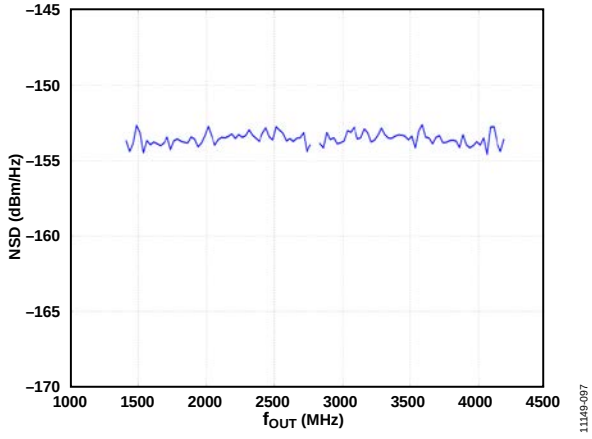


Figure 86. Single-Tone NSD vs. f_{OUT}

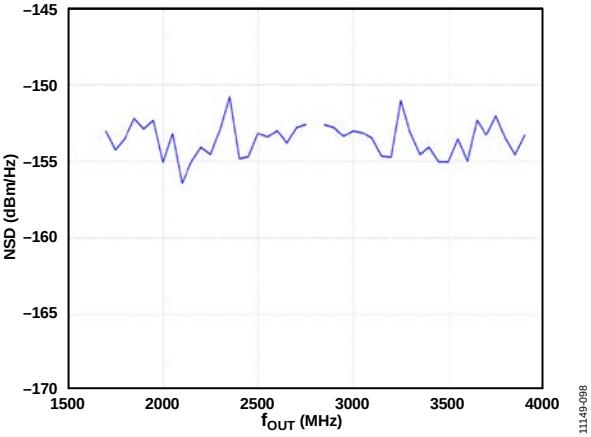


Figure 89. W-CDMA NSD vs. f_{OUT}

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

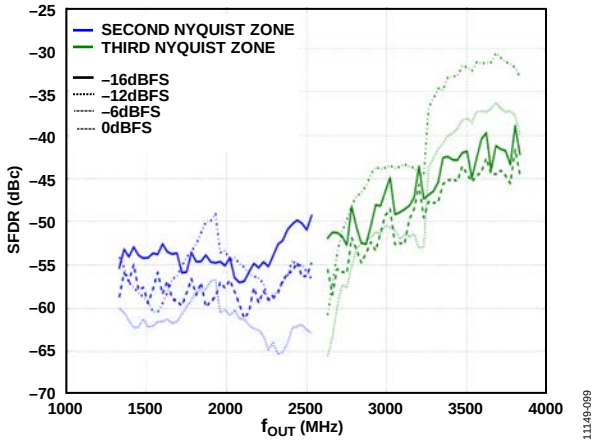


Figure 90. SFDR vs. f_{OUT} over Digital Full Scale

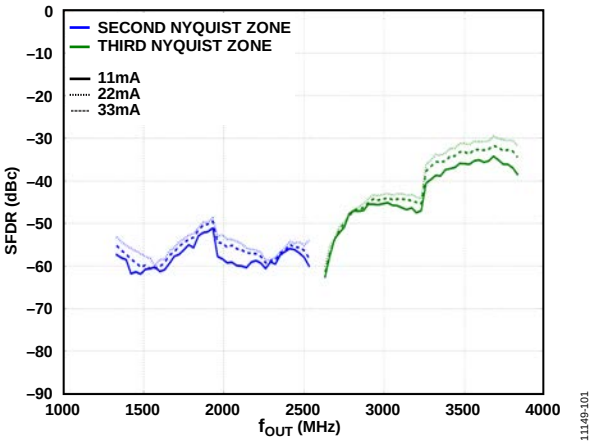


Figure 92. SFDR vs. f_{OUT} over DAC I_{OUTFS}

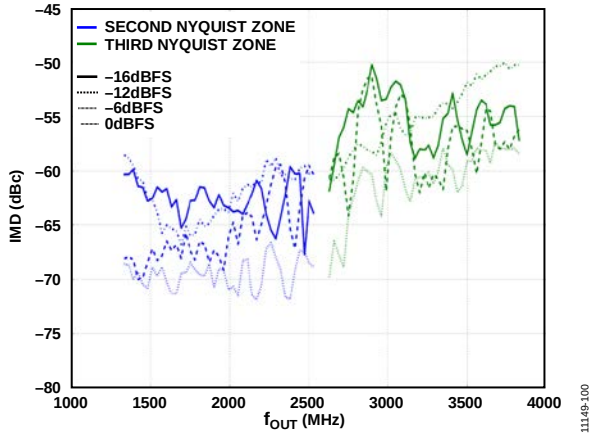


Figure 91. IMD vs. f_{OUT} over Digital Full Scale

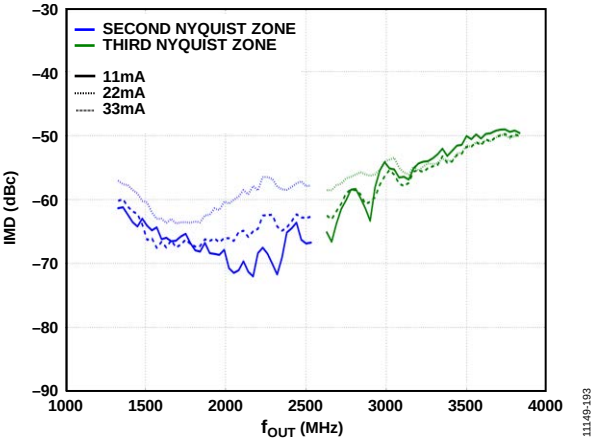


Figure 93. IMD vs. f_{OUT} over DAC I_{OUTFS}

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

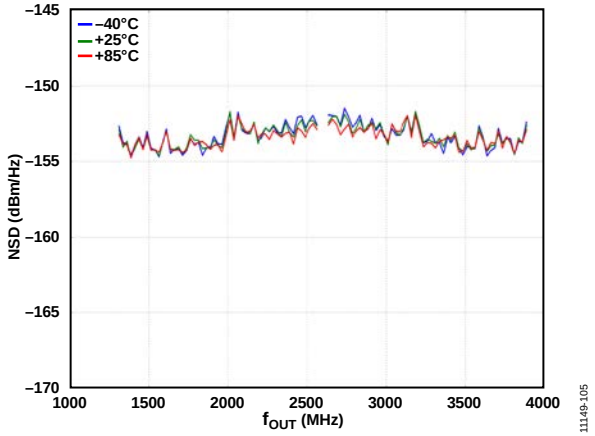


Figure 94. Single-Tone NSD vs. f_{OUT} over Temperature

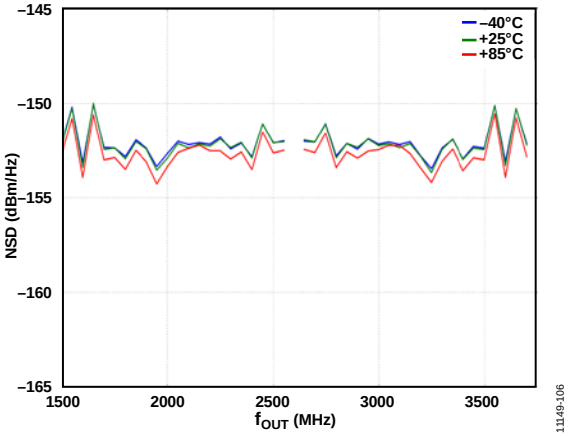
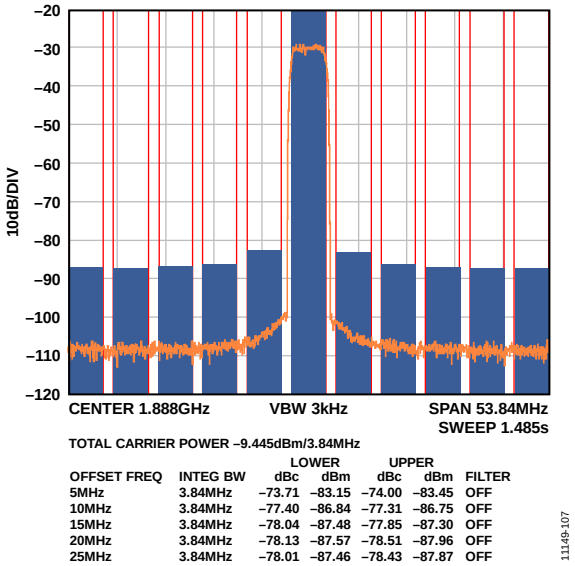
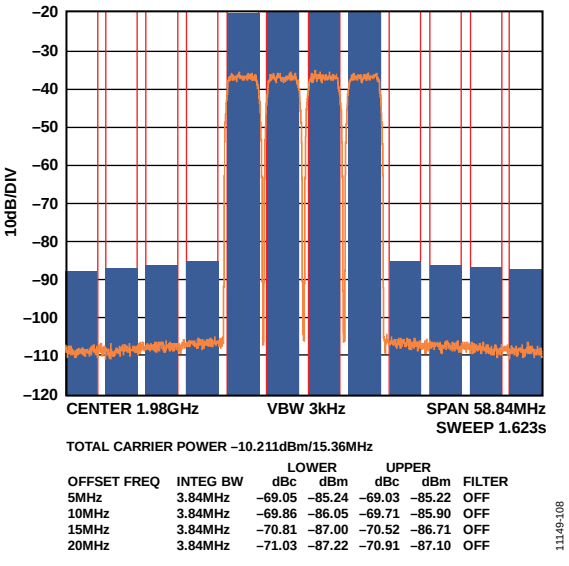


Figure 96. W-CDMA NSD vs. f_{OUT} over Temperature



OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm	FILTER
5MHz	3.84MHz	–73.71	–83.15	–74.00	–83.45	OFF
10MHz	3.84MHz	–77.40	–86.84	–77.31	–86.75	OFF
15MHz	3.84MHz	–78.04	–87.48	–77.85	–87.30	OFF
20MHz	3.84MHz	–78.13	–87.57	–78.51	–87.96	OFF
25MHz	3.84MHz	–78.01	–87.46	–78.43	–87.87	OFF

Figure 95. Single-Carrier W-CDMA at 1887.5 MHz



OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm	FILTER
5MHz	3.84MHz	–69.05	–85.24	–69.03	–85.22	OFF
10MHz	3.84MHz	–69.86	–86.05	–69.71	–85.90	OFF
15MHz	3.84MHz	–70.81	–87.00	–70.52	–86.71	OFF
20MHz	3.84MHz	–71.03	–87.22	–70.91	–87.10	OFF

Figure 97. Four-Carrier W-CDMA at 1980 MHz

Downloaded from Arrow.com.

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

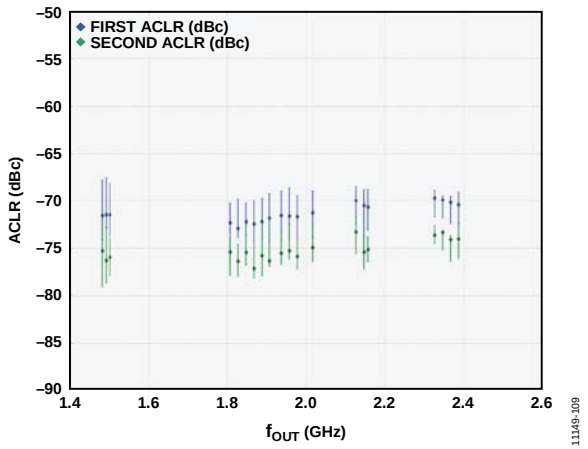


Figure 98. Single-Carrier W-CDMA ACLR vs. f_{OUT} (First ACLR, Second ACLR)

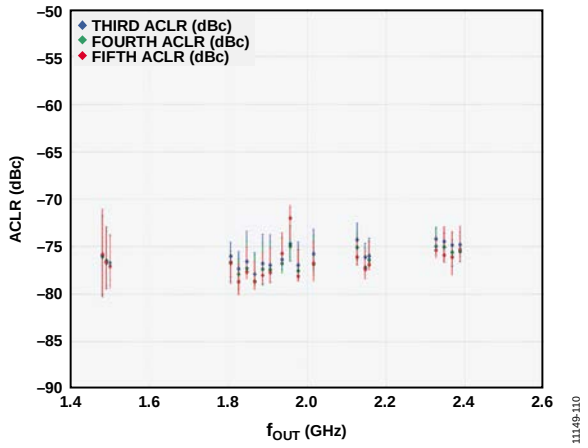


Figure 99. Single-Carrier W-CDMA ACLR vs. f_{OUT} (Third ACLR, Fourth ACLR, Fifth ACLR)

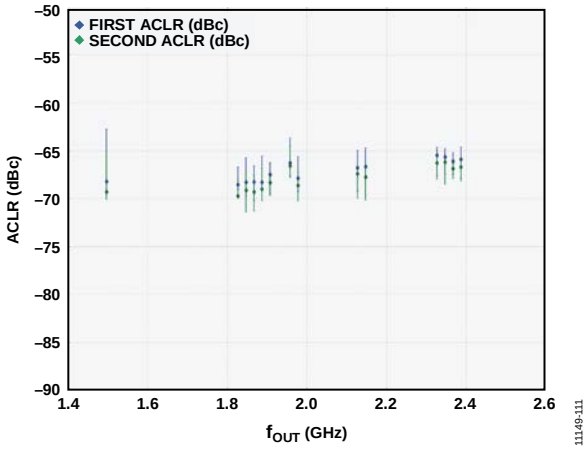


Figure 100. Four-Carrier W-CDMA ACLR vs. f_{OUT} (First ACLR, Second ACLR)

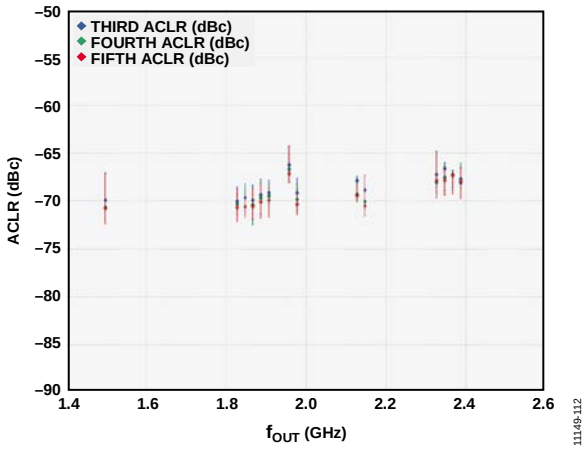


Figure 101. Four-Carrier W-CDMA ACLR vs. f_{OUT} (Third ACLR, Fourth ACLR, Fifth ACLR)

Downloaded from Arrow.com.

DOCSIS Performance (Normal Mode)

I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

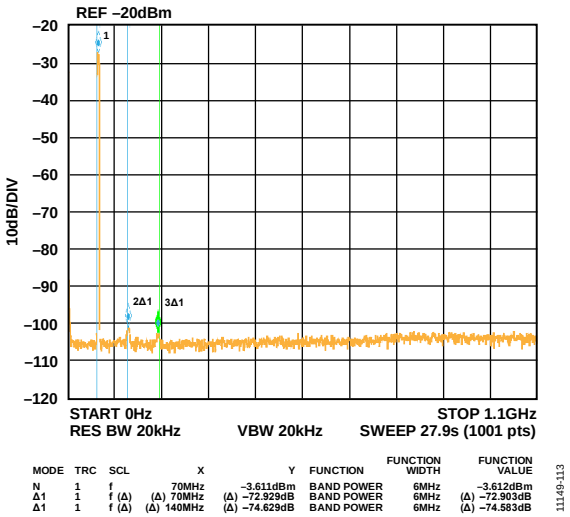


Figure 102. Single Carrier at 70 MHz Output

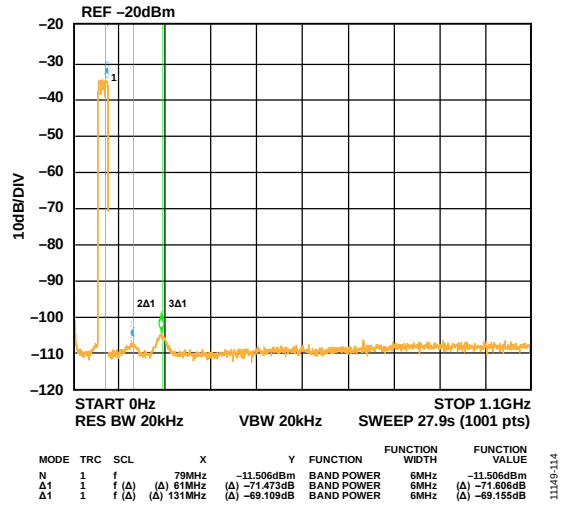


Figure 103. Four Carrier at 70 MHz Output

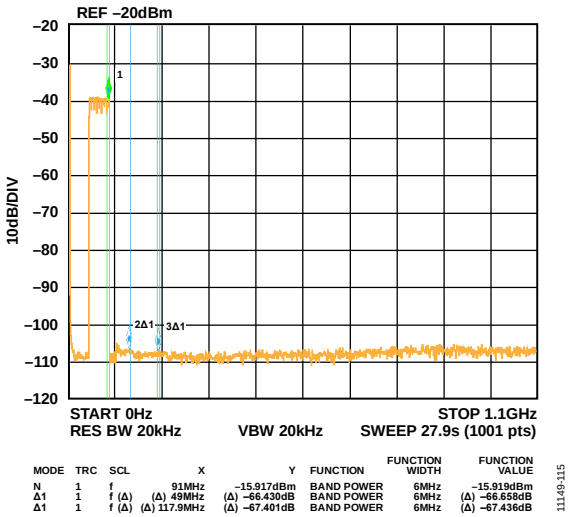


Figure 104. Eight Carrier at 70 MHz Output

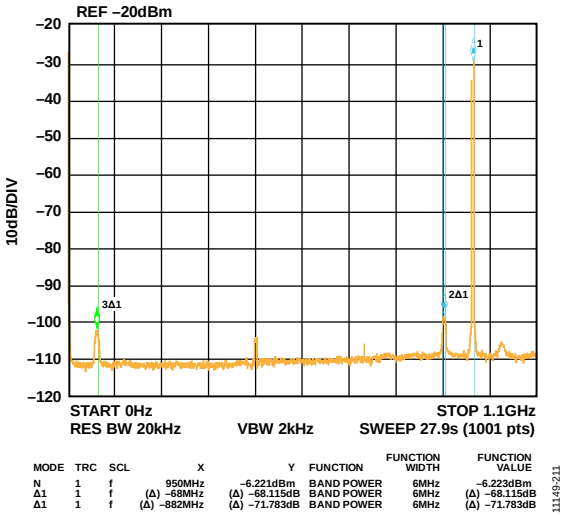


Figure 105. Single Carrier at 950 MHz Output

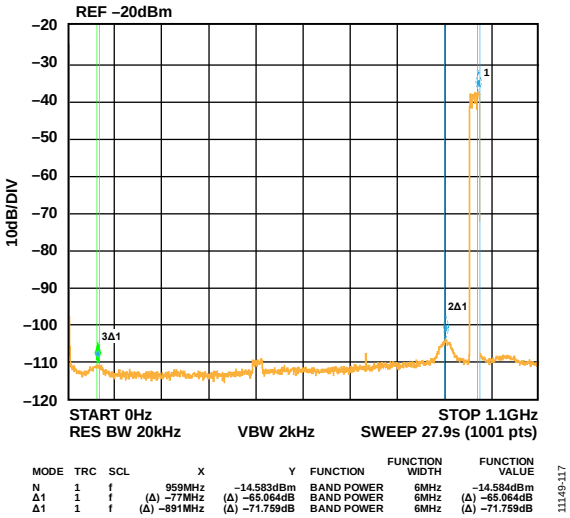


Figure 106. Four Carrier at 950 MHz Output

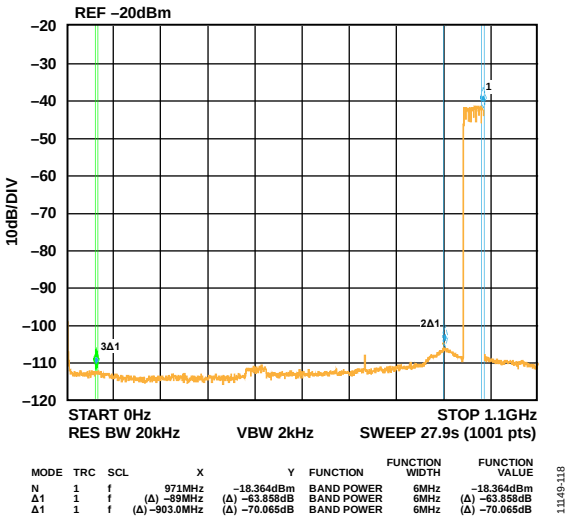


Figure 107. Eight Carrier at 950 MHz Output

Downloaded from Arrow.com.

I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

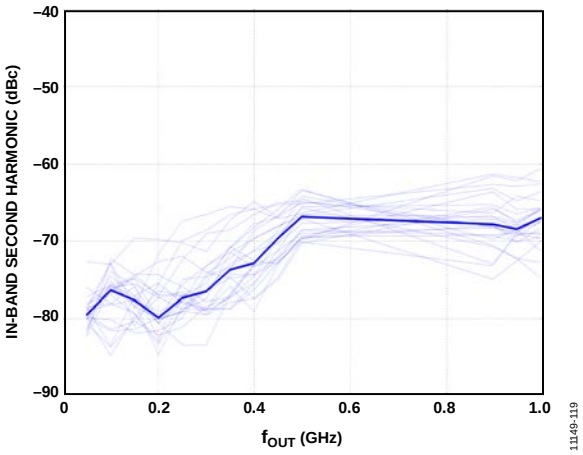


Figure 108. Second Harmonic vs. f_{OUT} Performance for One DOCSIS Carrier

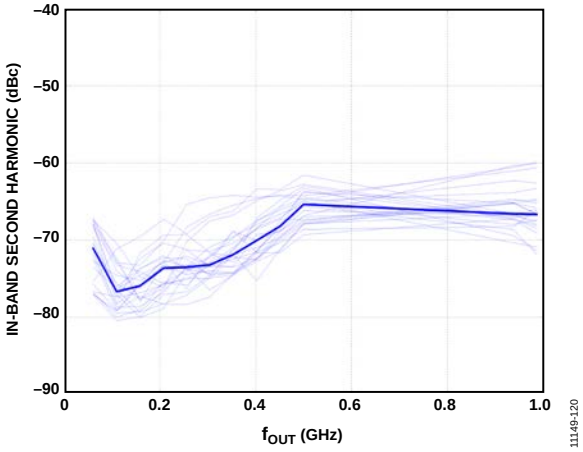


Figure 109. Second Harmonic vs. f_{OUT} Performance for Four DOCSIS Carriers

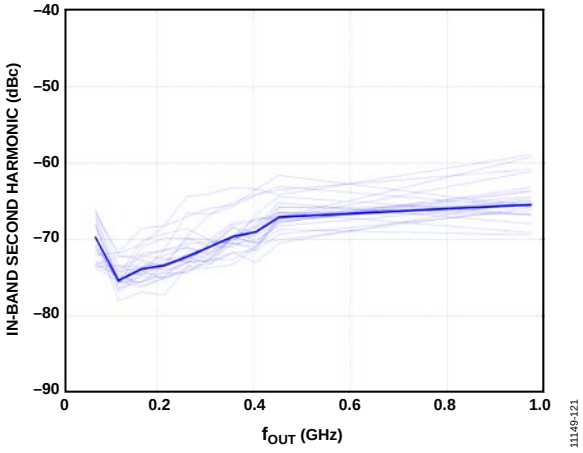


Figure 110. Second Harmonic vs. f_{OUT} Performance for Eight DOCSIS Carriers

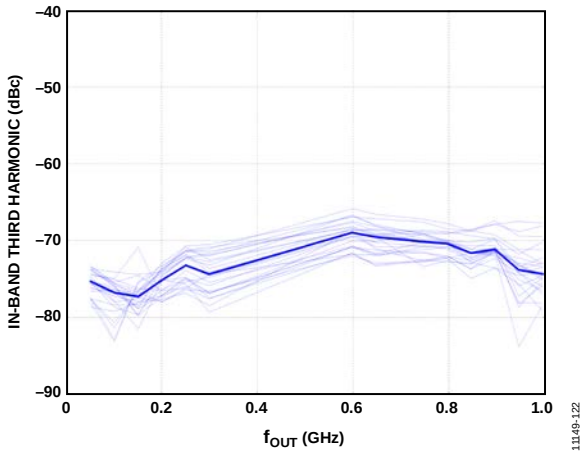


Figure 111. Third Harmonic vs. f_{OUT} Performance for One DOCSIS Carrier

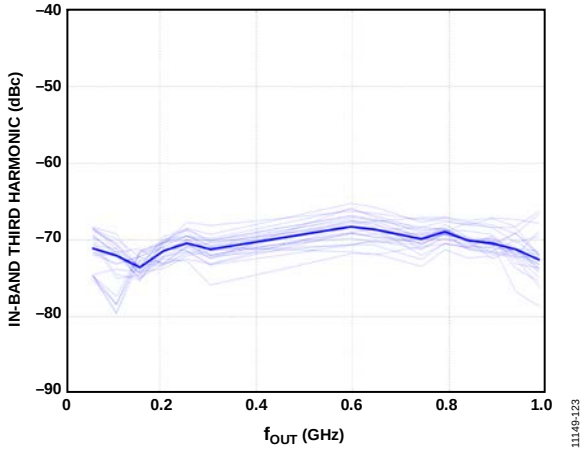


Figure 112. Third Harmonic vs. f_{OUT} Performance for Four DOCSIS Carriers

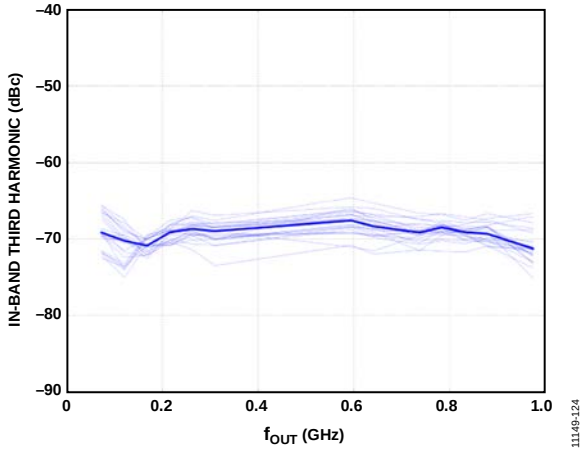


Figure 113. Third Harmonic vs. f_{OUT} Performance for Eight DOCSIS Carriers

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I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

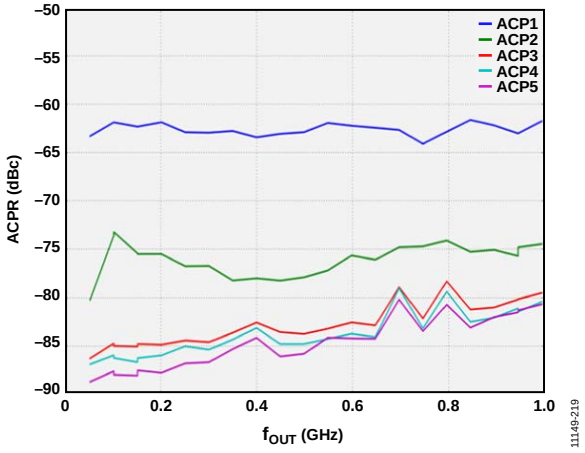

Figure 114. Single-Carrier ACPR vs. f_{OUT}

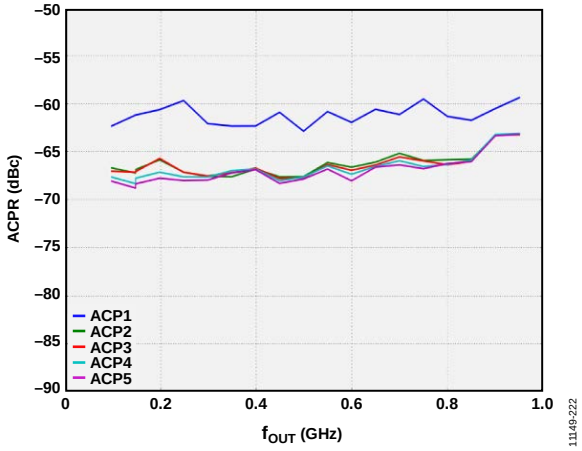

Figure 117. 16-Carrier ACPR vs. f_{OUT}

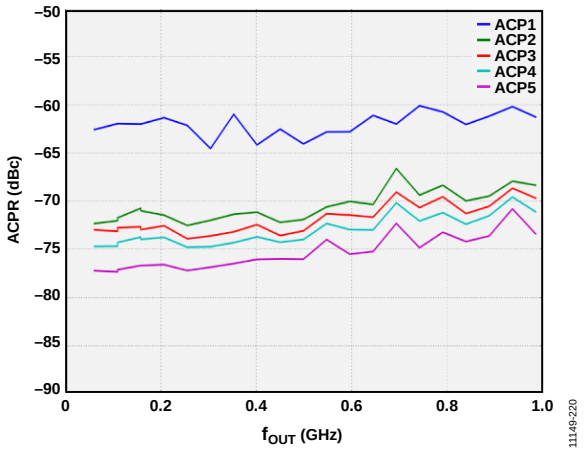

Figure 115. Four-Carrier ACPR vs. f_{OUT}

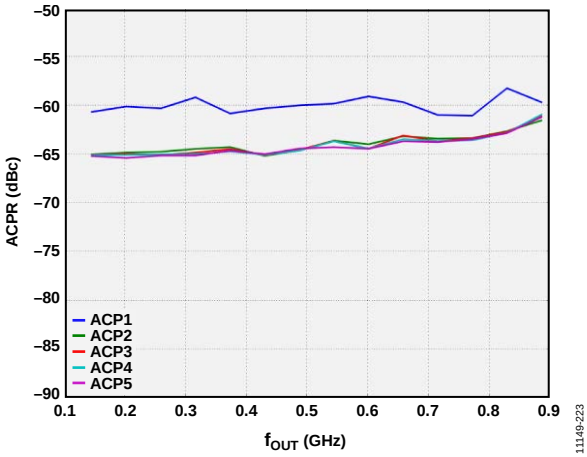

Figure 118. 32-Carrier ACPR vs. f_{OUT}

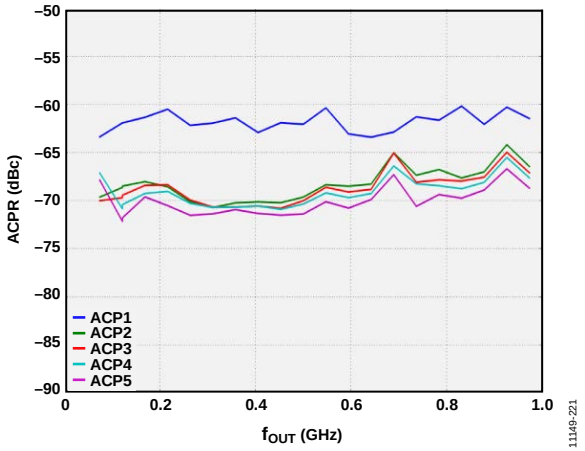

Figure 116. Eight-Carrier ACPR vs. fOUT

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I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

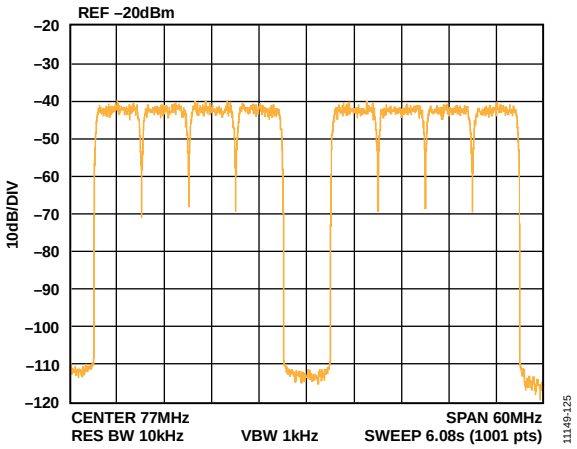

Figure 119. Gap Channel ACLR at 77 MHz

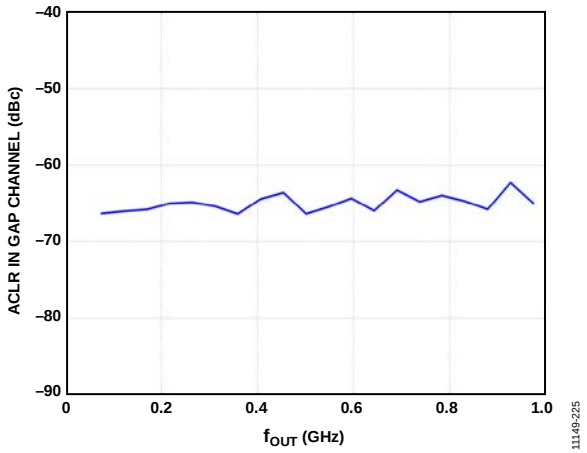

Figure 120. Gap Channel ACLR vs. f_{OUT}

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TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
The maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
The measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero. For IOUTP, 0 mA output is expected when the inputs are all 0s. For IOUTN, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1 minus the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius (°C). For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Spurious-Free Dynamic Range
The difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Noise Spectral Density (NSD)
The converter noise power per unit of bandwidth. This is usually specified in dBm/Hz in the presence of a 0 dBm full-scale signal.

Adjacent Channel Leakage Ratio (ACLR)
The ratio, in dBc, between the measured power within a channel relative to its adjacent channels.

Adjacent Channel Power Ratio (ACPR)
The ratio, in dBc, between the total power of an adjacent channel (intermodulation signal) to the main channel's power (useful signal).

Modulation Error Ratio (MER)
A measure of the discrepancy between the average output symbol magnitude and the rms error magnitude of the individual symbol. Modulated signals create a discrete set of output values referred to as a constellation, and each symbol creates an output signal corresponding to one point on the constellation.

Intermodulation Distortion (IMD)
The result of two or more signals at different frequencies mixing together. Many products are created according to the formula aF1 ± bF2, where a and b are integer values.

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SERIAL COMMUNICATIONS PORT OVERVIEW

The AD9119/AD9129 are 11-bit/14-bit DACs that operate at an update rate of up to 2.85 GSPS. Due to internal timing requirements, the minimum allowable sample rate is 1400 MSPS. Input data is sampled through two 11-/14-bit LVDS ports that are internally multiplexed. Each port has its own data inputs, but both ports share a common data clock input (DCI). The LVDS inputs meet the IEEE-1596 specification with the exception of input hysteresis, which is not guaranteed over all process corners. Each DCI input runs at one-quarter the input data rate in a double data rate (DDR) format. Each edge of the DCI is used to transfer data into the AD9119/AD9129.

The DACCLK_N and DACCLK_P inputs directly drive the DAC core to minimize clock jitter. The DACCLK signal is divided by 4 and then output as the DCO for each port. The DCO signal can be used to clock the data source. The DAC expects DDR LVDS data (P0_D[13:0]x, P1_D[13:0]x), with each channel aligned with the single DDR DCI signal.

Control of the AD9119/AD9129 functions is via a SPI.

SERIAL PERIPHERAL INTERFACE (SPI)

The AD9119/AD9129 SPI is a flexible, synchronous serial communications port, allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including the Motorola® SPI and the Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9119/AD9129. Most significant bit first (MSB-first) or least significant bit first (LSB-first) transfer formats are supported. The AD9119/AD9129 serial interface port can be configured as a single I/O pin (SDIO) or two unidirectional pins for input/output (SDIO and SDO).

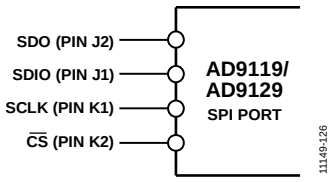

Figure 121. AD9119/AD9129 SPI Port

GENERAL OPERATION OF THE SPI

There are two phases to a communication cycle with the AD9119/AD9129. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9119/AD9129, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9119/AD9129 serial port controller with information about the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9119/AD9129.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9119/AD9129 and the system controller. Phase 2 of the communication cycle is a transfer of one byte only. Single-byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte. $\overline{CS}$ (chip select) can be raised after each sequence of eight bits (except the last byte) to stall the bus. The serial transfer resumes when $\overline{CS}$ is lowered. Stalling on nonbyte boundaries resets the SPI.

INSTRUCTION MODE (8-BIT INSTRUCTION)

The instruction byte is shown in the following table.

MSB							LSB
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/W	A6	A5	A4	A3	A2	A1	A0

R/W, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation, the data transfer cycle. A6 to A0 (Bit 6 through Bit 0 of the instruction byte) determine which register is accessed during the data transfer portion of the communications cycle.

SERIAL PERIPHERAL INTERFACE PIN DESCRIPTIONS

SCLK—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9119/AD9129 and to run the internal state machines. The maximum frequency of SCLK is 20 MHz. All data input to the AD9119/AD9129 is registered on the rising edge of SCLK. All data is driven out of the AD9119/AD9129 on the rising edge of SCLK.

$\overline{CS}$—Chip Select

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O

Data is always written into the AD9119/AD9129 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x00, Bit 7 (SDIO_DIR). The default is Logic 1, which configures the SDIO pin as bidirectional.

SDO—Serial Data Out

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. When the AD9119/AD9129 are operating in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

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MSB/LSB TRANSFERS

The AD9119/AD9129 serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by the LSB/MSB bit, Bit 6 in Register 0x00. The default is MSB first (LSB/MSB = 0). When the MSB-first data format is selected, the instruction and data bytes must be written from the most significant bit to the least significant bit.

When LSB/MSB = 1 (LSB first), the instruction and data bytes must be written from the least significant bit to the most significant bit.

SERIAL PORT CONFIGURATION

The AD9119/AD9129 serial port configuration is controlled by Register 0x00, Bits[7:5]. Note that the configuration changes immediately upon writing to the last bit of the register. When setting the software reset bit (SoftReset in Register 0x00, Bit 5), all registers are set to their default values except Register 0x00, which remains unchanged.

In the event of unexpected programming sequences, the AD9119/AD9129 SPI can become inaccessible. For example, if user code inadvertently changes the LSB/MSB bit, the bits that follow experience unexpected results. The SPI can be returned to a known state by writing an incomplete byte (1 to 7 bits) of all 0s, followed by three bytes of 0x00. This returns to the MSB-first instructions (Register 0x00 = 0x00) so that the device can be reinitialized.

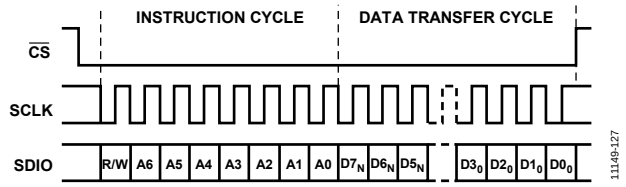

Figure 122. Serial Register Interface Timing, MSB-First Write

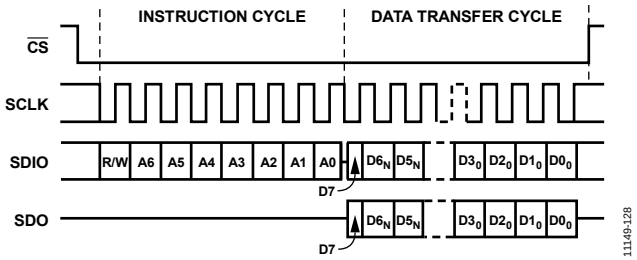

Figure 123. Serial Register Interface Timing, MSB-First Read

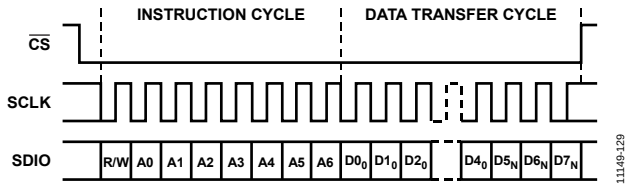

Figure 124. Serial Register Interface Timing, LSB-First Write

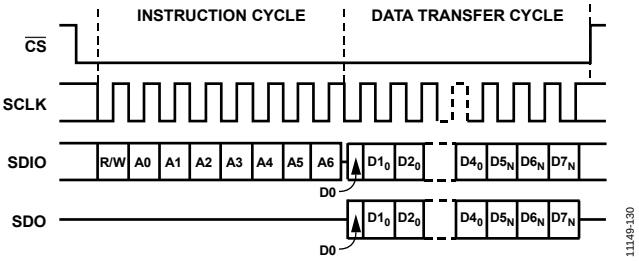

Figure 125. Serial Register Interface Timing, LSB-First Read

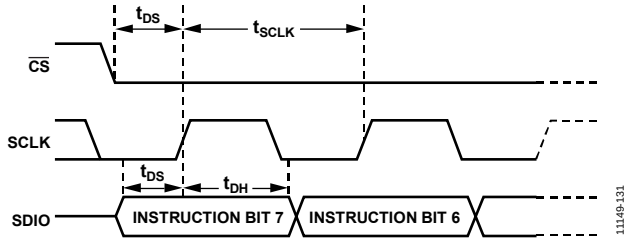

Figure 126. Timing Diagram for an SPI Register Write

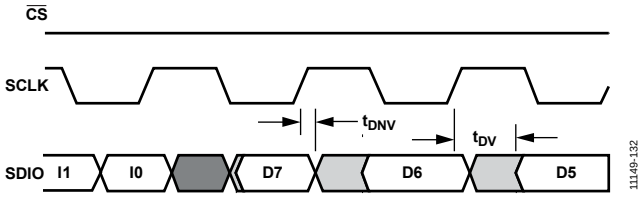

Figure 127. Timing Diagram for an SPI Register Read

After the last instruction bit is written to the SDIO pin, the driving signal must be set to a high impedance in time for the bus to turn around. The serial output data from the AD9119/AD9129 is enabled by the falling edge of SCLK. This causes the first output data bit to be shorter than the remaining data bits, as shown in Figure 127. To assure proper reading of data, read the SDIO pin or the SDO pin before changing SCLK from low to high. Due to the more complex multibyte protocol, multiple AD9119/ AD9129 devices cannot be daisy-chained on the SPI bus. Control multiple DACs by using independent $\overline{CS}$ signals.

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THEORY OF OPERATION

The AD9119/AD9129 are 11-bit/14-bit DACs that are capable of reconstructing signal bandwidths up to 1.425 GHz while operating with an input data rate up to 2.85 GSPS. Figure 128 shows a top level functional diagram of the AD9119/AD9129. A high perfor-mance NMOS DAC delivers a signal dependent, differential current to a balanced external load referenced a nominal 1.8 V analog supply. The current source array of the DAC is referenced to an external −1.5 V supply, and its full-scale current, I_{OUTFS}, can be adjusted over a 9.5 mA to 34.4 mA span.

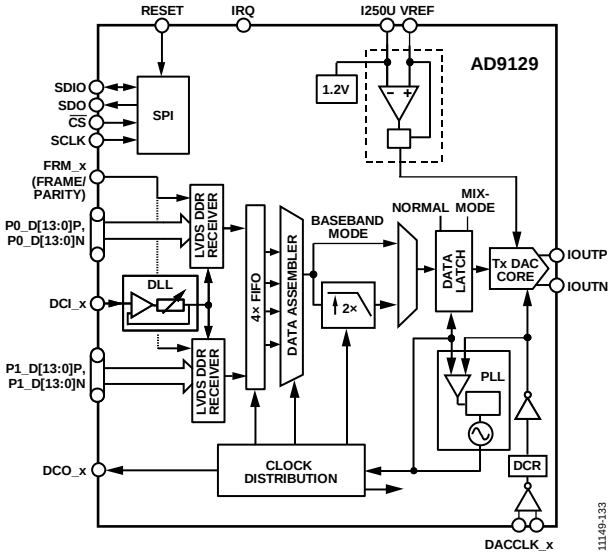

Figure 128. Functional Block Diagram of the AD9119/AD9129

A low jitter differential clock receiver is used to square up the signal appearing at the DACCLK_x input that sets the update rate of the DAC. The differential clock receiver can accept sinusoidal signals with negligible noise spectral density degradation if the input signal level is maintained above 0 dBm. A +1 dB degradation occurs at a −5 dBm input, and degradation increases as the signal approaches −10 dBm and its associated +2 dB additional degradation. A duty cycle restorer (DCR), following the clock receiver, ensures near 50% duty-cycle to the subsequent circuitry. The output of the DCR serves as the master clock and is routed directly to the DAC, as well as to a clock distribution block that generates all critical internal and external clocks. The clock source quality, as defined by its phase noise characteristics, jitter, and drive capability, is an important consideration in maintaining optimum ac performance.

The AD9119/AD9129 supports a source synchronous, LVDS double data-rate (DDR) data interface to the host processor. Two 11-bit/14-bit LVDS data ports (P0_DxP, P0_DxN and P1_DxP, P1_DxN) are used to sample de-interleaved data from the host on the rising and falling edge of the host DCI clock. This effectively reduces the bus interface speed to ½ the data rate (for example, $f_{DATA}/2$) with the DCI clock operating at $f_{DATA}/4$.

An optional parity bit can also be sent along with the data to enhance the robustness of the interface. In this case, a counter is available to count parity errors and generate an interrupt request (IRQ) when a programmable threshold is exceeded.

The AD9119/AD9129 provide the host with a DCO clock that is equal to the DCI clock frequency to establish synchronous operation. A delay locked loop (DLL) with programmable phase offset is used to generate an internal sampling clock with optimum edge placement for the input data latches of the LVDS DDR receivers. When data is latched into the AD9119/AD9129, an eight-sample-deep FIFO is used to hand off the data between the host and the AD9119/AD9129 clock domains. The FIFO can be reset with an external synchronization signal, f_{SYNC}, to ensure consistent pipeline latency. The pipeline delay, from a sample being latched into the data port to when it appears at the DAC output, varies depending on the chosen configuration (see the Pipeline Delay (Latency) section).

The de-interleaved data is reassembled into its original data stream after passing into the internal clock domain of the AD9119/AD9129. Because the quad-switch architecture of the DAC updates its output on both the rising and falling edge (for example, dual edge clocking) of the DACCLK signal, the following two additional modes of operation are available:

- A 2× interpolation filter can be selected to increase the effective DAC update rate (f_{DAC}) to be 2× the input data rate, hence simplifying the analog postfiltering requirements and reducing the effects of alias harmonics in the desired baseband region.
- A Mix-Mode option essentially generates the complement sample on the falling edge such that the original Nyquist spectrum is shifted to f_{DACCLK}, with the sinc null of the DAC falling at $2 \times f_{DACCLK}$.

The digital handoff between the digital domain and mixed signal domain of a high speed DAC is critical in preserving its output dynamic range. A phase locked loop (PLL) with programmable phase offset is used to optimize the timing handoff between these two clock domains. State machines are used to initialize both the DLL and the PLL during the initial boot sequence after receiving a stable DACCLK signal. Following initialization of the two loops, they maintain optimum timing alignment over temperature, time, and power supply variation. The AD9119/AD9129 also provide IRQ capability to monitor the DLL, the PLL, and other internal circuitry.

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LVDS DATA PORT INTERFACE

The AD9119/AD9129 can operate with input data rates of up to 2.85 GSPS. A source synchronous LVDS interface is used between the host and the AD9119/AD9129 to achieve these high data rates, while simplifying the interface. As shown in Figure 129, the host feeds the AD9119/AD9129 with de-interleaved input data into two 11-bit/14-bit LVDS data ports (P0_DxP, P0_DxN and P1_DxP, P1_DxN) at ½ the DAC clock rate (that is, $f_{DACCLK}/2$). Along with the input data, the host provides an embedded DDR data clock input (DCI_x) at $f_{DACCLK}/4$.

A DLL circuit that is designed to operate with DCI clock rates of between 350 MHz and 712.5 MHz is used to generate a phase shifted version of DCI, called the data sampling clock (DSC), to register the input data on both the rising and falling edges.

As shown in Figure 130, the DCI clock edges must be coincident with the data bit transitions with minimum skew and jitter. The nominal sampling point of the input data occurs in the middle of the DCI clock edges because this point corresponds to the center of the data eye. This is also equivalent to a nominal phase shift of 90°of the DCI clock.

The data timing requirements are defined by a minimum data valid margin that is dependent on the data clock input skew, input data jitter, and the variations of the DLL delay line across delay settings. This margin is defined by subtracting from the data period any data skew, data jitter, and the keep-out window (KOW) that is defined by the sum of the set and hold times, as follows:

$$t_{DATA\ VALID\ MARGIN} = t_{DATA\ PERIOD} - t_{DATA\ SKEW} - t_{DATA\ JITTER} - (t_H + t_S)$$

The keep-out window, which is the sum of the set and hold times, is the area where data transitions should not occur. The timing margin allows tuning of the DLL delay setting, either automatically or in manual mode (see Figure 130).

Figure 130 shows that the ideal location for the DSC signal is 90° out of phase from the DCI input. However, due to skew of the DCI relative to the data, it may be necessary to change the DSC phase offset to sample the data at the center of its eye diagram. The sampling instance can be varied in discrete increments by offsetting the nominal DLL phase shift value of 90° via Register 0x0A, Bits[3:0]. The following equation defines the phase offset relationship:

$$Phase\ Offset = 90° \pm n \times 11.25°,\ |n| < 8$$

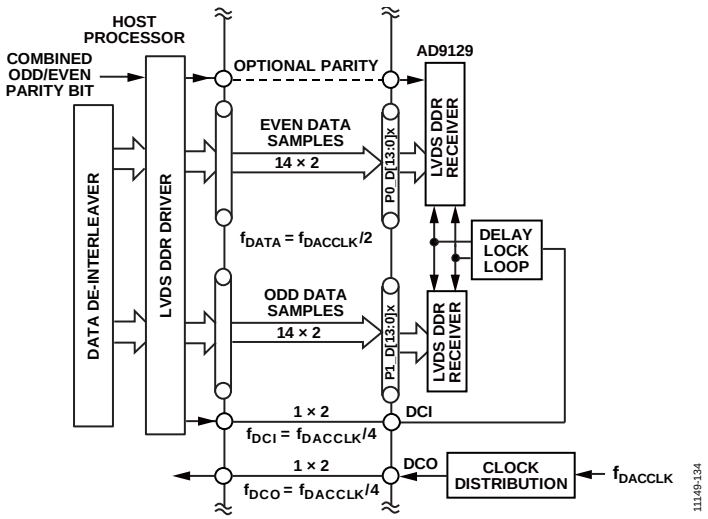

Figure 129. Recommended Digital Interface Between the AD9119/AD9129 and the Host Processor

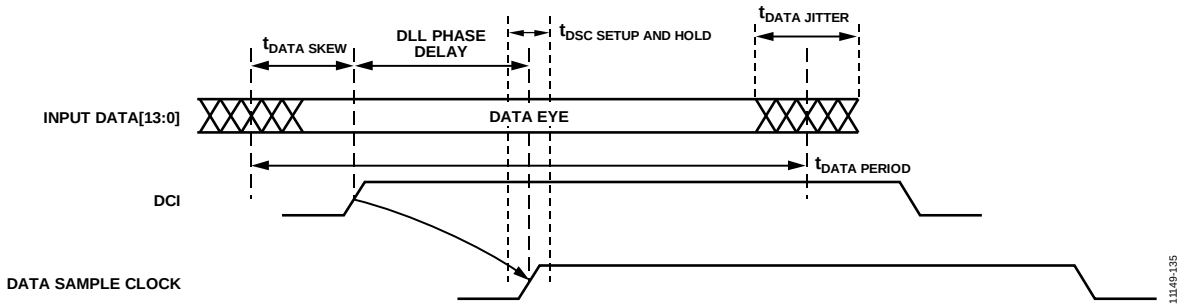

Figure 130. LVDS Data Port Timing Requirements

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Figure 131 shows the DSC set and hold times with respect to the DCI signal and data signals.

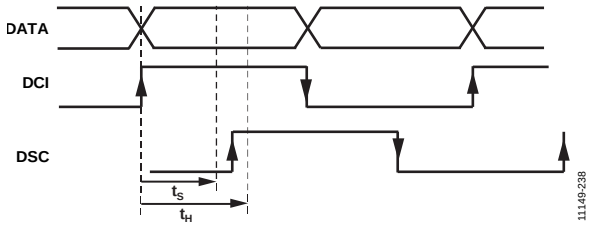

Figure 131. LVDS Data Port Set and Hold Times

Table 11 shows the typical times for various DAC clock frequencies that are required to calculate the data valid margin. The amount of margin that is available for tuning of the DSC sampling point can be determined using Table 11.

Table 10 lists the values that are guaranteed over the operating conditions. These values were taken with 50% duty cycle and DCI swing of 450 mV p-p. For best performance, the duty cycle variation should be kept below ±5%, and the DCI input should be as high as possible, up to 800 mV p-p.

Table 10. Data Port Set and Hold Time Window (Guaranteed)

Frequency, f_{DAC} (MHz)	Time (ps)	Data Port Set and Hold Times (ps) at DLL Phase		
		−3	0	+3
1600	t_S	−272	−489	−683
	t_H	682	911	1120
2300	t_S	−168	−292	−420
	t_H	564	705	839
2800	t_S	−88	−185	−285
	t_H	457	559	652

Table 11. Data Port Set and Hold Time Window (Typical)

Frequency, f_{DAC}[1] (MHz)	Time (ps)	Data Port Set and Hold Times (ps) at DLL Phase												
		−6	−5	−4	−3	−2	−1	0	+1	+2	+3	+4	+5	+6
1400	t_S	−106	−205	−274	−353	−436	−523	−604	−680	−798	−906	−993	−1064	−1131
	t_H	426	499	571	651	730	813	900	977	1069	1152	1235	1303	1387
1500	t_S	−124	−197	−291	−351	−453	−524	−600	−670	−732	−815	−908	−982	−1071
	t_H	427	490	556	637	713	795	870	942	1025	1100	1181	1241	1320
1600	t_S	−120	−191	−252	−335	−402	−495	−552	−626	−704	−776	−847	−902	−978
	t_H	421	485	550	619	689	760	836	910	989	1049	1128	1195	1250
1700	t_S	−111	−184	−226	−301	−370	−442	−528	−580	−641	−719	−784	−822	−895
	t_H	382	429	489	549	619	700	762	825	907	970	1032	1095	1151
1800	t_S	−93	−133	−209	−265	−326	−401	−475	−524	−596	−646	−709	−765	−823
	t_H	400	442	492	555	617	677	754	816	883	950	1003	1061	1122
1900	t_S	−90	−139	−182	−254	−298	−359	−430	−496	−547	−593	−663	−700	−765
	t_H	398	443	488	535	593	664	717	778	849	900	963	1021	1070
2000	t_S	−82	−122	−170	−220	−272	−346	−399	−452	−517	−565	−607	−660	−713
	t_H	389	423	468	522	571	625	683	733	789	854	908	958	1015
2100	t_S	−87	−133	−161	−206	−274	−331	−384	−443	−488	−540	−586	−623	−675
	t_H	370	409	451	491	536	592	636	696	751	794	855	911	954
2200	t_S	−94	−143	−182	−245	−283	−334	−378	−427	−487	−521	−565	−604	−659
	t_H	415	453	487	523	571	622	673	722	778	818	859	908	956
2300	t_S	−93	−131	−182	−227	−270	−312	−357	−388	−439	−485	−531	−570	−623
	t_H	390	422	456	500	542	595	644	686	731	778	821	858	902
2400	t_S	−130	−156	−196	−244	−277	−313	−366	−404	−457	−496	−534	−560	−615
	t_H	426	459	494	529	567	607	653	698	731	769	815	862	911
2500	t_S	−73	−106	−142	−177	−216	−258	−308	−348	−394	−430	−458	−486	−535
	t_H	370	407	433	467	502	546	582	619	662	702	740	780	828
2600	t_S	−43	−76	−115	−145	−184	−228	−275	−306	−351	−375	−402	−443	−491
	t_H	338	369	396	430	466	503	535	567	614	652	690	725	766
2700	t_S	−54	−77	−108	−144	−179	−228	−277	−305	−336	−354	−400	−424	−471
	t_H	316	340	372	406	441	475	499	539	580	622	654	685	729
2800	t_S	−36	−72	−101	−143	−175	−208	−243	−287	−320	−347	−382	−408	−463
	t_H	335	355	379	404	442	480	511	545	575	607	638	676	717

[1] Table 11 shows characterization data for selected f_{DAC} frequencies. Other frequencies are possible, and Table 11 can be used to estimate performance.

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Maximizing the opening of the eye in both the DCI and data signals improves reliability of the data port interface. Use differential controlled impedance traces of equal length (that is, delay) between the host processor and the AD9119/AD9129 input. To ensure coincident transitions with the data bits, implement the DCI as an additional data line with an alternating (010101…) bit sequence from the same output drivers that are used for the data.

For synchronous operation between the host and the AD9119/AD9129, the AD9119/AD9129 provide a data clock output, DCO, to the host at the same rate as DCI (that is, $f_{DACCLK}/4$). Note that the DCI signal can have arbitrary phase alignment with respect to the DCO because the DLL of the AD9119/AD9129 ensures proper data hand-off between the two clock domains (that is, the host processors and the internal digital core of the AD9119/AD9129).

The default reset state of the AD9119/AD9129 is to have the DCO signal disabled. To enable it, write a 1b to Register 0x0C, Bit 6. The DCO output level is controlled in Register 0x7C, Bits[7:6]. The default setting is 01b, or 2.8 mA, but it can be increased to as high as 4 mA (11b) if higher swing is necessary.

The DCI signal is ac-coupled internally; therefore, a possibility exists that removing the DCI signal can cause DAC output chatter due to randomness on the DCI input. To avoid this chatter, it is recommended that the DAC output be disabled when the DCI signal is not present. To do this, program the DAC output current power-down bit in Register 0x01, Bit 6, to 1b. When the DCI signal is again present, the DAC output can be enabled by programming Register 0x01, Bit 6, to 0b. The DAC output powers up in ~2 µs.

The status of the DLL can be polled by reading the data status register at Address 0x0E. Bit 0 indicates that the DLL is running and attempting lock, and Bit 7 is set to 1b when the DLL is locked. Bit 2 is set to 1b when a valid data clock is detected. The warning bits in Address 0x0E, Bits[6:4] can be used as indicators that the DAC may be operating in a nonideal location in the delay line. Note that these bits are read at the SPI port speed, which is much slower than the actual speed of the DLL. This means that these bits can show only a snapshot of what is happening, rather than giving real-time feedback.

Temperature Effects

The length of the delay line varies slightly across the operating temperature range, as the amount of delay through a delay cell expands or contracts slightly due to the temperature change. This can introduce a situation where the DLL may lock at one temperature extreme and then approach an unlocked state as the temperature changes (see Figure 132).

In the example shown in Figure 132, the DLL can lock at Phase Setting 0 at 90° in a cold temperature. As the temperature gets hotter, the delay line changes length, and the controller adjusts the DLL control voltage to keep the 90° offset. In this case, a voltage beyond the acceptable control voltage range is required to hold the 90° phase offset.

Before losing lock, the DLL controller issues a DLL warning by setting Register 0x0E, Bit 6, to 1b and setting either Bit 5 or Bit 4 to 1b. This setting indicates that the DLL is near to losing lock. If the DLL is going to reach the beginning of the delay line soon, the controller issues a start warning by setting Register 0x0E, Bit 5 and Bit 6 to 1b. This setting indicates that the DLL is at the start of the delay line, and losing lock is imminent.

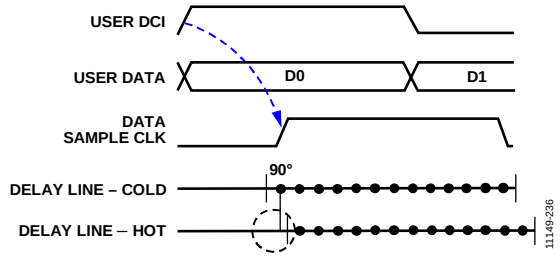

Figure 132. Example of DLL Length Variation Across Temperature

A similar situation can happen at the end of the delay line, in which case a DLL warning and a DLL end is issued. DLL end is indicated when Register 0x0E, Bit 4 and Bit 6 are set to 1b.

In case of a DLL warning, action must be taken to prevent loss of lock. On a start warning, reduce the minimum delay of the delay line by removing one or several of the delay cells. This can be accomplished by setting the bits in Registers 0x70 and Register 0x71 to 0b. Begin by setting Bit 0 of Register 0x70 to 0b, then Bit 1, and so on. In some cases, up to three delay cells may need to be disabled. It is possible to disable up to six delay cells. However, in most cases, none of the cells need to be disabled. The situation varies, depending on the temperature range needed, as well as the DACCLK signal rate used. The end warning case is a theoretical possibility, but practical conditions normally dictate that it is not reachable. If the end warning is reached, the DLL must be relocked immediately. When doing initial lock (or relock) of the DLL, all delay cells must be active, with all delay cell bits in Register 0x70 and Register 0x71 set to 1b.

Parity

The data interface can be continuously monitored by enabling the parity bit feature in Register 0x5C, Bit 7, and configuring the FRM_P, FRM_N pins (Pin K13 and Pin K14) as parity pins by setting Register 0x07, Bits[1:0] = 1 dec. When this pin configuration is used, the host sends a parity bit along with each data sample. This bit is set according to the following formulas, where n is the data sample that is being checked.

For even parity on the AD9129,

XOR[FRM(n), P0_D0(n), P0_D1(n), P0_D2(n), ..., P0_D13(n), P1_D0(n), P1_D1(n), P1_D2(n), …, P1_D13(n)] = 0.

For odd parity on the AD9129,

XOR[FRM(n), P0_D0(n), P0_D1(n), P0_D2(n), ..., P0_D13(n), P1_D0(n), P1_D1(n), P1_D2(n), …, P1_D13(n)] = 1.

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For the AD9119, the data port is 11-bit instead of 14-bit, so P0_D11, P0_D12, P0_D13, P1_D11, P1_D12, and P1_D13 are not used in the calculation of the parity bit. Thus, the parity bit is calculated over 29 bits (including the frame/parity bit) for the AD9129 and over 23 bits for the AD9119.

If a parity error occurs, the parity error counter (Register 0x5D or Register 0x5E) is incremented. Parity errors on the bits that are sampled by the rising edge of DCI increment the parity rising edge error counter (Register 0x5D) and set the parity error rising edge bit (Register 0x5C, Bit 0). Parity errors on the bits that are sampled by the falling edge of DCI increment the parity falling edge error counter (Register 0x5E) and set the parity error falling edge bit (Register 0x5C, Bit 1). The parity counter continues to accumulate until it is cleared, or until it reaches a maximum value of 255. The count can be cleared by writing 1b to Register 0x5C, Bit 5.

An IRQ can be enabled to trigger when a parity error occurs by writing 1b to Register 0x04, Bit 2 for rising edge-based parity detection or to Register 0x04, Bit 3 for falling edge-based parity.

The status of IRQ can be measured via Register 0x06, Bit 2 or Register 0x06, Bit 3 or by using the IRQ pin. When using the IRQ pin and more than one IRQ is enabled, check Register 0x06, Bits[3:2] when an IRQ event occurs to determine whether the IRQ was caused by a parity error. The IRQ can also be cleared by writing 1b to Register 0x06, Bit 2 or Register 0x06, Bit 3.

The parity bit feature can also be used to validate the interface timing. As described previously, the host provides a parity bit with the data samples and configures the AD9119/AD9129 to generate an IRQ. The user can then sweep the sampling instance of the AD9119/AD9129 input registers to determine at what point a sampling error occurs.

DIGITAL DATAPATH DESCRIPTION

Figure 133 provides a more detailed diagram of the AD9119/AD9129 digital datapath. The 22-bit/28-bit datapath with internal DDR clocking interfaces with the dual 11-bit/14-bit input data ports. Because two 11-bit/14-bit samples are captured on each clock edge of DCI, four consecutive samples are captured per DCI clock cycle. Samples captured on the rising edge of DCI propagate through the upper section at a rate of DACCLK/2 (DDR), and those captured on the falling edge propagate through the lower section.

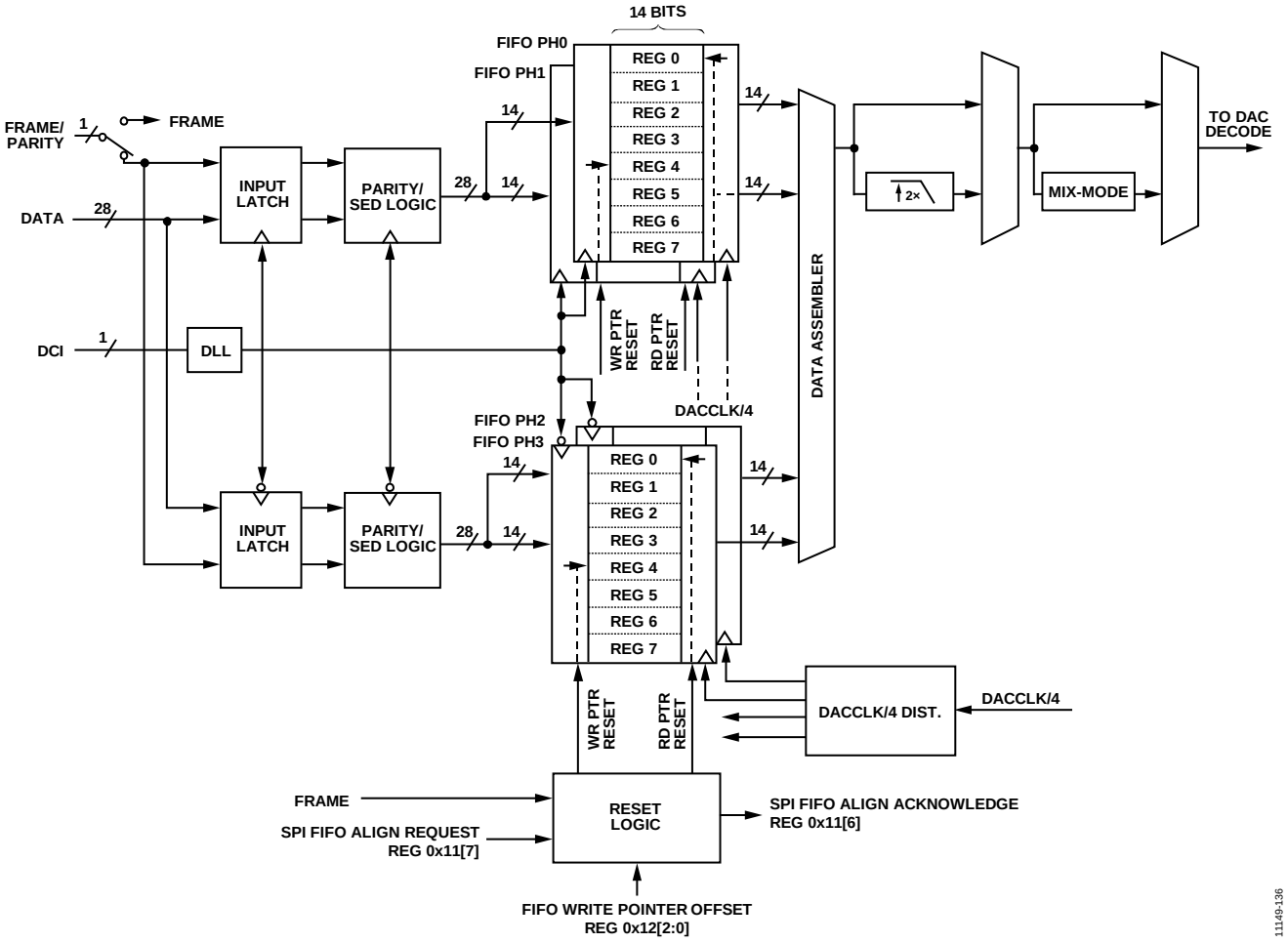

Figure 133. Digital Datapath of the AD9119/AD9129

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After the input data has been captured, the data is passed through a logic block that monitors and/or determines the signal integrity of the high speed digital data interface. The optional parity check is used to continuously monitor the digital interface on a sample-per-sample basis, and the sample error detection (SED) can be used to validate the input data interface for system debug/test purposes. Note that the FRAME and PARITY signals share the same pin assignment because the FRAME signal is typically used during system initialization (for FIFO synchronization purposes), and parity is used in normal operation.

FIFO Description

The next functional block in the datapath is a set of four FIFOs that are eight registers deep. The dual port data is clocked into the FIFOs on both the rising and the falling edge of the DCI signal. The FIFO acts as a buffer that absorbs timing variations between the data source and DAC, such as the clock-to-data variation of an FPGA or ASIC. For the greatest timing margin, maintain the FIFO level near half full (that is, a difference of four between the write and read pointers). The value of the write pointer determines the FIFO register into which the input data is written, and the value of the read pointer determines the register from which data is read and fed into the data assembler. The write and read pointers are updated every time new data is loaded and removed, respectively, from the FIFO.

Valid data is transmitted through the FIFO as long as the FIFO does not overflow or become empty. Note that an overflow or empty condition of the FIFO is the same as the write pointer and read pointer being equal. When both pointers are equal, an attempt is made to simultaneously read and write a single FIFO register. This simultaneous register access leads to unreliable data transfer through the FIFO and must be avoided by ensuring that data is written to the FIFO at the same rate that data is read from the FIFO, keeping the data level in the FIFO constant. This condition must be met by ensuring that DCI is equal to DACCLK/4 (or equivalently, DCO).

Resetting the FIFO Data Level

FIFO initialization is required to ensure a four-sample spacing and a deterministic pipeline latency. If the clocks are running at power-up, the FIFO initializes to 50% full. The AD9119/AD9129 has an internal delay that effectively offsets the FIFO pointers by 2, such that the optimal FIFO data level of 4 (center) reads back as 2 (0000011b) from Register 0x13 to Register 0x16. To achieve this level, set Register 0x12 to 0x20 (hexadecimal) before resetting the FIFO. This sets the read pointer to Level 2 and the write pointer to Level 0.

To maximize the timing margin between the DCI input and the internal DAC data rate clock, initialize the FIFO data level before beginning data transmission. The value of the FIFO data level can be initialized in three ways: by resetting the device, by strobing the FRM_x input, and via a write sequence to the serial port.

The two preferred methods are use of the FRAME signal and via a write sequence to the serial port. Before initializing the FIFO data level, the LVDS DLL and the DAC clock PLL must be locked.

The FRM_x input can be used to initialize the FIFO data level value. First, set up the FRM_N and FRM_P pins for frame mode (Register 0x07, Bits[1:0] = 2). Next, assert the FRAME signal high for at least one DCI clock cycle. When the FRAME signal is asserted in this manner, the write pointer is set to 4 (by default or to the FIFO start level (Register 0x12, Bits[2:0])) the next time the read pointer becomes 0 (see Figure 134).

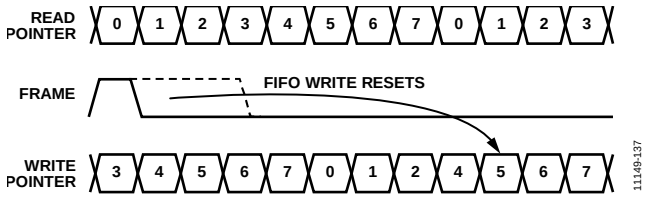

Figure 134. Timing of the Frame Input vs. Write Pointer Value

To initialize the FIFO data level through the serial port, toggle Bit 7 of Register 0x11 from 0b to 1b. When the write to the register is complete, the FIFO data level is initialized.

The recommended procedure for a serial port FIFO data level initialization is as follows:

1. Request FIFO level reset by setting Register 0x11, Bit 7, to 1b.
2. Verify that the part acknowledges the request by ensuring that Register 0x11, Bit 6, is set to 1b.
3. Remove the request by setting Register 0x11, Bit 7, to 0b.
4. Verify that the part drops the acknowledge signal by ensuring that Register 0x11, Bit 6, is set to 0b.

Monitoring the FIFO Status

The relative FIFO data levels can be read from Register 0x13 through Register 0x16 at any time. The FIFO data level reported by the serial port is denoted as a 7-bit thermometer code of the write counter state, relative to the absolute read counter being at 0.

For example, the FIFO data level of 2 is reported as a value of 0000011b in the status register. Adding the internal delay of 2 to this value makes the reported FIFO level equal to 4. It should be noted that, depending on the timing relationship between DCI and the main DACCLK signal, the FIFO level value can be off by a count of ±1. Therefore, it is important that the difference between the read and write pointers be maintained at ≥2.

Multiple DAC Synchronization

Synchronization of multiple AD9119/AD9129s implies that all of the DAC outputs are time aligned to the same phase when all devices are fed with the same data pattern (along with DCI) at the same instance of time. FIFO initialization ensures that the initial pipeline latency in the FIFO is set to four samples and remains at this level, assuming that no process, voltage, or temperature variations occur between the host and the AD9119/AD9129 clock domains.

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Figure 136 shows an example of two AD9119/AD9129 devices that are synchronized to the same host (that is, FPGA or ASIC). Note that, when the same resources are used to generate these output signals, synchronization to a single host IC ensures minimum data and DCI time skew between devices.

Synchronization within a data sample requires insight into the difference between the read pointers of the master and slave devices, as well as the ability to vary the delay of the slave device(s) within the host to compensate for initial offsets between devices. It is possible to calculate how many data samples the slave device(s) is offset from the master device for the following reasons:

- The pipeline delay of each device is the same after FIFO initialization (FIFO reset).
- The read counter of each device is derived from the same phase aligned DACCLK source.
- The state of the read counters of each device is sampled at the same instance in time via the FRAME signal.
- The readback value (Register 0x12[6:4]) is normalized to a data sample (that is, a DACCLK period).

By calculating the difference between the read pointer settings of the master and slave devices, the user can advance or delay the data stream of the slave device within the FPGA. Because this difference can be up to ±4 data samples, the FPGA must provide this adjustment range for DAC synchronization alone. Note that additional range must be added to compensate for any other system delay variation.

In addition to synchronizing to the data sample level, the AD9119/AD9129 can enable synchronization to the DACCLK level (see Figure 135). A 1.8 V CMOS output pin, SYNC, can be used to provide a DACCLK/8 signal. Using the SYNC output from each DAC, enabled by Register 0x1A, Bit 4 = 1, the user can create a simple phase detector with an external XOR gate.

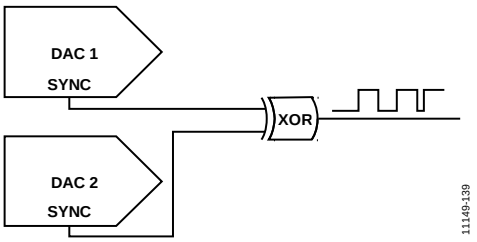

Figure 135. Example of Synchronization of Two DACs to ±1 DACCLK Accuracy

By adjusting the internal delay (incrementing or decrementing by one DACCLK cycle with each write to Register 0x1A, Bit 7 or Bit 6, respectively), the user can align the DACCLKs inside the two DACs to within ±1 DACCLK cycle, when errors from the external phase detector, low-pass filter, and delay differences are taken into account. The existing phase position can be read from Register 0x1A, Bits[2:0]. The value of each DAC in Register 0x1A Bits[2:0] can be different when the DACs are synchronized. Align the SYNC outputs first, then reset the FIFOs on each DAC to ensure that proper sync is achieved.

This calibration must be performed at each power-up because the FIFOs can be reset to any of four levels based on the divide-by-4 output of the clock distribution block (see Figure 133). For example, a FIFO reset to Level 2 could have an actual FIFO level of 1.5, 1.75, 2, or 2.25, based on the location of the div-by-4 clock edge. Adjusting the SYNC signals to align with each other eliminates this ambiguity. As with the Sync register (0x1A Bits[2:0]), the FIFO levels on each DAC do not have to match (i.e., can be different) when the DACs are synchronized.

The FIFO set or reset level is always a whole number (the recommended value is 2). Because of this, there is a possibility that the FIFO can be reset on the border of a rollover from a fractional level to a whole level (as in 1.75 to 2.0). In this case, an effect can occur that causes the FIFO Read level to increment before the final read, thereby shifting the level from 1.75 to 2.75 and thus effectively setting the level to 3 instead of 2. This can be noticed by a seeming 4 DAC sample offset in the output.

To avoid this issue (setting the FIFO before emptying its last read), the FIFO must be reset and then read back to understand its level. If it is a whole number, it is recommended that the DCI is advanced or delayed by 1 DACCLK cycle relative to the FIFO. This must be done in the FPGA if DCO is used as the timing reference for DCI. If this is not possible in the FPGA, then it is recommended that the DCO NOT be used to generate DCI, in order to decouple the two clocks and enable this necessary phase shift. If the DCI is generated independently from the DCO, then the 1 DACCLK delay or advance can be accomplished by incrementing or decrementing by 1 the SYNC output of both DACs in the same direction.

When the two DACs are aligned, the drift over temperature and supply voltage of the SYNC signal of one DAC, relative to another DAC, is expected to be no more than 450 ps.

The DCO signal is derived from the SYNC signal such that if the SYNC signal is adjusted by a DACCLK cycle, the DCO signal will also be adjusted by the same amount.

When all adjustments of the SYNC signal are complete, it is recommended to disable the SYNC output by programming Register 0x1A, Bit 4 = 0, to eliminate a possible source of clock spurious signals.

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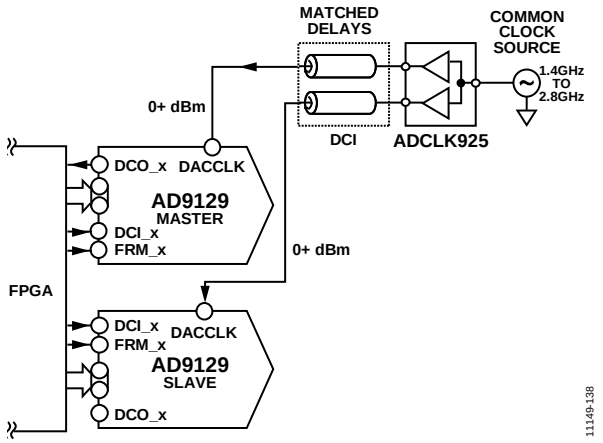

Figure 136. Example of Synchronization of Two DACs to One FPGA

Data Assembler and Signal Processing Modes

The data assembler reconstructs the original sample sequence. It consists of a 4:1 multiplexer operating at f_{DACCLK}. Each of the four FIFOs provides a sample that is now referenced to the internal clock domain of the AD9119/AD9129, f_{DACCLK}. The reconstructed sample sequence can be directed to the DAC decode logic or undergo additional signal processing. In 2× interpolation mode, a FIR filter is used to generate a new data sample that is inserted between each sample, such that it can update the DAC decode logic on the falling edge of DACCLK. In Mix-Mode, the complement of each data sample is generated and inserted after it, such that it also updates the DAC in a similar manner. The 2× interpolator can be used with Mix-Mode enabled.

2× Digital Filter

The AD9119/AD9129 include a bypassable 2× half-band interpolation filter to help simplify the analog reconstruction filter. The filter has the potential benefit of minimizing the impact of folded back harmonics in the desired baseband region. The filter operates in a dual-edge clocking mode, where it generates a new interpolated sample value for every alternate DACCLK edge. This effectively increases the DAC update rate to 2 × f_{DACCLK} with the DAC's sinc response null moving from f_{DACCLK} to 2 × f_{DACCLK}.

There are two different filters, FIR25 and FIR40, that can be chosen using Register 0x18, Bit 5, when the 2× interpolator is enabled with Register 0x18, Bit 7.

The FIR25 half-band filter provides 25 dB of stop-band rejection. Its response is shown in Figure 137. Coefficients were optimized for practical implementation purposes with the notion that the ±0.5 dB pass-band ripple effects on a multicarrier application (for example, DOCSIS) can be compensated by the digital host adjusting individual channel powers. Note that the worst-case tilt across any 6 MHz channel is less than −0.05 dB.

The FIR40 half-band filter provides 40 dB of stop-band rejection, and its response is shown in Figure 139. Coefficients were chosen to reduce pass-band ripple and increase out-of-band rejection for multicarrier applications (for example, DOCSIS). As a result, the frequency response has a flatter in-band response and a sharper transition region, and the trade-off is a higher phase count, leading to higher pipeline delay and higher power consumption. The two filters are compared in Table 12.

Table 12. Features of the Two 2× Interpolation Filters

Filter	Ripple (dB)	Attenuation (dB)	Power (mW)
FIR25	±0.5	25	150
FIR40	±0.1	40	450

A duty cycle restore circuit follows the DACCLK clock receiver to minimize impact of duty cycle errors on image rejection.

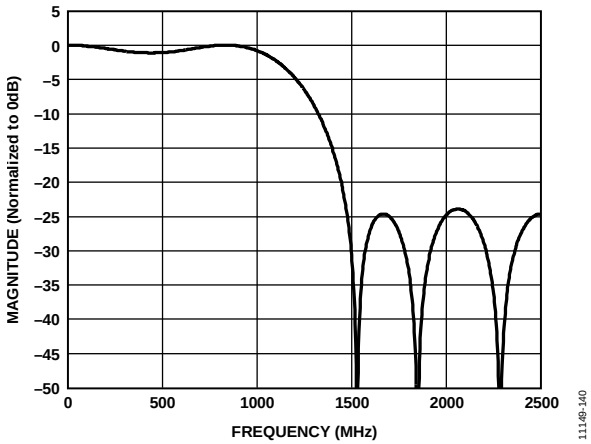

Figure 137. FIR25 2× Interpolation Filter Plot, Complete Frequency Response; f_{DAC} = 2.5 GHz

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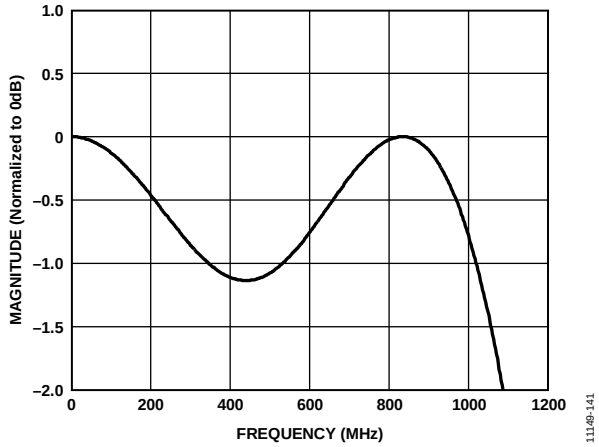

Figure 138. FIR25 2× Interpolation Filter Plot, Pass-Band Ripple; f_{DAC} = 2.5 GHz

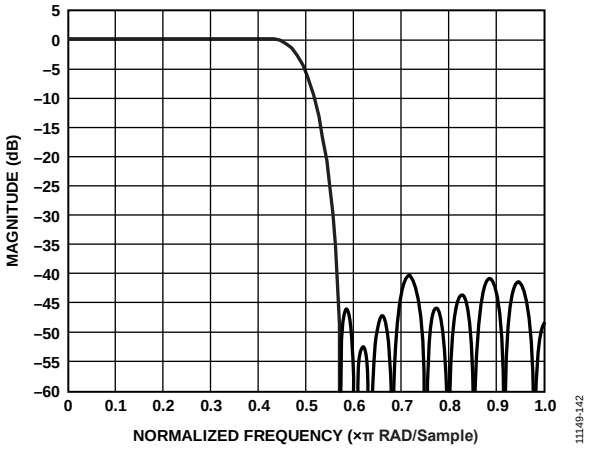

Figure 139. FIR40 2× Interpolation Filter Plot, Complete Frequency Response

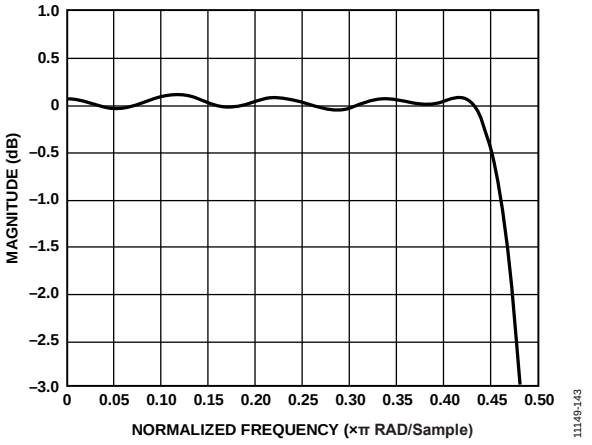

Figure 140. FIR40 2× Interpolation Filter Plot, Pass-Band Ripple

Pipeline Delay (Latency)

The pipeline delay, or latency, of the AD9129 varies, based on the configuration that is chosen and can be calculated using the following formula:

$$Pipeline_Total = Pipeline_Delay + 2\times_Delay + Group_Delay + FIFO_Level$$

The values listed in Table 13 can be used, depending on the mode of operation that is selected.

Table 13. Pipeline Delay Values for Each Block

Mode	Pipeline Delay (f_{DAC} cycles)	Group Delay (f_{DAC} cycles)	Total Pipeline (f_{DAC} cycles)	Total Delay (f_{DAC} cycles)
No 2× filter	74	N/A	74	74
With FIR25	43	2	117	119
With FIR40	67	9	141	150

The terms used in Table 13 are defined as follows:

- Pipeline delay is the time from DAC code latched until the DAC output begins to move.
- Group delay is the time for the maximum amplitude pulse to reach the DAC output, as compared to the first time the output moves.
- No 2× filter is the base pipeline delay, including data interface, analog circuitry (six cycles), and data FIFO at half-full/Position 3.
- FIR25 is the 2× interpolator with 25 dB of out-of-band rejection.
- FIR40 is the 2× interpolator with 40 dB of out-of-band rejection.

Note that the values for pipeline delay apply in both normal mode and Mix-Mode. After the total delay through the digital blocks is calculated, add the FIFO level to that delay to find the total pipeline delay. Note that the pipeline delay can be considered fixed, with the only ambiguity being the FIFO state. The FIFO state can be initialized as part of the startup sequence to ensure a four sample spacing and, therefore, a fixed pipeline delay, or deterministic latency (see the Resetting the FIFO Data Level section for more information).

To ensure repeatable pipeline delay over multiple power-up cycles, the SYNC output of the DAC must be aligned with a known system sync reference. Follow a calibration process that is similar to the multiple DAC sync process (see the Multiple DAC Synchronization section for more information) after each power-up event to align the DAC to the system sync reference.

Power-Up Time

The AD9119/AD9129 have a power-down register (Register 0x01) that enables the user to power down various portions of the DAC. The power-up time for several usage cases is shown in Table 14.

The recommended way to power up the AD9119/AD9129 is to power up all parts of the circuit with I_{REF} disabled (by setting Register 0x01, Bit 6 = 1b), and then enable I_{REF} by programming Register 0x01, Bit 6 = 0b.

Table 14. Power-Up Times for Several Usage Cases

State	Register State	Time (µs)
Power-Up	From 0x01 = 0xEF to 0x01 = 0x08	250
Clock Path Up	From 0x01 = 0x0C to 0x01 = 0x08	220
Wake-Up	From 0x01 = 0x48 to 0x01 = 0x08	2

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RESET

The hardware reset pin (Pin H1) is active high and resets all registers on the device. The software reset bit in Register 0x00 (Bit 5) performs the same reset function, except that it preserves the current contents of Register 0x00.

INTERRUPT REQUESTS

The AD9119/AD9129 can provide the host processor with an interrupt request output signal (IRQ), indicating that one or more of the following events has occurred:

- One of the clock controllers has established or lost lock.
- A parity error has occurred.
- A sample error detection status or result is ready.
- The FIFO is nearing an overwrite status.

The IRQ output signal is an active low output signal that is available on the IRQ pin (Pin H2). If used, connect the output to VDD via a 10 kΩ pull-up resistor.

Each IRQ is enabled by setting the enable bits in Register 0x03 and Register 0x04 that have the same bit mapping as the IRQ status bits in Registers 0x05 and Register 0x06. If an interrupt bit is not enabled, a read request of that bit shows a direct readback of the current state of the source. Thus, a read request of either register shows the current state of all eight interrupts in that register, regardless of whether each individual bit is actually enabled to generate an interrupt. When an interrupt bit is enabled, it captures a rising edge of the interrupt source and holds it, even if the source subsequently returns to its zero state. It is possible, for example, for the retimer lost interrupt enable and retimer lock interrupt enable status bits (Register 0x03[1:0], respectively) to be set when a controller temporarily loses lock but then reestablishes lock before the IRQ is serviced by the host. In such a case, the host should validate the present status of the suspect block by reading back its current status bits. Based on the status of these bits, the host can take appropriate action, if required.

The IRQ pin responds only to those interrupts that are enabled. To clear an IRQ, it is necessary to write a 1b to the bit in Register 0x05 or Register 0x06 that caused the interrupt. See Figure 141 for a detailed diagram of the interrupt circuitry.

The IRQ can also be used during the AD9119/AD9129 initialization phase after power-up to determine when the retimer PLL and data receiver controllers achieve lock. For example, before enabling the retimer PLL, the retimer lock interrupt enable bit (Register 0x03[0]) can be set, and the IRQ output signal can be monitored to determine when lock is established, before continuing in a similar manner with the data receiver controller. Clear the relevant lock bit, after locking, before continuing to the next controller. When all of the controllers are locked, set the appropriate lost lock enable bits in Register 0x03 to continuously monitor the controllers for loss of lock.

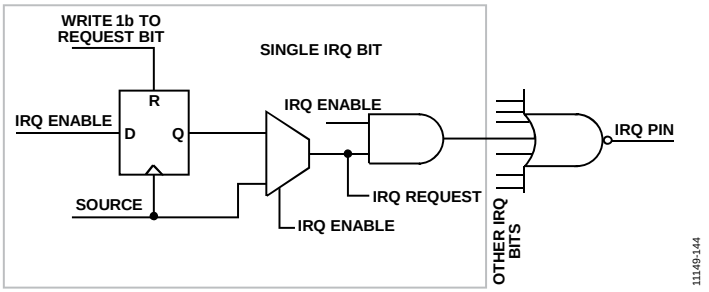

Figure 141. Interrupt Request Circuitry

Table 15. Interrupt Request Registers

Addr (Hex)	Bit	Bit Name	Description
0x05	7	FIFO_Warn2 interrupt status	Indicates that the FIFO is within two slots of overwrite
	6	FIFO_Warn1 interrupt status	Indicates that the FIFO is within one slot of overwrite
	5	SPIFrmAck interrupt status	Indicates acknowledgement that the SFrmReq bit has changed from 0b to 1b
	4	Reserved	Reserved
	3	DLL warn interrupt status	Indicates that the DLL is close to coming unlocked and action is needed
	2	DLL lock interrupt status	Indicates that the DLL is now locked
	1	Retimer lost interrupt status	Indicates that the retimer PLL is no longer locked
	0	Retimer lock interrupt status	Indicates that the retimer PLL is now locked
0x06	7	Reserved	Reserved
	6	AED pass interrupt status	Indicates that the AED logic has captured eight valid samples
	5	AED fail interrupt status	Indicates that the AED logic has detected a miscompare
	4	SED fail interrupt status	Indicates that the SED logic has detected a miscompare
	3	Parity error falling edge status	Indicates a parity fault due to data captured on the falling edge
	2	Parity error rising edge status	Indicates a parity fault due to data captured on the rising edge
	1	Reserved	Reserved
	0	Reserved	Reserved

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INTERFACE TIMING VALIDATION

The AD9119/AD9129 provide on-chip sample error detection (SED) circuitry that simplifies verification of the input data interface. The SED compares the input data samples captured at the digital input pins with a set of comparison values. The comparison values are loaded into registers through the SPI port. Differences between the captured values and the comparison values are detected and stored.

SAMPLE ERROR DETECTION (SED) OPERATION

The SED circuitry operates on a data set made up of eight 11-bit/14-bit input words, denoted as R0L, R1L, R0H, R1H, F0L, F1L, F0H, and F1H. These represent the rising edge and falling edge data of Data Port 0 and Data Port 1. (The AD9119/AD9129 use both edges of the DCI clock to sample data on each input port.) To properly align the input samples, the rising edge data-words of the data ports (that is, RxL and RxH) are indicated by asserting the FRAME signal for a minimum of two complete input samples.

Figure 142 shows the input timing of the interface in word mode. The FRAME signal can be issued once at the start of the data transmission, or it can be asserted repeatedly at intervals coinciding with the RxL and RxH data-words.

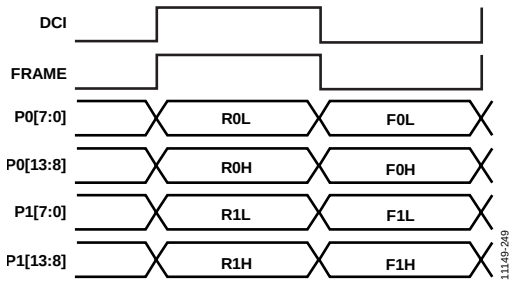

Figure 142. Timing Diagram of FRAME Signal Required to Align Input Data for SED

The SED has three flag bits (Register 0x50, Bit 0, Bit 1, and Bit 2) that indicate the results of the input sample comparisons. The SED fail bit (Register 0x50, Bit 0) is set when an error is detected and remains set until cleared. The SED also provides registers that indicate which input data bits experienced errors (Register 0x51 through Register 0x58). These bits are latched and indicate the accumulated errors detected until cleared. To clear the SED registers, write 1b to Register 0x50, Bit 6.

The autosample error detection (AED) mode is an autoclear mode that has the following two effects:

- AED mode activates the AED fail bit and the AED pass bit (Register 0x50, Bit 1 and Bit 2).
- AED mode changes the behavior of Register 0x51 through Register 0x58.

The compare pass bit is set if the last comparison indicates that the sample is error free. The compare fail bit is set if an error is detected. The compare fail bit is automatically cleared by the reception of eight consecutive error-free comparisons. When autoclear mode is enabled, Register 0x51 through Register 0x58 accumulate errors as previously described but reset to all 0s after eight consecutive error-free sample comparisons are made.

The sample error, compare pass, and compare fail flags can be configured to trigger an IRQ when active, if desired. This is accomplished by enabling the appropriate bits in the event flag register (Register 0x06, Bit 4, Bit 5, and Bit 6).

SED EXAMPLE

Normal Operation

The following example illustrates the SED configuration for continuously monitoring the input data and assertion of an IRQ when a single error is detected.

1. Write to the following registers to load the comparison values:
   a) Register 0x51: SED Patt/Err R0L, Bits[7:0].
   b) Register 0x52: SED Patt/Err R0H, Bits[13:8].
   c) Register 0x53: SED Patt/Err R1L, Bits[7:0].
   d) Register 0x54: SED Patt/Err R1H, Bits[13:8].
   e) Register 0x55: SED Patt/Err F0L, Bits[7:0].
   f) Register 0x56: SED Patt/Err F0H, Bits[13:8].
   g) Register 0x57: SED Patt/Err F1L, Bits[7:0].
   h) Register 0x58: SED Patt/Err F1H, Bits[13:8].
   i) Comparison values can be chosen arbitrarily; however, choosing values that require frequent bit toggling provides the most robust test.
2. Enable the SED error detect flag to assert the IRQ pin.
   a) Register 0x04: set to 0x10.
3. Begin transmitting the input data pattern.
4. Write three times to Register 0x50 to enable the SED.
   a) Register 0x50: set to 0x80.
   b) Register 0x50: set to 0xC0.
   c) Register 0x50: set to 0x80.

If IRQ is asserted, read Register 0x50 and Register 0x51 through Register 0x58 to verify that a SED error is detected and determine which input bits are in error. The bits in Register 0x51 through Register 0x58 are latched. This means that the bits indicate any errors that occur on those bits throughout the test and not just the errors that caused the error detected flag to be set.

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ANALOG INTERFACE CONSIDERATIONS

ANALOG MODES OF OPERATION

The AD9119/AD9129 use the quad-switch architecture shown in Figure 143. Only one pair of switches is enabled during a half-clock cycle, thus requiring each pair to be clocked on alternative clock edges. A key benefit of the quad-switch architecture is that it masks the code-dependent glitches that occur in the conventional two-switch DAC architecture.

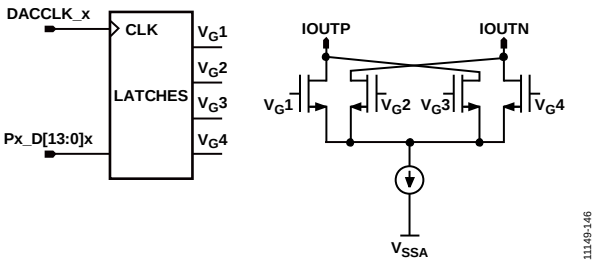

Figure 143. Quad-Switch Architecture

In two-switch architecture, when a switch transition occurs and D_1 and D_2 are in different states, a glitch occurs. But, if D_1 and D_2 happen to be at the same state, the switch transitions, and no glitches occur. This code-dependent glitching causes an increased amount of distortion in the DAC. In quad-switch architecture (no matter what the codes are), there are always two switches that are transitioning at each half-clock cycle, thus eliminating the code-dependent glitches but, in the process, creating a constant glitch at 2 × DACCLK. For this reason, a significant clock spur at 2 × f_{DACCLK} is evident in the DAC output spectrum.

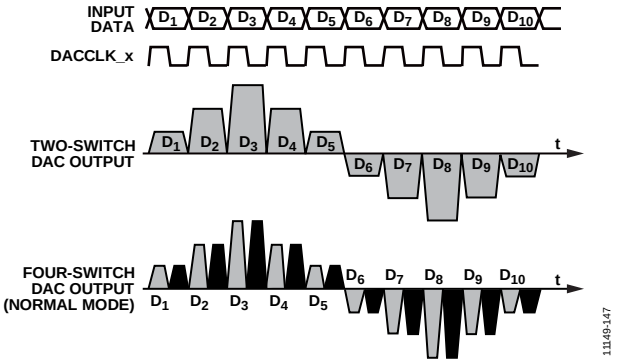

Figure 144. Two-Switch and Quad-Switch DAC Waveforms

As a consequence of the quad-switch architecture enabling updates on each half-clock cycle, it is possible to operate that DAC core at 2× the DACCLK rate if new data samples are latched into the DAC core on both the rising and falling edge of the DACCLK. This notion serves as the basis when operating the AD9119/AD9129 in either Mix-Mode or with the 2× interpolation filter enabled. In each case, the DAC core is presented with new data samples on each clock edge, albeit in Mix-Mode; the falling edge sample is simply the complement of the rising edge sample value.

When Mix-Mode is used, the output is effectively chopped at the DAC sample rate. This has the effect of reducing the power of the fundamental signal while increasing the power of the images centered around the DAC sample rate, thus improving the dynamic range of these images.

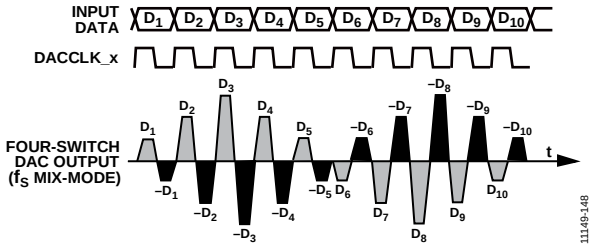

Figure 145. Mix-Mode Waveform

This ability to change modes provides the user the flexibility to place a carrier anywhere in the first three Nyquist zones, depending on the operating mode selected. Switching between baseband and Mix-Mode reshapes the sinc roll-off inherent at the DAC output. In baseband mode, the sinc null appears at f_{DACCLK} because the same sample latched on the rising clock edge is also latched again on the falling clock edge, thus resulting in the same ubiquitous sinc response of a traditional DAC. In Mix-Mode, the complement sample of the rising edge is latched on the falling edge, therefore pushing the sinc null to 2 × f_{DACCLK}. Figure 146 shows the ideal frequency response of both modes with the sinc roll-off included.

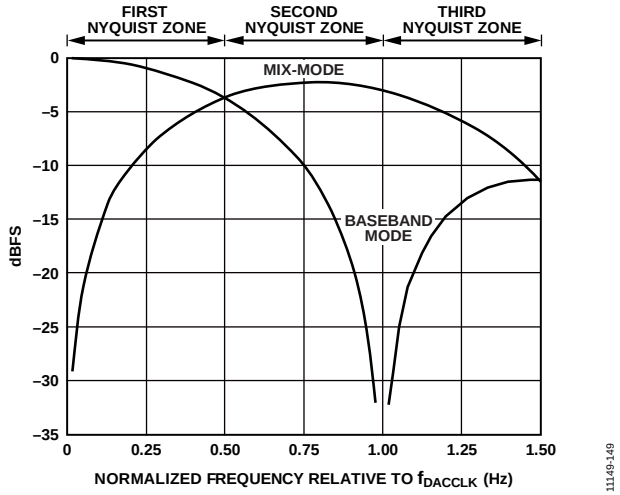

Figure 146. Sinc Roll-Off for Baseband Mode and Mix-Mode Operation

The quad-switch can be configured via SPI (Register 0x19, Bit 0) to operate in either baseband mode (0b) or Mix-Mode (1b).

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CLOCK INPUT

The AD9119/AD9129 contain a low jitter, differential clock receiver that is capable of interfacing directly to a differential or single-ended clock source. Because the input is self-biased to a nominal midsupply voltage of 1.25 V with a nominal impedance of 10 kΩ//2 pF, it is recommended that the clock source be ac-coupled to the DACCLK_x input pins with an external differential load of 100 Ω. When the nominal differential input span is 1 V p-p, the clock receiver can operate with a span that ranges from 250 mV p-p to 2.0 V p-p.

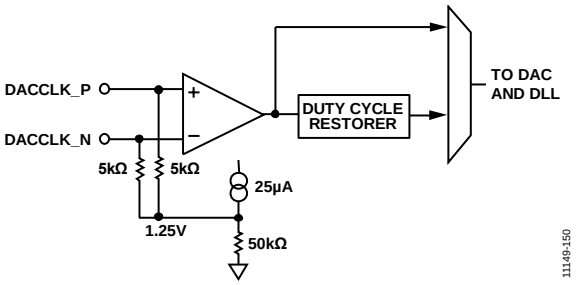

Figure 147. Clock Input

The quality of the clock source, as well as its interface to the AD9119/AD9129 clock input, directly impacts ac performance. Select the phase noise and spur characteristics of the clock source to meet the target application requirements. Phase noise and spurs at a given frequency offset on the clock source are directly translated to the output signal. It can be shown that the phase noise characteristics of a reconstructed output sine wave are related to the clock source by 20 × log10 (f_{OUT}/f_{CLK}) when the DAC clock path contribution is negligible. (The wideband noise is not dominated by the thermal and quantization noise of the DAC.)

Figure 148 shows a clock source based on the ADF4350 low phase noise/jitter PLL. The ADF4350 can provide output frequencies from 140 MHz up to 4.4 GHz with jitter as low as 0.5 ps rms. Its squared-up output level can be varied from −4 dBm to +5 dBm, allowing further optimization of the clock drive level.

A clock control register exists at Address 0x30. This register can be used to enable automatic duty cycle correction (Bit 1), enable zero-crossing control (Bit 6), and set the zero-crossing point (Bits[5:2]). Recommended settings for this register are listed in the recommended start-up sequence section (see the Start-Up Sequence section).

PLL

The DACCLK_x input goes to a high frequency PLL to ensure robust locking of the DAC sample clock to the input clock. The PLL is enabled by default such that the PLL locks upon power-up. The PLL (or DAC clock retimer) control registers are located at Register 0x33 and Register 0x34. Register 0x33 enables the user to set the phase detector phase offset level (Bits[7:4]), clear the PLL lost lock status bit (Bit 3), choose the PLL divider for optimum performance (Bit 2), and choose the phase detector mode (Bits[1:0]). These settings are determined during product characterization and are given in the recommended start-up sequence (see the Start-Up Sequence section). It is not normally necessary to change these values, nor is the product characterization data valid on any settings other than the recommended ones. Register 0x34 is used to reset the PLL, should that become necessary.

At DACCLK = 2.85 GSPS, the lock time is about 10 µs. In most situations, no action is required with the PLL. If the DACCLK is changed and, especially, if it is changed multiple times, as in a frequency hopping application, a phase slip or glitch may be caused by the change in frequency, and it may become necessary to reset the PLL. This can be checked by reading the PLL retimer lost lock bit (Register 0x35, Bit 6). If that is the case, toggle the PLL reset bit by programming Register 0x34, Bit 3, high and then low. In addition, clear the PLL retimer lost lock bit by writing 0b to Register 0x35, Bit 6. PLL lock can be verified by reading the PLL lock bit at Register 0x35, Bit 7. It is possible to use the IRQ registers to set an interrupt for these events. See the Interrupt Requests section for more details.

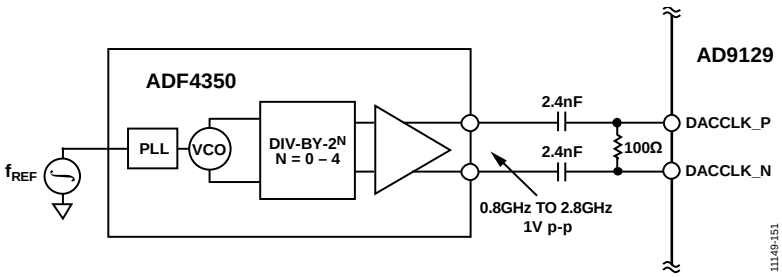

Figure 148. Possible Signal Chain for DACCLK_x Input

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VOLTAGE REFERENCE

The AD9119/AD9129 output current is set by a combination of digital control bits and the I250U reference current, as shown in Figure 149.

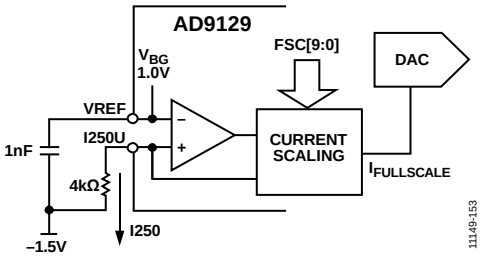

Figure 149. Voltage Reference Circuit

The reference current is obtained by forcing the band gap voltage across an external 4.0 kΩ resistor from I250U (Pin A1) to VSSA. The 1.0 V nominal band gap voltage (VREF) generates a 250 µA reference current in the 4.0 kΩ resistor. Note the following constraints when configuring the voltage reference circuit:

- Both the 4.0 kΩ resistor and 1 nF bypass capacitor are required for proper operation.
- Adjusting the DAC output full-scale current, I_{OUTFS}, from its default setting of 20 mA should be performed digitally.
- The AD9119/AD9129 are not multiplying DACs. Modulation of the reference current, I250U, with an ac signal is not supported.
- The band gap voltage appearing at the VREF pin must be buffered for use with an external circuitry because its output impedance is approximately 7.5 kΩ.
- An external reference can be used to overdrive the internal reference by connecting it to the VREF pin.

As mentioned, the I_{OUTFS} can be adjusted digitally over a 9.4 mA to 34.2 mA range by the FSC_x[9:0] bits (Register 0x20, Bits[7:0] and Register 0x21, Bits[1:0]). The following equation relates I_{OUTFS} to the FSC_x[9:0] bits, which can be set from 0 to 1023.

$$I_{OUTFS} = 24.21875 \text{ mA} \times FSC_x[9:0]/1000 + 9.4 \text{ mA} \quad (1)$$

Note that the default value of 0x200 generates 21.937 mA full scale, but most of the characterization presented in this datasheet uses 33 mA, unless noted otherwise.

ANALOG OUTPUTS

Equivalent DAC Output and Transfer Function

The AD9119/AD9129 provide complementary current outputs, IOUTP and IOUTN, that sink current from an external load that is referenced to the 1.8 V VDDA supply. Figure 150 shows an equivalent output circuit for the DAC. Compared to most current output DACs of this type, the outputs of the AD9119/AD9129 exhibit a slight offset current (that is, $I_{OUTFS}/17$), and the peak differential ac current is slightly below $I_{OUTFS}/2$ (that is, $8/17 \times I_{OUTFS}$).

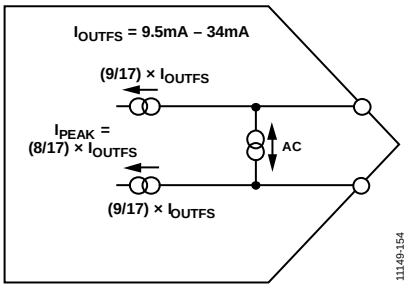

Figure 150. Equivalent DAC Output Circuit

The example shown in Figure 150 can be modeled as a pair of dc current sources that source a current of $9/17 \times I_{OUTFS}$ to each output. A differential ac current source, I_{PEAK}, is used to model the signal (that is, a digital code) dependent nature of the DAC output. The polarity and signal dependency of this ac current source is related to the digital code (F) by the following equation:

$$F\ (code) = (DACCODE - 8192)/8192 \quad (2)$$

$$-1 \leq F\ (code) < +1 \quad (3)$$

where *DACCODE* = 0 to 16,383 (decimal).

Because I_{PEAK} can swing $\pm(8/17) \times I_{OUTFS}$, the output currents that are measured at IOUTP and IOUTN can span from $I_{OUTFS}/17$ to I_{OUTFS}. However, because the ac signal-dependent current component is complementary, the sum of the two outputs is always constant (that is, IOUTP + IOUTN = $(18/17) \times I_{OUTFS}$).

The code-dependent current that is measured at the IOUTP (and IOUTN) output is as follows:

$$IOUTP = (9/17) \times I_{OUTFS}\ (\text{mA}) + (8/17) \times I_{OUTFS}\ (\text{mA}) \times F\ (code) \quad (4)$$

$$IOUTN = (9/17) \times I_{OUTFS}\ (\text{mA}) - (8/17) \times I_{OUTFS}\ (\text{mA}) \times F\ (code)$$

Figure 151 shows the IOUTP vs. DACCODE transfer function when I_{OUTFS} is set to 19.65 mA.

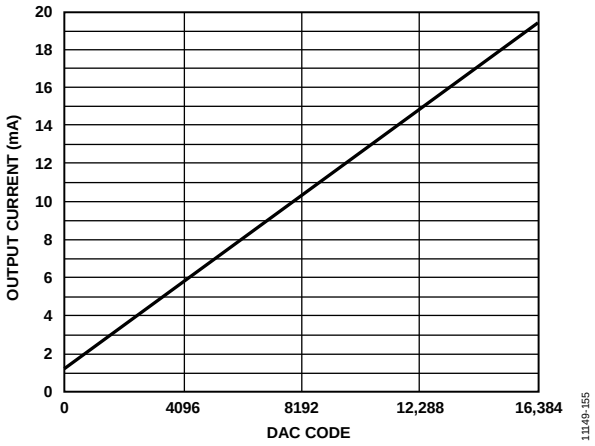

Figure 151. Gain Curve for FSC_x[9:0] = 512, DAC Offset = 1.228 mA

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Peak DAC Output Power Capability

The maximum peak power capability of a differential current output DAC is dependent on its peak differential ac current, I_{PEAK}, and the equivalent load resistance it sees. In the case of a 1:1 balun with 50 Ω source termination, the equivalent load that is seen by the DAC ac current source is 25 Ω. If the AD9119/AD9129 is programmed for an I_{OUTFS} = 20 mA, its peak ac current is 9.375 mA and its peak power, delivered to the equivalent load, is 2.2 mW (that is, $P = I^2R$). Because the source and load resistance seen by the 1:1 balun are equal, this power is shared equally. Hence, the output load receives 1.1 mW, or 0.4 dBm peak power.

To calculate the rms power delivered to the load, consider the following:

- Peak-to-rms of digital waveform
- Any digital backoff from digital full scale
- DAC sinc response and nonideal losses in the external network

For example, a reconstructed sine wave with no digital backoff ideally measures −2.6 dBm because it has a peak-to-rms ratio of 3 dB. If a typical balun loss of 0.4 dBm is included, the user would expect to measure −3 dBm of actual power in the region where the sinc response of the DAC has negligible influence. Increasing the output power is best accomplished by increasing I_{OUTFS}.

Output Stage Configuration

The AD9119/AD9129 are intended to serve high dynamic range applications that require wide signal reconstruction bandwidth (that is, a DOCSIS cable modem termination system (CMTS)) and/or high IF/RF signal generation. Optimum ac performance can be realized only if the DAC output is configured for differential (that is, balanced) operation with its output common-mode voltage biased to a stable, low noise 1.8 V nominal analog supply (VDDA). The ADP150 LDO can be used to generate a clean 1.8 V supply.

The output network used to interface to the DAC should provide a near 0 Ω dc bias path to VDDA. Any imbalance in the output impedance over frequency between the IOUTP and IOUTN pins degrades the distortion performance (mostly even order) and noise performance. Component selection and layout are critical in realizing the performance potential of the AD9119/AD9129.

Most applications that require balanced-to-unbalanced conversion from 10 MHz to 1 GHz can take advantage of the Mini-Circuits JTX series of transformers that offer impedance ratios of both 2:1 and 1:1.

Figure 152 shows the AD9119/AD9129 interfacing to the JTX-2-10T transformer. This transformer provides excellent amplitude/phase balance (that is, <1 dB/1°) up to 1 GHz while providing a 0 Ω D dc bias path to VDDA. If filtering of the DAC images and clock components is required, applying an analog LC filter on the single-ended side has the advantage of preserving the balance of the transformer.

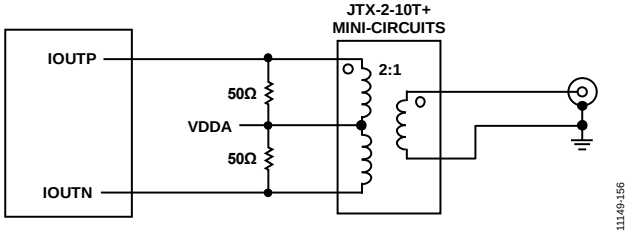

Figure 152. Recommended Transformer for Wideband Applications with Upper Bandwidths of up to 2.2 GHz

Figure 153 shows an interface that can be considered when interfacing the DAC output to a self-biased differential gain block. The inductors (L) shown serve as RF chokes that provide the dc bias path to AGND. Its value, along with the dc blocking capacitors, determines the lower cut-off frequency of the composite pass-band response. (The dc blocking capacitors form a high-pass response with the input resistance of the RF differential gain stage.)

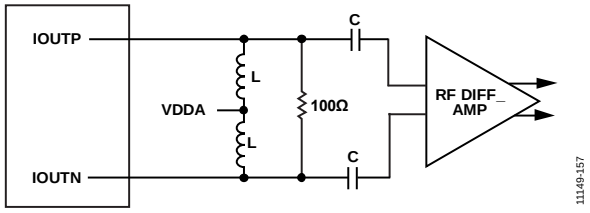

Figure 153. Interfacing the DAC Output to Self-Biased, Differential Gain Stage

Many RF differential amplifiers consist of two single-ended amplifiers with matched gain, thus providing no common-mode rejection while possibly degrading the balance, due to poor matching characteristics. Also, depending on the component tolerances, differential LC filters can further degrade the balance in a differential signal path. In both cases, the use of a balun could be advantageous in rejecting the common-mode distortion and noise components from the RF DAC prior to filtering or further amplification.

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For applications that operate the AD9119/AD9129 in Mix-Mode with output frequencies extending beyond 2.2 GHz, the user may want to consider the circuit shown in Figure 154. This circuit uses a wideband balun (for example, −3 dB at 4.0 GHz), with a configuration that is similar to the example shown in Figure 152, to provide a dc bias path for the DAC outputs. This circuit was implemented on an evaluation board, and the frequency response was measured to compare it with the ideal curve in Figure 146. The result is shown in Figure 155.

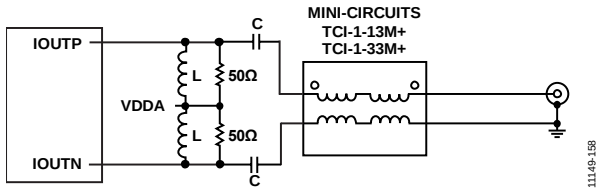

Figure 154. Recommended Mix-Mode Configuration Offering Extended RF Bandwidth Using TC1-1-13M+ Balun

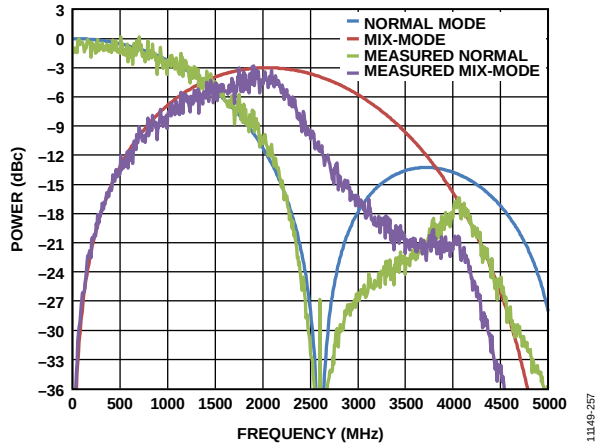

Figure 155. Measured vs. Ideal DAC Output Response; f_{DAC} = 2.6 GSPS

To assist in matching the AD9119/AD9129 output, a Smith chart is provided in Figure 156. The plot was taken using the circuit in Figure 154, with the balun and the coupling capacitors removed, and L = 270 nH. For the measured vs. ideal response of the DAC output, see Figure 155, which illustrates that a nonideal response occurs in the second half of the second Nyquist zone. This area corresponds to the low impedance area between 2 GHz and 3 GHz, as shown in the Smith chart in Figure 156. Output matching can be used to compensate for this nonideal response; the possible reduction in signal bandwidth must be considered if such matching is used.

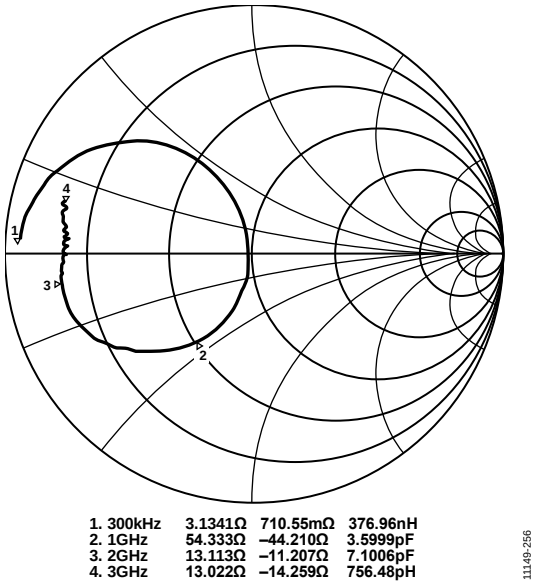

Figure 156. Measured Smith Chart Showing the DAC Output Impedance; f_{DAC} = 2.6 GSPS

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START-UP SEQUENCE

A small number of steps is required to program the AD9119/AD9129 to the proper operating state after the device is powered up. This sequence is listed in Table 16, along with an explanation of the purpose of each step.

Table 16. Start-Up Sequence After Power-Up

Register	Value	Description
0x00	0x00	4-wire SPI, MSB-first packing, short addressing mode
0x30	0x5C	Enable cross control, cross location = 7 dec, duty cycle correction off
0x0C	0x64	Set DLL minimum delay = 4 dec, enable DCO
0x0B	0x39	Set clock divider to DCI/512
0x01	0x68	Set bias power-down
0x34	0x6D or 0x5D	Set PLL mode for normal or 2× mode; normal mode or FIR25 on = 0x6D, FIR40 on = 0x5D
0x01	0x48	Enable bias
0x33	0x13	Initialize PLL to phase step = 1 dec
0x33	0xF8 or 0xD8	Select PFD, set PLL phase step, keep PLL lost bit cleared; phase step is as follows: normal mode or FIR25 on = 0xF8, FIR40 on = 0xD8
0x33	0xF0 or 0xD0	Deassert the PLL lost bit, keeping the phase step; normal mode or FIR25 on = 0xF0, FIR40 on = 0xD0
0x0D	0x06	Set duty correction bandwidth to lowest
0x0A	0xC0	Enable DLL
0x18	0xm0	Select data mode, filter mode to set value of m; for example: 0x40, unsigned data, interpolator off
0x20	0xC6	Set full-scale current (FSC) to 33 mA
0x21	0x03	Complete the setting of FSC
0x30	0x46	Enable cross control, cross location = 1 dec, enable duty cycle correction
0x12	0x20	Set the FIFO pointers
0x11	0x81	Assert FIFO reset
0x11	0x01	Deassert FIFO reset
0x01	0x08	Enable I_{REF} (DAC output)

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DEVICE CONFIGURATION REGISTERS

DEVICE CONFIGURATION REGISTER MAP

The blank bits in Table 17 are reserved and should be programmed to their default values. A setting of 1 or 0 indicates the required programming for the bit.

Table 17. Device Configuration Register Map

	Address											
Register Name	**Hex**	**Dec**	**Type**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Default**
Mode	0x00	0	R/W	SDIO_DIR	LSB/MSB	SoftReset	0	0	SoftReset	LSB/MSB	SDIO_DIR	0x81
Power-Down	0x01	1	R/W	BG_PD	IREF_PD	BIAS_PD		1	CLKPATH_PD	Retimer_PD	DLL_PD	0x48
IRQ Enable 0	0x03	3	R/W	FIFO_Warn2	FIFO_Warn1	SPIFrmAck		DLL warn	DLL lock	Retimer lost	Retimer lock	0x00
IRQ Enable 1	0x04	4	R/W		AED pass	AED fail	SED fail	Parity err fall	Parity err rise			0x00
IRQ Request 0	0x05	5	R/W	FIFO_Warn2	FIFO_Warn1	SPIFrmAck		DLL warn	DLL lock	Retimer lost	Retimer lock	0x00
IRQ Request 1	0x06	6	R/W		AED pass	AED fail	SED fail	Parity err fall	Parity err rise			0x00
Frame Pin Usage	0x07	7	R/W			ParUsage	FrmUsage			FRM_x pin usage mode, Bits[1:0]		0x00
Reserved_0	0x08	8	R/W	Must maintain default (reset) value of 0x58								0x58
Data Ctrl 0	0x0A	10	R/W	DLL enable	Duty cycle correction enable			Phase offset, Bits[3:0]				0x40
Data Ctrl 1	0x0B	11	R/W	Warn clear	Lock delay divider	Controller clock divider, Bits[1:0]		Delay line middle set, Bits[3:0]				0x29
Data Ctrl 2	0x0C	12	R/W		DCO enable	Maximum delay set, Bits[2:0]			Minimum delay set, Bits[2:0]			0x23
Data Ctrl 3	0x0D	13	R/W						Duty correction BW, Bits[1:0]			0x04
Data Status 0	0x0E	14	R	DLL lock	DLL warn	DLL delay line start warning	DLL delay line end warning	DLL correct phase	DCI on	DLL lock phase	DLL running	N/A
FIFO Ctrl	0x11	17	R/W	SPIFrmReq	SPIFrmAck	Enable pin framing					Phase report enable	0x00
FIFO Offset	0x12	18	R/W		RdPtrOff, Bits[2:0]				WtPtrOff, Bits[2:0]			0x04
FIFO Ph0 Thrm	0x13	19	R		Phz0Thrm, Bits[6:0]							N/A
FIFO Ph1 Thrm	0x14	20	R		Phz1Thrm, Bits[6:0]							N/A
FIFO Ph2 Thrm	0x15	21	R		Phz2Thrm, Bits[6:0]							N/A
FIFO Ph3 Thrm	0x16	22	R		Phz3Thrm, Bits[6:0]							N/A
Data Mode Ctrl	0x18	24	R/W	Filter enable	Binary select	FILT_SEL						0x00
Decode Ctrl	0x19	25	R/W								Mix-Mode en	0x00
Sync	0x1A	26	R/W	Inc latency	Dec latency		Sync enable	Sync done	Phase readback, Bits[2:0]			0x00
FSC_1	0x20	32	R/W	Full-scale current, Bits[7:0]								0x00
FSC_2	0x21	33	R/W							Full-scale current, Bits[9:8]		0x02
ANA_CNT1	0x22	34	R/W									0x00
ANA_CNT2	0x23	35	R/W									0x0C
CLK REG1	0x30	48	R/W	0	Cross enable	Cross location, Bits[3:0]				Duty enable	0	0x00
Retimer Ctrl 0	0x33	51	R/W	Phase step, Bits[3:0]				Clear lost	PLL divider	Retimer mode, Bits[1:0]		0x30
Retimer Ctrl 1	0x34	52	R/W					PLL reset_Z				0x55
Retimer Stat 0	0x35	53	R	PLL lock	PLL lost							N/A
SED Control	0x50	80	R/W	SED enable	SED error clear	AED enable	0	0	AED pass	AED fail	SED fail	0x00
SED Patt/Err R0L	0x51	81	R/W	SED Data Port 0 rising edge low part error, Bits[7:0]								N/A
SED Patt/Err R0H	0x52	82	R/W			SED Data Port 0 rising edge high part error, Bits[13:8]						N/A
SED Patt/Err R1L	0x53	83	R/W	SED Data Port 1 rising edge low part error, Bits[7:0]								N/A
SED Patt/Err R1H	0x54	84	R/W			SED Data Port 1 rising edge high part error, Bits[13:8]						N/A
SED Patt/Err F0L	0x55	85	R/W	SED Data Port 0 falling edge low part error, Bits[7:0]								N/A
SED Patt/Err F0H	0x56	86	R/W			SED Data Port 0 falling edge high part error, Bits[13:8]						N/A
SED Patt/Err F1L	0x57	87	R/W	SED Data Port 1 falling edge low part error, Bits[7:0]								N/A
SED Patt/Err F1H	0x58	88	R/W			SED Data Port 1 falling edge high part error, Bits[13:8]						N/A
Parity Control	0x5C	92	R/W	Parity enable	Parity even	Parity error clear				Parity error falling edge	Parity error rising edge	0x00
Parity Err Rising	0x5D	93	R	Parity rising edge error count, Bits[7:0]								N/A
Parity Err Falling	0x5E	94	R	Parity falling edge error count, Bits[7:0]								N/A
Delay Ctrl 0	0x70	112	R/W	Enable delay cell, Bits[7:0]								0xFF
Delay Ctrl 1	0x71	113	R/W						Enable delay cell, Bits[10:8]			0x67
Drive Strength	0x7C	124	R/W	DCO drive strength, Bits[1:0]								0x7C
Part ID	0x7F	127	R	Part ID, Bits[7:0]								0x07 or 0x87

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DEVICE CONFIGURATION REGISTER DESCRIPTIONS

SPI Communications Control Register

Address: 0x00, Reset: 0x81, Name: Mode

Table 18. Bit Descriptions for Mode

Bits	Bit Name	Description	Reset	Access
7	SDIO_DIR	Selects 3-wire or 4-wire mode 1: 3-wire bidirectional 0: 4-wire unidirectional	1	R/W
6	LSB/MSB	LSB/MSB data packing 1: LSB-first packing 0: MSB-first packing	0	R/W
5	SoftReset	1: performs a software-based reset	0	R/W
4	Reserved	Must be set to 0; reserved (short addressing mode)	0	R/W
3	Reserved	Mirror Bit 4 for safety	0	R
2	SoftReset	Mirror Bit 5 for safety	0	R
1	LSB/MSB	Mirror Bit 6 for safety	0	R
0	SDIO_DIR	Mirror Bit 7 for safety	1	R

Power Control Register

Address: 0x01, Reset: 0x48, Name: Power-Down

Table 19. Bit Descriptions for Power-Down

Bits	Bit Name	Description	Reset	Access
7	BG_PD	Band gap power-down 1: band gap is powered down 0: band gap is active	0	R/W
6	IREF_PD	I_{REF} power-down 1: FSC is 0 mA 0: FSC is as programmed	1	R/W
5	BIAS_PD	Bias power-down 1: all bias currents are off 0: all bias currents are on	0	R/W
4	Reserved	Reserved	0	R/W
3	Reserved	Must be set to 1; reserved	1	R/W
2	CLKPATH_PD	Clock path power-down 1: DAC clock is powered down 0: DAC clock is active	0	R/W
1	Retimer_PD	1: PLL is powered down	0	R/W
0	DLL_PD	DLL (data receiver) power-down 1: DLL (data receiver) is powered down	0	R/W

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Interrupt Enable Register 0

Address: 0x03, Reset: 0x00, Name: IRQ Enable 0

Table 20. Bit Descriptions for IRQ Enable 0

Bits	Bit Name	Description	Reset	Access
7	FIFO_Warn2 interrupt enable	Enables the FIFO warning within two slots of overwrite interrupt	0	R/W
6	FIFO_Warn1 interrupt enable	Enables the FIFO warning within one slot of overwrite interrupt	0	R/W
5	SPIFrmAck interrupt enable	Enables the FIFO SPI-based calibration acknowledgement of SPIFrmReq (Address 0x11, Bit 7) going from 0b to1b	0	R/W
4	Reserved	Reserved	0	R
3	DLL warn interrupt enable	Enables the DLL warning flag that the data receiver is no longer locked	0	R/W
2	DLL lock interrupt enable	Enables the DLL warning flag that the data receiver is now locked	0	R/W
1	Retimer lost interrupt enable	Enables the retimer lost interrupt indication	0	R/W
0	Retimer lock interrupt enable	Enables the retimer lock interrupt indication	0	R/W

Interrupt Enable Register 1

Address: 0x04, Reset: 0x00, Name: IRQ Enable 1

Table 21. Bit Descriptions for IRQ Enable 1

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R/W
6	AED pass interrupt enable	Enables the AED pass interrupt reporting saying that eight valid samples captured	0	R/W
5	AED fail interrupt enable	Enables the AED fail interrupt reporting that a miscompare occurred	0	R/W
4	SED fail interrupt enable	Enables the SED fail interrupt reporting that a miscompare occurred	0	R/W
3	Parity error falling edge enable	Enables the parity fail due to a falling edge-based parity detected error	0	R/W
2	Parity error rising edge enable	Enables the parity fail due to a rising edge-based parity detected error	0	R/W
1	Reserved	Reserved	0	R
0	Reserved	Reserved	0	R

Interrupt Status Register 0

Address: 0x05, Reset: 0x00, Name: IRQ Request 0

Table 22. Bit Descriptions for IRQ Request 0

Bits	Bit Name	Description	Reset	Access
7	FIFO_Warn2 interrupt status	Indicates that the FIFO is within two slots of overwrite	0	R
6	FIFO_Warn1 interrupt status	Indicates that the FIFO is within one slot of overwrite	0	R
5	SPIFrmAck interrupt status	Indicates acknowledgement of SPIFrmReq has changed from 0b to1b	0	R
4	Reserved	Reserved	0	R
3	DLL warn interrupt status	Indicates that the DLL (data receiver) is close to coming unlocked and action is needed	0	R
2	DLL lock interrupt status	Indicates that the DLL (data receiver) is now locked	0	R
1	Retimer lost interrupt status	Indicates that the retimer PLL is no longer locked	0	R
0	Retimer lock interrupt status	Indicates that the retimer PLL is now locked	0	R

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Interrupt Status Register1

Address: 0x06, Reset: 0x00, Name: IRQ Request 1

Table 23. Bit Descriptions for IRQ Request 1

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R/W
6	AED pass interrupt status	Indicates that the AED logic has captured eight valid samples	0	R/W
5	AED fail interrupt status	Indicates that the AED logic has detected a miscompare	0	R/W
4	SED fail interrupt status	Indicates that the SED logic has detected a miscompare	0	R/W
3	Parity error falling edge status	Indicates a parity fault due to data captured on the falling edge	0	R/W
2	Parity error rising edge status	Indicates a parity fault due to data captured on the rising edge	0	R/W
1	Reserved	Reserved	0	R/W
0	Reserved	Reserved	0	R/W

Frame Pin Usage Register

Address: 0x07, Reset: 0x00, Name: Frame Pin Usage

Table 24. Bit Descriptions for Frame Pin Usage

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R/W
6	Reserved	Reserved	0	R/W
5	ParUsage	1: FRM_x pin is in parity mode, and parity is enabled Note that parity must be enabled, and the type must be chosen in Register 0x5C[7:6]	0	R
4	FrmUsage	1: FRM_x pin is in frame mode and enable pin framing (Register 0x11[5] = 1b) is enabled	0	R
3	Reserved	Reserved	0	R
2	Reserved	Reserved	0	R
[1:0]	FRM_x pin usage mode	3: reserved 2: frame 1: parity 0: no effect	0x0	R/W

Reserved_0 Register

Address: 0x08, Reset: 0x58, Name: Reserved_0

Table 25. Bit Descriptions for Reserved_0

Bits	Bit Name	Description	Reset	Access
[7:0]	Reserved	Must keep default (reset) value; reserved	0x58	R

Data Receiver Control 0 Register

Address: 0x0A, Reset: 0x40, Name: Data Ctrl 0

Table 26. Bit Descriptions for Data Ctrl 0

Bits	Bit Name	Description	Reset	Access
7	DLL enable	1: enables DLL 0: disables DLL	0	R/W
6	Duty cycle correction enable	1: enables duty cycle correction 0: disables duty cycle correction	1	R/W
5	Reserved	Reserved	0	R/W
4	Reserved	Reserved	0	R/W
[3:0]	Phase offset	Locked phase = 90° ± n × 11.25°, where n is the 4-bit signed magnitude number	0x0	R/W

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Data Receiver Control 1 Register

Address: 0x0B, Reset: 0x29, Name: Data Ctrl 1

Table 27. Bit Descriptions for Data Ctrl 1

Bits	Bit Name	Description	Reset	Access
7	Warn clear	1: clears data receiver warning bit	0	R/W
6	Lock delay divider	1: long delay 0: short delay	0	R/W
[5:4]	Controller clock divider	Controller clock divider 00: DCI/4 01: DCI/16 10: DCI/64 11: DCI/512	0x2	R/W
[3:0]	Delay line middle set	Sets nominal delay line delay	0x9	R/W

Data Receiver Control 2 Register

Address: 0x0C, Reset: 0x23, Name: Data Ctrl 2

Table 28. Bit Descriptions for Data Ctrl 2

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R/W
6	DCO enable	1: enables DCO output driver	0	R/W
[5:3]	Maximum delay set	Sets maximum delay line delay (larger number = longer delay line)	0x2	R/W
[2:0]	Minimum delay set	Sets minimum delay line delay (larger number = smaller delay line)	0x3	R/W

Data Receiver Control 3 Register

Address: 0x0D, Reset: 0x04, Name: Data Ctrl 3

Table 29. Bit Descriptions for Data Ctrl 3

Bits	Bit Name	Description	Reset	Access
[7:3]	Reserved	Reserved.	0x00	R
[2:1]	Duty correction BW set	Sets the bandwidth of the duty cycle correction circuit. 00: highest BW. 01: higher BW. 10: lower BW. 11: lowest BW.	0x2	R/W
0	Reserved	Reserved	0	R/W

Data Receiver Status 0 Register

Address: 0x0E, Reset: 0x00, Name: Data Status 0

Table 30. Bit Descriptions for Data Status 0

Bits	Bit Name	Description	Reset	Access
7	DLL lock	1: DLL lock	0	R
6	DLL warning	1: DLL near beginning/end of delay line	0	R
5	DLL delay line start warning	1: DLL at beginning of delay line	0	R
4	DLL delay line end warning	1: DLL at end of delay line	0	R
3	DLL correct phase	1: data is sampled on correct phase 0: data is sampled on incorrect phase.	0	R
2	DCI on	1: user has provided a clock > 100 MHz	0	R
1	DLL lock phase	1: DLL is locked on negative half of DCI. 0: DLL is locked on positive half of DCI	0	R
0	DLL running	1: closed loop DLL attempting to lock 0: delay fixed at middle of delay line	0	R

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FIFO Control Register

Address: 0x11, Reset: 0x00, Name: FIFO Ctrl

Table 31. Bit Descriptions for FIFO Ctrl

Bits	Bit Name	Description	Reset	Access
7	SPIFrmReq	Requests a SPI-based FIFO alignment (FIFO reset)	0	R/W
6	SPIFrmAck	Acknowledges SPIFrmReq change (tracks SPIFrmReq setting)	0	R/W
5	Enable pin framing	1: enables hardware pin-based FIFO framing	0	R/W
[4:1]	Reserved	Reserved	0x0	R
0	Phase report enable	1: enables FIFO phase reporting	0	R/W

FIFO Offset Register

Address: 0x12, Reset: 0x04, Name: FIFO Offset

Table 32. Bit Descriptions for FIFO Offset

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R
[6:4]	RdPtrOff[2:0]	FIFO read pointer offset	0x0	R/W
3	Reserved	Reserved	0	R
[2:0]	WtPtrOff[2:0]	FIFO write pointer offset	0x4	R/W

FIFO Thermometer for Phase 0 Status Register

Address: 0x13, Reset: 0x00, Name: FIFO PH0 THRM

Table 33. Bit Descriptions for FIFO PH0 THRM

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R
[6:0]	Phz0Thrm	Phase 0-based FIFO thermometer status. Phase 0 relative FIFO phasing, as 0000000b to 1111111b, where 0000011b is considered the middle of the FIFO storage space.	0x00	R

FIFO Thermometer for Phase 1 Status Register

Address: 0x14, Reset: 0x00, Name: FIFO PH1 THRM

Table 34. Bit Descriptions for FIFO PH1 THRM

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R
[6:0]	Phz1Thrm	Phase 1-based FIFO thermometer status. Phase 1 relative FIFO phasing, as 0000000b to 1111111b, where 0000011b is considered the middle of the FIFO storage space.	0x00	R

FIFO Thermometer for Phase 2 Status Register

Address: 0x15, Reset: 0x00, Name: FIFO PH2 THRM

Table 35. Bit Descriptions for FIFO PH2 THRM

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R
[6:0]	Phz2Thrm	Phase 2-based FIFO thermometer status. Phase 2 relative FIFO phasing, as 0000000b to 1111111b, where 0000011b is considered the middle of the FIFO storage space.	0x00	R

FIFO Thermometer for Phase 3 Status Register

Address: 0x16, Reset: 0x00, Name: FIFO PH3 THRM

Table 36. Bit Descriptions for FIFO PH3 THRM

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R
[6:0]	Phz3Thrm	Phase 3-based FIFO thermometer status. Phase 3 relative FIFO phasing, as 0000000b to 1111111b, where 0000011b is considered the middle of the FIFO storage space.	0x00	R

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Data Mode Control Register

Address: 0x18, Reset: 0x00, Name: Data Mode Ctrl

Table 37. Bit Descriptions for Data Mode Ctrl

Bits	Bit Name	Description	Reset	Access
7	Filter enable	1: enables 2× interpolation filter 0: bypasses 2× interpolation filter	0	R/W
6	Binary select	Selects input data format 1: unsigned 0: signed (Twos complement)	0	R/W
5	FILT_SEL	2× interpolator filter select 1: 40 dB OOB rejection 0: 25 dB out-of-band (OOB) rejection	0	R/W
[4:0]	Reserved	Reserved	0	R

Decoder Control (Program Thermometer Type) Register

Address: 0x19, Reset: 0x00, Name: Decode Ctrl

Table 38. Bit Descriptions for Decode Ctrl

Bits	Bit Name	Description	Reset	Access
[7:1]	Reserved	Reserved	0x00	R
0	Mix-Mode enable	1: Mix-Mode 0: normal	0	R/W

Sync Control Register

Address: 0x1A, Reset: 0x00, Name: Sync

Table 39. Bit Descriptions for Sync

Bits	Bit Name	Description	Reset	Access
7	Inc latency	Increment delay by 1	0	R/W
6	Dec latency	Decrement delay by 1	0	R/W
5	Reserved	Reserved	0	R
4	Sync enable	1: multi-DAC sync output pin enabled 0: multi-DAC sync output pin disabled	0	R/W
3	Sync done	1: last increment or decrement request is complete	0	R
[2:0]	Phase readback	Readback of existing SYNC phase delay value	0	R

Full-Scale Current Adjust (Lower) Register

Address: 0x20, Reset: 0x00, Name: FSC_1

Table 40. Bit Descriptions for FSC_1

Bits	Bit Name	Description	Reset	Access
[7:0]	Full-scale current, Bits[7:0]	DAC gain adjust; DAC full-scale current (LSB)	0x00	R/W

Full-Scale Current Adjust (Upper) Register

Address: 0x21 Reset: 0x02, Name: FSC_2

Table 41. Bit Descriptions for FSC_2

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved	0	R/W
[6:2]	Reserved	Reserved	0	R
[1:0]	Full-scale current, Bits[9:8]	DAC gain adjust; DAC full-scale current (MSB)	0x02	R/W

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Analog Control 1 Register

Address: 0x22, Reset: 0x00, Name: ANA_CNT1

Table 42. Bit Descriptions for ANA_CNT1

Bits	Bit Name	Description	Reset	Access
[7:0]	Reserved	Reserved	0x0	R/W

Analog Control 2 Register

Address: 0x23, Reset: 0x0C, Name: ANA_CNT2

Table 43. Bit Descriptions for ANA_CNT2

Bits	Bit Name	Description	Reset	Access
[7:0]	Reserved	Reserved	0x0C	R/W

Clock Control 1 Register

Address: 0x30, Reset: 0x00, Name: CLK REG1

Table 44. Bit Descriptions for CLK REG1

Bits	Bit Name	Description	Reset	Access
7	Reserved	Must be set to 0; reserved	0	R/W
6	Cross enable	Enables zero-crossing control	0	R/W
[5:2]	Cross location	Adjusts zero-crossing control location (signed magnitude)	0	R/W
1	Duty enable	Enables duty cycle correction	0	R/W
0	Select internal	Must be set to 0	0	R/W

Retimer Control 0 Register

Address: 0x33, Reset: 0x30, Name: Retimer Ctrl 0

Table 45. Bit Descriptions for Retime Ctrl 0

Bits	Bit Name	Description	Reset	Access
[7:4]	Phase step	4-bit signed magnitude; PFD phase step = n × 30°	0x3	R/W
3	Clear lost	Clear lost status bit	0	
2	PLL divider	1: divide-by-4 0: divide-by-8	0	
[1:0]	Retimer mode	0: enable PFD, normal mode 1: reserved 2: reserved 3: reserved	0x0	

Retimer Control 1 Register

Address: 0x34, Reset: 0x55, Name: Retimer Ctrl 1

Table 46. Bit Descriptions for Retimer Ctrl 1

Bits	Bit Name	Description	Reset	Access
[7:4]	Reserved	Reserved	0x5	R/W
3	PLL reset_Z	1: normal operation for DAC clock PLL 0: resets the DAC clock PLL	0	R/W
[2:0]	Reserved	Reserved	0x5	R/W

Retimer Status 0 Register

Address: 0x35, Reset: 0x00, Name: Retimer Stat 0

Table 47. Bit Descriptions for Retimer Stat 0

Bits	Bit Name	Description	Reset	Access
7	PLL lock	1: retimer PLL locked	0	R
6	PLL lost	1: retimer PLL lost (can be sticky)	0	R
[5:4]	Reserved	Reserved	0x0	R
[3:0]	Reserved	Reserved	0x0	R

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Sample Error Detection (SED) Control Register

Address: 0x50, Reset: 0x00, Name: SED Control

Table 48. Bit Descriptions for SED Control

Bits	Bit Name	Description	Reset	Access
7	SED enable	1: setting this bit to 1 enables the SED compare logic	0	R/W
6	SED error clear	1: clears all SED reported error bits below	0	R/W
5	AED enable	1: enables the AED function (SED with autoclear after eight passing sets)	0	R/W
4	Reserved	Must be set to 0; reserved	0	R
3	Reserved	Must be set to 0; reserved	0	R
2	AED pass	1: signals eight true compare cycles	0	R/W
1	AED fail	1: signals a miscompare	0	R
0	SED fail	1: signals an SED miscompare (with SED or AED enabled)	0	R

Sample Error Detection (SED) Data Port 0 Rising Edge Status Low Register

Address: 0x51, Reset: 0x00, Name: SED Patt/Err R0L

Table 49. Bit Descriptions for SED Patt/Err R0L

Bits	Bit Name	Description	Reset	Access
[7:0]	SED Data Port 0 rising edge low part error bits	SED Data Port 0 rising edge error, Bits[7:0]	0x00	R/W

Sample Error Detection (SED) Data Port 0 Rising Edge Status High Register

Address: 0x52, Reset: 0x000, Name: SED Patt/Err R0H

Table 50. Bit Descriptions for SED Patt/Err R0H

Bits	Bit Name	Description	Reset	Access
[7:6]	Reserved	Reserved	0x0	R
[5:0]	SED Data Port 0 rising edge high part error bits	SED Data Port 0 rising edge error, Bits[13:8]	0x00	R/W

Sample Error Detection (SED) Data Port 1 Rising Edge Status Low Register

Address: 0x53, Reset: 0x00, Name: SED Patt/Err R1L

Table 51. Bit Descriptions for SED Patt/Err R1L

Bits	Bit Name	Description	Reset	Access
[7:0]	SED Data Port 1 rising edge low part error bits	SED Data Port 1 rising edge error, Bits[7:0]	0x00	R/W

Sample Error Detection (SED) Data Port 1 Rising Edge Status High Register

Address: 0x54, Reset: 0x00, Name: SED Patt/Err R1H

Table 52. Bit Descriptions for SED Patt/Err R1H

Bits	Bit Name	Description	Reset	Access
[7:6]	Reserved	Reserved	0x0	R
[5:0]	SED Data Port 1 rising edge high part error bits	SED Data Port 1 rising edge error, Bits[13:8]	0x00	R/W

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Sample Error Detection (SED) Data Port 0 Falling Edge Status Low Register

Address: 0x55, Reset: 0x00, Name: SED Patt/Err F0L

Table 53. Bit Descriptions for SED Patt/Err F0L

Bits	Bit Name	Description	Reset	Access
[7:0]	SED Data Port 0 falling edge low part error bits	SED Data Port 0 falling edge error, Bits[7:0]	0x00	R/W

Sample Error Detection (SED) Data Port 0 Falling Edge Status High Register

Address: 0x56, Reset: 0x000, Name: SED Patt/Err F0H

Table 54. Bit Descriptions for SED Patt/Err F0H

Bits	Bit Name	Description	Reset	Access
[7:6]	Reserved	Reserved	0x0	R
[5:0]	SED Data Port 0 falling edge high part error bits	SED Data Port 0 falling edge error, Bits[13:8]	0x00	R/W

Sample Error Detection (SED) Data Port 1 Falling Edge Status Low Register

Address: 0x57, Reset: 0x00, Name: SED Patt/Err F1L

Table 55. Bit Descriptions for SED Patt/Err F1L

Bits	Bit Name	Description	Reset	Access
[7:0]	SED Data Port 1 falling edge low part error bits	SED Data Port 1 falling edge error, Bits[7:0]	0x00	R/W

Sample Error Detection (SED) Data Port 1 Falling Edge Status High Register

Address: 0x58, Reset: 0x00, Name: SED Patt/Err F1H

Table 56. Bit Descriptions for SED Patt/Err F1H

Bits	Bit Name	Description	Reset	Access
[7:6]	Reserved	Reserved	0x0	R
[5:0]	SED Data Port 1 falling edge high part error bits	SED Data Port 1 falling edge error, Bits[13:8]	0x00	R/W

Parity Control Register

Address: 0x5C, Reset: 0x00, Name: Parity Control

Table 57. Bit Descriptions for Parity Control

Bits	Bit Name	Description	Reset	Access
7	Parity enable	1: enables parity	0x00	R/W
6	Parity even	1: even parity. Even parity is defined as XOR[FRM(n), P0_D0(n), P0_D1(n), P0_D2(n), ..., P0_D13(n), P1_D0(n), P1_D1(n), P1_D2(n), …, P1_D13(n)] = 0. 0: odd parity. Odd parity is defined as XOR[FRM(n), P0_D0(n), P0_D1(n), P0_D2(n), ..., P0_D13(n), P1_D0(n), P1_D1(n), P1_D2(n), …, P1_D13(n)] = 1 Note that the parity bit must be enabled in Register 0x07.	0	R/W
5	Parity error clear	1: clears parity error counters	0	R/W
[4:2]	Reserved	Reserved	0x0	R
1	Parity error falling edge	1: signals detection of a falling edge parity error	0	R
0	Parity error rising edge	1: signals detection of a rising edge parity error	0	R

Parity Rising Edge Count Register

Address: 0x5D, Reset: 0x00, Name: Parity Err Rising

Table 58. Bit Descriptions for Parity Err Rising

Bits	Bit Name	Description	Reset	Access
[7:0]	Parity rising edge error count	Number of rising edge-based errors detected, clipped to 256	0x00	R

Parity Falling Edge Count Register

Address: 0x5E, Reset: 0x00, Name: Parity Err Falling

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Table 59. Bit Descriptions for Parity Err Falling

Bits	Bit Name	Description	Reset	Access
[7:0]	Parity falling edge error count	Number of falling edge-based errors detected, clipped to 256	0x00	R

Delay Control Register 0

Address: 0x70, Reset: 0xFF, Name: Delay Ctrl 0

Table 60. Bit Descriptions for Delay Ctrl 0

Bits	Bit Name	Description	Reset	Access
[7:0]	Enable delay cell	Sets each bit to enable or disable the delay cell, Bits[7:0]; delay cell number corresponds to bit number 1: enables delay cell (default) 0: disables delay cell	0xFF	R/W

Delay Control Register 1

Address: 0x71, Reset: 0x67, Name: Delay Ctrl 1

Table 61. Bit Descriptions for Delay Ctrl 1

Bits	Bit Name	Description	Reset	Access
[7:3]	Reserved	Reserved	0x60	R/W
[2:0]	Enable delay cell	Sets each bit to enable or disable the delay cell, Bits[10:8]; delay cell numbers are 10, 9, and 8, which correspond to Bit 2, Bit 1, and Bit 0, respectively 1: enables delay cell (default) 0: disables delay cell	0x7	R/W

Drive Strength Register

Address: 0x7C, Reset: 0x7C, Name: Drive Strength

Table 62. Bit Descriptions for Drive Strength

Bits	Bit Name	Description	Reset	Access
[7:6]	DCO drive strength	Sets DCO drive strength 00: 2 mA 01: 2.8 mA (default) 10: 3.4 mA 11: 4 mA	0x1	R/W
[5:0]	Reserved	Reserved	0x3C	R/W

Part ID Register

Address: 0x7F, Reset: 0x03 or 0x83, Name: Part ID

Table 63. Bit Descriptions for Part ID

Bits	Bit Name	Description	Reset	Access
[7:0]	Part ID	Version information 0x07 = the AD9129 (14-bit version) 0x87 = the AD9119 (11-bit version)	0x07 or 0x87	R

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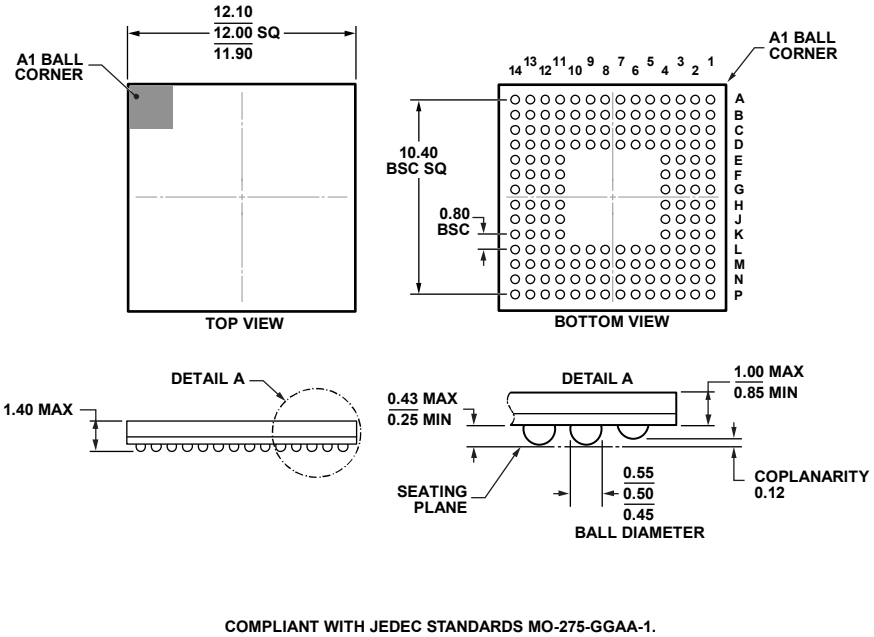
OUTLINE DIMENSIONS



COMPLIANT WITH JEDEC STANDARDS MO-275-GGAA-1.

Figure 157. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-160-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9119BBCZ	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9119BBCZRL	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9119-EBZ		Evaluation Board for Normal Mode Evaluation	
AD9119-MIX-EBZ		Evaluation Board for Mix-Mode Evaluation	
AD9119-CBLTX-EBZ		Evaluation Board for Cable Transmitter Evaluation	
AD9129BBCZ	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9129BBCZRL	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9129BBC	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9129BBCRL	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9129-EBZ		Evaluation Board for Normal Mode Evaluation	
AD9129-MIX-EBZ		Evaluation Board for Mix-Mode Evaluation	
AD9129-CBLTX-EBZ		Evaluation Board for Cable Transmitter Evaluation	

[1] Z = RoHS Compliant Part.

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