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REVISION HISTORY

6/12—Rev. A to Rev. B

Added Text to Absolute Maximum Ratings Section ... 6
Changes to Equation 8 ... 18

5/12—Revision A: Initial Version

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SPECIFICATIONS

5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} ≤ 0.2 V p-p	14.1	17		MHz
Full Power Response	V_{OUT} = 2 V p-p		4.8		MHz
Slew Rate	G = −1, V_{OUT} = 4 V step	25	30		V/µs
Settling Time					
To 0.1%	G = −1, V_{OUT} = 2 V step		240		ns
To 0.01%	G = −1, V_{OUT} = 2 V step		325		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	f = 10 kHz		14		nV/√Hz
Input Current Noise	f = 1 kHz		1		fA/√Hz
Harmonic Distortion (SFDR)	V_{OUT} = 2 V p-p, f = 20 kHz, G = −1, R_F = R_G = 4 kΩ		−108		dBc
	V_{OUT} = 2 V p-p, f = 20 kHz, G = +1, R_L = 1 kΩ		−99		dBc
Crosstalk					
f = 1 kHz	R_L = 5 kΩ		−123		dB
f = 1 MHz	R_L = 5 kΩ		−77		dB
DC PERFORMANCE					
Initial Offset			0.12	0.7	mV
Maximum Offset over Temperature			0.2	1.3	mV
Offset Drift			1		µV/°C
Input Bias Current	V_{CM} = 0 V to 4 V		0.3	25	pA
At T_{MAX}	V_{CM} = 0 V to 4 V		10	25	pA
Input Offset Current			0.3	20	pA
At T_{MAX}			3.5		pA
Open-Loop Gain	V_{OUT} = 0.2 V to 4 V, R_L = 2 kΩ	40	175		V/mV
T_{MIN} to T_{MAX}		25			V/mV
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		−0.2 to +3	−0.2 to +3.8		V
Input Resistance			10^{13}		Ω
Input Capacitance	Differential Mode		0.6		pF
	Common Mode		1.3		pF
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3 V	60	73		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
I_L = ±100 µA			0.009 to 4.98		V
I_L = ±2 mA			0.026 to 4.96		V
I_L = ±10 mA			0.097 to 4.88		V
Linear Output Current	V_{OUT} = 0.5 V to 4.5 V		40		mA
Short-Circuit Current	Sourcing to 2.5 V		50		mA
	Sinking to 2.5 V		101		mA
Capacitive Load Drive	G = +1		500		pF
POWER SUPPLY					
Operating Range		3		36	V
Quiescent Current	T_{MIN} to T_{MAX}, total		5.1	5.7	mA
Power Supply Rejection Ratio	V_S = 5 V to 15 V, T_{MIN} to T_{MAX}	70	94		dB

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3.3 V OPERATION

T_A = 25°C, $+V_S$ = 3.3 V, R_L = 2 kΩ to 1.65 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} ≤ 0.2 V p-p, V_{CM} = 0.65 V	13.8	17.3		MHz
Full Power Response	V_{OUT} = 2 V p-p		3.7		MHz
Slew Rate	G = −1, V_{OUT} = 2 V step, V_{CM} = 0.65 V	18	23		V/µs
Settling Time					
To 0.1%	G = −1, V_{OUT} = 2 V step		350		ns
To 0.01%	G = −1, V_{OUT} = 2 V step		460		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	f = 10 kHz		14		nV/√Hz
Input Current Noise	f = 1 kHz		1		fA/√Hz
Harmonic Distortion (SFDR)	V_{OUT} = 2 V p-p, f = 20 kHz, G = −1, R_F = R_G = 4 kΩ		−108		dBc
	V_{OUT} = 2 V p-p, f = 20 kHz, G = +1, R_L = 100 Ω		−70		dBc
Crosstalk					
f = 1 kHz	R_L = 5 kΩ		−123		dB
f = 1 MHz	R_L = 5 kΩ		−77		dB
DC PERFORMANCE					
Initial Offset			0.14	1	mV
Maximum Offset over Temperature			0.3	1.8	mV
Offset Drift			1		µV/°C
Input Bias Current	V_{CM} = 0 V to 2 V		0.3	25	pA
At T_{MAX}	V_{CM} = 0 V to 2 V		10	25	pA
Input Offset Current			0.3	20	pA
At T_{MAX}			3.5		pA
Open-Loop Gain	V_{OUT} = 0.2 V to 2 V, R_L = 2 kΩ	16	63		V/mV
T_{MIN} to T_{MAX}		14			V/mV
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		−0.2 to +1	−0.2 to +1.8		V
Input Resistance			10^{13}		Ω
Input Capacitance	Differential Mode		0.6		pF
	Common Mode		1.3		pF
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1 V	54	71		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
I_L = ±100 µA			0.006 to 3.28		V
I_L = ±2 mA			0.04 to 3.26		V
I_L = ±10 mA			0.093 to 3.18		V
Linear Output Current	V_{OUT} = 0.5 V to 2.5 V		40		mA
Short-Circuit Current	Sourcing to 1.5 V		44		mA
	Sinking to 1.5 V		86		mA
Capacitive Load Drive	G = +1		500		pF
POWER SUPPLY					
Operating Range		3		36	V
Quiescent Current	T_{MIN} to T_{MAX}, total		5.0	5.7	mA
Power Supply Rejection Ratio	V_S = 3.3 V to 15 V, T_{MIN} to T_{MAX}	70	80		dB

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±15 V OPERATION

T_A = 25°C, V_S = ±15 V, R_L = 2 kΩ to 0 V, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} ≤ 0.2 V p-p	16.5	19		MHz
Full Power Response	V_{OUT} = 2 V p-p		5.6		MHz
Slew Rate	G = −1, V_{OUT} = 10 V step	31	35		V/µs
Settling Time					
To 0.1%	G = −1, V_{OUT} = 10 V step		380		ns
To 0.01%	G = −1, V_{OUT} = 10 V step		510		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	f = 10 kHz		13		nV/√Hz
Input Current Noise	f = 1 kHz		1		fA/√Hz
Harmonic Distortion (SFDR)	V_{OUT} = 10 V p-p, f = 20 kHz, G = −1, R_F = R_G = 4 kΩ		−101		dBc
	V_{OUT} = 10 V p-p, f = 20 kHz, G = +1, R_L = 600 Ω		−89		dBc
Crosstalk					
f = 1 kHz	R_L = 5 kΩ		−123		dB
f = 1 MHz	R_L = 5 kΩ		−77		dB
DC PERFORMANCE					
Initial Offset			0.8	3.5	mV
Maximum Offset over Temperature			1.0	5	mV
Offset Drift			1		µV/°C
Input Bias Current	V_{CM} = 0 V		1.3	25	pA
	V_{CM} = −10 V		3.5		pA
At T_{MAX}	V_{CM} = 0 V		55	95	pA
Input Offset Current			1.3	20	pA
At T_{MAX}			9.5		pA
Open-Loop Gain	V_{OUT} = +10 V to −10 V, R_L = 2 kΩ	100	450		V/mV
T_{MIN} to T_{MAX}		80			V/mV
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		−15.2 to +13	−15.2 to +13.8		V
Input Resistance			10^{13}		Ω
Input Capacitance	Differential Mode		0.6		pF
	Common Mode		1.3		pF
Common-Mode Rejection Ratio	V_{CM} = −15 V to +13 V	70	90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
I_L = ±100 µA			−14.9 to +14.96		V
I_L = ±2 mA			−14.97 to +14.96		V
I_L = ±10 mA			−14.91 to +14.89		V
Linear Output Current	V_{OUT} = −14.5 V to +14.5 V		44		mA
Short-Circuit Current	Sourcing to 0 V		78		mA
	Sinking to 0 V		124		mA
Capacitive Load Drive	G = +1		500		pF
POWER SUPPLY					
Operating Range		3		36	V
Quiescent Current	T_{MIN} to T_{MAX}, total		6.3	8.4	mA
Power Supply Rejection Ratio	V_S = 5 V to 15 V, T_{MIN} to T_{MAX}	70	94		dB

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ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Power Dissipation	See Figure 4
Input Voltage (Common Mode)	$\pm V_S \pm 0.7$ V
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	See Figure 4
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
ESD Ratings (Human Body Model)	4500 V
ESD Ratings (Charged Device Model)	1250 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Use the part with caution at the 30 V supply as excessive output current may overheat and damage the part.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

The specification is for the device in free air.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOIC_N	120	°C/W
8-Lead MSOP	133	°C/W

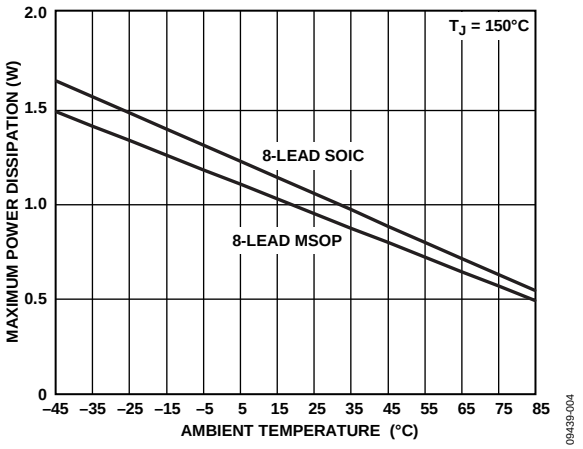

Figure 4. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

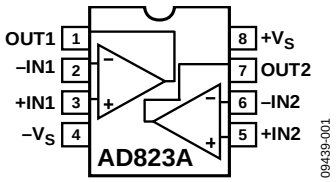

Figure 5. 8-Lead SOIC Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT1	Output 1.
2	–IN1	Inverting Input 1.
3	+IN1	Noninverting Input 1.
4	$-V_S$	Negative Supply.
5	+IN2	Noninverting Input 2.
6	–IN2	Inverting Input 2.
7	OUT2	Output 2.
8	$+V_S$	Positive Supply.

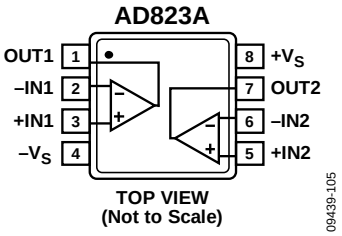

Figure 6. 8-Lead MSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT1	Output 1.
2	–IN1	Inverting Input 1.
3	+IN1	Noninverting Input 1.
4	$-V_S$	Negative Supply.
5	+IN2	Noninverting Input 2.
6	–IN2	Inverting Input 2.
7	OUT2	Output 2.
8	$+V_S$	Positive Supply.

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TYPICAL PERFORMANCE CHARACTERISTICS

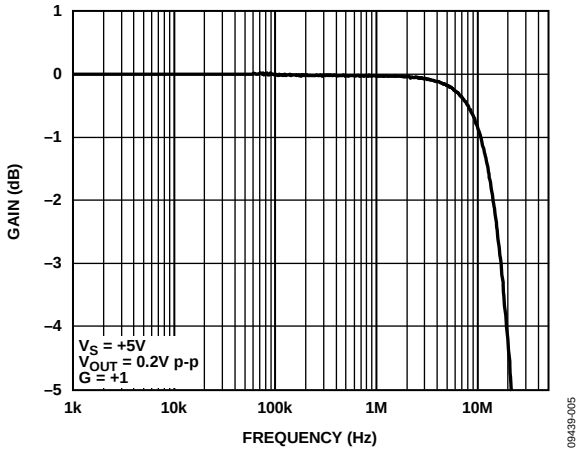

Figure 7. Small Signal Bandwidth, G = +1

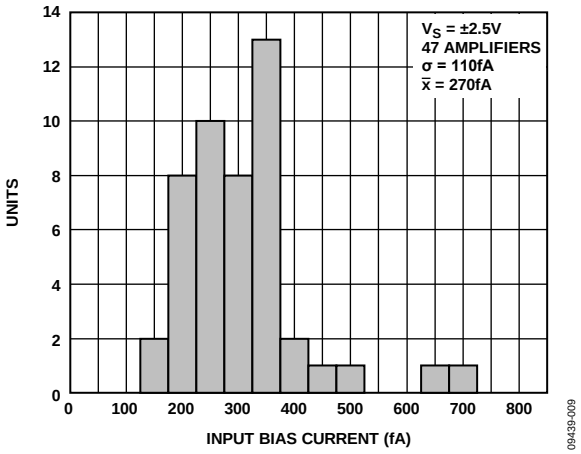

Figure 10. Typical Distribution of Input Bias Current

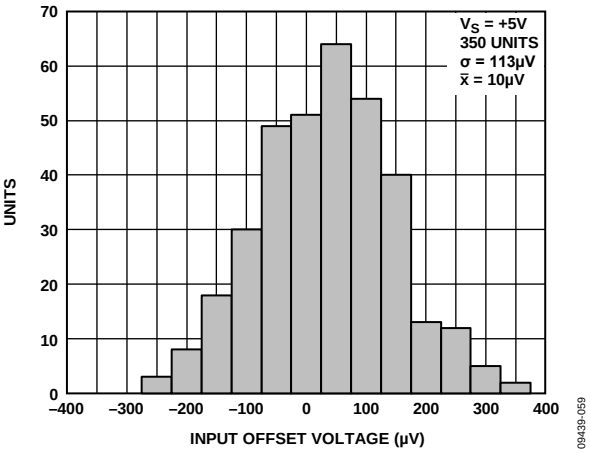

Figure 8. Typical Distribution of Input Offset Voltage

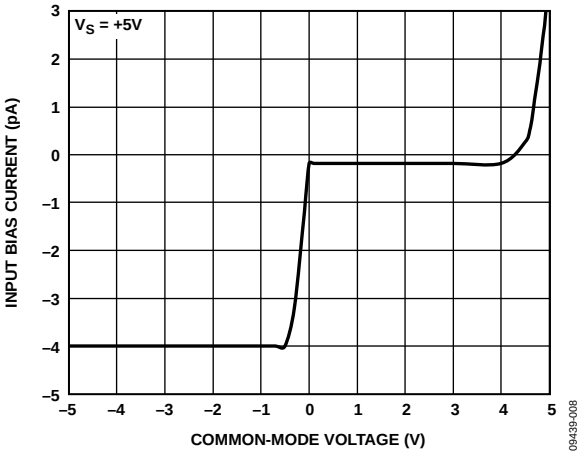

Figure 11. Input Bias Current vs. Common-Mode Voltage

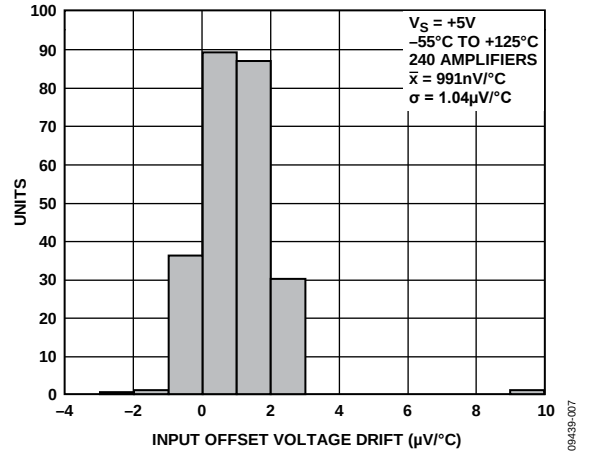

Figure 9. Typical Distribution of Input Offset Voltage Drift

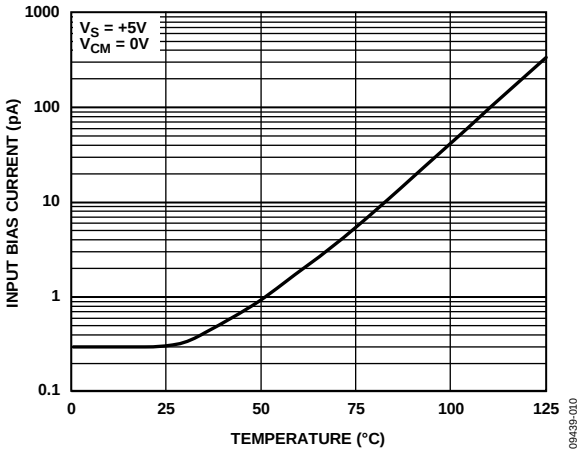

Figure 12. Input Bias Current vs. Temperature

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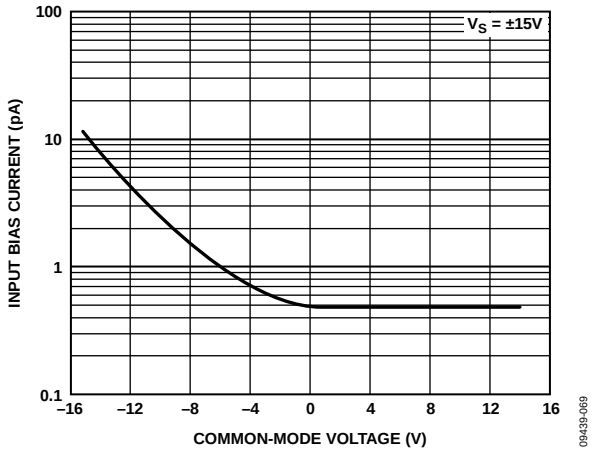

Figure 13. Input Bias Current vs. Common-Mode Voltage

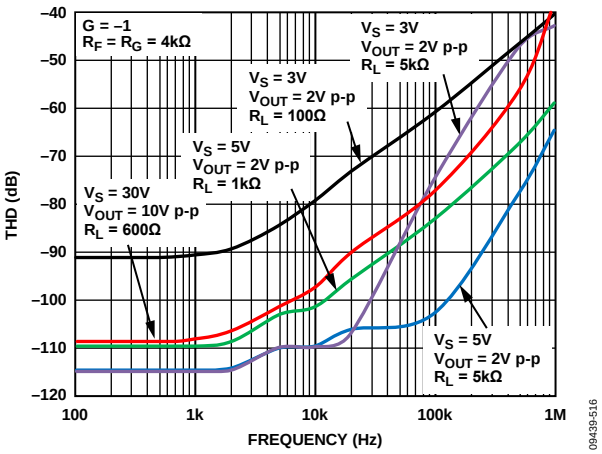

Figure16. Total Harmonic Distortion vs. Frequency

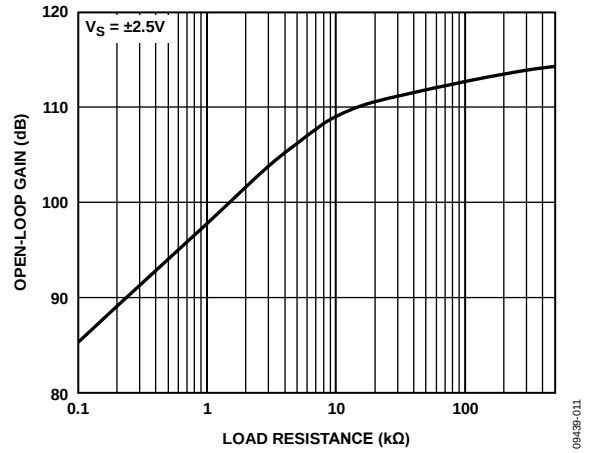

Figure 14. Open-Loop Gain vs. Load Resistance

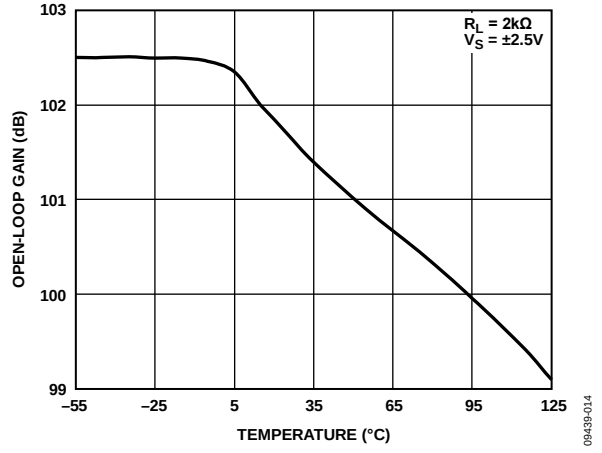

Figure 17. Open-Loop Gain vs. Temperature

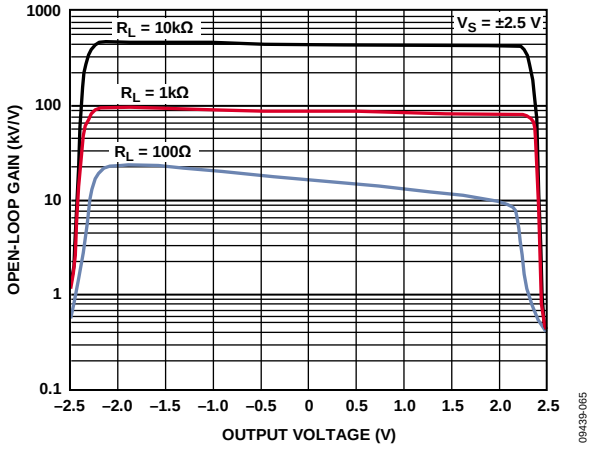

Figure 15. Open-Loop Gain vs. Output Voltage, V_S = ±2.5 V

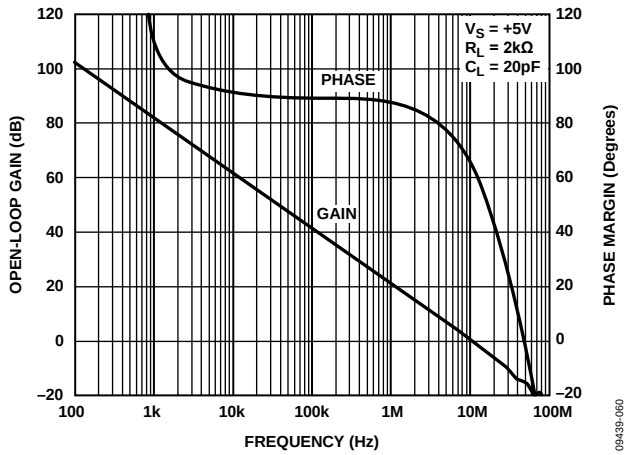

Figure 18. Open-Loop Gain and Phase Margin vs. Frequency

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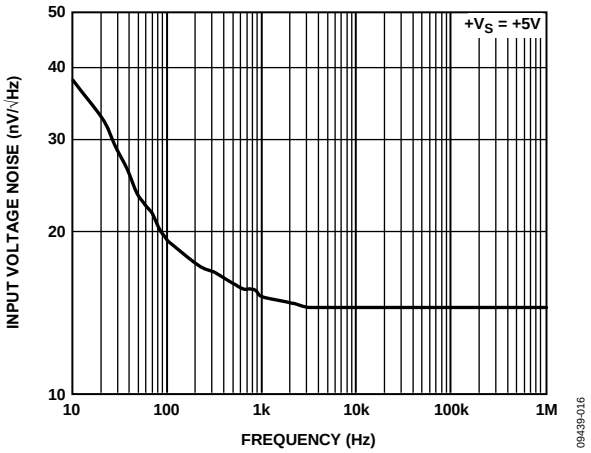

Figure 19. Input Voltage Noise vs. Frequency

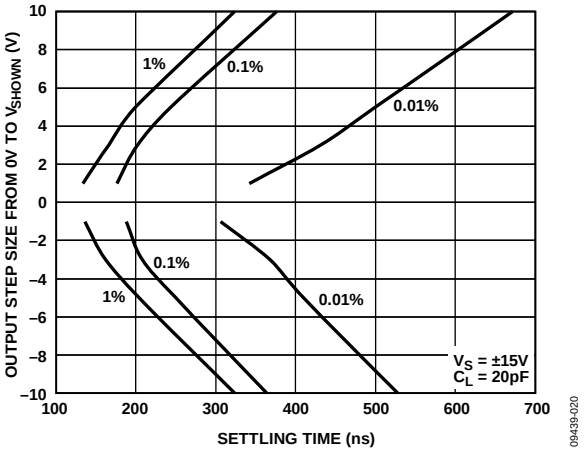

Figure 22. Output Step Size vs. Settling Time (Inverter)

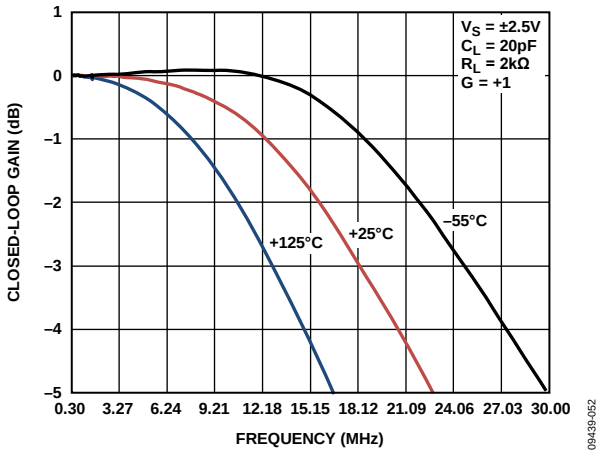

Figure 20. Closed-Loop Bandwidth vs. Temperature

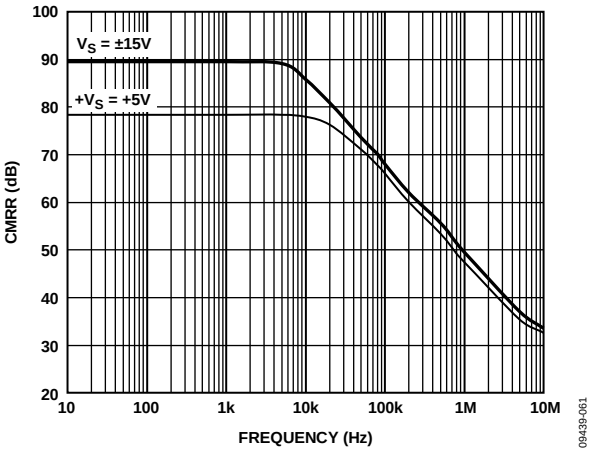

Figure 23. Common-Mode Rejection Ratio vs. Frequency

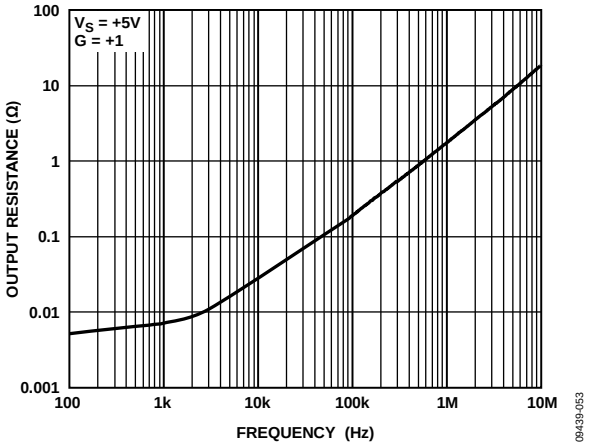

Figure 21. Output Resistance vs. Frequency, $+V_S$ = +5 V, G = +1

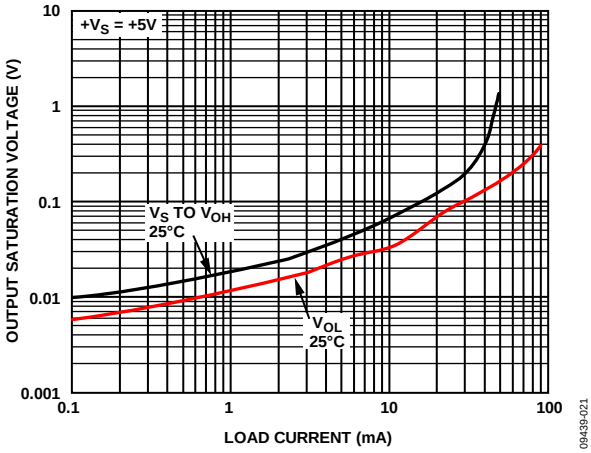

Figure 24. Output Saturation Voltage vs. Load Current

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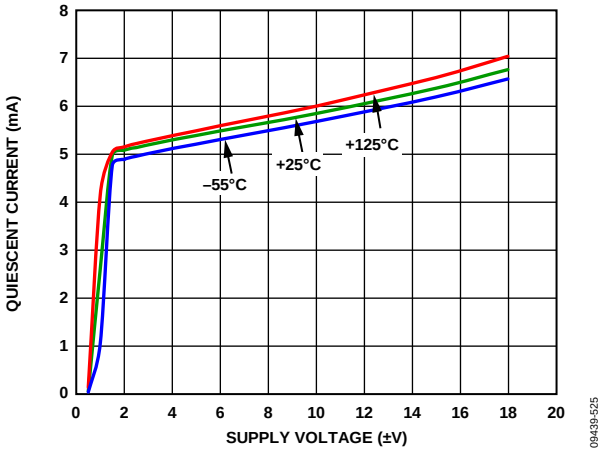

Figure 25. Quiescent Current vs. Supply Voltage

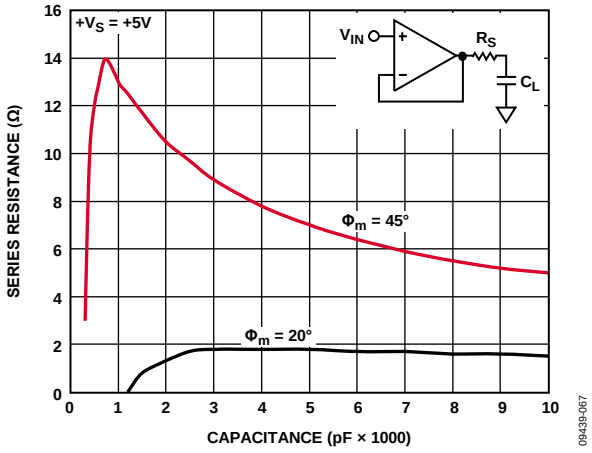

Figure 28. Series Resistance vs. Capacitive Load

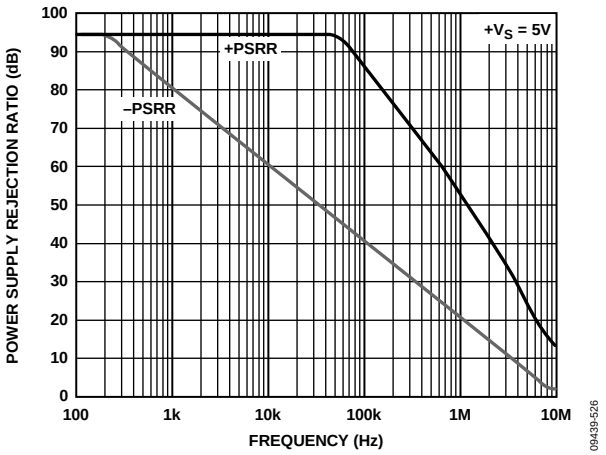

Figure 26. Power Supply Rejection Ratio vs. Frequency

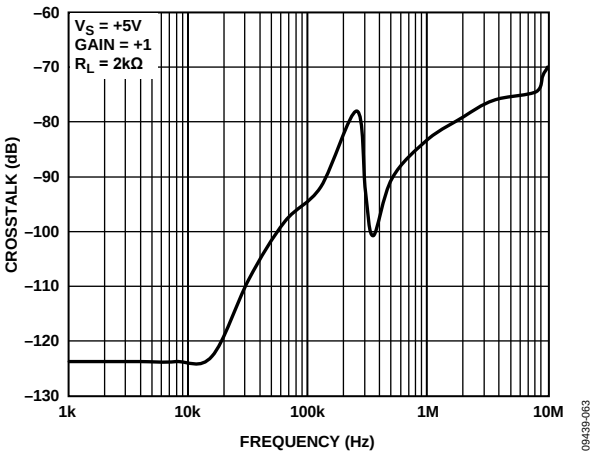

Figure 29. Crosstalk vs. Frequency

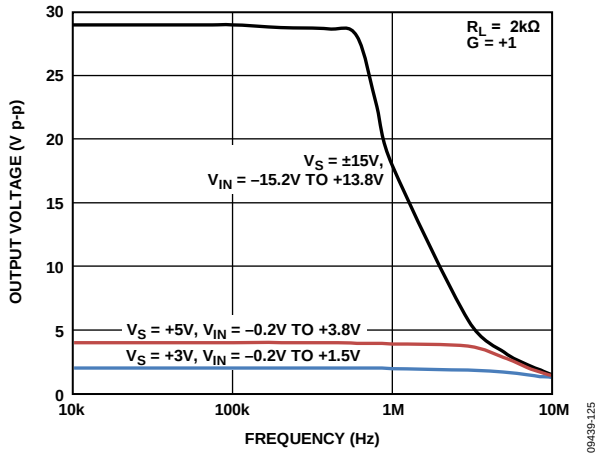

Figure 27. Large Signal Frequency Response

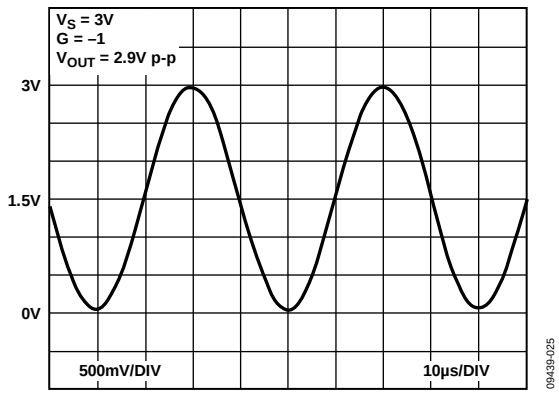

Figure 30. Output Swing, $+V_S = \pm 1.5$ V, $G = -1$

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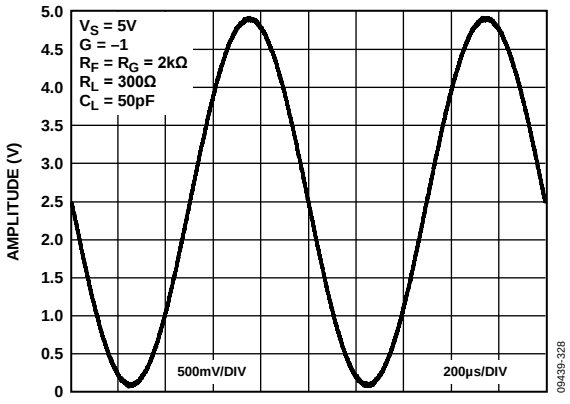

Figure 31. Output Swing, $+V_S$ = +5 V, G = –1

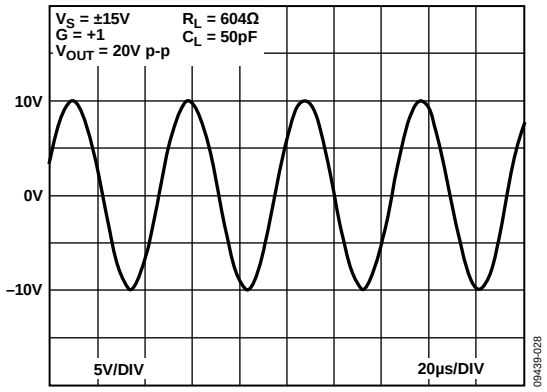

Figure 32. Output Swing, V_S = ±15 V, G = +1

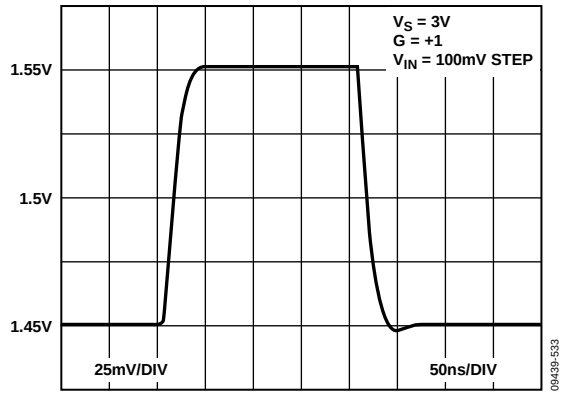

Figure 33. Pulse Response, $+V_S$ = ±3 V, G = +1

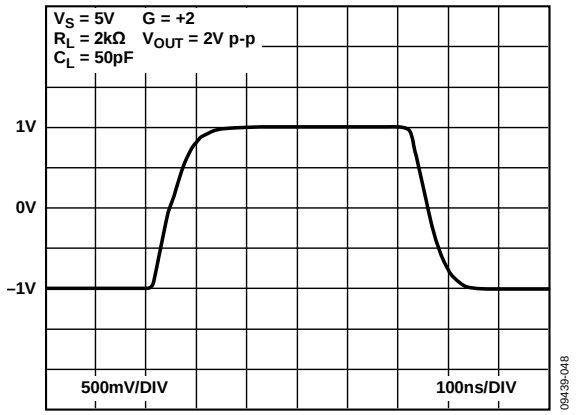

Figure 34. Pulse Response, $+V_S$ = ±2.5 V, G = +2

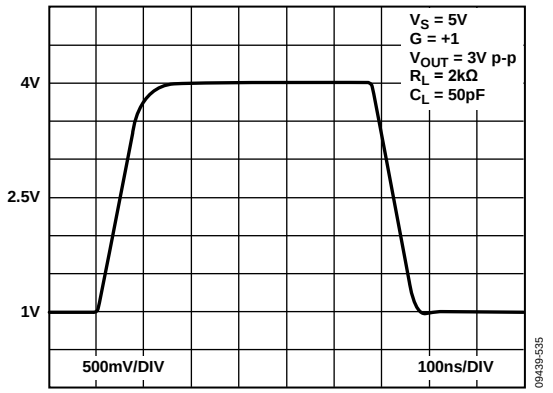

Figure 35. Pulse Response, $+V_S$ = ±2.5 V, G = +1

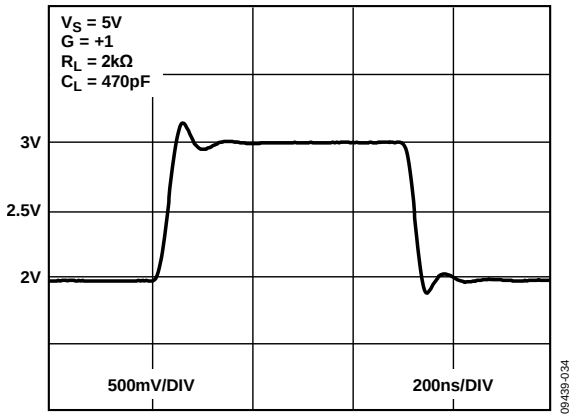

Figure 36. Pulse Response, $+V_S$ = +5 V, G = +1, C_L = 470 pF

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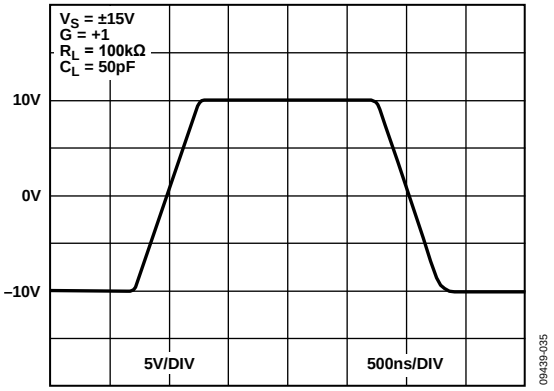

Figure 37. Pulse Response, V_S = ±15 V, G = +1

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THEORY OF OPERATION

The AD823A is a dual voltage feedback amplifier with an N-channel JFET input stage and a rail-to-rail bipolar output stage. It is fabricated on the Analog Devices, Inc. XFCB process, a dielectrically isolated complementary bipolar process featuring high speed 36 V bipolar devices along with JFETs and thin film resistors. The N-channel input stage handles signals up to 200 mV below the negative supply while maintaining picoamp level input currents. The rail-to-rail output maximizes the amplifier's output range and can provide up to 40 mA linear drive current with output voltages within .5 V of either power rail. Laser-trimmed thin film resistors are used to optimize offset voltage (3.5 mV max over the entire supply range) and offset voltage drift (typical 1 uV/°C).

Figure 38 shows the architecture of an amplifier. Two stages are used, with the first stage folded cascode input driving the differential input of the second stage output. The voltage swing at nodes S1p and S1n are kept small to minimize the generation of nonlinear currents due to junction capacitances. This improves distortion performance. Inputs and outputs of the amplifier are fully protected with dedicated ESD diodes.

OUTPUT IMPEDANCE

The low frequency open-loop output impedance of the common-emitter output stage used in this design is approximately 50 kΩ. Although this is significantly higher than a typical emitter follower output stage, when it is connected with feedback, the open-loop gain of the op amp reduces the output impedance.

With 105 dB of open-loop gain, the output impedance is reduced to <0.01 Ω. At higher frequencies, the output impedance rises as the open-loop gain of the op amp drops; however, the output also becomes capacitive due to the integrator capacitor. This prevents the output impedance from ever becoming excessively high (see Figure 21), which can cause stability problems when driving capacitive loads. In fact, the AD823A has excellent capacitive load drive capability for a high frequency op amp.

Figure 36 shows the results of the AD823A connected as a follower while driving a 470 pF direct capacitive load. Under these conditions, the phase margin is approximately 35°. For a greater phase margin, use a low value resistor in series with the output to decouple the effect of the load capacitance from the op amp (see Figure 28). In addition, running the part at higher gains also improves the capacitive load drive capability of the op amp.

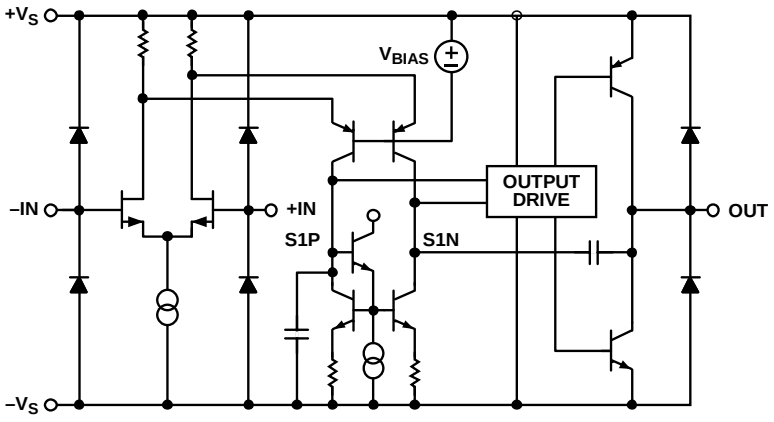

Figure 38. Simplified Schematic

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APPLICATIONS INFORMATION

INPUT CHARACTERISTICS

In the AD823A, N-channel JFETs provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1.2 V < $+V_S$. Driving the input voltage closer to the positive rail causes a loss of amplifier bandwidth and increased common-mode voltage error.

The AD823A does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 39 shows the response of an AD823A voltage follower to a 0 V to 5 V ($+V_S$) square wave input. The input and output are superimposed. The output polarity tracks the input polarity up to $+V_S$, with no phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output waveform. For input voltages greater than $+V_S$, a resistor (R_P) in series with the AD823A noninverting input prevents phase reversal, at the expense of greater input voltage noise. The value of R_P ranges from 1 kΩ to 10 kΩ. This is illustrated in Figure 40.

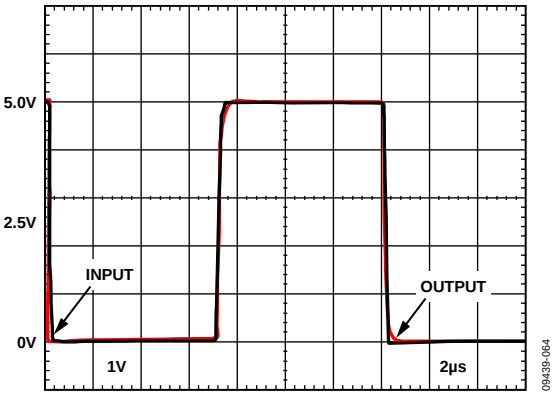

Figure 39. Input and Output Response: R_P = 0 kΩ, V_{IN} = 0 V to $+V_S$

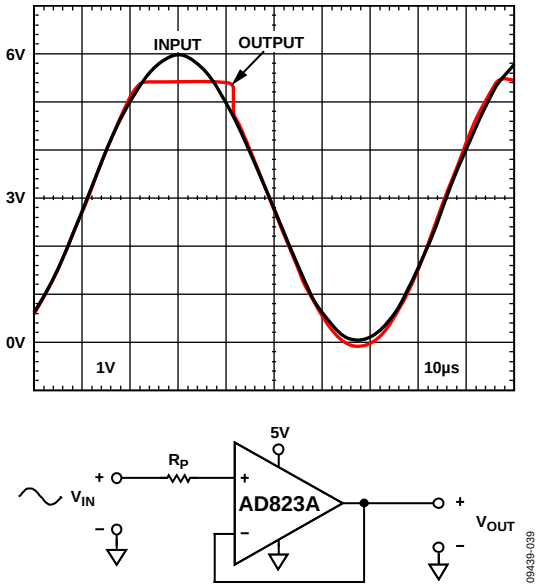

Figure 40. Input and Output Response: V_{IN} = 0 V to $+V_S$ + 1 V, V_{OUT} = 0 V to $+V_S$ + 400 mV, R_P = 4.99 kΩ

Because the input stage uses N-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than +VS − 0.7 V, the input current reverses direction as internal device junctions become forward biased. This is illustrated in Figure 11.

A current limiting resistor should be used in series with the input of the AD823A if the input voltage can be driven over 300 mV more positive than +Vs or 300 mV more negative than −Vs. The amplifier will be damaged if either condition persists for more than 10 seconds. A 1 kΩ resistor in series with the AD823A input allows the amplifier to withstand up to 10 V of continuous overvoltage and increases input voltage noise by a negligible amount.

The AD823A is designed for 14 nV/√Hz wideband input voltage noise (see Figure 19). This noise performance, along with the AD823A low input current and current noise, means that the AD823A contributes negligible noise for applications with high source resistances. Figure 41 shows that the source resistance contributes to negligible noise for source impedances lower than 10 kΩ. The low input capacitance of 0.6 pF also means that one can use a source impedance up to 13 kΩ without cutting into the G = +1 small signal bandwidth region.

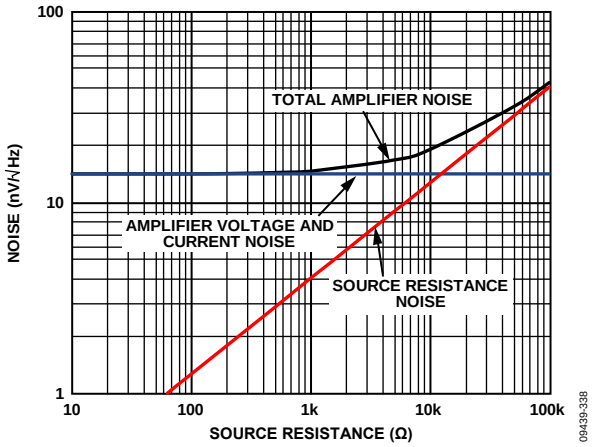

Figure 41. RTI Noise vs. Source Resistance

OUTPUT CHARACTERISTICS

The unique bipolar rail-to-rail output stage of the amplifier swings within 20 mV of the supplies with no external resistive load.

The approximate output saturation resistance of the AD823A is 33 Ω sourcing and sinking. This can be used to estimate the output saturation voltage when driving heavier current loads. For instance, when driving 5 mA, the saturation voltage to the rails is approximately 165 mV.

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WIDEBAND PHOTODIODE PREAMP

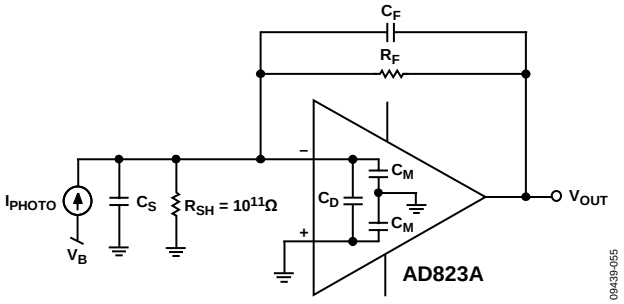

Figure 42. Wideband Photodiode Preamp

The AD823A is an excellent choice for photodiode preamp application. Its low input bias current minimizes the DC error at the preamp output. In addition, its high gain bandwidth product and low input capacitance maximizes the signal bandwidth of the photodiode preamp. Figure 42 shows the AD823A as a current-to-voltage (I/V) converter with an electrical model of a photodiode.

The transimpedance gain of the photodiode preamp can be described by the basic transfer function:

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F} \quad (1)$$

where I_{PHOTO} is the output current of the photodiode, and the parallel combination of R_F and C_F sets the signal bandwidth (see the I to V gain curve in Figure 43). Note that one should set R_F such that the maximum attainable output voltage corresponds to the maximum diode current I_{PHOTO}. This allows one to utilize the full output swing.

The signal bandwidth that is attainable with this preamp is a function of R_F, the gain bandwidth product (f_u) of the amplifier, and the total capacitance at the amplifier summing junction, including C_S and the amplifier input capacitance C_D and C_M. R_F and the total capacitance produce a pole with loop frequency (f_p).

$$f_p = \frac{1}{2\pi R_F C_S} \quad (2)$$

With the additional pole from the amplifier's open loop response, the two-pole system results in peaking and instability due to an insufficient phase margin (Figure 43(A), Without Compensation).

Adding C_F creates a zero in the loop transmission that compensates for the effect of the input pole. This stabilizes the photodiode preamp design because of the increased phase margin. It also sets the signal bandwidth (Figure 43(B), With Compensation). The signal bandwidth and the zero frequency are determined by

$$f_z = \frac{1}{2\pi R_F C_F} \quad (3)$$

Setting the zero at the frequency f_x maximizes the signal bandwidth with a 45° phase margin. Since f_x is the geometric mean of f_p and f_u, it can be calculated by

$$f_x = \sqrt{f_p \times f_u} \quad (4)$$

Combining Equation 2, Equation 3 and Equation 4, the value of C_F that produces f_x is defined by

$$C_F = \sqrt{\frac{C_S}{2\pi \times R_F \times f_u}} \quad (5)$$

The frequency response in this case shows about 2 dB of peaking and 15% overshoot. Doubling C_F and cutting the bandwidth in half results in a flat frequency response with about 5% transient overshoot.

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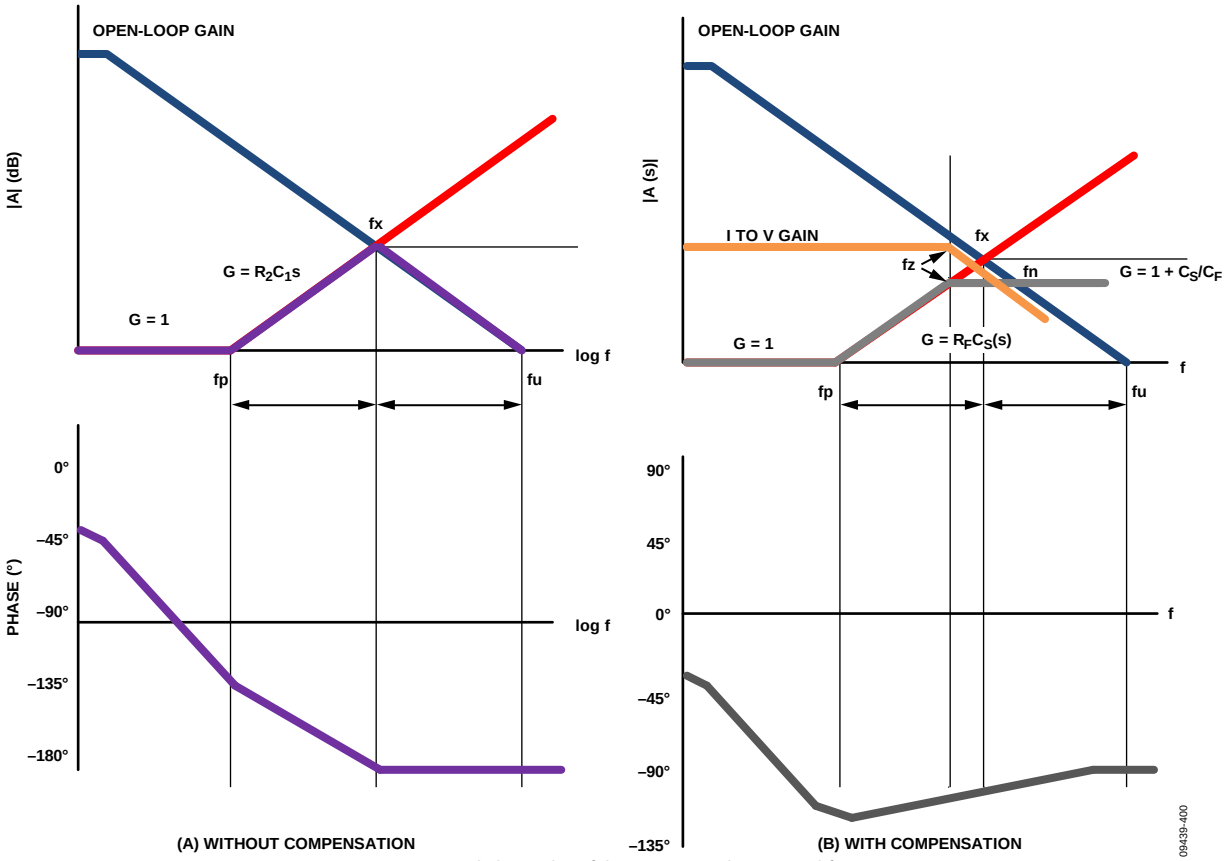

Figure 43. Gain and Phase Plot of the Transimpedance Amplifier Design

The dominant sources of output noise in the wideband photodiode preamp design are the input voltage noise of the amplifier, V_{NOISE} and the resistor noise due to R_F. The gray curve in Figure 43 shows the noise gain over frequencies for the photodiode preamp. The noise bandwidth is at the frequency f_N, and it can be calculated by

$$f_N = \frac{f_u}{(C_S + C_F)/C_F} \quad (6)$$

Figure 44 shows the AD823A configured as a transimpedance photodiode amplifier. The amplifier is used in conjunction with a photodiode detector with input capacitance of 5 pF. Figure 45 shows the transimpedance response of the AD823A when I_{PHOTO} is 1 µA p-p. The amplifier has a bandwidth of 2.2 MHz when it is maximized for a 45° phase margin with C_F = 1.2 pF. Note that with the PCB parasitics added to C_F, the peaking is only 0.5 dB and the bandwidth is slightly reduced. Increasing C_F to 2.7 pF completely eliminates the peaking. However, it reduces the bandwidth to 1.2 MHz.

Table 8 shows the noise sources and total output noise for the photodiode preamp, where the preamplifier is configured to have a 45° phase margin for maximal bandwidth and $f_z = f_x = f_n$ in this case.

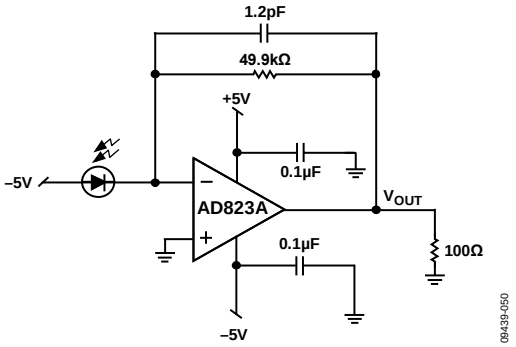

Figure 44. Photodiode Preamplifier

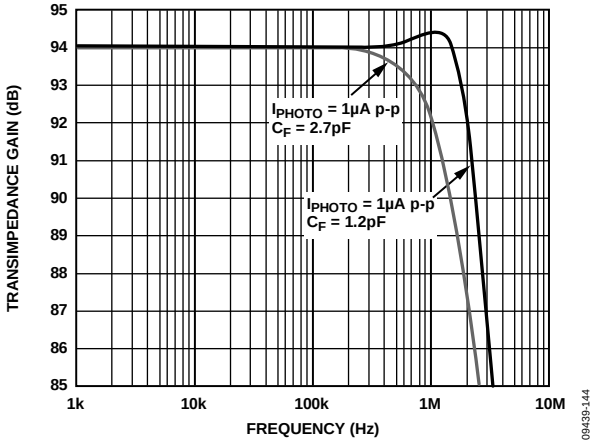

Figure 45. Photodiode Preamplifier Frequency Response

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Table 8. RMS Noise Contributions of Photodiode Preamp

Contributor	Expression	(μV)[1]
R_F	$\sqrt{4kT \times R_F \times f_N \times \frac{\pi}{2}}$	55.17
V_{NOISE}	$V_{NOISE} \times \sqrt{\frac{(C_S + C_M + C_F + 2C_D)}{C_F}} \times \sqrt{\frac{\pi}{2} \times f_N}$	138.5
	RSS Total	149.1

[1] RMS noise with R_F = 50 kΩ, C_S = 5 pF, C_F = 1.2 pF, C_M = 1.3 pF, and C_D = 0.6 pF.

ACTIVE FILTER

The AD823A is an ideal candidate for an active filter because of its low input bias current and its low input capacitance. Low input bias current reduces dc error in the signal path while low input capacitance improves the accuracy of the active filter.

As a general rule of thumb, the bandwidth of the amplifier should be at least 10 times bigger than the cutoff frequency of the filter implemented. Therefore, the AD823A is capable of implementing active filters of up to 1.7 MHz.

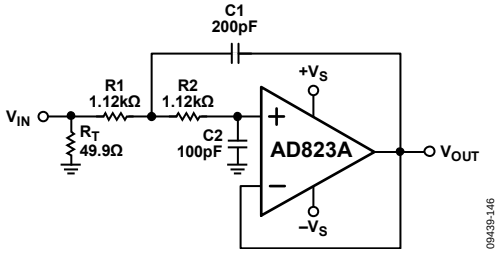

Figure 46. Two-Pole Sallen-Key Active Filter

Figure 46 shows an example of a second-order Butterworth filter, which is implemented by the Sallen-Key topology. This structure can be duplicated to produce higher-order filters.

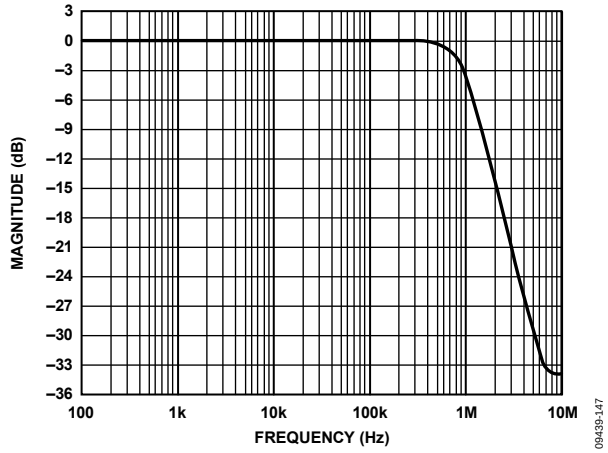

Figure 47. Two-Pole Butterworth Active Filter Response

Figure 47 shows the two-pole Butterworth active filter's response. Note that it has a maximally flat pass band, a −3 dB bandwidth of 1 MHz, and a 12 dB/octave roll-off in the stop band.

The cutoff frequency (f_c) and the Q factor of the Butterworth filter can be calculated by:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (7)$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{(R_1 + R_2) \times C_2} \quad (8)$$

Therefore, one can easily adjust the cutoff frequency by appropriately factoring the resistor and capacitor values. For example, a 100 kHz filter can be implemented by increasing the values of R1 and R2 by 10 times. Note that the Q factor remains the same in this case.

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MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the AD823A, care should be taken in the circuit board layout. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 48 shows how the guard rings should be configured, and Figure 49 shows the top view of how a surface-mount layout can be arranged. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon® standoff insulators.

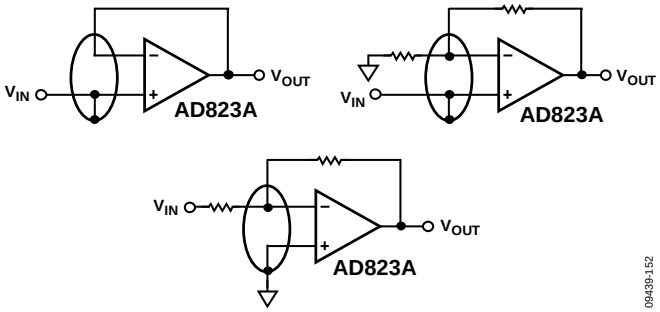

Figure 48. Guard Ring Layout and Connections to Reduce PCB Leakage Currents

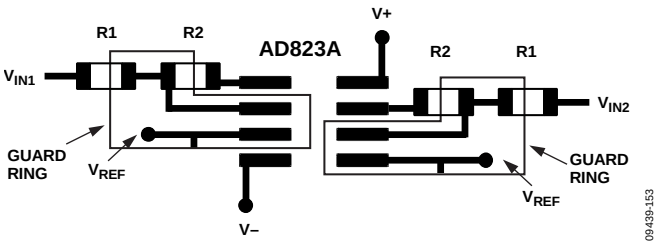

Figure 49. Top View of AD823A SOIC Layout with Guard Rings

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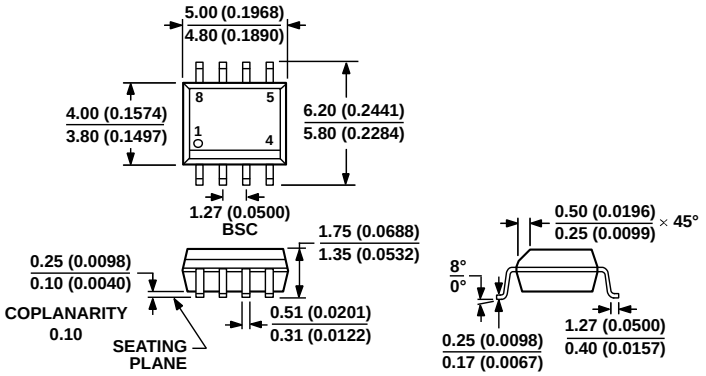
OUTLINE DIMENSIONS



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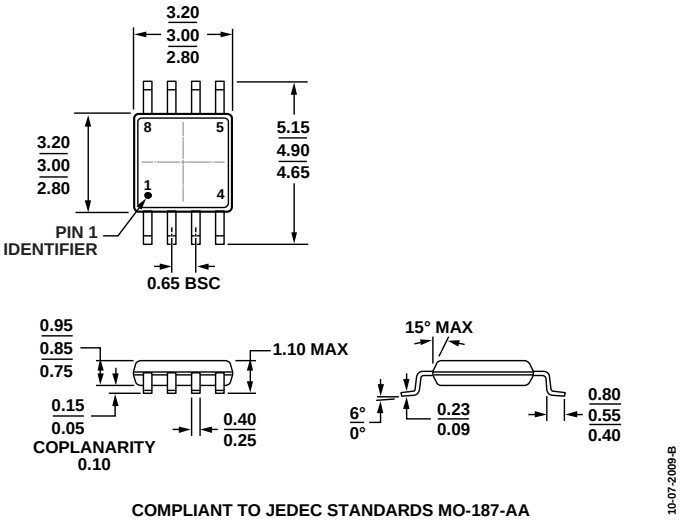
012407-A

Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 51. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Models[1]	Temperature Range	Package Description	Package Option	Branding
AD823AARZ	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD823AARZ-RL	−40°C to +85°C	8-Lead SOIC_N, 13″Tape and Reel	R-8	
AD823AARZ-R7	−40°C to +85°C	8-Lead SOIC_N, 7″Tape and Reel	R-8	
AD823AARMZ	−40°C to +85°C	8-lead MSOP	RM-8	H34
AD823AARMZ-R7	−40°C to +85°C	8-lead MSOP, 7″Tape and Reel	RM-8	H34
AD823A-2AR-EBZ		Evaluation Board for 8-Lead SOIC		
AD823A-2ARM-EBZ		Evaluation Board for 8-Lead MSOP		

[1] Z = RoHS Compliant Part.

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