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SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, GND = 0 V, REF_{IN} = 2.5 V, unless otherwise noted. The AD7817 temperature sensor is specified with an external 2.5 V reference, and the AD7818 temperature sensor is specified with an on-chip reference. For V_{DD} = 2.7 V, T_A = 85°C maximum and temperature sensor measurement error = ±3°C.

Table 1.

Parameter	A Version[1]	B Version[1]	S Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE (AD7817 ONLY)					Sample rate = 100 kSPS, any channel, f_{IN} = 20 kHz
Signal-to-(Noise + Distortion) Ratio[2]	58	58	58	dB min	
Total Harmonic Distortion[2]	−65	−65	−65	dB max	−75 dB typical
Peak Harmonic or Spurious Noise[2]	−65	−65	−65	dB max	−75 dB typical
Intermodulation Distortion[2]					fa =19.9 kHz, fb = 20.1 kHz
Second-Order Terms	−67	−67	−67	dB typ	
Third-Order Terms	−67	−67	−67	dB typ	
Channel-to-Channel Isolation[2]	−80	−80	−80	dB typ	f_{IN} = 20 kHz
DC ACCURACY (AD7817 ONLY)					Any channel
Resolution	10	10	10	Bits	
Minimum Resolution for Which No Missing Codes are Guaranteed	10	10	10		
Relative Accuracy[2]	±1	±1	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	
Gain Error[2]	±2	±2	±2	LSB max	External reference
	±10	±10	+20/−10	LSB max	Internal reference
Gain Error Match[2]	±1/2	±1/2	±1/2	LSB max	
Offset Error[2]	±2	±2	±2	LSB max	
Offset Error Match	±1/2	±1/2	±1/2	LSB max	
TEMPERATURE SENSOR (AD7817 ONLY)					
Measurement Error					External reference V_{REF} = 2.5 V
Ambient Temperature 25°C	±2	±1	±2	°C max	
T_{MIN} to T_{MAX}	±3	±2	±3	°C max	
Measurement Error					On-chip reference
Ambient Temperature 25°C	±2.25	±2.25	±2.25	°C max	
T_{MIN} to T_{MAX}	±3	±3	±6	°C max	
Temperature Resolution	1/4	1/4	1/4	°C/LSB	
REFERENCE INPUT (AD7817 ONLY)[3, 4]					
REF_{IN} Input Voltage Range[3]	2.625	2.625	2.625	V max	2.5 V + 5%
	2.375	2.375	2.375	V min	2.5 V − 5%
Input Impedance	40	40	40	kΩ min	
Input Capacitance	10	10	10	pF max	
ON-CHIP REFERENCE (AD7817 ONLY)[5]					Nominal 2.5 V
Temperature Coefficient[3]	80	80	150	ppm/°C typ	
CONVERSION RATE (AD7817 ONLY)					
Track-and-Hold Acquisition Time[4]	400	400	400	ns max	Source Impedance < 10 Ω
Conversion Time					
Temperature Sensor	27	27	27	µs max	
Channel 1 to Channel 4	9	9	9	µs max	

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Parameter	A Version[1]	B Version[1]	S Version[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS (AD7817 ONLY)					
V_{DD}	5.5	5.5	5.5	V max	For specified performance
	2.7	2.7	2.7	V min	
I_{DD}					Logic inputs = 0 V or V_{DD}
Normal Operation	2	2	2	mA max	1.6 mA typical
Using External Reference	1.75	1.75	1.75	mA max	2.5 V external reference connected
Power-Down (V_{DD} = 5 V)	10	10	12.5	µA max	5.5 µA typical
Power-Down (V_{DD} = 3 V)	4	4	4.5	µA max	2 µA typical
Auto Power-Down Mode					V_{DD} = 3 V
10 SPS Throughput Rate	6.4	6.4	6.4	µW typ	See the Power vs. Throughput section for description of power dissipation in auto power-down mode
1 kSPS Throughput Rate	48.8	48.8	48.8	µW typ	
10 kSPS Throughput Rate	434	434	434	µW typ	
Power-Down	12	12	13.5	µW max	Typically 6 µW
DYNAMIC PERFORMANCE (AD7818 ONLY)[6]					Sample rate = 100 kSPS, any channel, f_{IN} = 20 kHz
Signal-to-(Noise + Distortion) Ratio[2]	57			dB min	
Total Harmonic Distortion[2]	−65			dB max	−75 dB typical
Peak Harmonic or Spurious Noise[2]	−67			dB typ	−75 dB typical
Intermodulation Distortion[2]					fa = 19.9 kHz, fb = 20.1 kHz
Second-Order Terms	−67			dB typ	
Third-Order Terms	−67			dB typ	
Channel-to-Channel Isolation[2]	−80			dB typ	f_{IN} = 20 kHz
DC ACCURACY (AD7818 ONLY)[6]					Any channel
Resolution	10			Bits	
Minimum Resolution for Which No Missing Codes are Guaranteed	10			Bits	
Relative Accuracy[2]	±1			LSB max	
Differential Nonlinearity[2]	±1			LSB max	
Gain Error[2]	±10			LSB max	
Offset Error[2]	±4			LSB max	
TEMPERATURE SENSOR (AD7818 ONLY)[6]					
Measurement Error					Internal reference V_{REF} = 2.5 V
Ambient Temperature 25°C	±2			°C max	
T_{MIN} to T_{MAX}	±3			°C max	
Measurement Error					On-chip reference
Ambient Temperature 25°C	±2			°C max	
T_{MIN} to T_{MAX}	±3			°C max	
Temperature Resolution	1/4			°C/LSB	
ON-CHIP REFERENCE (AD7818 ONLY)[5]					Nominal 2.5 V
Temperature Coefficient[3]	30			ppm/°C typ	
CONVERSION RATE (AD7818 ONLY)[6]					
Track-and-Hold Acquisition Time[4]	400			ns max	Source impedance < 10 Ω
Conversion Time					
Temperature Sensor	27			µs max	
Channel 1	9			µs max	

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Parameter	A Version[1]	B Version[1]	S Version[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS (AD7818 ONLY)[6]					
V_{DD}	5.5			V max	For specified performance
	2.7			V min	
I_{DD}					Logic inputs = 0 V or V_{DD}
Normal Operation	2			mA max	1.3 mA typical
Using External Reference	1.75			mA max	2.5 V internal reference connected
Power-Down (V_{DD} = 5 V)	10.75			µA max	6 µA typ
Power-Down (V_{DD} = 3 V)	4.5			µA max	2 µA typ
Auto Power-Down Mode					V_{DD} = 3 V
10 SPS Throughput Rate	6.4			µW typ	See the Power vs. Throughput section for description of power dissipation in auto power-down mode
1 kSPS Throughput Rate	48.8			µW typ	
10 kSPS Throughput Rate	434			µW typ	
Power-Down	13.5			µW max	Typically 6 µW
ANALOG INPUTS (AD7817/AD7818)[7]					
Input Voltage Range	V_{REF}	V_{REF}	V_{REF}	V max	
	0	0	0	V min	
Input Leakage	±1	±1	±1	µA min	
Input Capacitance	10	10	10	pF max	
LOGIC INPUTS (AD7817/AD7818)[4]					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ±10%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ±10%
Input High Voltage, V_{INH}	2	2	2	V min	V_{DD} = 3 V ±10%
Input Low Voltage, V_{INL}	0.4	0.4	0.4	V max	V_{DD} = 3 V ±10%
Input Current, I_{IN}	±3	±3	±3	µA max	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	10	pF max	
LOGIC OUTPUTS (AD7817/AD7818)[4]					
Output High Voltage, V_{OH}					I_{SOURCE} = 200 µA
	4	4	4	V min	V_{DD} = 5 V ± 10%
	2.4	2.4	2.4	V min	V_{DD} = 3 V ± 10%
Output Low Voltage, V_{OL}					I_{SINK} = 200 µA
	0.4	0.4	0.4	V max	V_{DD} = 5 V ± 10%
	0.2	0.2	0.2	V max	V_{DD} = 3 V ± 10%
High Impedance Leakage Current	±1	±1	±1	µA max	
High Impedance Capacitance	15	15	15	pF max	

[1] The B Version and the S Version only apply to the AD7817. The A Version applies to the AD7817 or the AD7818 (as stated in specification).
[2] See Terminology.
[3] The accuracy of the temperature sensor is affected by reference tolerance. The relationship between the two is explained in the Temperature Measurement Error Due to Reference Error section.
[4] Sample tested during initial release and after any redesign or process change that may affect this parameter.
[5] On-chip reference shuts down when external reference is applied.
[6] These specifications are typical for AD7818 at temperatures above 85°C and with V_{DD} greater than 3.6 V.
[7] This refers to the input current when the part is not converting. Primarily due to the reverse leakage current in the ESD protection diodes.

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TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, GND = 0 V, REF_{IN} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Sample tested during initial release and after any redesign or process changes that may affect the parameters. All input signals are measured with tr = tf = 1 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V. See Figure 17, Figure 18, Figure 21, and Figure 22.

Table 2.

Parameter	A Version/B Version	Unit	Test Conditions/Comments
$t_{POWER-UP}$	2	µs max	Power-up time from rising edge of $\overline{CONVST}$
t_{1a}	9	µs max	Conversion time Channel 1 to Channel 4
t_{1b}	27	µs max	Conversion time temperature sensor
t_2	20	ns min	$\overline{CONVST}$ pulse width
t_3	50	ns max	$\overline{CONVST}$ falling edge to BUSY rising edge
t_4	0	ns min	$\overline{CS}$ falling edge to RD/$\overline{WR}$ falling edge setup time
t_5	0	ns min	RD/$\overline{WR}$ falling edge to SCLK falling edge setup
t_6	10	ns min	D_{IN} setup time before SCLK rising edge
t_7	10	ns min	D_{IN} hold time after SCLK rising edge
t_8	40	ns min	SCLK low pulse width
t_9	40	ns min	SCLK high pulse width
t_{10}	0	ns min	$\overline{CS}$ falling edge to RD/$\overline{WR}$ rising edge setup time
t_{11}	0	ns min	RD/$\overline{WR}$ rising edge to SCLK falling edge setup time
t_{12}[1]	20	ns max	D_{OUT} access time after RD/$\overline{WR}$ rising edge
t_{13}[1]	20	ns max	D_{OUT} access time after SCLK falling edge
t_{14a}[1, 2]	30	ns max	D_{OUT} bus relinquish time after falling edge of RD/$\overline{WR}$
t_{14b}[1, 2]	30	ns max	D_{OUT} bus relinquish time after rising edge of $\overline{CS}$
t_{15}	150	ns max	$\overline{BUSY}$ falling edge to $\overline{OTI}$ falling edge
t_{16}	40	ns min	RD/$\overline{WR}$ rising edge to $\overline{OTI}$ rising edge
t_{17}	400	ns min	SCLK rising edge to $\overline{CONVST}$ falling edge (acquisition time of T/H)

[1] These figures are measured with the load circuit of Figure 3. They are defined as the time required for D_{OUT} to cross 0.8 V or 2.4 V for V_{DD} = 5 V ± 10% and 0.4 V or 2 V for V_{DD} = 3 V ± 10%, as shown in Table 1.

[2] These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of the external bus loading capacitances.

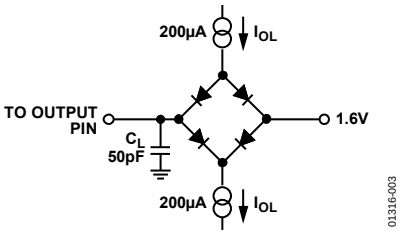

Figure 3. Load Circuit for Access Time and Bus Relinquish Time

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
Analog Input Voltage to AGND	
V_{IN1} to V_{IN4}	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to AGND[1]	−0.3 V to V_{DD} + 0.3V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	120°C/W
Lead Temperature, Soldering	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
16-Lead SOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	100°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
8-Lead SOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	157°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
8-Lead MSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	206°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] If the reference input voltage is likely to exceed V_{DD} by more than 0.3 V (that is, during power-up) and the reference is capable of supplying 30 mA or more, it is recommended to use a clamping diode between the REF_{IN} pin and V_{DD} pin.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

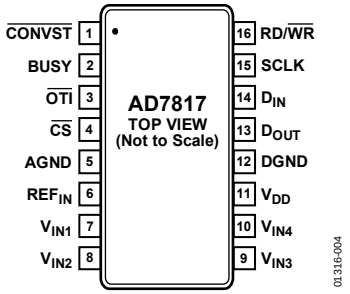

Figure 4. AD7817 Pin Configuration

Table 4. AD7817 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Logic Input Signal. The convert start signal. A 10-bit analog-to-digital conversion is initiated on the falling edge of this signal. The falling edge of this signal places track-and-hold in hold mode. Track-and-hold goes into track mode again at the end of the conversion. The state of the $\overline{\text{CONVST}}$ signal is checked at the end of a conversion. If it is logic low, the AD7817 powers down. See the Operating Modes section.
2	BUSY	Logic Output. The busy signal is logic high during a temperature or voltage A/D conversion. The signal can be used to interrupt a microcontroller when a conversion has finished.
3	$\overline{\text{OTI}}$	Logic Output. The overtemperature indicator ($\overline{\text{OTI}}$) is set logic low if the result of a conversion on Channel 0 (temperature sensor) is greater that an 8-bit word in the overtemperature register (OTR). The signal is reset at the end of a serial read operation, that is, a rising RD/$\overline{\text{WR}}$ edge when $\overline{\text{CS}}$ is low.
4	$\overline{\text{CS}}$	Logic Input Signal. The chip select signal is used to enable the serial port of the AD7817. This is necessary if the AD7817 is sharing the serial bus with more than one device.
5	AGND	Analog Ground. Ground reference for track-and-hold comparator and capacitor DAC.
6	REF_{IN}	Analog Input. An external 2.5 V reference can be connected to the AD7817 at this pin. To enable the on-chip reference, tie the REF_{IN} pin to AGND. If an external reference is connected to the AD7817, the internal reference shuts down.
7 to 10	V_{IN1} to V_{IN4}	Analog Input Channels. The AD7817 has four analog input channels. The input channels are single-ended with respect to AGND (analog ground). The input channels can convert voltage signals in the range 0 V to V_{REF}. A channel is selected by writing to the address register of the AD7817. See the Control Byte section.
11	V_{DD}	Positive Supply Voltage, 2.7 V to 5.5 V.
12	DGND	Digital Ground. Ground reference for digital circuitry.
13	D_{OUT}	Logic Output with a High Impedance State. Data is clocked out of the AD7817 serial port at this pin. This output goes into a high impedance state on the falling edge of RD/$\overline{\text{WR}}$ or on the rising edge of the $\overline{\text{CS}}$ signal, whichever occurs first.
14	D_{IN}	Logic Input. Data is clocked into the AD7817 at this pin.
15	SCLK	Clock Input for the Serial Port. The serial clock is used to clock data into and out of the AD7817. Data is clocked out on the falling edge and clocked in on the rising edge.
16	RD/$\overline{\text{WR}}$	Logic Input Signal. The read/write signal is used to indicate to the AD7817 whether the data transfer operation is a read or a write. Set the RD/$\overline{\text{WR}}$ logic high for a read operation and logic low for a write operation.

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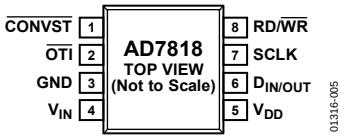

Figure 5. AD7818 Pin Configuration

Table 5. AD7818 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Logic Input Signal. The convert start signal initiates a 10-bit analog-to-digital conversion on the falling edge of this signal. The falling edge of this signal places track-and-hold in hold mode. Track-and-hold goes into track mode again at the end of the conversion. The state of the $\overline{\text{CONVST}}$ signal is checked at the end of a conversion. If it is logic low, the AD7818 powers down. See the Operating Modes section.
2	$\overline{\text{OTI}}$	Logic Output. The overtemperature indicator ($\overline{\text{OTI}}$) is set logic low if the result of a conversion on Channel 0 (temperature sensor) is greater that an 8-bit word in the overtemperature register (OTR). The signal is reset at the end of a serial read operation, that is, a rising RD/$\overline{\text{WR}}$ edge.
3	GND	Analog and Digital Ground.
4	V_{IN}	Analog Input Channel. The input channel is single-ended with respect to GND. The input channel can convert voltage signals in the range 0 V to 2.5 V. The input channel is selected by writing to the address register of the AD7818. See the Control Byte section.
5	V_{DD}	Positive Supply Voltage, 2.7 V to 5.5 V.
6	$D_{IN/OUT}$	Logic Input and Output. Serial data is clocked in and out of the AD7818 at this pin.
7	SCLK	Clock Input for the Serial Port. The serial clock is used to clock data into and out of the AD7818. Data is clocked out on the falling edge and clocked in on the rising edge.
8	RD/$\overline{\text{WR}}$	Logic Input. The read/write signal is used to indicate to the AD7818 whether the next data transfer operation is a read or a write. Set the RD/$\overline{\text{WR}}$ logic high for a read operation and logic low for a write.

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TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02N + 1.76)\ \text{dB}$$

Thus, for a 10-bit converter, this is 62 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7817/AD7818, it is defined as:

$$THD(dB) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum; however, for devices where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7817/AD7818 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second- and third-order terms are of different significance. The second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 20 kHz sine wave signal to one input channel and determining how much that signal is attenuated in each of the other channels. The figure given is the worst case across all four channels.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Gain Error
This is the deviation of the last code transition (1111 . . . 110) to (1111 . . . 111) from the ideal, that is, VREF – 1 LSB, after the offset error has been adjusted out.

Gain Error Match
This is the difference in gain error between any two channels.

Offset Error
This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match
This is the difference in offset error between any two channels.

Track-and-Hold Acquisition Time
The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track-and-hold returns to track mode). It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7817 or the AD7818. It means that the user must wait for the duration of the track-and-hold acquisition time after the end of conversion or after a channel change/step input change to V_{IN} before starting another conversion, to ensure that the device operates to specification.

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CONTROL BYTE

The AD7817/AD7818 contain two on-chip registers, the address register and the overtemperature register. These registers can be accessed by carrying out an 8-bit serial write operation to the devices. The 8-bit word or control byte written to the AD7817/AD7818 is transferred to one of the two on-chip registers as follows.

Address Register

If the five MSBs of the control byte are logic zero, the three LSBs of the control byte are transferred to the address register (see Figure 6). The address register is a 3-bit-wide register used to select the analog input channel on which to carry out a conversion. It is also used to select the temperature sensor, which has the 000 address. Table 6 shows the channel selection. The internal reference selection connects the input of the ADC to a band gap reference. When this selection is made and a conversion is initiated, the ADC output must be approximately midscale. After power-up, the default channel selection is DB2 = DB1 = DB0 = 0 (temperature sensor).

Table 6. Channel Selection

DB2	DB1	DB0	Channel Selection	Device
0	0	0	Temperature sensor	All
0	0	1	Channel 1	All
0	1	0	Channel 2	AD7817
0	1	1	Channel 3	AD7817
1	0	0	Channel 4	AD7817
1	1	1	Internal reference (1.23 V)	All

Overtemperature Register

If any of the five MSBs of the control byte are logic one, the entire eight bits of the control byte are transferred to the overtemperature register (see Figure 6). At the end of a temperature conversion, a digital comparison is carried out between the 8 MSBs of the temperature conversion result (10 bits) and the contents of the overtemperature register (8 bits). If the result of the temperature conversion is greater than the contents of the overtemperature register (OTR), the overtemperature indicator ($\overline{OTI}$) goes logic low. The resolution of the OTR is 1°C. The lowest temperature that can be written to the OTR is −95°C and the highest is +152°C (see Figure 7). However, the usable temperature range of the temperature sensor is −55°C to +125°C. Figure 7 shows the OTR and how to set T_{ALARM} (the temperature at which the $\overline{OTI}$ goes low).

$$OTR\ (Dec) = T_{ALARM}\ (°C) + 103°C$$

For example, to set T_{ALARM} to 50°C, OTR = 50 + 103 = 153 Dec or 10011001 bin. If the result of a temperature conversion exceeds 50°C, $\overline{OTI}$ goes logic low. The $\overline{OTI}$ logic output is reset high at the end of a serial read operation or if a new temperature measurement is lower than T_{ALARM}. The default power on T_{ALARM} is 50°C.

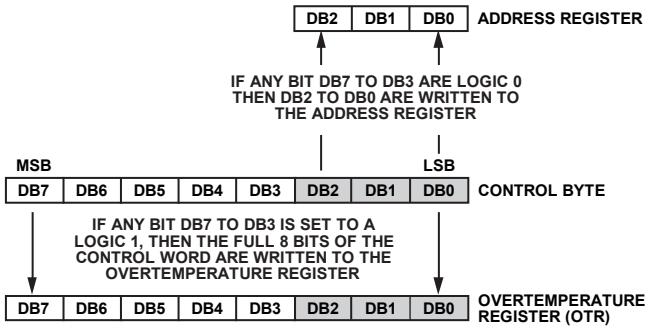

Figure 6. Address and Overtemperature Register Selection

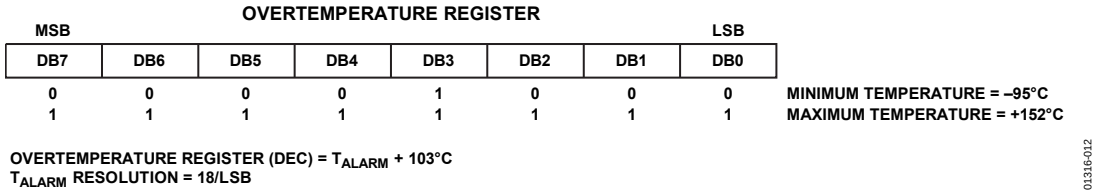

Figure 7. The Overtemperature Register (OTR)

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CIRCUIT INFORMATION

The AD7817/AD7818 are single- and four-channel, 9 µs conversion time, 10-bit ADCs with an on-chip temperature sensor, reference, and serial interface logic functions on a single chip. The ADC section consists of a conventional, successive approximation converter based around a capacitor DAC. The AD7817/AD7818 are capable of running on a 2.7 V to 5.5 V power supply, and they accept an analog input range of 0 V to V_{REF}. The on-chip temperature sensor allows an accurate measurement of the ambient device temperature to be made. The working measurement range of the temperature sensor is −55°C to +125°C. The AD7817/AD7818 require a 2.5 V reference, which can be provided from their internal reference or from an external reference source. The on-chip reference is selected by connecting the REF_{IN} pin to analog ground.

CONVERTER DETAILS

Conversion is initiated by pulsing the $\overline{CONVST}$ input. The conversion clock for the device is internally generated; therefore, an external clock is not required, except when reading from and writing to the serial port. The on-chip, track-and-hold goes from track mode to hold mode, and the conversion sequence is started on the falling edge of the $\overline{CONVST}$ signal. At this point, the BUSY signal goes high and low again 9 µs or 27 µs later (depending on whether an analog input or the temperature sensor is selected) to indicate the end of the conversion process. A microcontroller can use this signal to determine when the result of the conversion is to be read. The track-and-hold acquisition time of the AD7817/AD7818 is 400 ns.

A temperature measurement is made by selecting the Channel 0 of the on-chip mux and carrying out a conversion on this channel. A conversion on Channel 0 takes 27 µs to complete. Temperature measurement is explained in the Temperature Measurement section.

The on-chip reference is not available, however, REF_{IN} can be overdriven by an external reference source (2.5 V only). The effect of reference tolerances on temperature measurements is discussed in the Temperature Measurement Error Due to Reference Error section.

Tie all unused analog inputs to a voltage within the nominal analog input range to avoid noise pickup. For minimum power consumption, tie the unused analog inputs to AGND.

TYPICAL CONNECTION DIAGRAM

Figure 8 shows a typical connection diagram for the AD7817. The AGND and DGND are connected together at the device for good noise suppression. The BUSY line is used to interrupt the microcontroller at the end of the conversion process, and the serial interface is implemented using three wires (see the AD7817 Serial Interface section for more details). An external 2.5 V reference can be connected at the REF_{IN} pin. If an external reference is used, connect a 10 µF capacitor between REF_{IN} and AGND. For applications where power consumption is a concern, use the automatic power-down at the end of a conversion to improve power performance. See the Power vs. Throughput section.

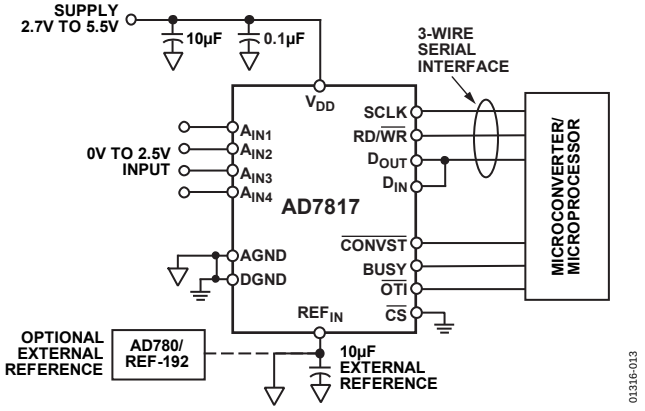

Figure 8. Typical Connection Diagram

ANALOG INPUTS

Analog Input

Figure 9 shows an equivalent circuit of the analog input structure of the AD7817/AD7818. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Take care to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This causes these diodes to become forward-biased and start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the device is 20 mA. The C2 capacitor in Figure 9 is typically about 4 pF and can mostly be attributed to pin capacitance. The R1 resistor is a lumped component made up of the on resistance of a multiplexer and a switch. This resistor is typically about 1 kΩ. The C1 capacitor is the ADC sampling capacitor and has a capacitance of 3 pF.

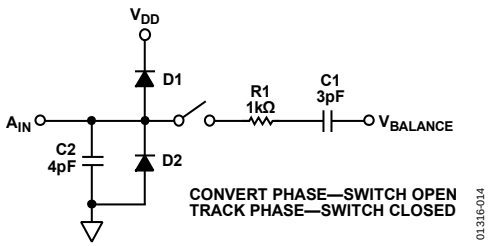

Figure 9. Equivalent Analog Input Circuit

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DC Acquisition Time

The ADC starts a new acquisition phase at the end of a conversion and ends on the falling edge of the $\overline{\text{CONVST}}$ signal. At the end of a conversion, a settling time is associated with the sampling circuit. This settling time lasts approximately 100 ns. The analog signal on V_{IN} is also being acquired during this settling time. Therefore, the minimum acquisition time needed is approximately 100 ns.

Figure 10 shows the equivalent charging circuit for the sampling capacitor when the ADC is in its acquisition phase. R2 represents the source impedance of a buffer amplifier or resistive network, R1 is an internal multiplexer resistance, and C1 is the sampling capacitor.

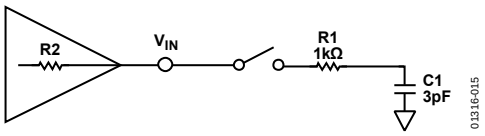

Figure 10. Equivalent Sampling Circuit

During the acquisition phase, the sampling capacitor must be charged to within a 1/2 LSB of its final value. The time it takes to charge the sampling capacitor (T_{CHARGE}) is given by

$$T_{CHARGE} = 7.6 \times (R2 + 1\ \text{k}\Omega) \times 3\ \text{pF}$$

For small values of source impedance, the settling time associated with the sampling circuit (100 ns) is, in effect, the acquisition time of the ADC. For example, with a source impedance (R2) of 10 Ω, the charge time for the sampling capacitor is approximately 23 ns. The charge time becomes significant for source impedances of 1 kΩ and greater.

AC Acquisition Time

In ac applications, it is recommended to always buffer analog input signals. The source impedance of the drive circuitry must be kept as low as possible to minimize the acquisition time of the ADC. Large values of source impedance cause the THD to degrade at high throughput rates.

ON-CHIP REFERENCE

The AD7817/AD7818 have an on-chip, 1.2 V band gap reference that is gained up to give an output of 2.5 V. By connecting the REF_{IN} pin to analog ground, the on-chip reference is selected. This selection causes SW1 to open and the reference amplifier to power up during a conversion (see Figure 11). Therefore, the on-chip reference is not available externally. An external 2.5 V reference can be connected to the REF_{IN} pin, which has the effect of shutting down the on-chip reference circuitry and reducing I_{DD} by approximately 0.25 mA.

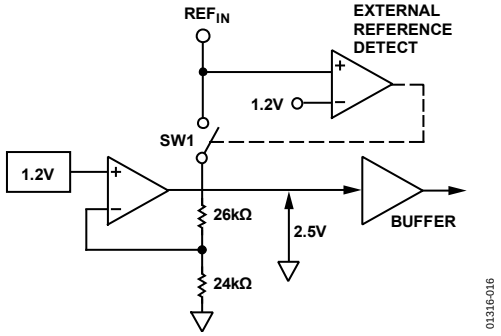

Figure 11. On-Chip Reference

ADC TRANSFER FUNCTION

The output coding of the AD7817/AD7818 is straight binary. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSBs, and so on). The LSB size is = 2.5 V/1024 = 2.44 mV. The ideal transfer characteristic is shown in Figure 12.

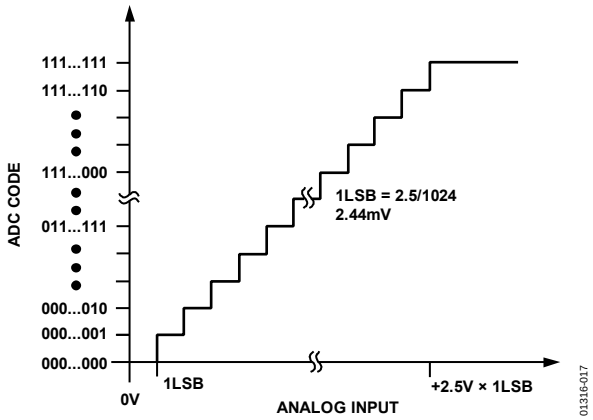

Figure 12. ADC Transfer Function

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TEMPERATURE MEASUREMENT

The on-chip temperature sensor can be accessed via multiplexer Channel 0, that is, by writing 0 0 0 to the channel address register. The temperature is also the power on default selection. The transfer characteristic of the temperature sensor is shown in Figure 13. The result of the 10-bit conversion on Channel 0 can be converted to degrees centigrade by the following:

$$T_{AMB} = -103°C + (ADC\ Code/4)$$

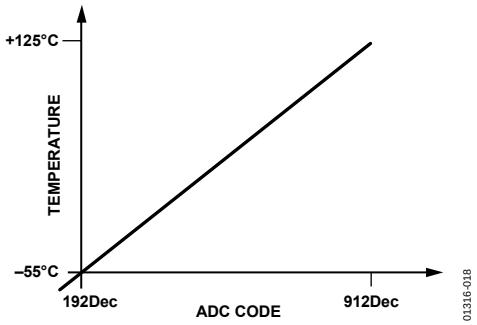

Figure 13. Temperature Sensor Transfer Characteristics

For example, if the result of a conversion on Channel 0 was 1000000000 (512 Dec), the ambient temperature is equal to −103°C + (512/4) = +25°C.

Table 7 shows some ADC codes for various temperatures.

Table 7. Temperature Sensor Output

ADC Code	Temperature
00 1100 0000	−55°C
01 0011 1000	−25°C
01 1001 1100	0°C
10 0000 0000	+25°C
10 0111 1000	+55°C
11 1001 0000	+125°C

TEMPERATURE MEASUREMENT ERROR DUE TO REFERENCE ERROR

The AD7817/AD7818 are trimmed using a precision 2.5 V reference to give the transfer function previously described. To show the effect of the reference tolerance on a temperature reading, the temperature sensor transfer function can be rewritten as a function of the reference voltage and the temperature.

$$CODE\ (DEC) = ([113.3285 \times K \times T]/[q \times V_{REF}] - 0.6646) \times 1024$$

where:
K = Boltzmann's Constant, 1.38×10^{-23}
q = charge on an electron, 1.6×10^{-19}
T = temperature (K)

So, for example, to calculate the ADC code at 25°C,

$$CODE = ([113.3285 \times 298 \times 1.38 \times 10^{-23}]/[1.6 \times 10^{-19} \times 2.5] - 0.6646) \times 1024$$

$$= 511.5\ (200\ Hex)$$

As can be seen from the expression, a reference error produces a gain error. This means that the temperature measurement error due to reference error will be greater at higher temperatures. For example, with a reference error of −1%, the measurement error at −55°C is 2.2 LSBs (+0.5°C) and 16 LSBs (+4°C) at +125°C.

SELF-HEATING CONSIDERATIONS

The AD7817/AD7818 have an analog-to-digital conversion function capable of a throughput rate of 100 kSPS. At this throughput rate, the AD7817/AD7818 consume between 4 mW and 6.5 mW of power. Because a thermal impedance is associated with the IC package, the temperature of the die rises as a result of this power dissipation. Figure 14 to Figure 16 show the self-heating effect in a 16-lead SOIC. Figure 14 and Figure 15 show the self-heating effect on a two-layer and four-layer PCB. The plots were generated by assembling a heater (resistor) and temperature sensor (diode) in the package being evaluated. In Figure 14, the heater (6 mW) is turned off after 30 sec. The PCB has little influence on the self-heating over the first few seconds after the heater is turned on. This can be more clearly seen in Figure 15 where the heater is switched off after 2 sec. Figure 16 shows the relative effects of self-heating in air, fluid, and thermal contact with a large heat sink.

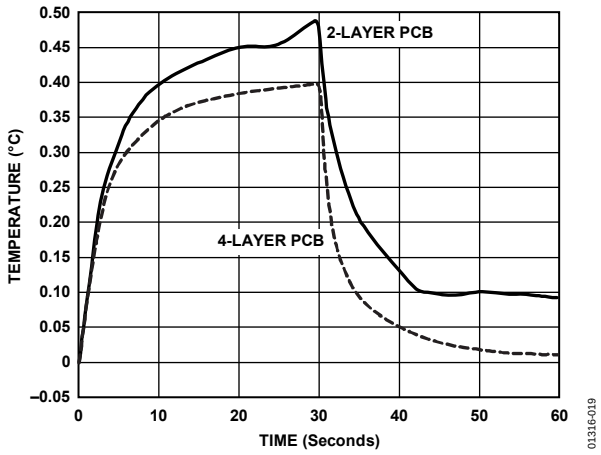

Figure 14. Self-Heating Effect 2-Layer and 4-Layer PCB with the Heater (6 mW) Turned Off After 30 sec

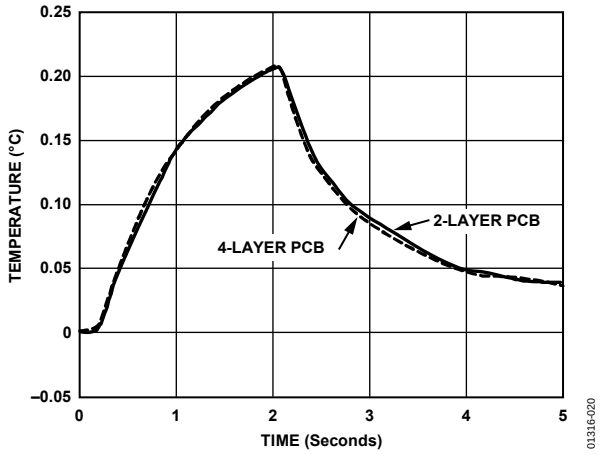

Figure 15. Self-Heating Effect 2-Layer and 4-Layer PCB with the Heater Switched Off After 2 sec

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Figure 16 represents the worst-case effects of self-heating. The heater delivered 6 mW to the interior of the package in all cases. This power level is equivalent to the ADC continuously converting at 100 kSPS. The effects of the self-heating can be reduced at lower ADC throughput rates by operating in Mode 2 (see Operating Modes section). When operating in this mode, the on-chip power dissipation reduces dramatically and, as a consequence, the self-heating effects.

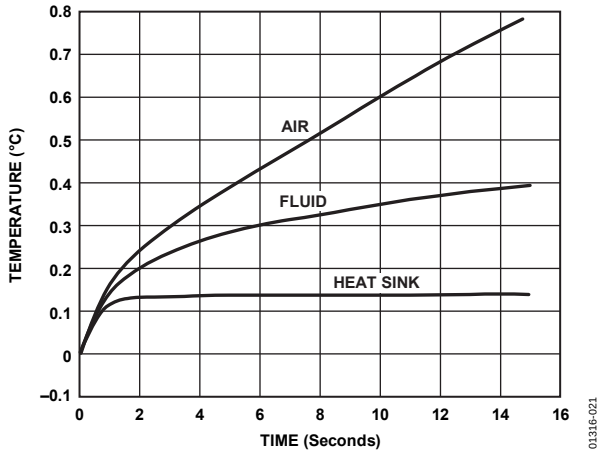

Figure 16. Self-Heating Effect in Air, Fluid, and Thermal Contact with a Heat Sink

OPERATING MODES

The AD7817/AD7818 have two possible modes of operation depending on the state of the $\overline{\text{CONVST}}$ pulse at the end of a conversion.

Mode 1

In this mode of operation, the $\overline{\text{CONVST}}$ pulse is brought high before the end of a conversion, that is, before BUSY goes low (see Figure 17). When operating in this mode, do not initiate a new conversion until 100 ns after the end of a serial read operation. This quiet time is to allow the track-and-hold to accurately acquire the input signal after a serial read.

Mode 2

In this mode of operation, AD7817/AD7818 automatically power down at the end of a conversion (see Figure 18). The $\overline{\text{CONVST}}$ is brought low to initiate a conversion and is left logic low until after the end of the conversion. At this point, that is, when BUSY goes low, the devices power down.

The devices are powered up again on the rising edge of the $\overline{\text{CONVST}}$ signal. Superior power performance can be achieved in this mode of operation by powering up the AD7817/AD7818 only to carry out a conversion (see the Power VS. Throughput section). In Figure 18, the $\overline{\text{CS}}$ line is applicable to the AD7817 only.

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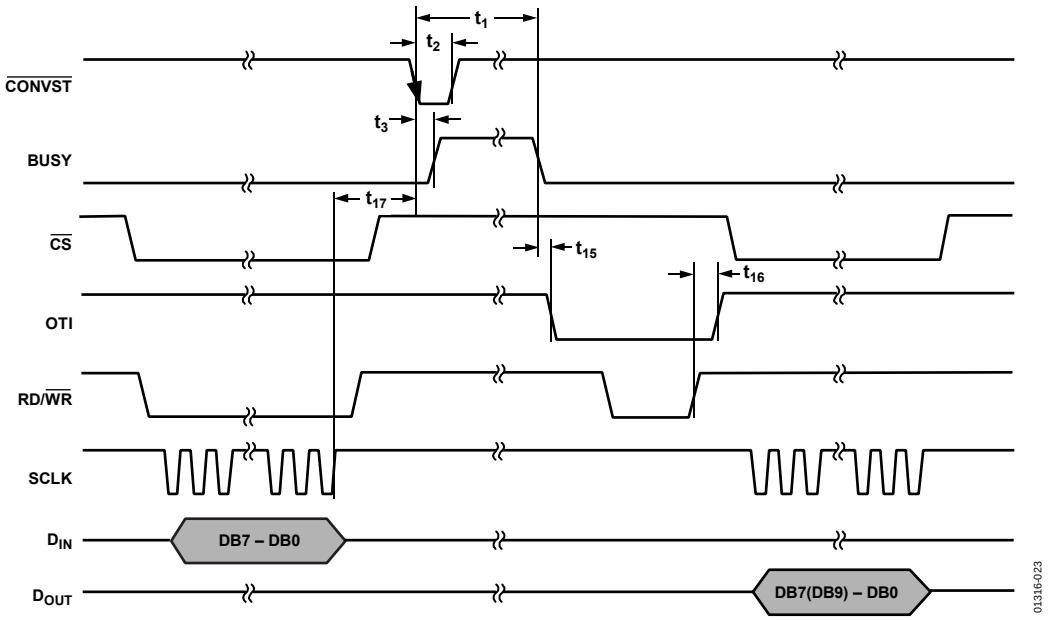

Figure 17. Mode 1 Operation

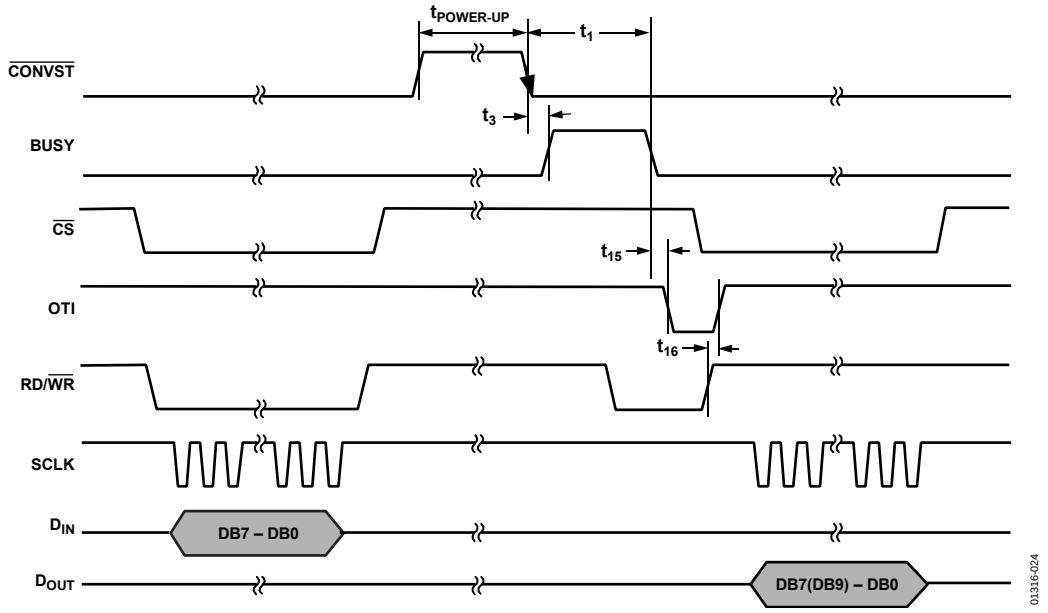

Figure 18. Mode 2 Operation

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POWER vs. THROUGHPUT

Superior power performance can be achieved by using the automatic power-down (Mode 2) at the end of a conversion (see the Operating Modes section).

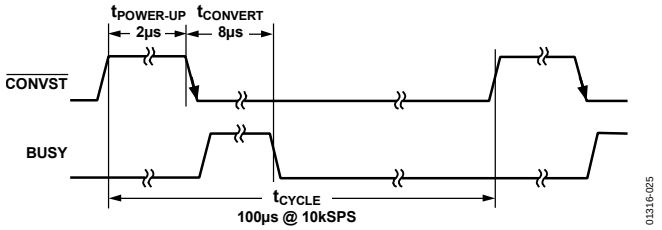

Figure 19. Automatic Power-Down

Figure 19 shows how the automatic power-down is implemented to achieve the optimum power performance from the AD7817 and AD7818. The devices operate in Mode 2, and the duration of $\overline{\text{CONVST}}$ pulse is set equal to the power-up time (2 µs). As the throughput rate of the device is reduced, the device remains in its power-down state longer, and the average power consumption over time drops accordingly.

For example, if the AD7817 operates in continuous sampling mode with a throughput rate of 10 kSPS, the power consumption is calculated as follows. The power dissipation during normal operation is 4.8 mW, V_{DD} = 3 V. If the power-up time is 2 µs, and the conversion time is 9 µs, the AD7817 can typically dissipate 4.8 mW for 11 µs (worst case) during each conversion cycle. If the throughput rate is 10 kSPS, the cycle time is 100 µs, and the power dissipated while powered up during each cycle is (11/100) × (4.8 mW) = 528 µW typical. Power dissipated while powered down during each cycle is (89/100) × (3 V × 2 µA) = 5.34 µW typ. Overall power dissipated is 528 µW + 5.34 µW = 533 µW.

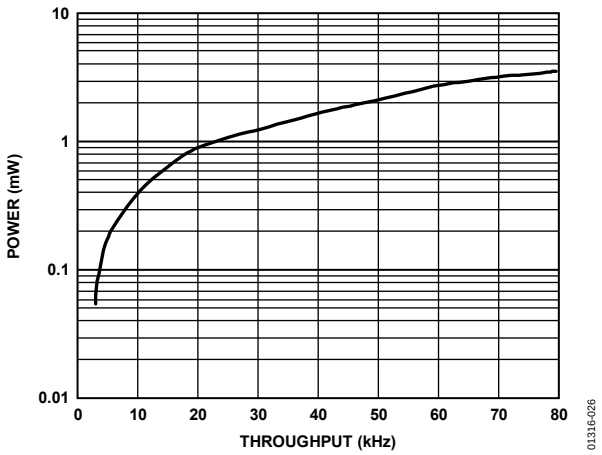

Figure 20. Power vs. Throughput Rate

AD7817 SERIAL INTERFACE

The serial interface on the AD7817 is a 5-wire interface that has read and write capabilities, with data being read from the output register via the D_{OUT} line and data being written to the control register via the D_{IN} line. The AD7817 operates in slave mode and requires an externally applied serial clock to the SCLK input to access data from the data register or write to the control byte. The RD/$\overline{\text{WR}}$ line is used to determine whether data is being written to or read from the AD7817. When data is being written to the AD7817, the RD/$\overline{\text{WR}}$ line is set logic low, and when data is being read from the device, the RD/$\overline{\text{WR}}$ line is set logic high (see Figure 21). The serial interface on the AD7817 is designed to allow the device to be interfaced to systems that provide a serial clock that is synchronized to the serial data, such as the 80C51, 87C51, 68HC11, 68HC05, and PIC16Cxx microcontrollers.

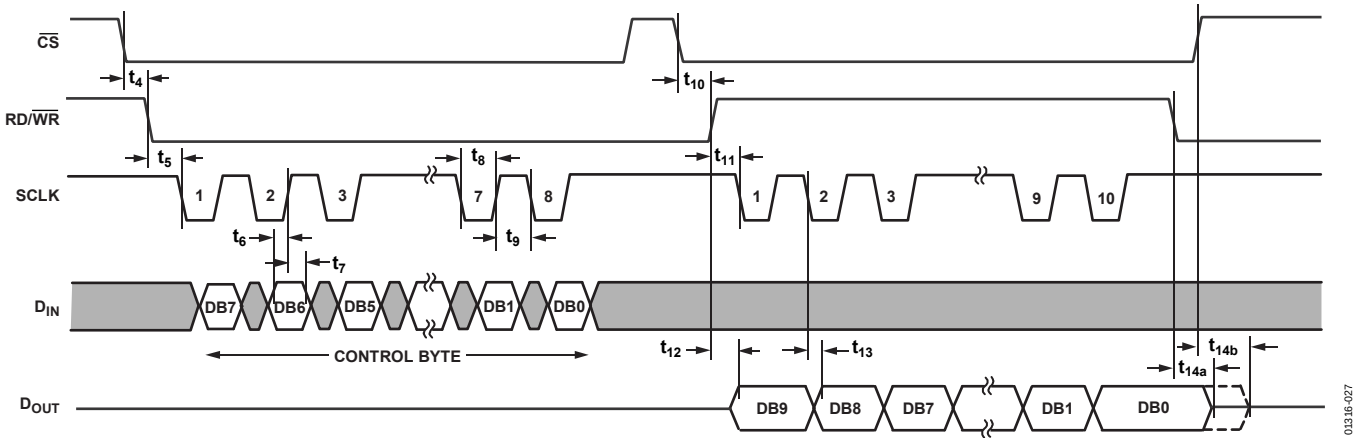

Figure 21. AD7817 Serial Interface Timing Diagram

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Read Operation

Figure 21 shows the timing diagram for a serial read from the AD7817. $\overline{CS}$ is brought low to enable the serial interface, and RD/$\overline{WR}$ is set logic high to indicate that the data transfer is a serial read from the AD7817. The rising edge of RD/$\overline{WR}$ clocks out the first data bit (DB9), subsequent bits are clocked out on the falling edge of SCLK (except for the first falling SCLK edge) and are valid on the rising edge. During a read operation, 10 bits of data are transferred. However, a choice is available to only clock eight bits if the full 10 bits of the conversion result are not required. The serial data can be accessed in a number of bytes if 10 bits of data are being read. However, RD/$\overline{WR}$ must remain high for the duration of the data transfer operation. Before starting a new data read operation, the RD/$\overline{WR}$ signal must be brought low and high again. At the end of the read operation, the D_{OUT} line enters a high impedance state on the rising edge of the $\overline{CS}$, or the falling edge of RD/$\overline{WR}$, whichever occurs first. The readback process is a destructive process, in that once data is read back, it is erased. A conversion must be done again; otherwise, no data is read back.

Write Operation

Figure 21 also shows the control byte write operation to the AD7817. The RD/$\overline{WR}$ input goes low to indicate to the device that a serial write is about to occur. The AD7817 control byte is loaded on the rising edge of the first eight clock cycles of the serial clock with data on all subsequent clock cycles being ignored. To carry out a second successive write operation, the RD/$\overline{WR}$ signal must be brought high and low again.

Simplifying the Serial Interface

To minimize the number of interconnect lines to the AD7817, connect the $\overline{CS}$ line to DGND. This is possible if the AD7817 is not sharing the serial bus with another device. It is also possible to tie the D_{IN} and D_{OUT} lines together. This arrangement is compatible with the 8051 microcontroller. The 68HC11, 68HC05, and PIC16Cxx can be configured to operate with a single serial data line. In this way, the number of lines required to operate the serial interface can be reduced to three, that is, RD/$\overline{WR}$, SCLK, and D_{IN}/D_{OUT} (see Figure 8).

AD7818 SERIAL INTERFACE MODE

The serial interface on the AD7818 is a 3-wire interface that has read and write capabilities. Data is read from the output register and the control byte is written to the AD7818 via the D_{IN}/D_{OUT} line. The AD7818 operates in slave mode and requires an externally applied serial clock to the SCLK input to access data from the data register or write to the control byte. The RD/$\overline{WR}$ line is used to determine whether data is being written to or read from the AD7818. When data is being written to the AD7818, the RD/$\overline{WR}$ line is set logic low, and when data is being read from the AD7818 the line is set logic high (see Figure 22). The serial interface on AD7818 is designed to allow the AD7818 to interface with systems that provide a serial clock that is synchronized to the serial data, such as the 80C51, 87C51, 68HC11, 68HC05, and PIC16Cxx microcontrollers.

Read Operation

Figure 22 shows the timing diagram for a serial read from the AD7818. The RD/$\overline{WR}$ is set logic high to indicate that the data transfer is a serial read from the devices. When RD/$\overline{WR}$ is logic high, the D_{IN}/D_{OUT} pin becomes a logic output, and the first data bit (DB9) appears on the pin. Subsequent bits are clocked out on the falling edge of SCLK, starting with the second SCLK falling edge after RD/$\overline{WR}$ goes high, and are valid on the rising edge of SCLK. Ten bits of data are transferred during a read operation. However, a choice is available to only clock eight bits if the full 10 bits of the conversion result are not required. The serial data can be accessed in a number of bytes if 10 bits of data are being read. However, RD/$\overline{WR}$ must remain high for the duration of the data transfer operation. To carry out a successive read operation, the RD/$\overline{WR}$ pin must be brought logic low and high again. At the end of the read operation, the D_{IN}/D_{OUT} pin becomes a logic input on the falling edge of RD/$\overline{WR}$.

Write Operation

A control byte write operation to the AD7818 is also shown in Figure 22. The RD/$\overline{WR}$ input goes low to indicate to the device that a serial write is about to occur. The AD7818 control bytes are loaded on the rising edge of the first eight clock cycles of the serial clock with data on all subsequent clock cycles being ignored. To carry out a successive write to the AD7818 the RD/$\overline{WR}$ pin must be brought logic high and low again.

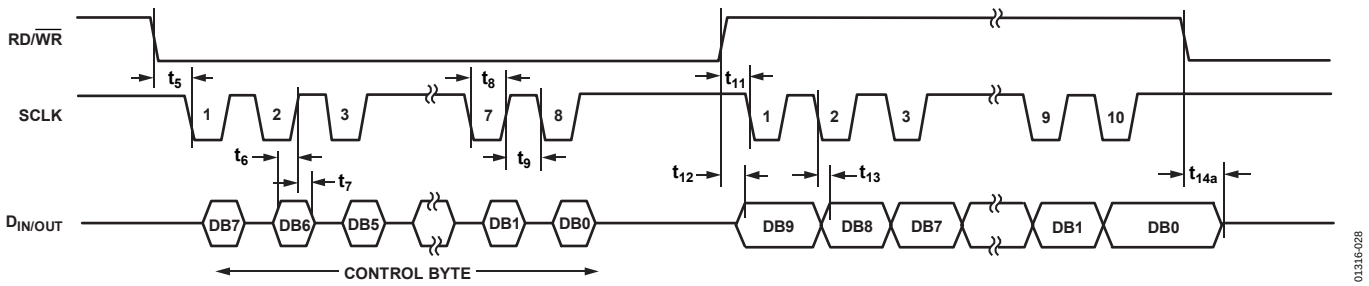

Figure 22. AD7818 Serial Interface Timing Diagram

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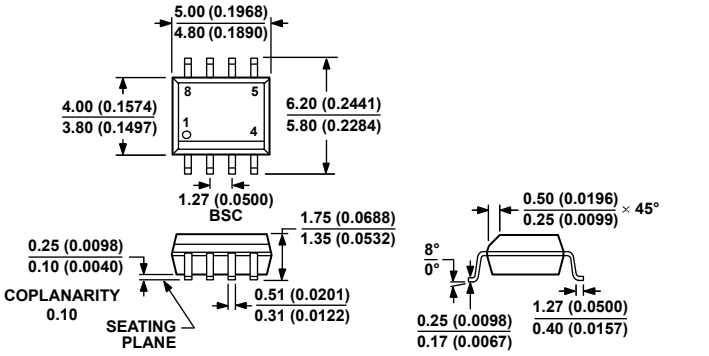
OUTLINE DIMENSIONS

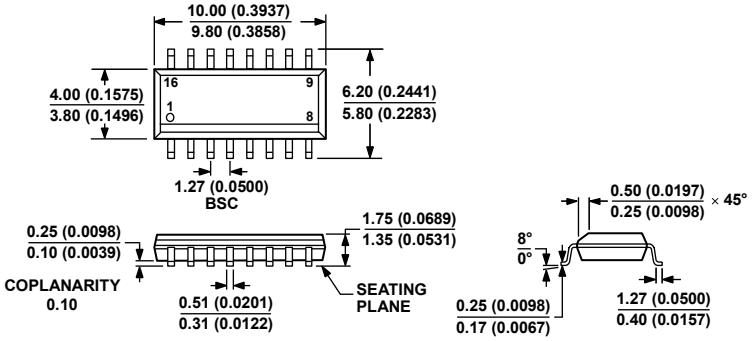


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 23. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

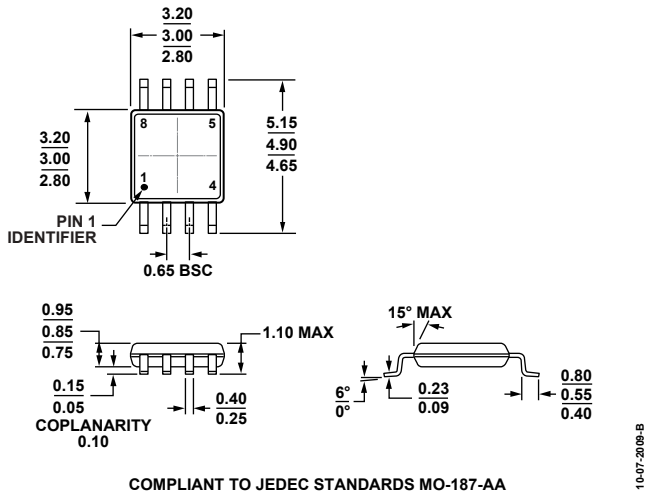


COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 24. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 25.8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

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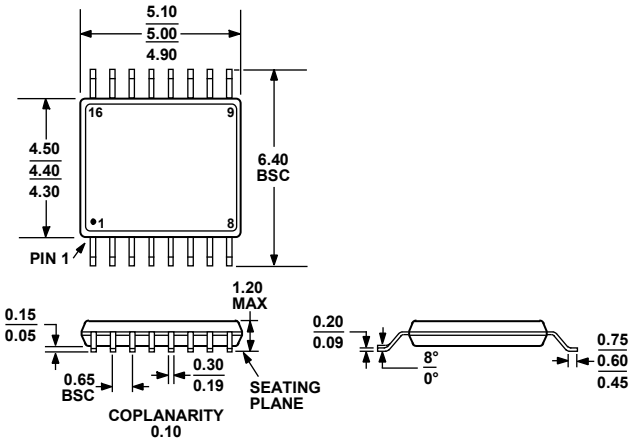

Figure 26. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Temperature Error at 25°C	Package Description	Package Option	Branding
AD7817ARZ	−40°C to +85°C	±2°C	16-Lead SOIC_N	R-16	
AD7817ARZ-REEL7	−40°C to +85°C	±2°C	16-Lead SOIC_N	R-16	
AD7817ARU	−40°C to +85°C	±2°C	16-Lead TSSOP	RU-16	
AD7817ARU-REEL7	−40°C to +85°C	±2°C	16-Lead TSSOP	RU-16	
AD7817ARUZ	−40°C to +85°C	±2°C	16-Lead TSSOP	RU-16	
AD7817ARUZ-REEL7	−40°C to +85°C	±2°C	16-Lead TSSOP	RU-16	
AD7817BRZ	−40°C to +85°C	±2°C	16-Lead SOIC_N	R-16	
AD7817BRZ-REEL	−40°C to +85°C	±2°C	16-Lead SOIC_N	R-16	
AD7817BRZ-REEL7	−40°C to +85°C	±2°C	16-Lead SOIC_N	R-16	
AD7817BRU	−40°C to +85°C	±1°C	16-Lead TSSOP	RU-16	
AD7817BRU-REEL7	−40°C to +85°C	±1°C	16-Lead TSSOP	RU-16	
AD7817BRUZ	−40°C to +85°C	±1°C	16-Lead TSSOP	RU-16	
AD7817BRUZ-REEL	−40°C to +85°C	±1°C	16-Lead TSSOP	RU-16	
AD7817BRUZ-REEL7	−40°C to +85°C	±1°C	16-Lead TSSOP	RU-16	
AD7817SR	−40°C to +85°C	±2°C	16-Lead SOIC_N	R-16	
AD7818ARZ-REEL7	−40°C to +85°C	±2°C	8-Lead SOIC_N	R-8	
AD7818ARM	−40°C to +85°C	±2°C	8-Lead MSOP	RM-8	C3A
AD7818ARMZ	−40°C to +85°C	±2°C	8-Lead MSOP	RM-8	T1P
AD7818ARMZ-REEL	−40°C to +85°C	±2°C	8-Lead MSOP	RM-8	T1P
AD7818ARMZ-REEL7	−40°C to +85°C	±2°C	8-Lead MSOP	RM-8	T1P

[1] Z = RoHS Compliant Part.

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