AD7680* Product Page Quick Links

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- AD7680: 3 mW, 100 kSPS,16-Bit ADC in 6-Lead SOT-23 Data Sheet

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- Lowest-Power 16-Bit ADC Optimizes Portable Designs (eeProductCenter, 10/4/2006)

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- MS-2210: Designing Power Supplies for High Speed ADC

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REVISION HISTORY

5/11—Rev. 0 to Rev. A

Deleted the Evaluating the AD7680 Performance Section 19
Changes to Ordering Guide 21

1/04—Revision 0: Initial Version

SPECIFICATIONS[1]

Table 2. V_{DD} = 4.5 V to 5.5 V, f_{SCLK} = 2.5 MHz, f_{SAMPLE} = 100 kSPS, unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted

Parameter	A, B Versions[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 10 kHz sine wave
Signal-to-Noise + Distortion (SINAD)[2]	83	dB min	
	85	dB typ	
Signal-to-Noise Ratio (SNR)[2]	84	dB min	
	86	dB typ	
Total Harmonic Distortion (THD)[2]	−97	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	−95	dB typ	
Intermodulation Distortion (IMD)[2]			
Second-Order Terms	−94	dB typ	
Third-Order Terms	−100	dB typ	
Aperture Delay	20	ns max	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	8	MHz typ	@ −3 dB
	2.2	MHz typ	@ −0.1 dB
DC ACCURACY			
No Missing Codes	15	Bits typ	
Integral Nonlinearity[2]	±4	LSB typ	
Offset Error[2]	±1.68	mV max	
Gain Error[2]	±0.038	% FS max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±0.3	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.8	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±0.3	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[2, 3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±0.3	µA max	
Floating-State Output Capacitance[2, 3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	8	µs max	20 SCLK cycles with SCLK at 2.5 MHz
	9.6	µs max	24 SCLK cycles with SCLK at 2.5 MHz
Track-and-Hold Acquisition Time	1.5	µs max	
	400	ns max	Sine wave input ≤ 10 kHz
Throughput Rate	100	kSPS	See the Serial Interface section
POWER REQUIREMENTS			
V_{DD}	4.5/5.5	V min/V max	
I_{DD}			Digital I/P_S = 0 V or V_{DD}
Normal Mode (Static)	5.2	mA max	SCLK on or off. V_{DD} = 5.5 V
Normal Mode (Operational)	4.8	mA max	f_{SAMPLE} = 100 kSPS. V_{DD} = 5.5 V; 3.3 mA typ
Full Power-Down Mode	0.5	µA max	SCLK on or off. V_{DD} = 5.5 V
Power Dissipation[4]			V_{DD} = 5.5 V
Normal Mode (Operational)	26.4	mW max	f_{SAMPLE} = 100 kSPS
Full Power-Down	2.75	µW max	

[1] Temperature range as follows: B Version: −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] See the Power vs. Throughput Rate section.

SPECIFICATIONS[1]

Table 3. V_{DD} = 2.5 V to 4.096 V, f_{SCLK} = 2.5 MHz, f_{SAMPLE} = 100 kSPS, unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 10 kHz sine wave
Signal-to-Noise + Distortion (SINAD)[2]	83	83	dB min	V_{DD} = 4.096 V
	82	82	dB min	V_{DD} = 2.5 V to 3.6 V
	86	86	dB typ	
Signal-to-Noise Ratio (SNR)[2]	84	84	dB min	V_{DD} = 4.096 V
	83	83	dB min	V_{DD} = 2.5 V to 3.6 V
	86	86	dB typ	
Total Harmonic Distortion (THD)[2]	−98	−98	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	−95	−99	dB typ	
Intermodulation Distortion (IMD)[2]				
Second-Order Terms	−94	−94	dB typ	
Third-Order Terms	−100	−100	dB typ	
Aperture Delay	20	10	ns max	
Aperture Jitter	30	30	ps typ	
Full Power Bandwidth	7	7	MHz typ	@ −3 dB; V_{DD} = 4.096 V
	5	5	MHz typ	@ −3 dB; V_{DD} = 2.5 V to 3.6 V
	2	2	MHz typ	@ −0.1 dB; V_{DD} = 4.096 V
	1.6	1.6	MHz typ	@ −0.1 dB; V_{DD} = 2.5 V to 3.6 V
DC ACCURACY				
No Missing Codes	14	15	Bits min	
Integral Nonlinearity[2]	±3.5	±3.5	LSB max	V_{DD} = 4.096 V
	±3	±3	LSB max	V_{DD} = 2.5 V to 3.6 V
Offset Error[2]	±1.25	±1.25	mV max	V_{DD} = 4.096 V
	±1.098	±1.098	mV max	V_{DD} = 2.5 V to 3.6 V
Gain Error[2]	±0.038	±0.038	% FS max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±0.3	±0.3	µA max	
Input Capacitance	30	30	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±0.3	±0.3	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[2, 3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} − 0.2	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±0.3	±0.3	µA max	
Floating-State Output Capacitance[2, 3]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	8	8	µs max	20 SCLK cycles with SCLK at 2.5 MHz
	9.6	9.6	µs max	24 SCLK cycles with SCLK at 2.5 MHz
Track-and-Hold Acquisition Time	1.5	1.5	µs max	Full-scale step input
	400	400	ns max	Sine wave input ≤ 10 kHz
Throughput Rate	100	100	kSPS	See the Serial Interface section

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	2.5/4.096	2.5/4.096	V min/max	
I_{DD}				Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2.8	2.8	mA max	SCLK on or off; V_{DD} = 4.096 V
	2	2	mA max	SCLK on or off; V_{DD} = 3.6 V
Normal Mode (Operational)	2.6	2.6	mA max	f_{SAMPLE} = 100 kSPS; V_{DD} = 4.096 V; 1.75 mA typ
	1.9	1.9	mA max	f_{SAMPLE} = 100 kSPS; V_{DD} = 3.6 V; 1.29 mA typ
Full Power-Down Mode	0.3	0.3	µA max	SCLK on or off
Power Dissipation[4]				
Normal Mode (Operational)	10.65	10.65	mW max	f_{SAMPLE} = 100 kSPS; V_{DD} = 4.096 V
	6.84	6.84	mW max	f_{SAMPLE} = 100 kSPS; V_{DD} = 3.6 V
	3	3	mW typ	V_{DD} = 2.5 V
Full Power-Down	1.23	1.23	µW max	V_{DD} = 4.096V
	1.08	1.08	µW max	V_{DD} = 3.6 V

[1] Temperature range as follows: A, B Versions: –40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS[1]

Table 4. V_{DD} = 2.5 V to 5.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

	Limit at T_{MIN}, T_{MAX}			
Parameter	**3 V**	**5 V**	**Unit**	**Description**
f_{SCLK}[2]	250	250	kHz min	
	2.5	2.5	MHz max	
$t_{CONVERT}$	20 × t_{SCLK}	20 × t_{SCLK}	min	
t_{QUIET}	100	100	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_1	10	10	ns min	Minimum $\overline{CS}$ pulse width
t_2	10	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[3]	48	35	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
t_4[3]	120	80	ns max	Data access time after SCLK falling edge
t_5	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_7	10	10	ns min	SCLK to data valid hold time
t_8[4]	45	35	ns max	SCLK falling edge to SDATA high impedance
$t_{POWER-UP}$[5]	1	1	µs typ	Power up time from full power-down

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[4] t_8 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[5] See Power vs. Throughput Rate section.

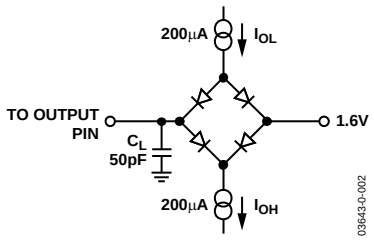

Figure 2. Load Circuit for Digital Output Timing Specification

ABSOLUTE MAXIMUM RATINGS

Table 5. T_A = 25°C, unless otherwise noted.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOT-23 Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	229.6°C/W
θ_{JC} Thermal Impedance	91.99°C/W
MSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	205.9°C/W
θ_{JC} Thermal Impedance	43.74°C/W
Lead Temperature, Soldering	
Vapor Phase (60 secs)	215°C
Infared (15 secs)	220°C
ESD	2 kV

[1]Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

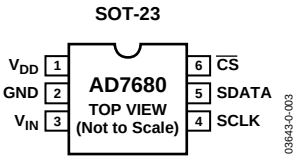

Figure 3. SOT-23 Pin Configuration

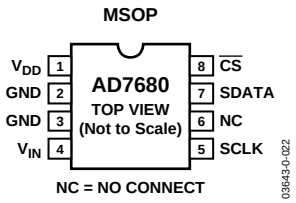

Figure 4. MSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No. SOT-23	Pin No. MSOP	Mnemonic	Function
1	1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7680 is from 2.5 V to 5.5 V.
2	2, 3	GND	Analog Ground. Ground reference point for all circuitry on the AD7680. All analog input signals should be referred to this GND voltage.
3	4	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to V_{DD}.
4	5	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from this part. This clock input is also used as the clock source for the AD7680's conversion process.
5	7	SDATA	Data Out. Logic output. The conversion result from the AD7680 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7680 consists of four leading zeros followed by 16 bits of conversion data that are provided MSB first. This will be followed by four trailing zeroes if $\overline{CS}$ is held low for a total of 24 SCLK cycles. See the Serial Interface section.
6	8	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7680 and framing the serial data transfer.
N/A	6	NC	No Connect. This pin should be left unconnected.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} − 1 LSB) after the offset error has been adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion. See the Serial Interface section for more details.

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2, excluding dc). The ratio depends on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to-(Noise + Distortion)} = (6.02\ N + 1.76)\ dB$$

Thus, for a 16-bit converter, this is 98 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7680, it is defined as

$$THD(dB) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at the sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa −2fb).

The AD7680 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5 shows a typical FFT plot for the AD7680 at 100 kSPS sample rate and 10 kHz input frequency. Figure 6 shows the signal-to-(noise + distortion) ratio performance versus the input frequency for various supply voltages while sampling at 100 kSPS with an SCLK of 2.5 MHz.

Figure 7 shows a graph of the total harmonic distortion versus the analog input frequency for various supply voltages, while Figure 8 shows a graph of the total harmonic distortion versus the analog input frequency for various source impedances (see the Analog Input section). Figure 9 and Figure 10 show the typical INL and DNL plots for the AD7680.

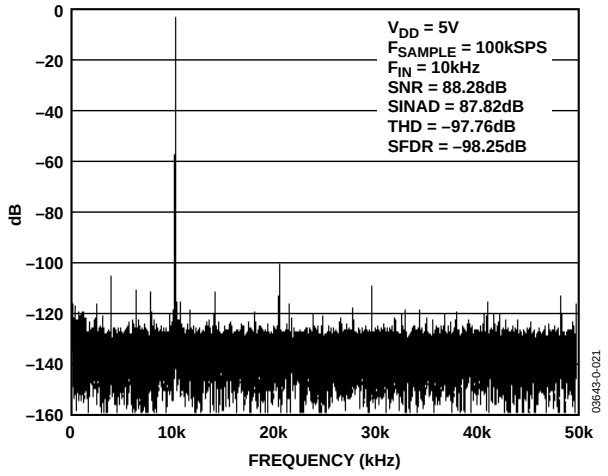

Figure 5. AD7680 Dynamic Performance at 100 kSPS

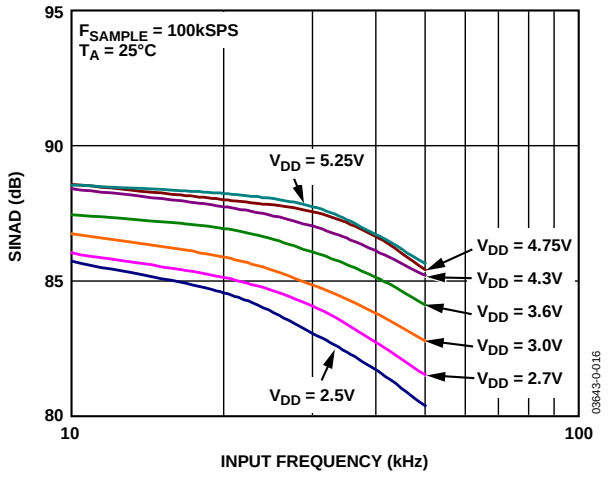

Figure 6. AD7680 SINAD vs. Analog Input Frequency for Various Supply Voltages at 100 kSPS

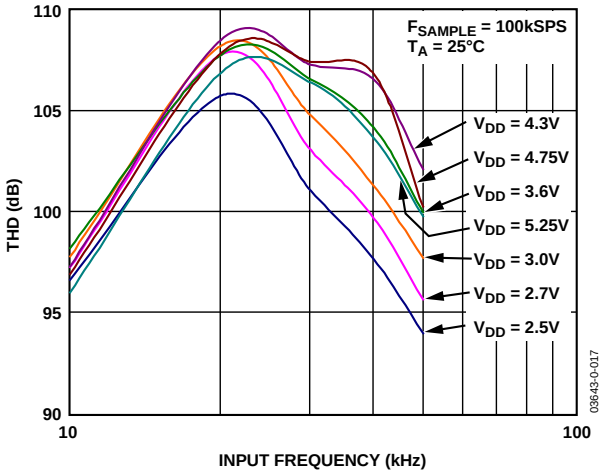

Figure 7. AD7680 THD vs. Analog Input Frequency for Various Supply Voltages at 100 kSPS

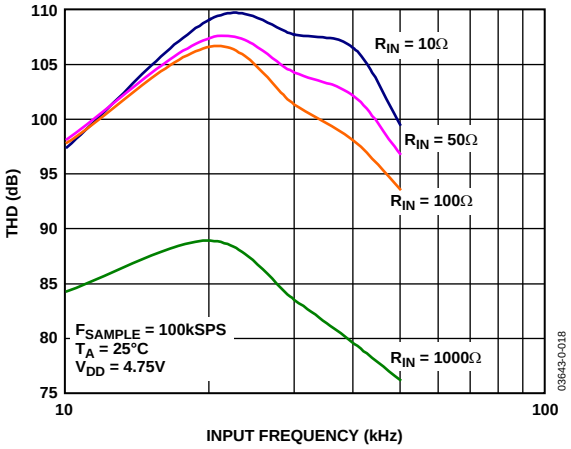

Figure 8. AD7680 THD vs. Analog Input Frequency for Various Source Impedances

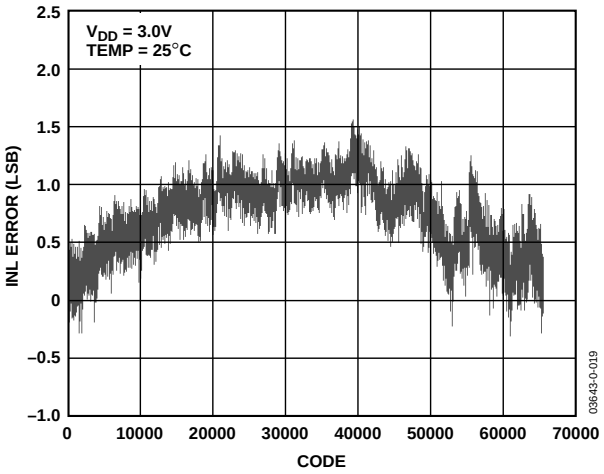

Figure 9. AD7680 Typical INL

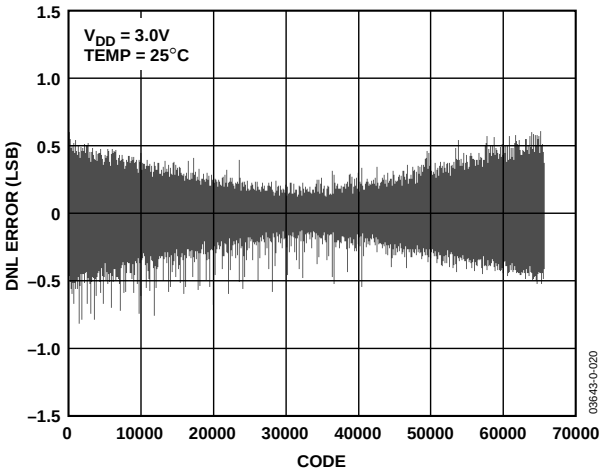

Figure 10. AD7680 Typical DNL

CIRCUIT INFORMATION

The AD7680 is a fast, low power, 16-bit, single-supply ADC. The part can be operated from a 2.5 V to 5.5 V supply and is capable of throughput rates of 100 kSPS when provided with a 2.5 MHz clock.

The AD7680 provides the user with an on-chip track-and-hold ADC and a serial interface housed in a tiny 6-lead SOT-23 package or in an 8-lead MSOP package, which offer the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part and also provides the clock source for the successive approximation ADC. The analog input range for the AD7680 is 0 V to V_{DD}. An external reference is not required for the ADC nor is there a reference on-chip. The reference for the AD7680 is derived from the power supply and thus gives the widest dynamic input range.

The AD7680 also features a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7680 is a 16-bit, successive approximation ADC based around a capacitive DAC. The AD7680 can convert analog input signals in the 0 V to V_{DD} range. Figure 11 and Figure 12 show simplified schematics of the ADC. The ADC comprises control logic, SAR, and a capacitive DAC. Figure 11 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected V_{IN} channel.

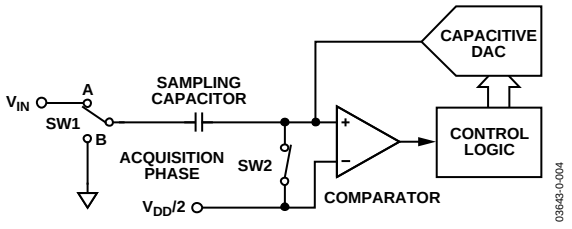

Figure 11. ADC Acquisition Phase

When the ADC starts a conversion, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced (Figure 12). The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code (see the ADC Transfer Function section).

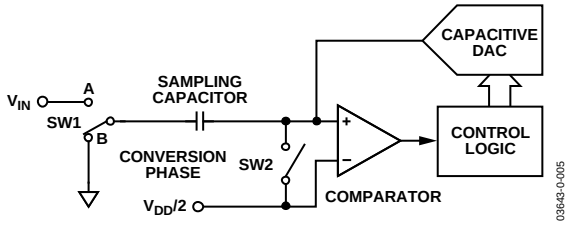

Figure 12. ADC Conversion Phase

ANALOG INPUT

Figure 13 shows an equivalent circuit of the analog input structure of the AD7680. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. This causes these diodes to become forward-biased and to start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 10 mA. Capacitor C1 in Figure 13 is typically about 5 pF and can be attributed primarily to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a track-and-hold switch. This resistor is typically about 25 Ω. Capacitor C2 is the ADC sampling capacitor and has a capacitance of 25 pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application. When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases, and performance degrades (see Figure 8).

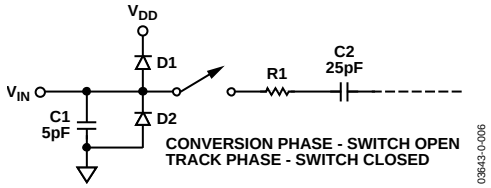

Figure 13. Equivalent Analog Input Circuit

ADC TRANSFER FUNCTION

The output coding of the AD7680 is straight binary. The designed code transitions occur at successive integer LSB values, i.e., 1 LSB, 2 LSBs. The LSB size is V_{DD}/65536. The ideal transfer characteristic for the AD7680 is shown in Figure 14.

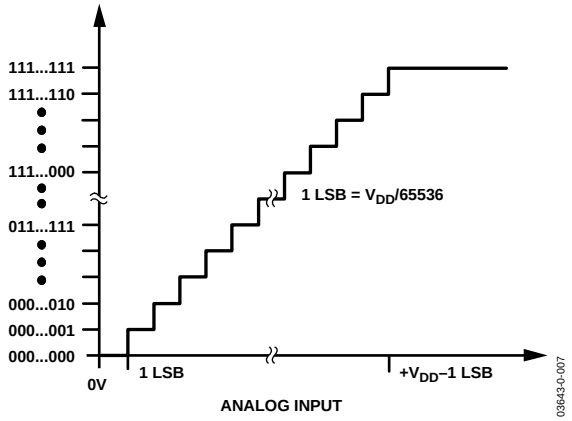

Figure 14. AD7680 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 15 shows a typical connection diagram for the AD7680. V_{REF} is taken internally from V_{DD} and as such should be well decoupled. This provides an analog input range of 0 V to V_{DD}. The conversion result is output in a 24-bit word, or alternatively, all 16 bits of the conversion result may be accessed using a minimum of 20 SCLKs. This 20-/24-bit data stream consists of a four leading zeros, followed by the 16 bits of conversion data, followed by four trailing zeros in the case of the 24 SCLK transfer. For applications where power consumption is of concern, the power-down mode should be used between conversions or bursts of several conversions to improve power performance (see the Modes of Operation section).

In fact, because the supply current required by the AD7680 is so low, a precision reference can be used as the supply source to the AD7680. For example, a REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) or an AD780 can be used to supply the required voltage to the ADC (see Figure 15). This configuration is especially useful if the power supply available is quite noisy, or if the system supply voltages are at some value other than the required operating voltage of the AD7680, e.g., 15 V. The REF19x or AD780 outputs a steady voltage to the AD7680. Recommended decoupling capacitors are a 100 nF low ESR ceramic (Farnell 335-1816) and a 10 µF low ESR tantalum (Farnell 197-130).

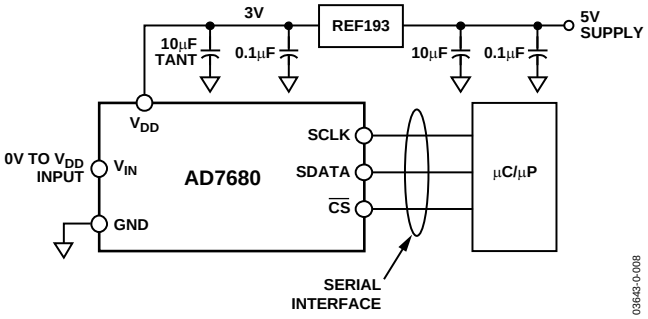

Figure 15. Typical Connection Diagram

Digital Inputs

The digital inputs applied to the AD7680 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the V_{DD} + 0.3 V limit as on the analog inputs. For example, if the AD7680 were operated with a V_{DD} of 3 V, 5 V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA still has 3 V logic levels when V_{DD} = 3 V.

Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If one of these digital inputs is applied before V_{DD}, then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to V_{DD}.

MODES OF OPERATION

The mode of operation of the AD7680 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, normal and power-down. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated determines whether or not the AD7680 enters power-down mode. Similarly, if the AD7680 is already in power-down, $\overline{CS}$ can control whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can optimize the power dissipation/throughput rate ratio for differing application requirements.

NORMAL MODE

This mode provides the fastest throughput rate performance, because the user does not have to worry about the power-up times with the AD7680 remaining fully powered all the time. Figure 16 shows the general diagram of the operation of the AD7680 in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge, but before the 20th SCLK falling edge, the part remains powered up, but the conversion is terminated and SDATA goes back into three-state. At least 20 serial clock cycles are required to complete the conversion and access the complete conversion result. In addition, a total of 24 SCLK cycles accesses four trailing zeros. $\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion, effectively idling $\overline{CS}$ low.

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

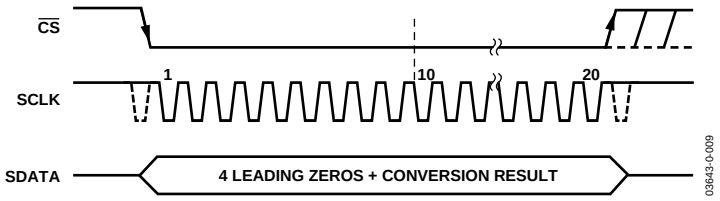

Figure 16. Normal Mode Operation

POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate, and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7680 is in power-down, all analog circuitry is powered down.

To enter power-down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK as shown in Figure 17. Once $\overline{CS}$ has been brought high in this window of SCLKs, the part enters power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and SDATA goes back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part remains in normal mode and will not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power up the AD7680 again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device is fully powered up once at least 16 SCLKs (or approximately 6 µs) have elapsed and valid data results from the next conversion as shown in Figure 18. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, regardless of the SCLK frequency, the AD7680 goes back into power-down again. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of 8 SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power-up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

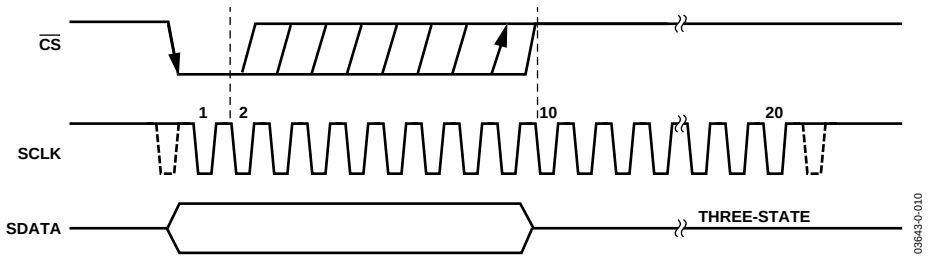

Figure 17. Entering Power-Down Mode

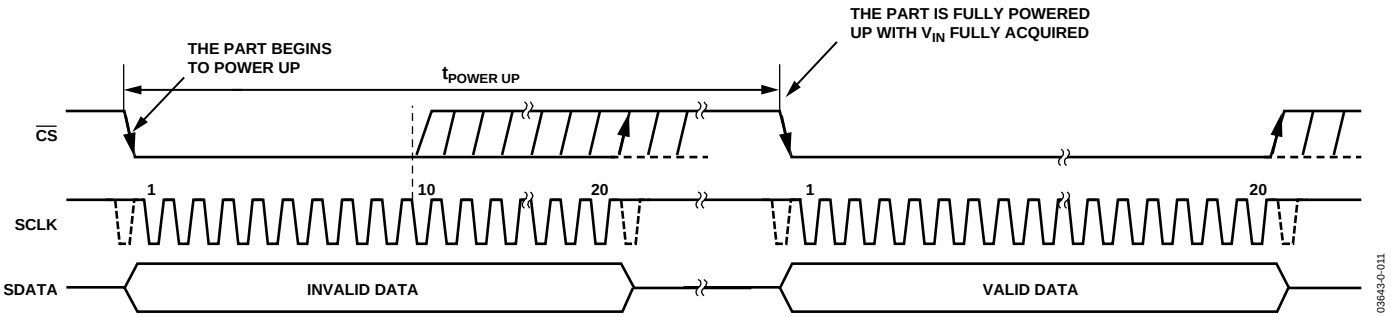

Figure 18. Exiting Power-Down Mode

POWER VS. THROUGHPUT RATE

By using the power-down mode on the AD7680 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 19 shows how as the throughput rate is reduced, the part remains in its shut-down state longer, and the average power consumption over time drops accordingly.

For example, if the AD7680 is operated in a continuous sampling mode, with a throughput rate of 10 kSPS and an SCLK of 2.5 MHz (V_{DD} = 3.6 V), and the device is placed in power-down mode between conversions, the power consumption is calculated as follows. The maximum power dissipation during normal operation is 6.84 mW (V_{DD} = 3.6 V). If the power-up time from power-down is 1 µs, and the remaining conversion time is 8 µs, (using a 20 SCLK transfer), then the AD7680 can be said to dissipate 6.84 mW for 9 µs during each conversion cycle. With a throughput rate of 10 kSPS, the cycle time is 100 µs.

For the remainder of the conversion cycle, 91 µs, the part remains in power-down mode. The AD7680 can be said to dissipate 1.08 µW for the remaining 91 µs of the conversion cycle. Therefore, with a throughput rate of 10 kSPS, the average power dissipated during each cycle is

(9/100) × (6.84 mW) + (91/100) × (1.08 µW) = 0.62 mW

Figure 19 shows the power dissipation versus the throughput rate when using the power-down mode with 3.6 V supplies, a 2.5 MHz SCLK, and a 20 SCLK serial transfer.

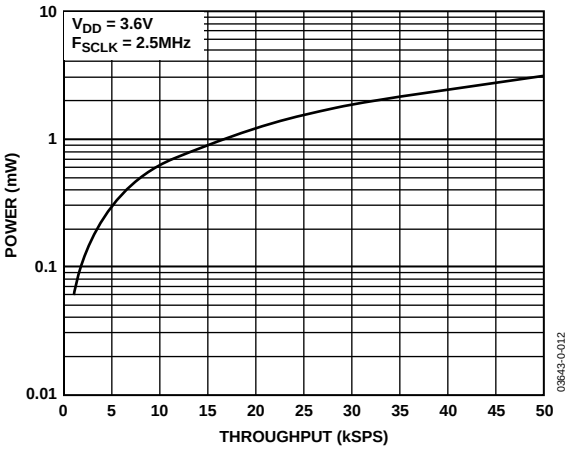

Figure 19. Power vs. Throughput Using Power-Down Mode with 20 SCLK Transfer at 3.6 V

SERIAL INTERFACE

Figure 20 shows the detailed timing diagram for serial interfacing to the AD7680. The serial clock provides the conversion clock and also controls the transfer of information from the AD7680 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, takes the bus out of three-state, and samples the analog input. The conversion is also initiated at this point and requires at least 20 SCLK cycles to complete. Once 17 SCLK falling edges have elapsed, the track-and-hold goes back into track mode on the next SCLK rising edge. Figure 20 shows a 24 SCLK transfer that allows a 100 kSPS throughput rate. On the 24th SCLK falling edge, the SDATA line goes back into three-state. If the rising edge of $\overline{CS}$ occurs before 24 SCLKs have elapsed, the conversion terminates and the SDATA line goes back into three-state; otherwise SDATA returns to three-state on the 24th SCLK falling edge as shown in Figure 20.

A minimum of 20 serial clock cycles are required to perform the conversion process and to access data from the AD7680. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the second leading zero; thus the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. If a 24 SCLK transfer is used as in Figure 20, the data transfer consists of four leading zeros followed by the 16 bits of data, followed by four trailing zeros. The final bit (fourth trailing zero) in the data transfer is valid on the 24th falling edge, having been clocked out on the previous (23rd) falling edge. If a 20 SCLK transfer is used as shown in Figure 21, the data output stream consists of only four leading zeros followed by 16 bits of data with the final bit valid on the 20th SCLK falling edge. A 20 SCLK transfer allows for a shorter cycle time and therefore a faster throughput rate is achieved.

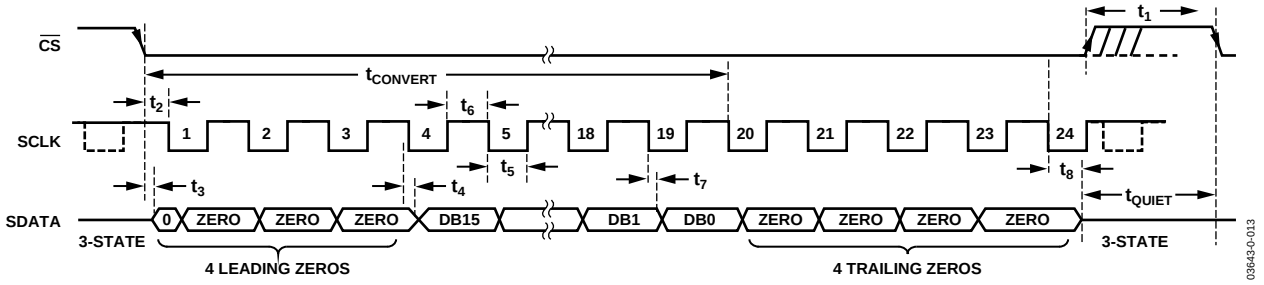

Figure 20. AD7680 Serial Interface Timing Diagram—24 SCLK Transfer

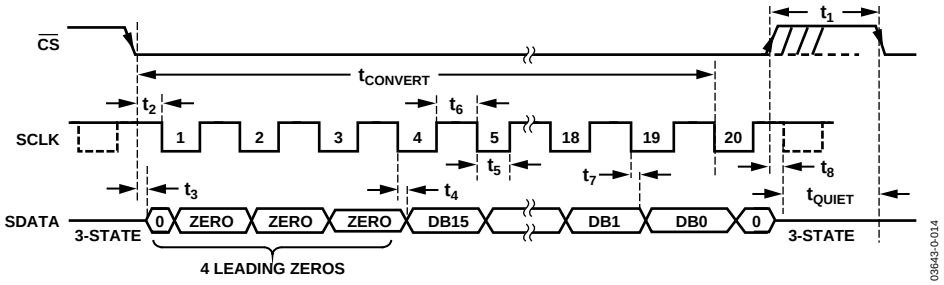

Figure 21. AD7680 Serial Interface Timing Diagram—20 SCLK Transfer

It is also possible to take valid data on each SCLK rising edge rather than falling edge, since the SCLK cycle time is long enough to ensure the data is ready on the rising edge of SCLK. However, the first leading zero is still driven by the $\overline{CS}$ falling edge, and so it can be taken on only the first SCLK falling edge. It may be ignored and the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the second leading zero provided and the 23rd rising SCLK edge would have the final trailing zero provided. This method may not work with most microcontrollers/DSPs but could possibly be used with FPGAs and ASICs.

AD7680 TO ADSP-218x

The ADSP-218x family of DSPs can be interfaced directly to the AD7680 without any glue logic required. The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing

INVRFS = INVTFS = 1, Active Low Frame Signal

DTYPE = 00, Right Justify Data

SLEN = 0111, 8-Bit Data-Words

ISCLK = 1, Internal Serial Clock

TFSR = RFSR = 0, Frame First Word

IRFS = 0

ITFS = 1

To implement the power-down mode, SLEN should be set to 0111 to issue an 8-bit SCLK burst. The connection diagram is shown in Figure 22. The ADSP-218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode and the SPORT control register is set up as described. Transmit and receive autobuffering is used in order to get a 24 SCLK transfer. Each buffer contains three 8-bit words. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$, and as with all signal processing applications, equidistant sampling is necessary. In this example, the timer interrupt is used to control the sampling rate of the ADC.

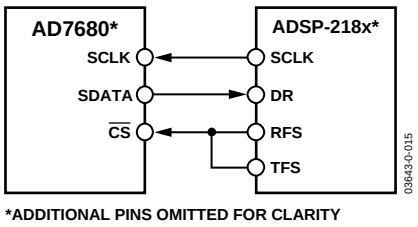

Figure 22. Interfacing to the ADSP-218x

The timer register is loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, the values in the transmit autobuffer start to be transmitted and TFS is generated. The TFS is used to control the RFS and therefore the reading of data. The data is stored in the receive autobuffer for processing or to be shifted later. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, i.e., TX0 = AX0, the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high again before transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

APPLICATION HINTS

GROUNDING AND LAYOUT

The printed circuit board that houses the AD7680 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes, because it gives the best shielding. Digital and analog ground planes should be joined at only one place. If the AD7680 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7680.

Avoid running digital lines under the device because these couple noise onto the die. The analog ground plane should be allowed to run under the AD7680 to avoid noise coupling. The power supply lines to the AD7680 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other, which reduces the effects of feedthrough on the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while the signals are placed on the solder side.

Good decoupling is also very important. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND, as discussed in the Typical Connection Diagram section. To achieve the best performance from these decoupling components, the user should attempt to keep the distance between the decoupling capacitors and the V_{DD} and GND pins to a minimum, with short track lengths connecting the respective pins.

OUTLINE DIMENSIONS

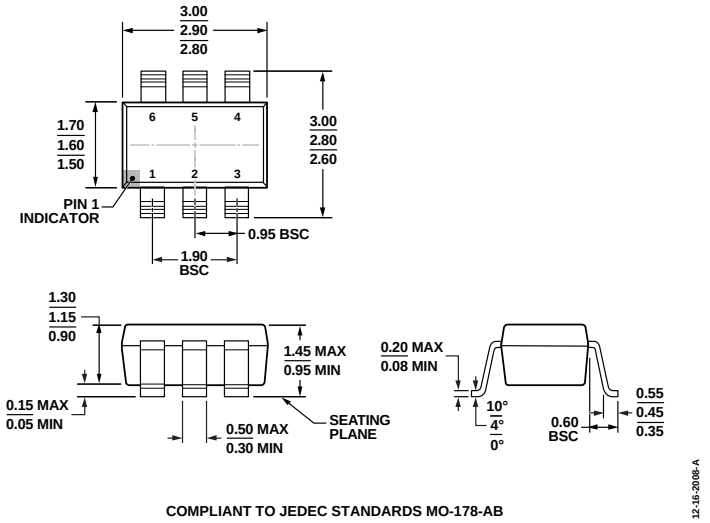

Figure 23. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6) Dimensions shown in millimeters

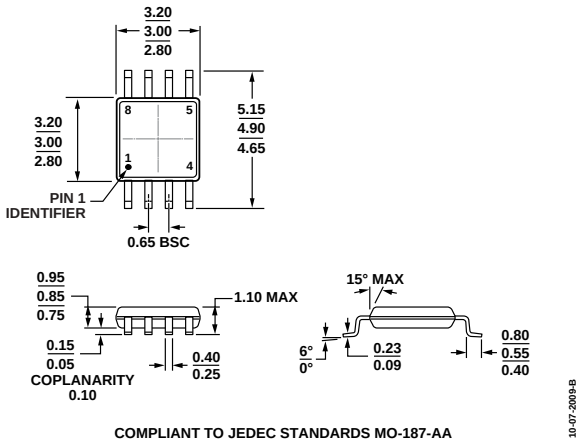

Figure 24. 8-Lead Micro Small Outline Package [MSOP] (RM-8) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error (LSB)[2]	Package Description	Package Option	Branding
AD7680ARJZ-REEL7	−40°C to +85°C	14 Bits Min	6-Lead Small Outline Transistor Package (SOT-23)	RJ-6	C40
AD7680ARM	−40°C to +85°C	14 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	CQA
AD7680ARM-REEL	−40°C to +85°C	14 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	CQA
AD7680ARM-REEL7	−40°C to +85°C	14 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	CQA
AD7680ARMZ	−40°C to +85°C	14 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	C40
AD7680BRJZ-R2	−40°C to +85°C	15 Bits Min	6-Lead Small Outline Transistor Package (SOT-23)	RJ-6	C3H
AD7680BRJZ-REEL7	−40°C to +85°C	15 Bits Min	6-Lead Small Outline Transistor Package (SOT-23)	RJ-6	C3H
AD7680BRM	−40°C to +85°C	15 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	CQB
AD7680BRM-REEL	−40°C to +85°C	15 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	CQB
AD7680BRM-REEL7	−40°C to +85°C	15 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	CQB
AD7680BRMZ	−40°C to +85°C	15 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	C3H
AD7680BRMZ-REEL	−40°C to +85°C	15 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	C3H
AD7680BRMZ-REEL7	−40°C to +85°C	15 Bits Min	8-Lead Mini Small Outline Package (MSOP)	RM-8	C3H

[1] Z = RoHS Compliant Part.
[2] Linearity error here refers to no missing codes.

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