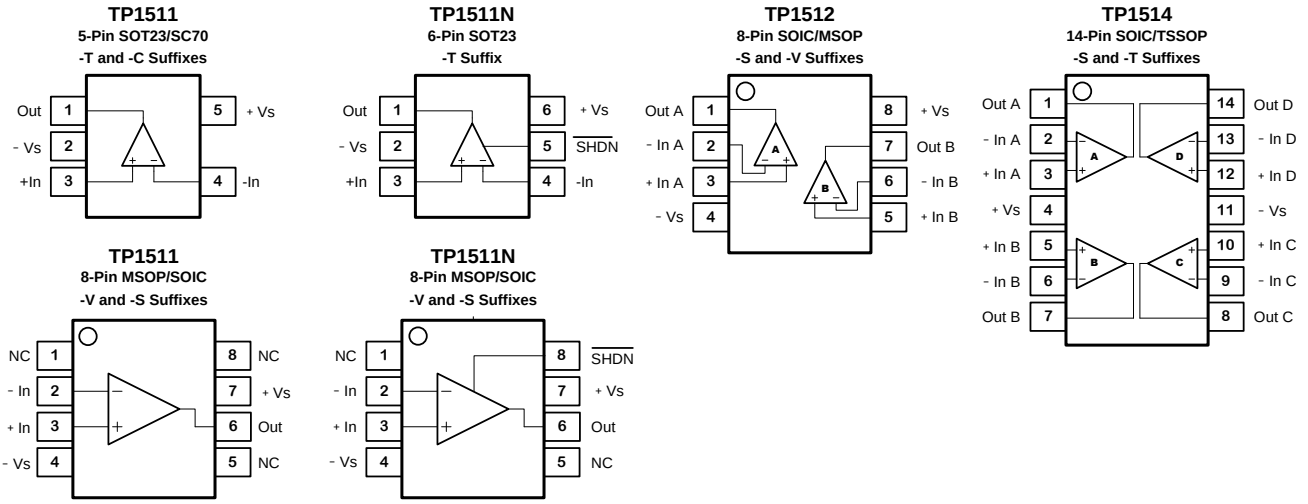
Stable 150kHz, 4μA, Rail-to-Rail, EveryCap™ Op Amps

Pin Configuration (Top View)



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP1511	TP1511-TR	5-Pin SOT23	Tape and Reel, 3000	A1TYW Note1
	TP1511-CR	5-Pin SC70	Tape and Reel, 3000	A1CYW Note1
TP1512	TP1512-SR	8-Pin SOIC	Tape and Reel, 4000	1512S
	TP1512-VR	8-Pin MSOP	Tape and Reel, 3000	1512S
TP1514	TP1514-SR	14-Pin SOIC	Tape and Reel, 2500	A14S
	TP1514-TR	14-Pin TSSOP	Tape and Reel, 3000	A14T

Note 1: 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ - V^-$.....6.0V
Input Voltage..... V^- – 0.5 to V^+ + 0.5
Input Current: +IN, –IN, SHDN Note 2..... ±10mA
SHDN Pin Voltage……V^- to V^+
Output Current: OUT..... ±40mA

Output Short-Circuit Duration Note 3..... Indefinite
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
MM	Machine Model ESD	JEDEC-EIA/JESD22-A115	500	V
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

5V Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 27°C. V_{SUPPLY} = 5V, V_{CM} = V_{OUT} = V_{SUPPLY}/2, R_L = 100KΩ, C_L =100pF, V_{SHDN} is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V_{SUPPLY}/2	●	-3.0	±0.2	+3.0	mV
V_{OS} TC	Input Offset Voltage Drift				0.6		μV/°C
I_B	Input Bias Current				1.0		pA
I_{OS}	Input Offset Current				1.0		pA
V_n	Input Voltage Noise	f = 0.1Hz to 10Hz			3.6		μV_{P-P}
e_n	Input Voltage Noise Density	f = 1kHz f = 10kHz			95 82		nV/√Hz
R_{IN}	Input Resistance			>100			GΩ
C_{IN}	Input Capacitance	Differential Common Mode			1.5 3.0		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.1V to 4.9V	●	80	110		dB
V_{CM}	Common-mode Input Voltage Range		●	V^--0.3		V_{DD}+0.3	V
PSRR	Power Supply Rejection Ratio		●	80	110		dB
A_{VOL}	Open-Loop Large Signal Gain	V_{OUT} = 2.5V, R_{LOAD}= 100kΩ	●	80	102		dB
		V_{OUT} = 0.1V to 4.9V, R_{LOAD}= 100kΩ	●	72	102		dB
V_{OL}, V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 100kΩ			5		mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f = 1kHz, I_{OUT} = 0			30		Ω
R_O	Open-Loop Output Impedance	f = 1kHz, 10kHz, I_{OUT} = 0			4		kΩ
I_{SC}	Output Short-Circuit Current	Sink or source current			40		mA
V_{DD}	Supply Voltage			2.1		6.0	V
I_Q	Quiescent Current per Amplifier		●		4	5.6	μA
$I_{Q(off)}$	Supply Current in Shutdown Note 1				0.1		μA
I_{SHDN}	Shutdown Pin Current Note 1	V_{SHDN} = 0.5V V_{SHDN} = 1.5V			-0.15 -0.15		μA
I_{LEAK}	Output Leakage Current in Shutdown Note1	V_{SHDN} = 0V, V_{OUT} = 0V V_{SHDN} = 0V, V_{OUT} = 5V			-20 20		pA
V_{IL}	SHDN Input Low Voltage Note 1	Disable	●			0.5	V
V_{IH}	SHDN Input High Voltage Note 1	Enable	●	1.0			V
t_{ON}	Turn-On Time Note 1	SHDN Toggle from 0V to 5V			20		μs
t_{OFF}	Turn-Off Time Note 1	SHDN Toggle from 5V to 0V			20		μs
PM	Phase Margin	R_{LOAD} = 100kΩ, C_{LOAD} = 100pF			67		°

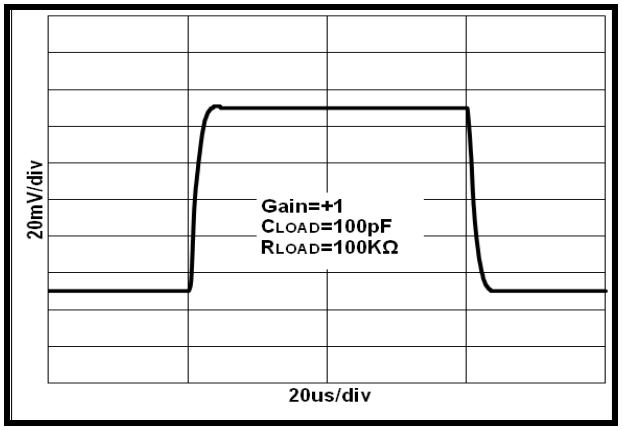
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GM	Gain Margin	R_{LOAD} = 100kΩ, C_{LOAD} = 100pF			-15		dB
GBWP	Gain-Bandwidth Product	f = 1kHz			150		kHz
t_{OV}	Overload Recovery Time	G = -10			15		μs
t_S	Settling Time, 1.5V to 3.5V, Unity Gain 0.1% 0.01% Settling Time, 2.45V to 2.55V, Unity Gain 0.1% 0.01%				 22 26 10 12		μs
SR	Slew Rate	A_V = 1, V_{OUT} = 1.5V to 3.5V, C_{LOAD} = 100pF, R_{LOAD} = 100kΩ			0.09		V/μs
FPBW	Full Power Bandwidth Note 2	$2V_{P-P}$			14		kHz
THD+N	Total Harmonic Distortion and Noise	f=0.1kHz, A_V=1, R_L=100kΩ, V_{OUT} = $2V_{PP}$ f=1kHz, A_V=1, R_L=100kΩ, V_{OUT} = $2V_{PP}$			 -94 -70		dB

Note 1: Specifications apply to the TP1511N with shutdown.

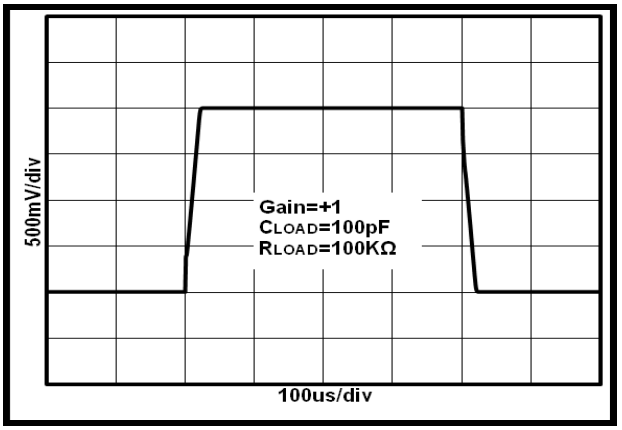
Note 2: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}.

Typical Performance Characteristics

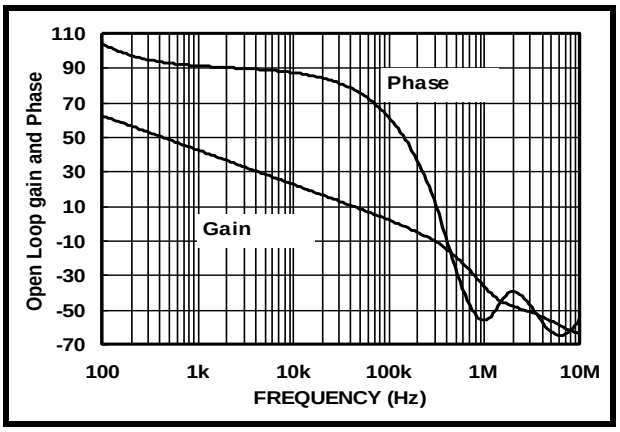
Small-Signal Step Response, 100mV Step



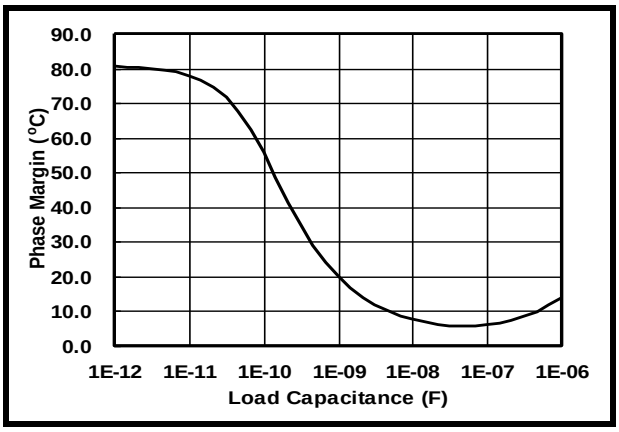
Large-Signal Step Response, 2V Step



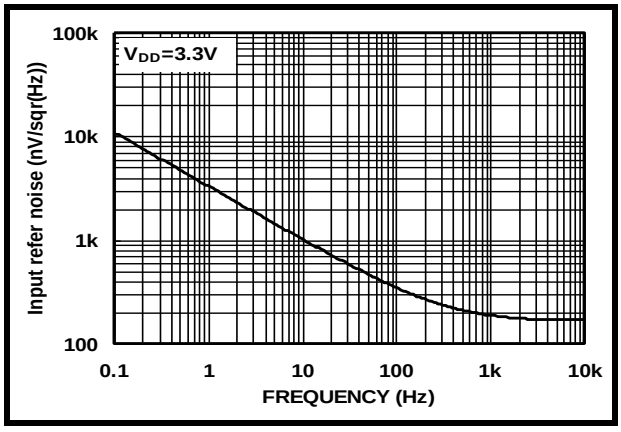
Open-Loop Gain and Phase



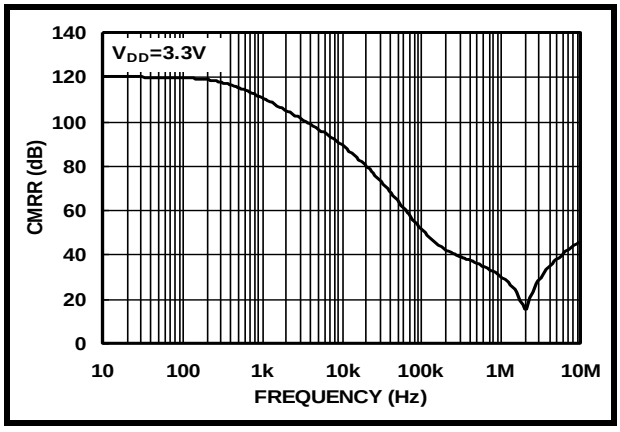
Phase Margin vs. C_{LOAD} (Stable for Any C_{LOAD})



Input Voltage Noise Spectral Density

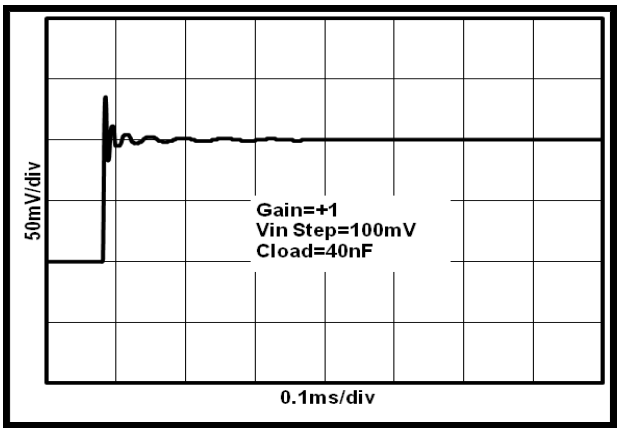


Common-Mode Rejection Ratio

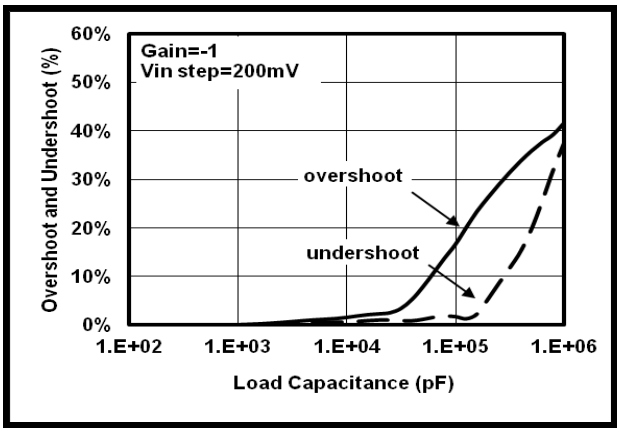


Typical Performance Characteristics

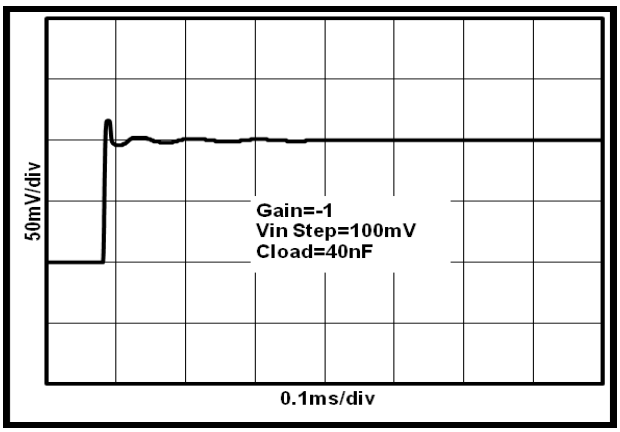
Over-Shoot Voltage, C_{LOAD} = 40nF, Gain = +1



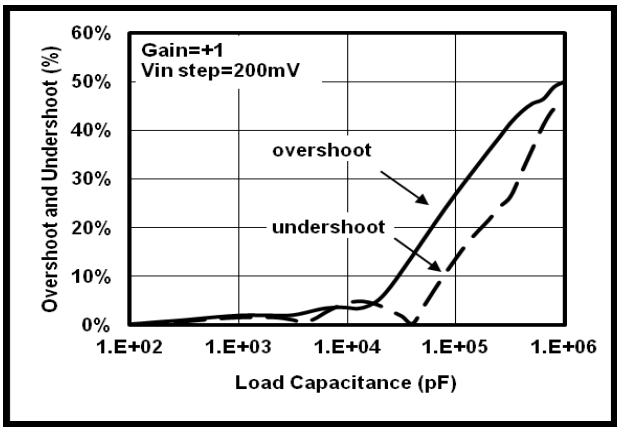
Over-Shoot % vs. C_{LOAD}, Gain = -1, RFB = 20kΩ



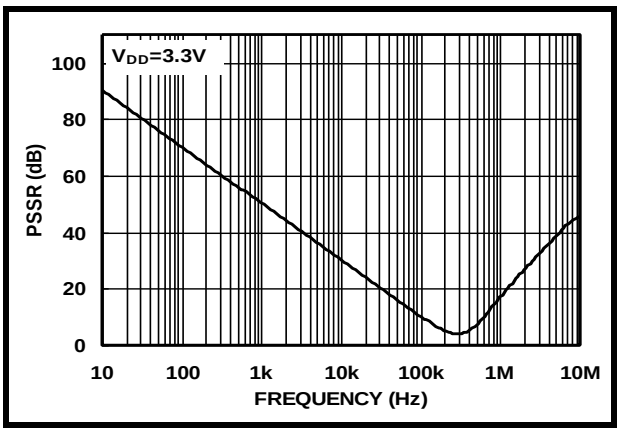
Over-Shoot Voltage, C_{LOAD}=40nF, Gain= -1, RFB=100kΩ



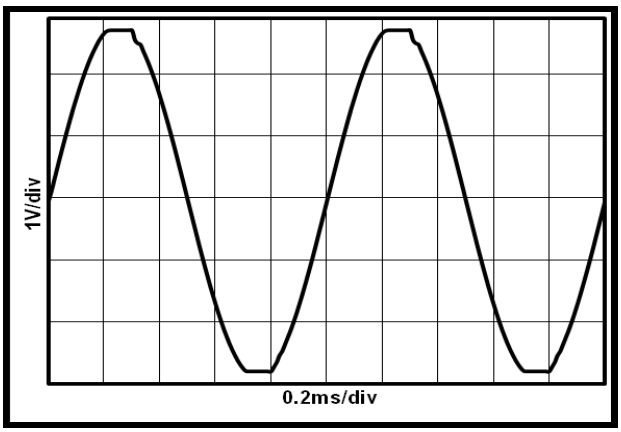
Small-Signal Over-Shoot % vs. C_{LOAD}, Gain = +1



Power-Supply Rejection Ratio

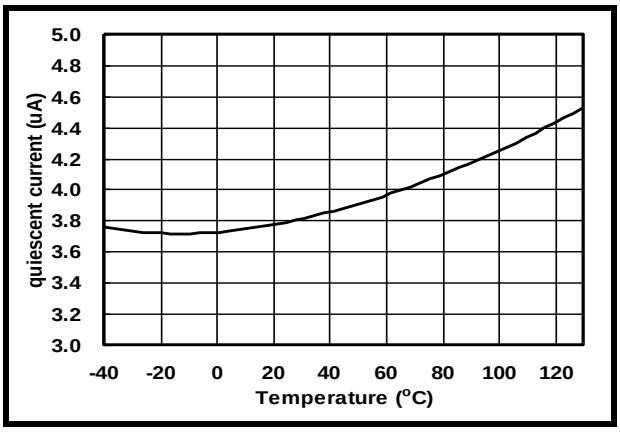


V_{IN} = -0.2V to 5.7V, No Phase Reversal

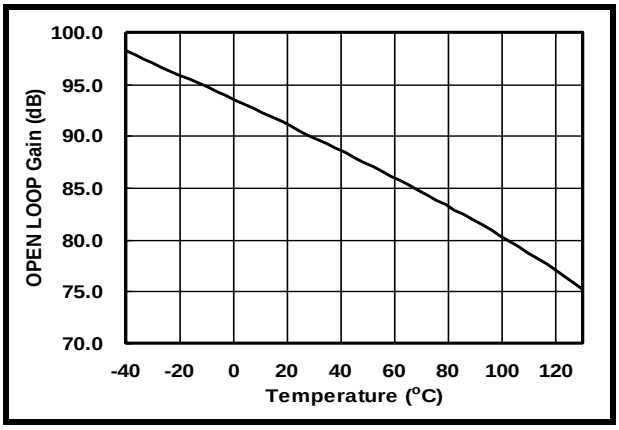


Typical Performance Characteristics

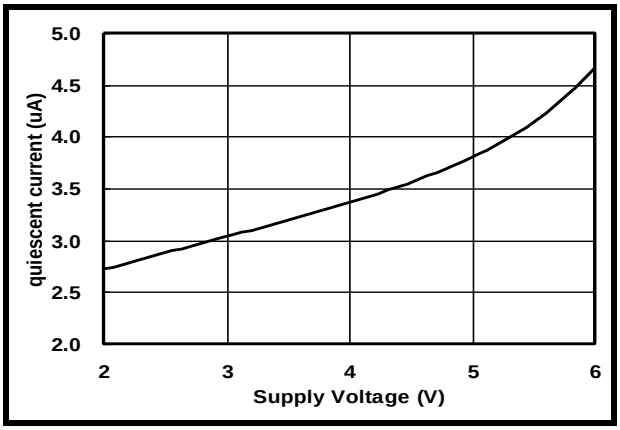
Quiescent Supply Current vs. Temperature



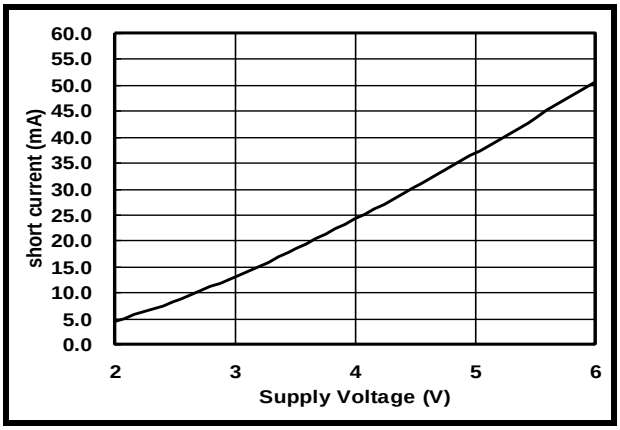
Open-Loop Gain vs. Temperature



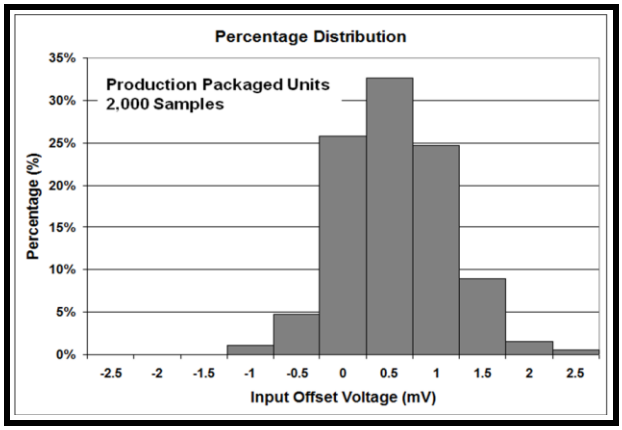
Quiescent Supply Current vs. Supply Voltage



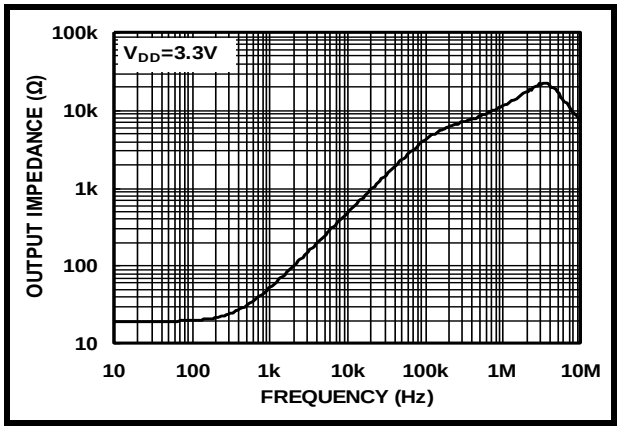
Short-Circuit Current vs. Supply Voltage



Input Offset Voltage Distribution

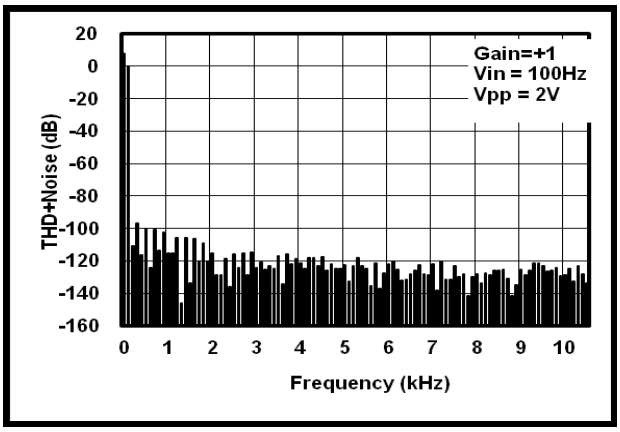


Closed-Loop Output Impedance vs. Frequency

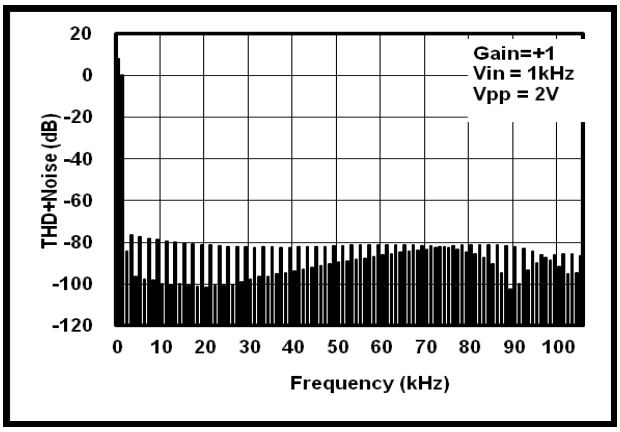


Typical Performance Characteristics

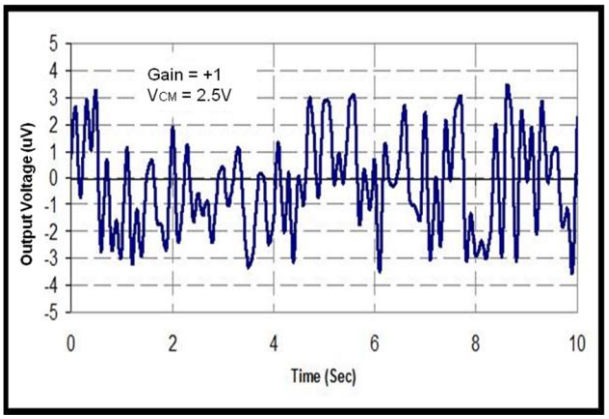
THD+Noise, Gain = +1, V_{IN} = 100Hz, V_{PP} = 2V



THD+Noise, Gain = +1, V_{IN} = 1kHz, V_{PP} = 2V



0.1Hz to 10Hz Time Domain Output Voltage Noise



Pin Functions

–IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- – 0.3V to V^+ + 0.3V.

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN.

+V_S: Positive Power Supply. Typically the voltage is from 2.1V to 5.25V. Split supplies are possible as long as the voltage between V+ and V– is between 2.1V and 5.25V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pins or between supply pins and ground.

N/C: No Connection.

-V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2.1V to 5.25V. If it is not connected to ground, bypass it with a capacitor of 0.1μF as close to the part as possible.

SHDN: Active **Low** Shutdown. Shutdown threshold is **1.0V** above negative supply rail. If unconnected, the amplifier is automatically enabled.

OUT: Amplifier Output. The voltage range extends to within millivolts of each supply rail.

Operation

The TP151x family input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is comprised of two CMOS differential amplifiers, a PMOS stage and NMOS stage that are active over different ranges of common mode input voltage. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

Low Supply Voltage and Low Power Consumption

The TP151x family of operational amplifiers can operate with power supply voltages from 2.1V to 6.0V. Each amplifier draws only 4μA quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding HIGH CAPACITIVE LOAD DRIVING CAPABILITY and STABLE WIDE BANDWIDTH. The TP151x family is optimized for wide bandwidth low power applications. They have an industry leading high GBW to power ratio and are unity gain stable for ANY CAPACITIVE load. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin.

Low Input Referred Noise

The TP151x family provides a low input referred noise of 95nV/ √ Hz at 1kHz. The noise density will grow slowly with the frequency in wideband range, and the input voltage noise density is typically 3.6μV_{P-P} at the frequency of 0.1Hz to 10Hz.

Low Input Offset Voltage and Low Offset Voltage Temperature Drift

The TP151x family has a low offset voltage of 3.0mV maximum which is essential for precision applications. The offset voltage is trimmed with a proprietary trim algorithm to ensure low offset voltage for precision signal processing requirement. 3PEAK's proprietary precision temperature compensation technique makes offset voltage temperature drift at 0.6μV/°C.

Low Input Bias Current

The TP151x family is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on "PCB Surface Leakage" for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the TP151x OPA's input bias current at +27°C (±1pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 2 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

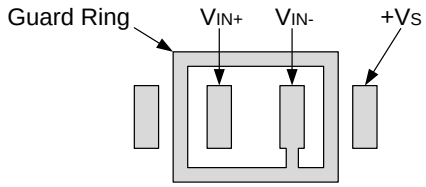


Figure 2

Ground Sensing and Rail to Rail Output

The TP151x family has excellent output drive capability, delivering over 10mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 5mV of either rail. Since the inputs can go 500mV beyond either rail, the op-amp can easily perform 'true ground' sensing.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The TP151x family has reverse-biased ESD protection diodes on all inputs and output. Input and out pins can not be biased more than 300mV beyond either supply rail.

Shut-down

The single channel OPA versions have SHDN pins that can shut down the amplifier to less than 0.1μA supply current. The SHDN pin voltage needs to be within 0.5V of V– for the amplifier to shut down. During shutdown, the output will be in high output resistance state, which is suitable for multiplexer applications. When left floating, the SHDN pin is internally pulled up to the positive supply and the amplifier remains enabled.

Driving Large Capacitive Load

The TP151x family of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for "Phase Margin vs. Load Capacitance". As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP151x OPA family (e.g., > 200 pF when G = +1V/V), a small series resistor at the output (R_{ISO} in Figure 3) improves the feedback loop's phase margin and stability by making the output load resistive at higher frequencies.

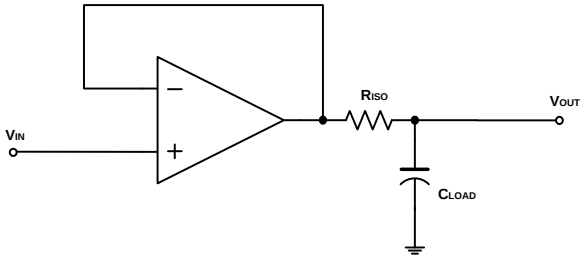


Figure 3

Low-Side Current Monitor Application

As shown in Figure 4. Please be noted: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

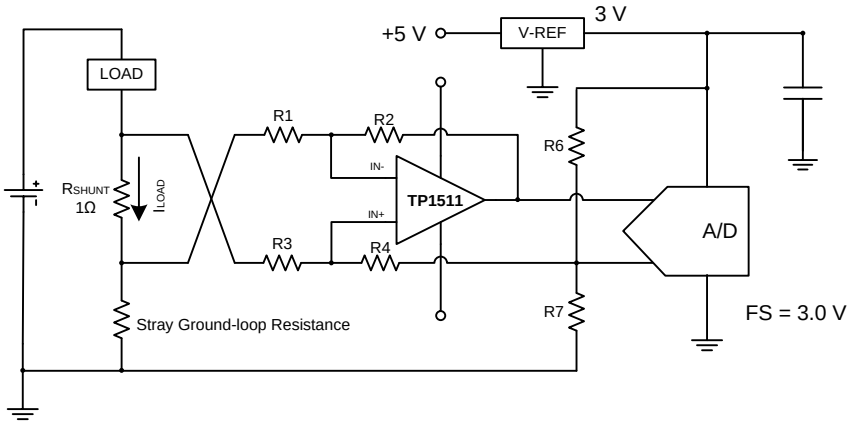


Figure 4

High-Side Current Monitor Application

As shown in Figure 5. Please be noted:

(1) Zener rated for op amp supply capability.

(2) Current-limiting resistor.

(3) Choose zener biasing resistor or dual N-MOSMETs.

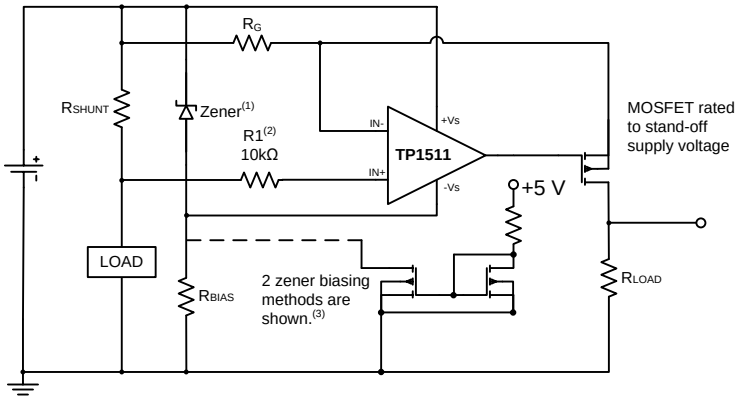


Figure 5

Window Comparator Application

As shown in Figure 6. Please be noted:

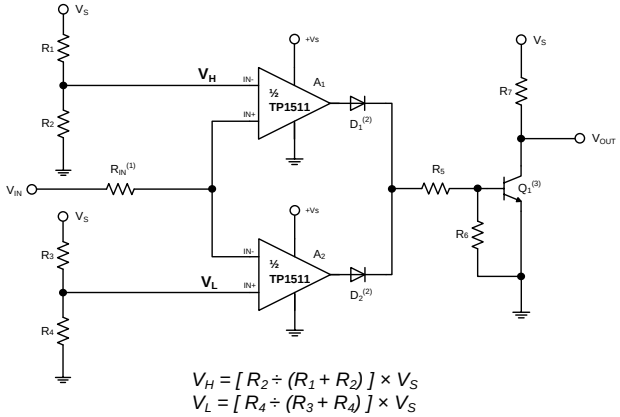
(1) R_{IN} protects A1 and A2 from possible excess current flow.

(2) IN4446 or equivalent diodes, and 2N2222 or equivalent NPN transistor.

(3) The threshold limits are set by V_H and V_L, with $V_H > V_L$. When $V_{IN} < V_H$, the output of A1 is low. When $V_{IN} > V_L$, the output of A2 is low. Therefore, both op amp outputs are at 0V as long as V_{IN} is between V_H and V_L. This architecture results in no current flowing through either diode, Q1 in cutoff, with the base voltage at 0V, and V_{OUT} forced high.

(4) If V_{IN} falls below V_L, the output of A2 is high, current flows through D2, and V_{OUT} is low. Likewise, if V_{IN} rises above V_H, the output of A1 is high, current flows through D1, and V_{OUT} is low.

(5) The window comparator threshold voltages are set as follows:



$V_H = [\, R_2 \div (R_1 + R_2)\,] \times V_S$

$V_L = [\, R_4 \div (R_3 + R_4)\,] \times V_S$

Figure 6

Pulse Oximeter Current Source Application

A pulse oximeter is a noninvasive medical device used for continuously measuring the percentage of Hemoglobin (Hb) saturated with oxygen and the pulse rate of a patient. Hemoglobin that is carrying oxygen (oxy-hemoglobin) absorbs light in the infrared (IR) region of the spectrum; hemoglobin that is not carrying oxygen (deoxy-hemoglobin) absorbs visible red (R) light. In pulse oximetry, a clip containing two LEDs (sometimes more, depending on the complexity of the measurement algorithm) and the light sensor (photodiode) is placed on the

finger or earlobe of the patient. One LED emits red light (600 nm to 700 nm) and the other emits light in the near IR (800 nm to 900 nm) region. The clip is connected by a cable to a processor unit. The LEDs are rapidly and sequentially excited by two current sources (one for each LED), whose dc levels depend on the LED being driven, based on manufacturer requirements, and the detector is synchronized to capture the light from each LED as it is transmitted through the tissue.

An example design of a dc current source driving the red and infrared LEDs is shown in Figure 7. Pulse Oximeter Red and Infrared Current Sources Using the TP1512 as a Buffer to the Voltage Reference Device.

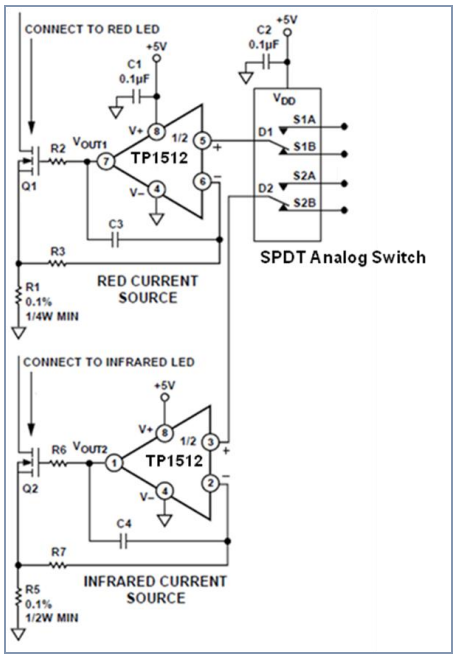


Figure 7

Portable Gas Meter Application

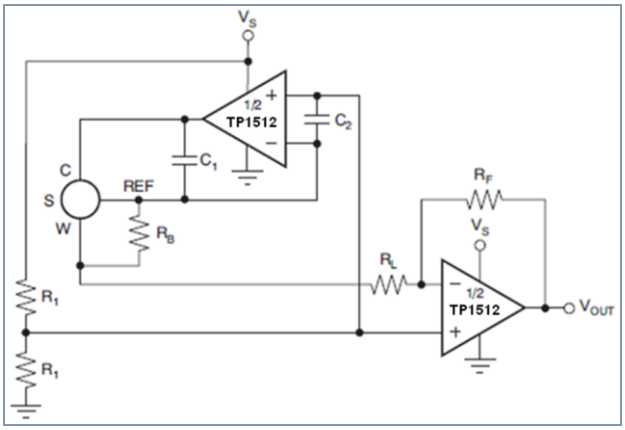


Figure 8

Four-Pole, Low-pass Butterworth Filter for Glucose Monitor Application

There are several methods of glucose monitoring: spectroscopic absorption of infrared light in the 2 μm to 2.5 μm range, reflectance spectrophotometry, and the amperometric type using electrochemical strips with glucose oxidase enzymes. The amperometric type generally uses three electrodes: a reference electrode, a control electrode, and a working electrode. Although this is a well established and widely used technique, signal-to-noise

ratio and repeatability can be improved using the TP1511/TP1512/TP1514 amplifiers with their low peak-to-peak voltage noise of 3.6μV from 0.1 Hz to 10 Hz and voltage noise density of 95nV/√Hz at 1 kHz.

Another consideration is operation from a 3.3 V battery. Glucose signal currents are usually less than 3μA full scale; therefore, the I-to-V converter requires low input bias current. The TP1511/TP1512/TP1514 are excellent choices because these amplifiers provide 1pA typical and 10pA maximum of input bias current at ambient temperature.

A low-pass filter with a cutoff frequency of 80Hz to 100Hz is desirable in a glucose meter device to remove extraneous noise; this can be a simple two-pole or four-pole Butterworth filter. Low power op amps with bandwidths of 50kHz to 500kHz should be adequate. The TP1511/TP1512/TP1514 amplifiers with their 150kHz GBWP and 4μA typical current consumption meet these requirements. A circuit design of a four-pole Butterworth filter (preceded by a one-pole, low-pass filter) is shown in Figure 9. With a 3.3 V battery, the total power consumption of this design is 80μW typical at ambient temperature.

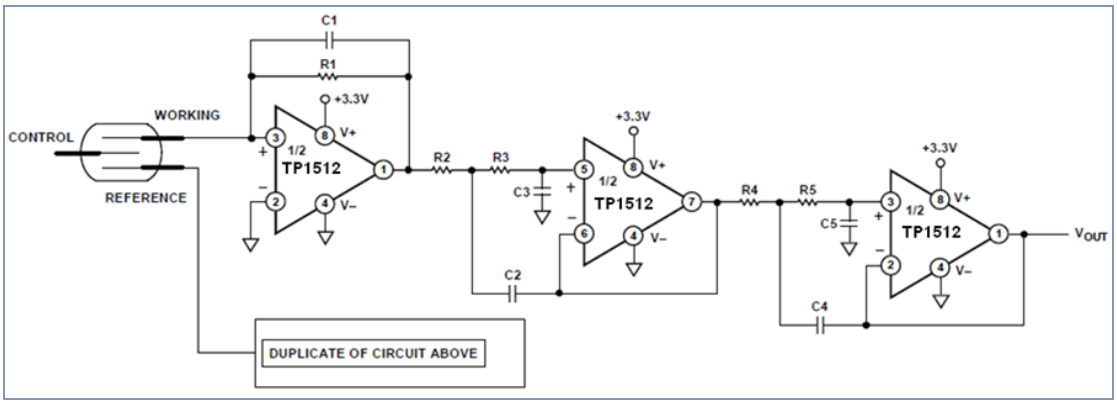


Figure 9

Two Op Amp Instrumentation Amplifier

The TP151x OPA series is well suited for conditioning sensor signals in battery-powered applications. Figure 10 shows a two op-amp instrumentation amplifier, using the TP151x OPA.

The circuit works well for applications requiring rejection of Common Mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, V_{REF} is typically $V_{DD}/2$.

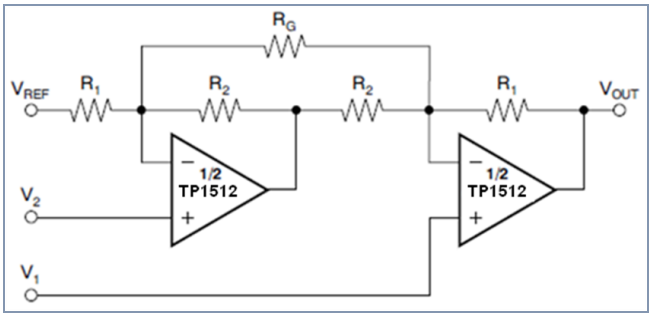
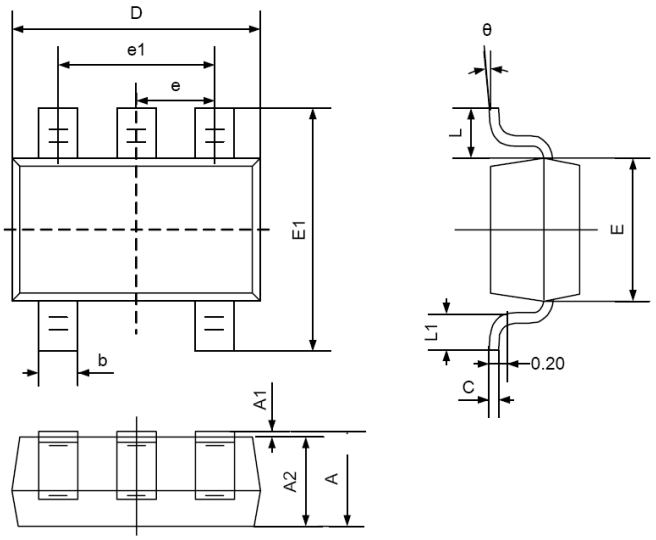


Figure 10

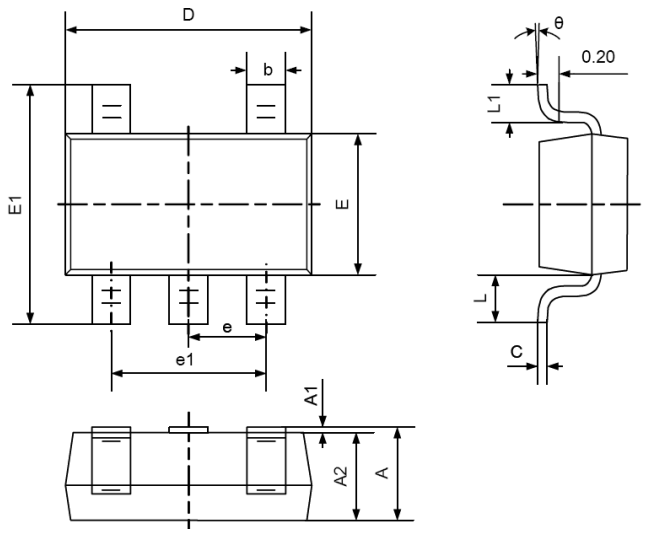
Package Outline Dimensions

SC70-5 /SOT-353



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

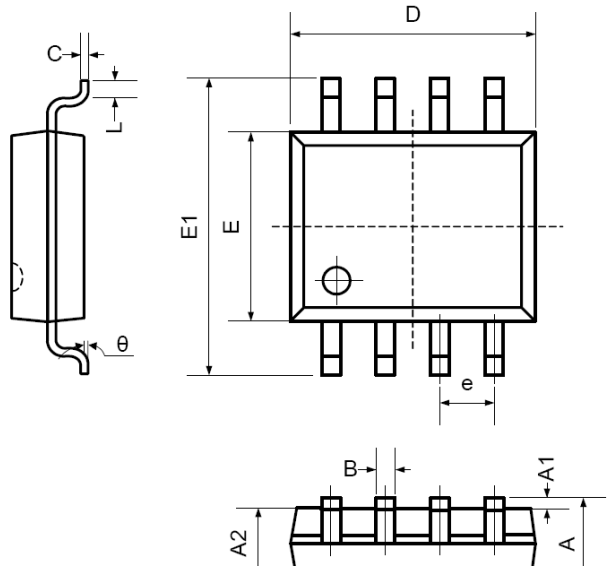
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

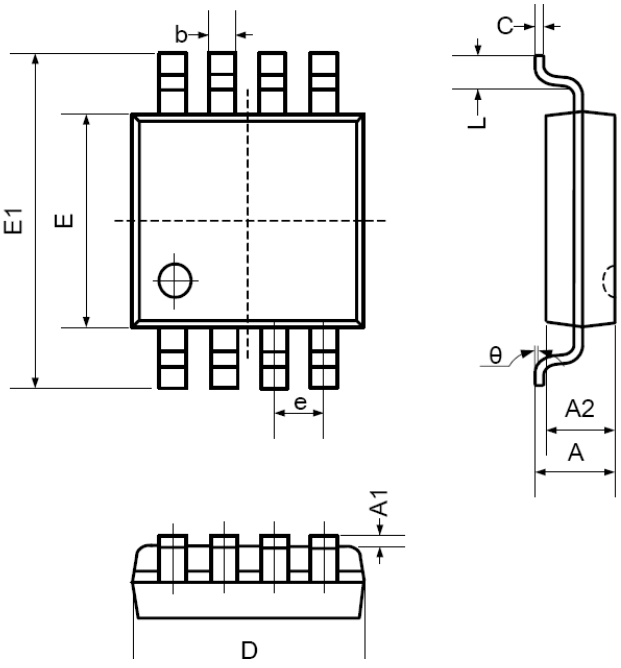
Package Outline Dimensions

SOIC-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

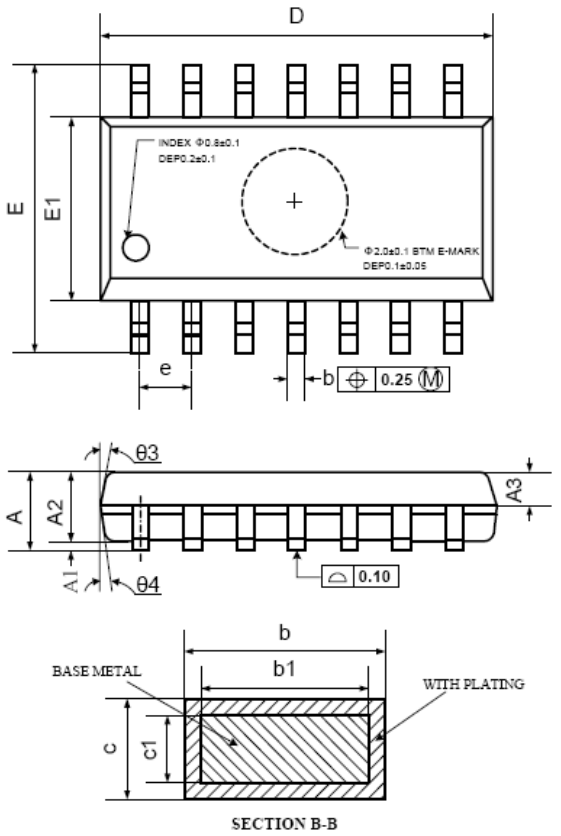
MSOP-8

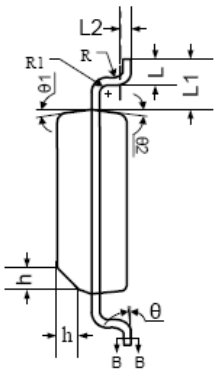


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package Outline Dimensions

SOIC-14

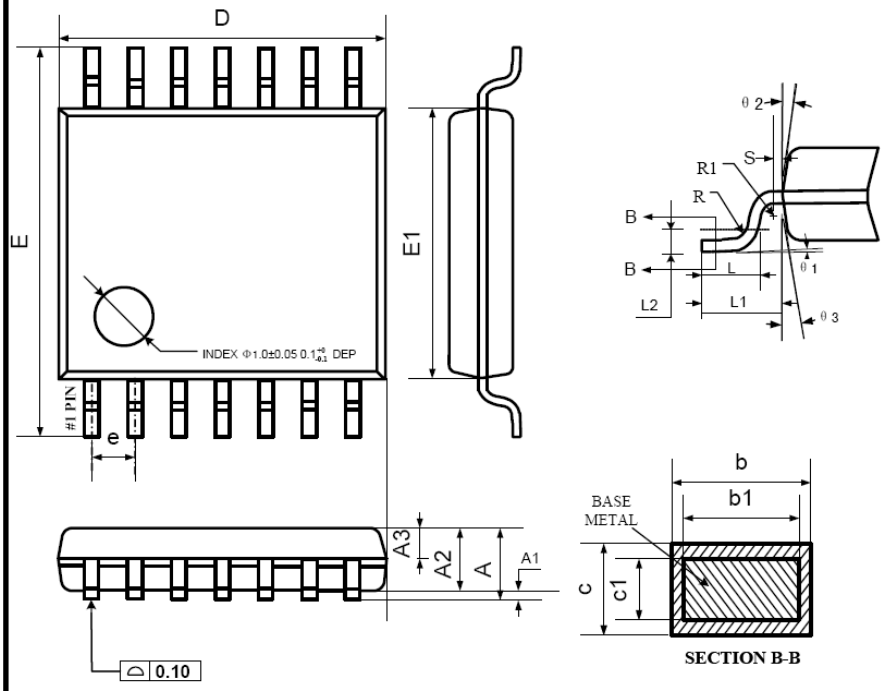




Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36		0.49
b1	0.35	0.40	0.45
c	0.16		0.25
c1	0.15	0.20	0.25
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07		
R1	0.07		
h	0.30	0.40	0.50
θ	0°		8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.28
b1	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	0.13	0.15
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
R1	0.09	-	-
s	0.20	-	
θ1	0°	-	8°
θ2	10°	12°	14°
θ3	10°	12°	14°