TISP83121D Unidirectional P & N-Gate Protector

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Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, 0 °C to 70 °C	V _{DRM}	100	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)			
10/1000 μs (GR-1089-CORE, open-circuit voltage wave shape 10/1000 μs)		150	А
5/310 μs (CCITT K20/21, open-circuit voltage wave shape 7 kV, 10/700 μs)	I _{TSP}	250	
8/20 μs (ANSI C62.41, open-circuit voltage wave shape 1.2/50 μs)		500	
Non-repetitive peak on-state current, 50 Hz, halfwave rectified sinewave, (see Notes 1 and 2)			
100 ms		22	
1 s	I _{TSM}	8	Α
900 s		3	
Junction temperature	T _J	-40 to +150	°C
Storage temperature range	T _{stg}	-65 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with 0 °C < T_J < 70 °C. The surge may be repeated after the device returns to its initial conditions. For operation at the rated current value, pins 1, 4, 5 and 8 must be connected together.

2. Above 70 °C, derate linearly to zero at 150 °C lead temperature.

Electrical Characteristics, T_J = 25 °C (Unless Otherwise Noted)

	Parameter	Test Conditions		Min	Тур	Max	Unit
I_D	Off-state current	$V_d = 70 \text{ V, } I_G = 0$				1	μΑ
I _{DRM}	Repetitive peak off- state current	V _d = V _{DRM} = 100 V, I _G = 0, 0 °C to 70 °C				10	μΑ
		T _J = 0 to 7	O °C			300	
I _H	Holding current	$I_T = 1 \text{ A, di/dt} = -1 \text{A/ms}$ $T_J = 2$	5 °C	90			mA
		$T_{J} = 7$	0 °C	60			
I_R	Reverse current	V _R = 0.3 V				1	mA
I _{G1T}	Gate G1 trigger current	$I_T = +1 \text{ A, } t_{p(g)} = 20 \mu\text{s}$				+200	mA
I _{G2T}	Gate G2 trigger current	$I_T = +1 \text{ A, } t_{p(g)} = 20 \mu\text{s}$				-180	mA
V_{G1T}	G1-K trigger voltage	$I_T = +1 \text{ A, } t_{p(g)} = 20 \mu\text{s}$				+1.8	V
V_{G2T}	G2-A trigger voltage	$I_T = +1 \text{ A, } t_{p(g)} = 20 \mu\text{s}$				-1.8	V
C _{AK}	Anode-cathode off- state capacitance	$f = 1 \text{ MHz}$, $V_d = 1 \text{ V rms}$, $V_D = 5 \text{ V}$, $I_G = 0$ (see Note 3)				100	pF

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Thermal Characteristics

	Parameter	Test Conditions	Min	Тур	Max	Unit
П	lunction to free air thormal resis	$T_A = 25 ^{\circ}\text{C}$, EIA/JESD51-3 PCB,			105	°C/W
r _θ JA	$R_{ heta JA}$ Junction to free air thermal resis	EIA/JESD51-2 environment, $I_T = I_{TSM(900)}$			105	C/VV

Users should verify actual device performance in their specific applications.

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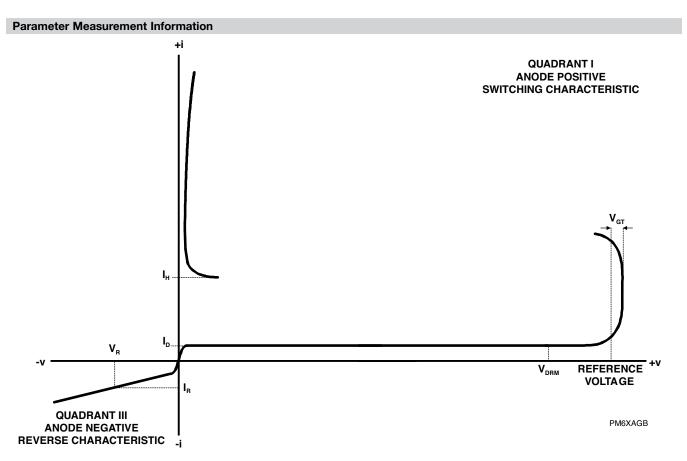


Figure 1. Voltage-Current Characteristic

APPLICATIONS INFORMATION

Multiple Line Overvoltage Protection

Figure 2 shows two TISP83121D devices protecting many lines. Line conductor positive overvoltage protection is given by the steering diode array connected to the anode of the upper TISP83121D and the TISP83121D itself. The TISP83121D gate reference voltage is the positive battery supply, $+V_{BAT}$. The initial limiting voltage will be the sum of the voltages of the battery, the forward biased conductor diode, the gate trigger of the TISP83121D and the forward biased reference voltage blocking diode. Typically the conductor voltage will be initially limited at 2.5 V above the $+V_{BAT}$ value.

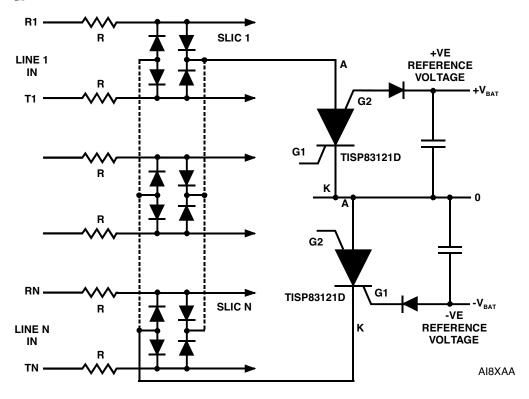


Figure 2. N Line Positive and Negative Overvoltage Protection

Line conductor negative overvoltage protection is given by the diode steering array connected to the cathode of the lower TISP83121D and the TISP83121D itself. The TISP83121D gate reference voltage is the negative battery supply, $-V_{\text{pAT}}$. The initial limiting voltage will be the sum of the voltages of the battery, the forward biased conductor diode, the gate trigger of the TISP83121D and the forward biased reference voltage blocking diode. Typically the conductor voltage will be initially limited at 2.5 V below the $-V_{\text{PAT}}$ value.

When a TISP83121D crowbars and grounds all conductors of the appropriate polarity, the device current will be the sum of all the SLIC output currents. This will usually exceed the TISP83121D holding current. To switch off the TISP83121D and restore normal operation, the grounded condition of the SLIC output must be detected and the SLIC outputs turned off.

The 150 A rating of the TISP83121D allows a large number of lines to be protected against currents caused by lightning. For example, if a recommendation K.20 10/700 generator was connected to all lines, together with 350 V primary protection and a series conductor resistance (R) of 25 Ω , the maximum conductor current before the primary protection operated would be 350/25 = 14 A or 28 A per line. For a total return current of about 150 A the number of lines would be 150/28 = 5. At this current level, 5x28 = 140 A, the generator voltage would be 140((25+25)/10+15) = 2800 V. Another limitation is long term power cross. The long term power cross capability of the TISP83121D is 3 A peak or 2.1 A rms. If the line conductor overcurrent protection was given by a PTC thermistor which tripped at 0.2 A, the maximum number of conductors becomes 2.1/0.2 = 10 or 5 lines.

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Battery Supply Impedance

In many designs, the battery supply voltages are generated by switching mode power supplies. This type of power supply cannot be charged like a battery. Feeding a charging current to a switching mode power supply will usually cause the supply to stop switching and the voltage to rise. The gate current of the TISP83121D is a charging current for the supply. To avoid the supply voltage from rising and damaging the connected SLICs, an avalanche diode voltage clamp can be connected across the supply (Figure 3. (A)).

Another approach is to reduce the gate charging current for the supply by a transistor buffer (Figure 3. (B)). If the transistor gain was 50, a 200 mA gate current would be reduced to a supply charging current of 200/50 = 4 mA. In both cases, the dissipation in the control devices can be substantial and power capability needs to be taken into account in device selection.

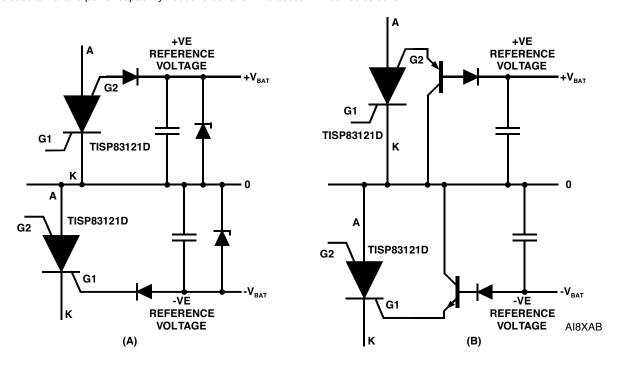


Figure 3. Reference Voltage Control by (A) Breakdown Diodes or (B) by Transistor Buffers

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