MAXIMUM RATINGS

Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector−Base Voltage	V_{CB}	60	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current − Continuous − Peak	I_C	2.0 4.0			Adc
Base Current	I_B	50			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4			W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			W W/°C
Unclamped Inductive Load Energy − Figure 13	E	25			mJ
Operating and Storage Junction	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 30 mAdc, I_B = 0)	TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	$V_{CEO(sus)}$	 60 80 100	 − − −	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 TIP110, TIP115 TIP111, TIP116 TIP112 ,TIP117	I_{CEO}	 − − −	 2.0 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	I_{CBO}	 − − −	 1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	2.0	mAdc
ON CHARACTERISTICS (Note 1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 1000 500	 − −	−
Collector−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc)		$V_{CE(sat)}$	−	2.5	Vdc
Base−Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	−	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		h_{fe}	25	−	−
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 TIP115, TIP116, TIP117 TIP110, TIP111, TIP112	C_{ob}	 − −	 200 100	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Downloaded from Arrow.com.

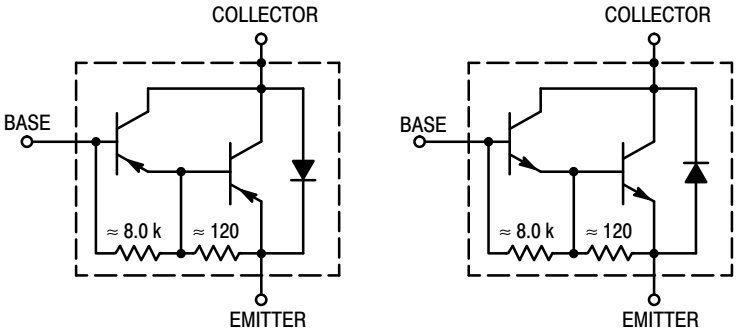


Figure 1. Darlington Circuit Schematic

ORDERING INFORMATION

Device	Package	Shipping
TIP110	TO−220	50 Units / Rail
TIP110G	TO−220 (Pb−Free)	50 Units / Rail
TIP111	TO−220	50 Units / Rail
TIP111G	TO−220 (Pb−Free)	50 Units / Rail
TIP112	TO−220	50 Units / Rail
TIP112G	TO−220 (Pb−Free)	50 Units / Rail
TIP115	TO−220	50 Units / Rail
TIP115G	TO−220 (Pb−Free)	50 Units / Rail
TIP116	TO−220	50 Units / Rail
TIP116G	TO−220 (Pb−Free)	50 Units / Rail
TIP117	TO−220	50 Units / Rail
TIP117G	TO−220 (Pb−Free)	50 Units / Rail

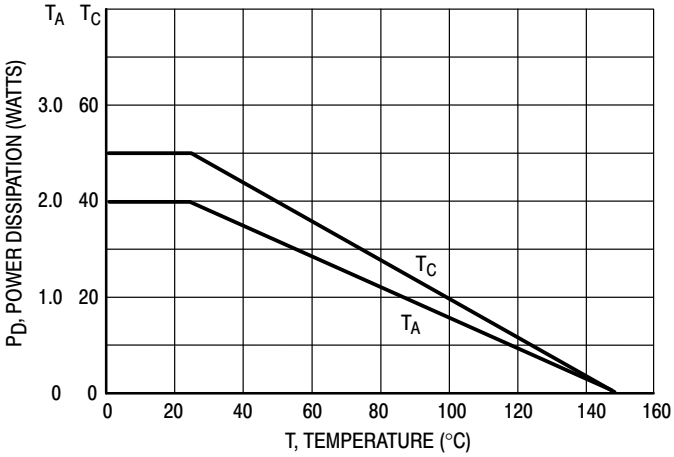


Figure 2. Power Derating

Downloaded from Arrow.com.

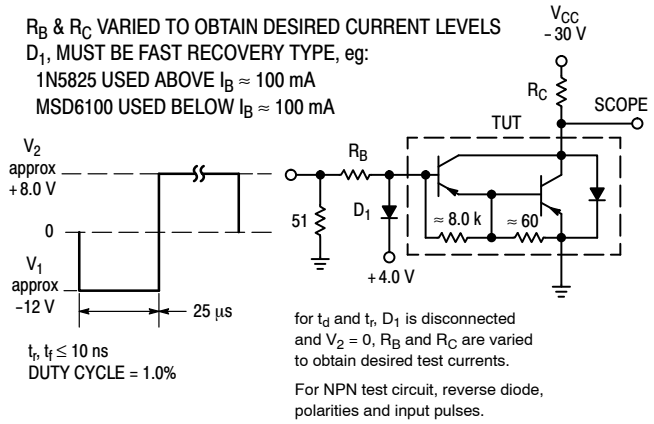


Figure 3. Switching Times Test Circuit

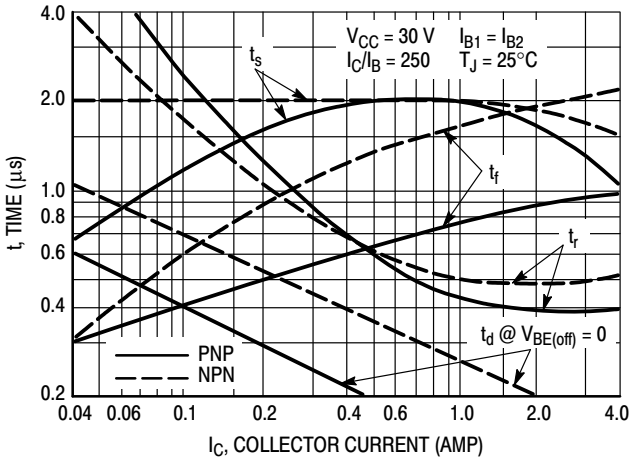


Figure 4. Switching Times

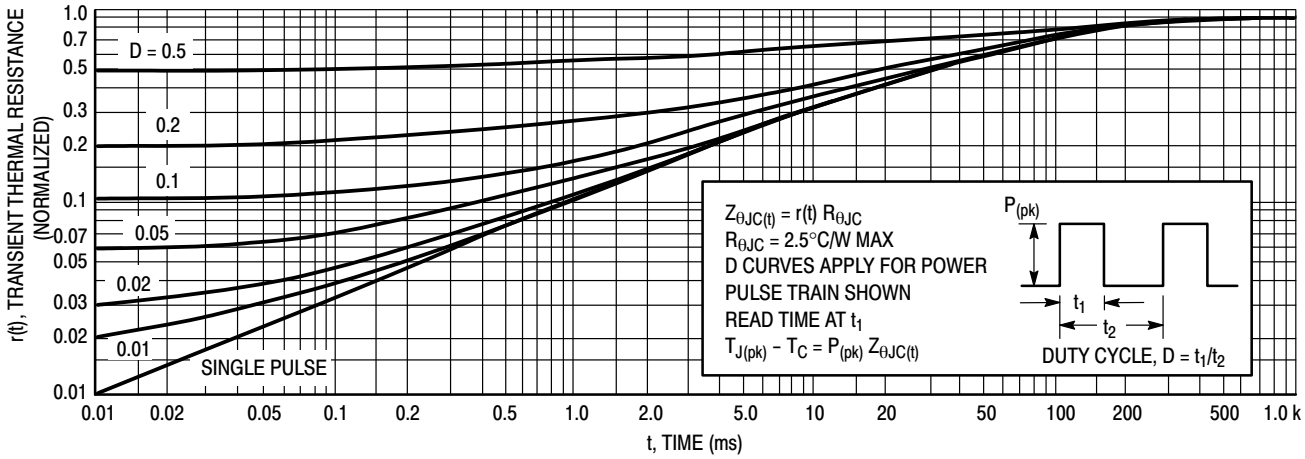


Figure 5. Thermal Response

Downloaded from Arrow.com.

ACTIVE−REGION SAFE−OPERATING AREA

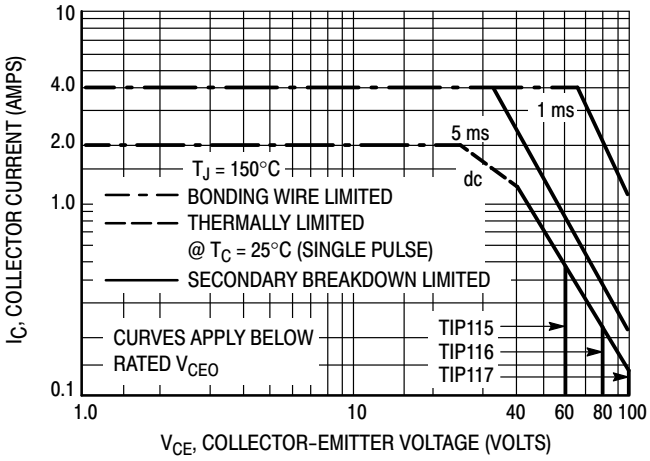


Figure 6. TIP115, 116, 117

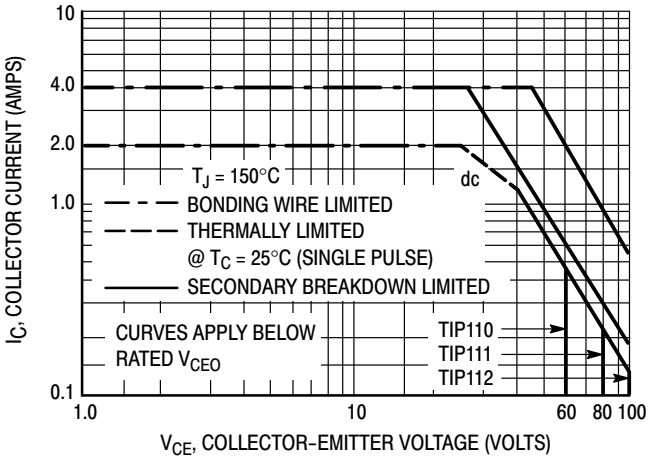


Figure 7. TIP110, 111, 112

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

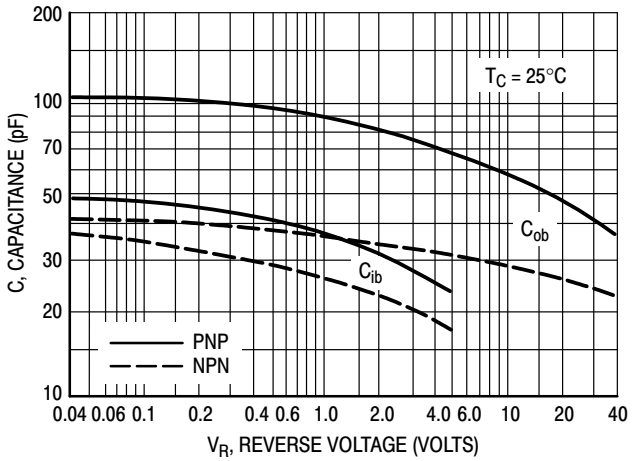
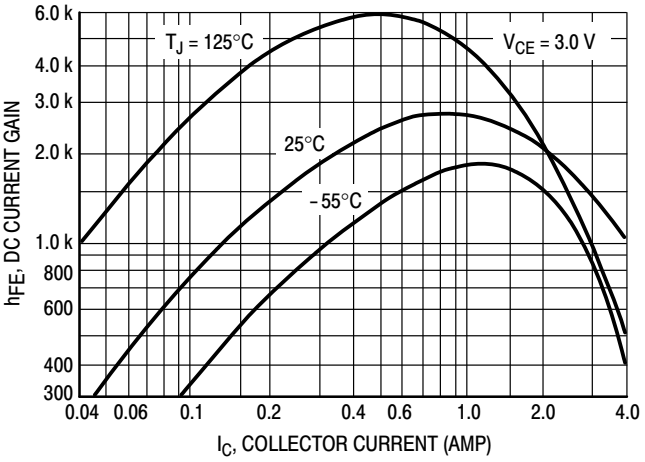


Figure 8. Capacitance

Downloaded from Arrow.com.

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

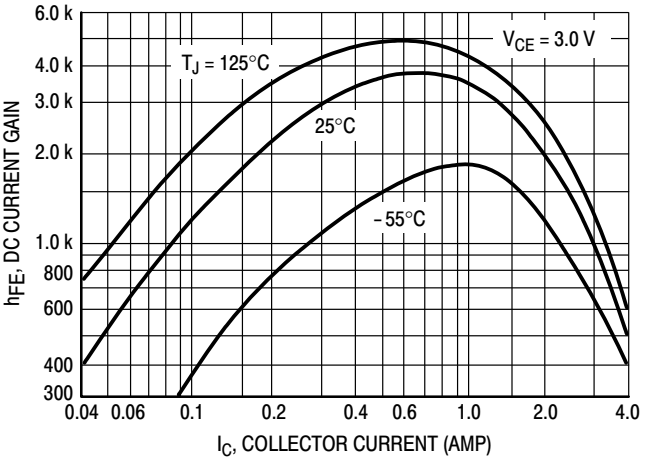
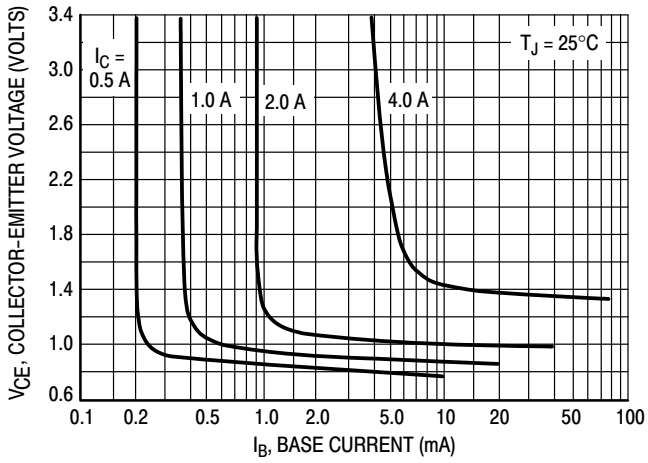


Figure 9. DC Current Gain



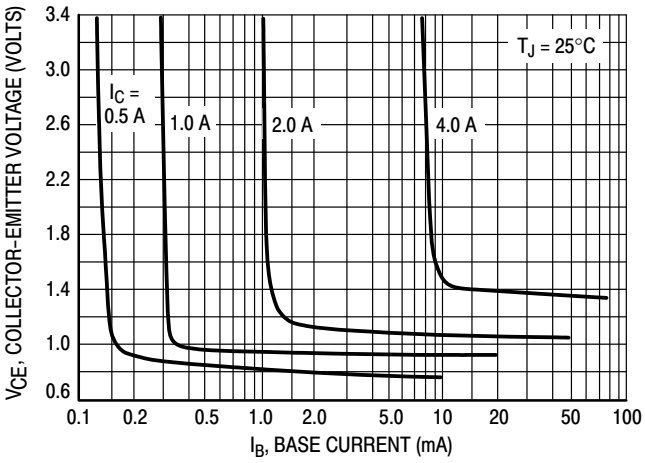
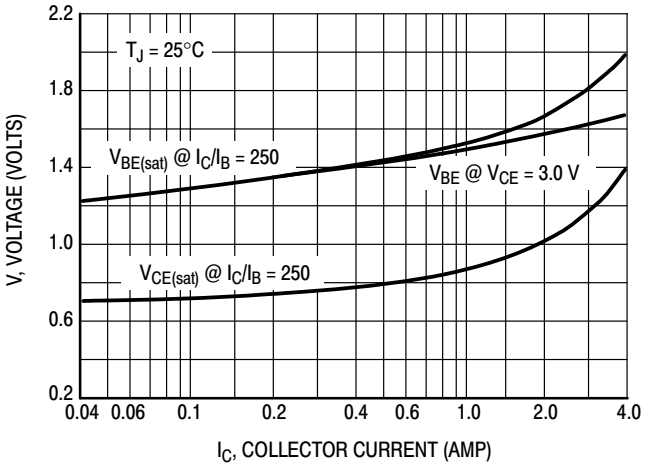


Figure 10. Collector Saturation Region



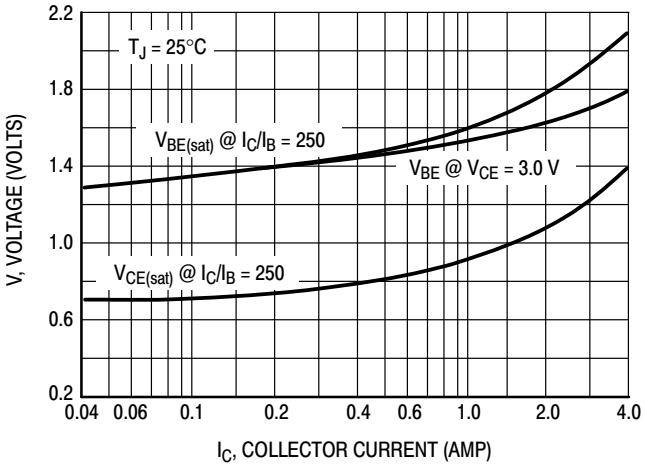
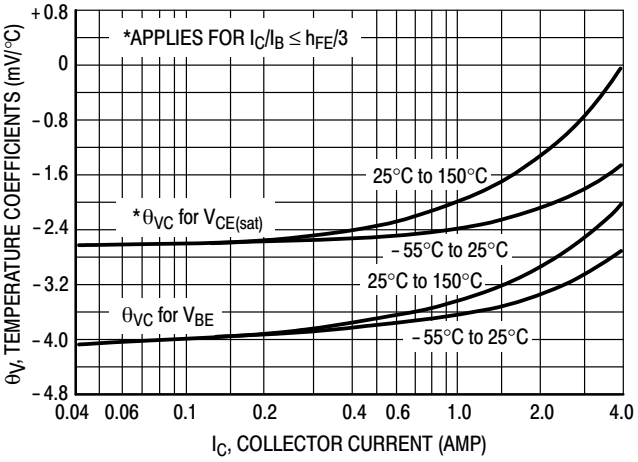


Figure 11. “On” Voltages

Downloaded from Arrow.com.

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

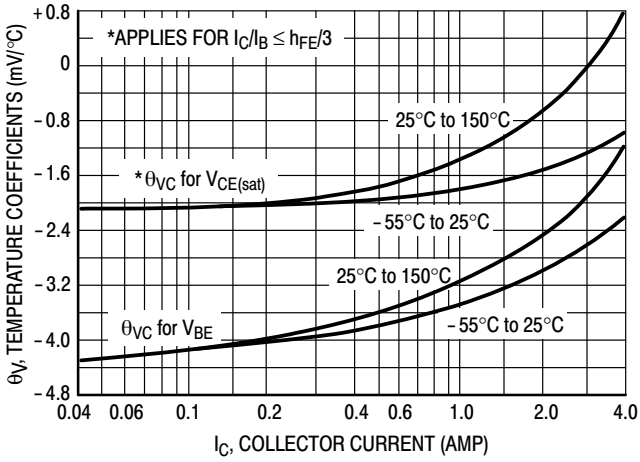
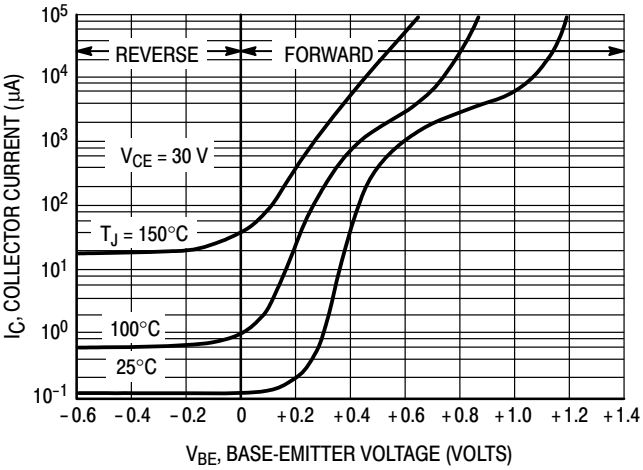


Figure 12. Temperature Coefficients



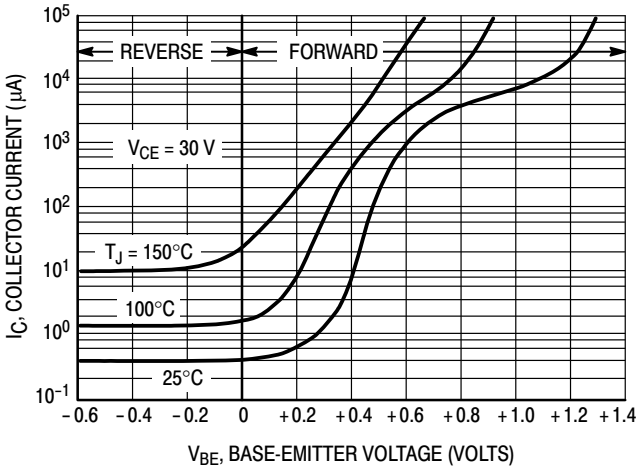
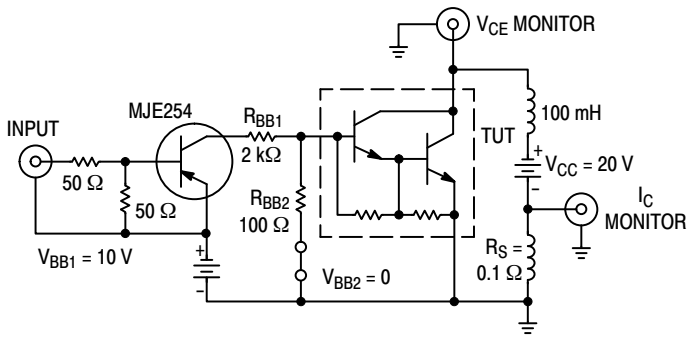
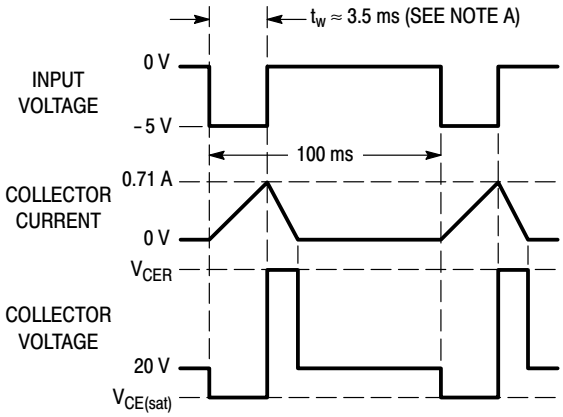


Figure 13. Collector Cut-Off Region

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



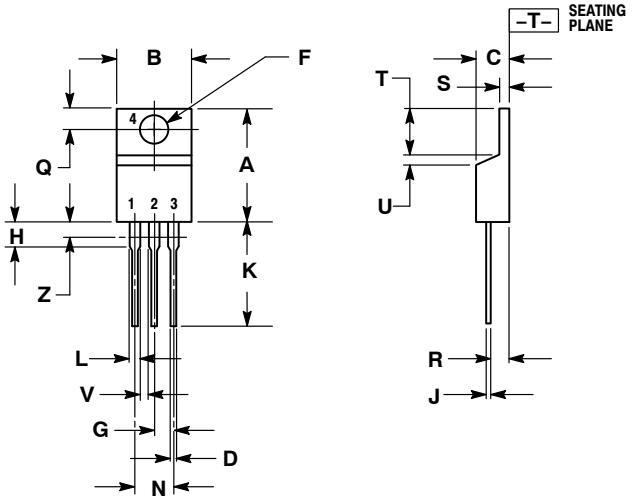
Note A: Input pulse width is increased until I_{CM} = 0.71 A,
NPN test shown; for PNP test
reverse all polarity and use MJE224 driver.

Figure 14. Inductive Load Switching

Downloaded from Arrow.com.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

ON Semiconductor and the ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

TIP110/D

Downloaded from Arrow.com.